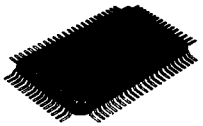
HD613901 (LCD-IV)
4-Bit CMOS Microcomputer

AUTOMOTIVE VERSION

The LCD-IV is the CMOS 4-bit single chip microcomputer which contains ROM, RAM, I/O, Timer/Event Counter and Control Circuit, Direct Drive Circuit for LCD on single chip. The LCD-IV is designed to drive LCD directly and perform efficient controller function as well as arithmetic function for both binary and BCD data. With the on-chip crystal oscillator for timer, the clock function is easily realized. The CMOS technology of the LCD-IV provides the flexibility of microcomputers for battery powered and battery back-up applications in combination with low power consuming LCD.

- **FEATURES**
- 4-bit Architecture
- 4,096 Words of Program ROM (10 bits/Word)
- 256 Digits of Data RAM and Display Data RAM (4 bits/Digit)
- Control Circuit and Direct Drive Circuit for LCD
  - 4 Commons (Duty Ratio; Static, 1/2, 1/3, 1/4)
  - 32 Segments (Externally expandable up to 96 Segments using external Drivers HD44100Hs)
- 32 I/O Lines and 2 External Interrupt Lines
- Timer/Event Counter
- All Instructions except One Instruction; Single Word and Single Cycle
- BCD Arithmetic Instructions
- Pattern Generation Instruction
  – Table Look Up Capability –
- Powerful Interrupt Function
  - 3 Interrupt Sources
    - 2 External Interrupt Lines
    - Timer/Event Counter
  - Multiple Interrupt Capability
- Bit Manipulation Instructions for Both RAM and I/O
- Option of I/O Configuration Selectable on Each Pin; Pull Up MOS or CMOS or Open Drain
- Built-in Oscillator for System Clock (Resistor or Ceramic Filter)
- Built-in Crystal Oscillator for Timer
- Low Operating Power Dissipation
- Stand-by Mode (Halt Mode)
- 2 Versions;
  - V_{CC} = 5V ± 10%, 5 μs Instruction Cycle Time
  - V_{CC} = 2.5V to 5.5V, 20 μs Instruction Cycle Time

LCD-IV



(FP-80)

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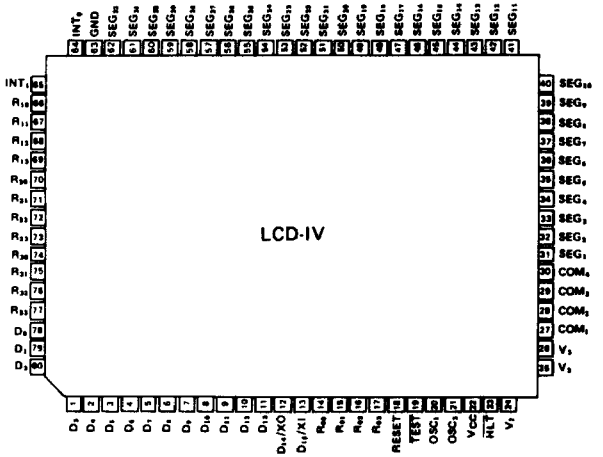
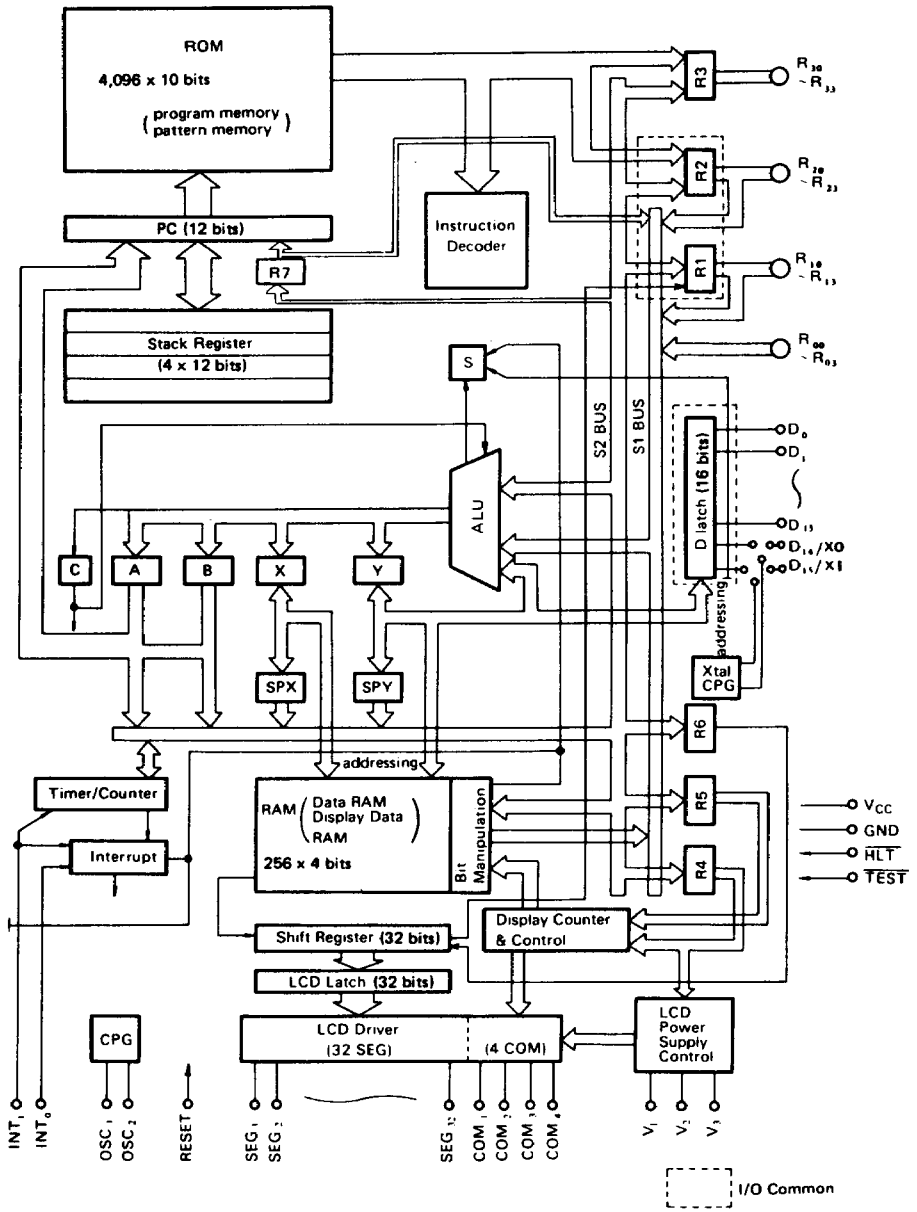
- **PIN ARRANGEMENT**



(Top View)

Data Sheets contain information for automotive operation only. Refer to **Reference Guide** (Section 9) for a listing of supplementary publications which provide complete specifications.

■ BLOCK DIAGRAM



■ ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%)

• ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	−0.3 to +7.0	V	
Pin Voltage	V_T	−0.3 to V_{CC} +0.3	V	
Maximum Total Output Current (1)	$-\Sigma I_{O1}$	25	mA	(Note 3)
Maximum Total Output Current (2)	ΣI_{O2}	25	mA	(Note 3)
Operating Temperature	T_{opr}	−40 to +85	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

(NOTE) 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under the conditions of "ELECTRICAL CHARACTERISTICS-1, -2". If these conditions are exceeded, it could be cause of malfunction of LSI and affects reliability of LSI.
2. All voltages are with respect to GND.
3. Maximum Total Output Current is the total sum of output currents which can flow out or in simultaneously.
4. Power supply condition $V_{CC} \geqq V1 \geqq V2 \geqq V3 \geqq GND$ should be maintained.

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• ELECTRICAL CHARACTERISTICS – 1 (V_{CC} = 5V ± 10%, Ta = -40 to +85°C)

Item	Symbol	Test Conditions	Value min	Value typ	Value max	Unit	Note
Input "Low" Voltage	V_{IL}		-0.3	–	1.0	V	
Input "High" Voltage	V_{IH}		V_{CC}-1.0	–	V_{CC}+0.3	V	(12)
Output "Low" Voltage	V_{OL}	I_{OL} = 1.6 mA	–	–	0.8	V	
Output "High" Voltage (1)	V_{OH1}	$-I_{OH}$ = 1.0 mA	2.4	–	–	V	(1)
Output "High" Voltage (2)	V_{OH2}	$-I_{OH}$ = 0.01 mA	V_{CC}-0.3	–	–	V	(2)
Driver Voltage Descending (COM)	V_{d1}	Id = 0.05 mA, V_{LCD} = 5V	–	–	0.4	V	(16)
Driver Voltage Descending (SEG)	V_{d2}	Id = 0.01 mA, V_{LCD} = 5V	–	–	0.4	V	(16)
Dividing Resistor of LCD Power Supply	Rwell		25	–	300	kΩ	
Interrupt Input Hold Time	t_{INT}		2·Tinst	–	–	μs	(14)
Output "High" Current	I_{OH}	V_{OH} = V_{CC}	–	–	4	μA	(3)
Input Leakage Current	I_{IL}	V_{in} = 0 to V_{CC}	–	–	2	μA	(4), (12)
Pull up MOS Current	$-I_P$	V_{CC} = 5V	45	–	250	μA	
Supply Current (1)	I_{CC1}	V_{in} = V_{CC}, V_{CC} = 5V Ceramic Filter Oscillation (f_{osc} = 800 kHz)	–	–	3	mA	(5)
		V_{in} = V_{CC}, V_{CC} = 5V Ceramic Filter Oscillation (f_{osc} = 400 kHz)	–	–	1.5	mA	(5)
Supply Current (2)	I_{CC2}	V_{in} = V_{CC}, V_{CC} = 5V R_f Oscillation (f_{osc} = 800 kHz) External Clock Operation (f_{cp} = 800 kHz)	–	–	2	mA	(5)
		V_{in} = V_{CC}, V_{CC} = 5V R_f Oscillation (f_{osc} = 400 kHz) External Clock Oscillation (f_{cp} = 400 kHz)	–	–	1	mA	(5)
Standby I/O Leakage Current	I_{LS}	$\overline{HLT}$ = 1.0V, V_{in} = 0 to V_{CC}	–	–	1.0	μA	(6), (12)
Standby Supply Current (1)	I_{CCS1}	V_{in} = V_{CC}, $\overline{HLT}$ = 0.2V	–	–	10	μA	(15)
Standby Supply Current (2)	I_{CCS2}	V_{in} = V_{CC}, $\overline{HLT}$ = 0.2V	–	50*	120	μA	(7)
LCD Display Voltage	V_{LCD}	V_{CC}-V_3	2.5	–	V_{CC}	V	(11)
Frame Frequency of LCD Drive	f_F	n = 1 (static) n = 2 (1/2 Duty) n = 3 (1/3 Duty) n = 4 (1/4 Duty)	$\frac{1}{256 \times n \times T_{inst}}$			Hz	(13)
External Clock Operation; System Clock							
External Clock Frequency	f_{cp}		130	–	1,000	kHz	(8), (13)
External Clock Duty	Duty		45	–	55	%	(8)
External Clock Rise Time	t_{rcp}		0	–	0.2	μs	(8)
External Clock Fall Time	t_{fcp}		0	–	0.2	μs	(8)
Instruction Cycle Time	T_{inst}	T_{inst} = 4/fcp	4.0	–	30.7	μs	(8)
Internal Clock Operation (R_f Oscillation); System Clock							
Clock Oscillation Frequency	f_{osc}	R_f = 62kΩ ± 2%	600	–	1,000	kHz	(9)
Instruction Cycle Time	T_{inst}	T_{inst} = 4/f_{osc}	4.0	–	6.7	μs	(9)
Internal Clock Operation (Ceramic Filter Oscillation); System Clock							
Clock Oscillation Frequency	f_{osc}	Ceramic Filter	784	–	816	kHz	(10)
Instruction Cycle Time	T_{inst}	T_{inst} = 4/f_{osc}	4.9	–	5.1	μs	(10)

(NOTE) All voltages are with respect to GND.
* A typical value of I_{CCS2} is a reference value when Ta is at 25°C.

• ELECTRICAL CHARACTERISTICS – 2 (Ta = -40 to +85°C)

Item	Symbol	Test Conditions	Value min	Value max	Unit	Note
Halt Duration Voltage	V_{DH}	$\overline{HLT}$ = 0.2V	2.3	–	V	(17)
Halt Current	I_{DH}	V_{in} = V_{CC}, $\overline{HLT}$ = 0.2V, V_{DH} = 2.3V	–	4.0	μA	(17), (19)
Halt Delay Time	t_{HD}		100	–	μs	(17)
Operation Recovery Time	t_{RC}		100	–	μs	(17)
$\overline{HLT}$ Fall Time	t_{fHLT}		–	1000	μs	(17)
$\overline{HLT}$ Rise Time	t_{rHLT}		–	1000	μs	(17)
$\overline{HLT}$ "Low" Hold Time	t_{HLT}		400	–	μs	(17)
$\overline{HLT}$ "High" Hold Time	t_{OPR}	R_f Oscillation, External Clock Operation	100	–	μs	(17)
		Ceramic Filter Oscillation	4000	–		
RESET Pulse Width (1)	t_{RST1}	R_f Oscillation, External Clock Operation	1	–	ms	(18)
		Ceramic Filter Oscillation	4	–		
RESET Pulse Width (2)	t_{RST2}	External Reset, $\overline{HLT}$ = V_{CC}, V_{CC} = 4.5 to 5.5V	2·T_{inst}	–	μs	(18)
RESET Rise Time	t_{rRST}	External Reset, $\overline{HLT}$ = V_{CC}, V_{CC} = 4.5 to 5.5V	–	100	μs	(18)
RESET Fall Time	t_{fRST}	External Reset, $\overline{HLT}$ = V_{CC}, V_{CC} = 4.5 to 5.5V	–	100	μs	(18)
INT_0, INT_1 Rise Time	t_{rINT}		–	50	μs	(14)
INT_0, INT_1 Fall Time	t_{fINT}		–	50	μs	(14)

(NOTE)
1. Applied to PMOS load of CMOS output pins and CMOS I/O common pins among D and R pins.
2. Applied to CMOS output pins, CMOS I/O common pins, input pins with pull up MOS, and I/O common pins with pull up MOS among D and R pins.
3. Applied to open-drain output pins and open-drain I/O common pins among D and R pins.
4. Pull up MOS current is excluded.
5. Applied to the supply current when the LCD-IV is in the reset state and the crystal oscillation for timer doesn't operate. (Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded).
   Test Conditions: RESET, HLT, TEST = V_{CC} (Reset State)
   INT_0, INT_1, R_{00} to R_{33}, D_0 to D_{13} = V_{CC}
   D_{14}/XO, D_{15}/XI ——— D_{14}/XO, D_{15}/XI = V_{CC} (Crystal oscillation for timer is not selected).
   D_{14}/XO = Open, D_{15}/XI = V_{CC} (Crystal oscillation for timer is selected).
   V_1, V_2, V_3 = V_{CC}
   COM_1 to COM_4, SEG_1 to SEG_{32} = Open
   When the crystal oscillation for timer operates, the standby supply current (2) I_{CCS2} flows in addition to I_{CC1} or I_{CC2}. When the LCD-IV is installed in the user's system, and in operation current increases according to the external circuitry and devices. Those are connected to the LCD-IV. User should design the power supply in consideration of this point (The difference between the measured current in the above reset state and that measured in the operational state in the user's system is the increased part of the supply current).
6. Standby I/O leakage current is the leakage current of I/O pins in the "Halt" and "Disable" state.
7. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded. The standby supply current (2) is the supply current at V_{CC} = 5V ± 10% in "Halt" state in the case that the crystal oscillation for timer is selected (only the crystal oscillator for timer, 5-bit divider and 6-bit prescaler are in operation).

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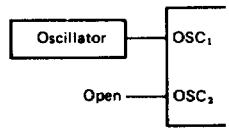
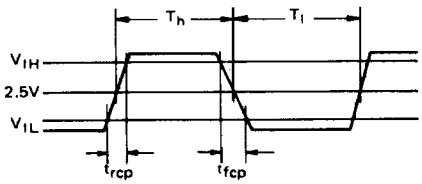
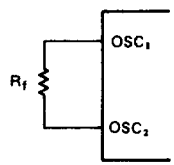
8. Applied to external clock operation (system clock).





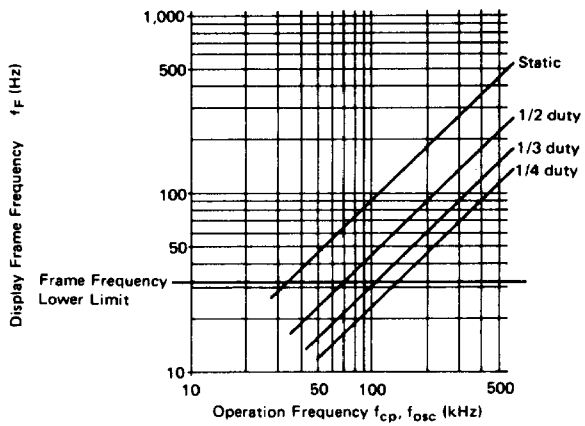
$$\text{Duty} = \frac{T_l}{T_h + T_l} \times 100\%$$

9. Applied to internal clock operation using resistor R_f. (system clock)

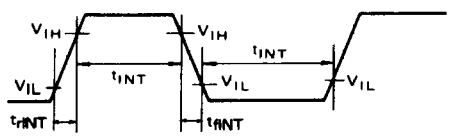


Wiring of OSC_1 and OSC_2 pins should be as short as possible because the oscillation frequency is modified by capacitance of these pins.

10. Applied to internal clock operation using ceramic filter. (system clock)
11. Power supply condition $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq GND$ should be maintained.
12. Applied to input pins, I/O common pins among D and R pins, and RESET, $\overline{HLT}$, OSC_1, INT_0, INT_1 pins.
13. Lower limit of operation frequency is determined by liquid crystal display duty. Flutter occurs on liquid crystal display if frame frequency is under 32 Hz. Therefore operation frequency should be determined to prevent that frame frequency becomes under 32 Hz.
The following shows the relation between liquid crystal display frame frequency and operation frequency.

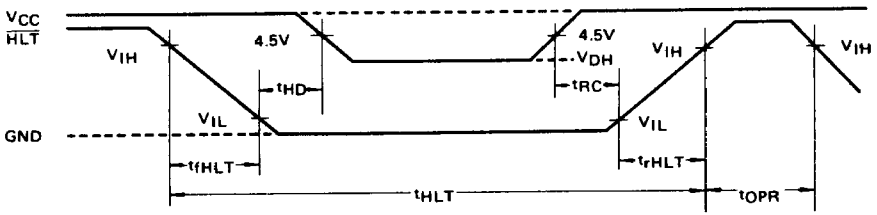


14. INT_0 and INT_1 inputs must be retained for two or more instruction cycle time at both "High" and "Low" levels.

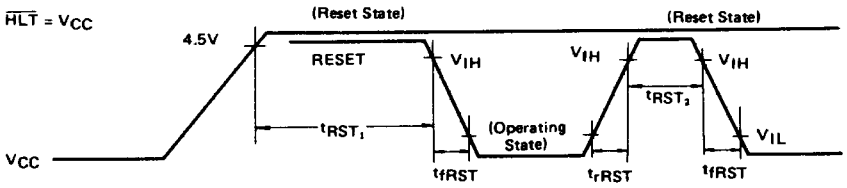


15. Power supply circuit for LCD is excluded. The standby supply current (1) is the supply at V_{CC} = 5V ± 10% in "Halt" state in the case that the crystal oscillation for timer is not selected. The supply current when supply voltage falls to the Halt Duration Voltage is called "Halt Current" (I_{DH}). (shown in ELECTRICAL CHARACTERISTICS–2)

16. The voltage that drops between the power supply pins (V_{CC}, V_1, V_2, V_3) and each common or segment output pin.
17. External Halt Timing Chart

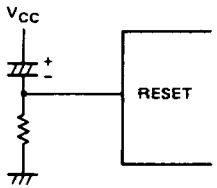


18. RESET Input Condition



- t_{RST_1} includes the time that required from the power ON until the operation gets into the constant state.
- t_{RST_2} is applied when the operation is in the constant state.

Reset circuit at power on is not installed. Simple reset circuit at power on is the following.



19. The supply current at $V_{CC} = V_{DH} = 2.3V$ in "Halt" state, in the case that the crystal oscillation for timer is not selected. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded.

■ ELECTRICAL CHARACTERISTICS (V_{CC} = 2.5 to 5.5V)

• ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	−0.3 to +7.0	V	
Pin Voltage	V_{T1}	−0.3 to V_{CC} +0.3	V	
Maximum Total Output Current (1)	$-\Sigma I_{O1}$	25	mA	(Note 3)
Maximum Total Output Current (2)	ΣI_{O2}	25	mA	(Note 3)
Operating Temperature	T_{opr}	−40 to +85	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

(NOTE) 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under the conditions of "ELECTRICAL CHARACTERISTICS-1, -2." If these conditions are exceeded, it could be cause of malfunction of LSI and affects reliability of LSI.
2. All voltages are with respect to GND.
3. Maximum Total Output Current is the total sum of output currents which can flow out or in simultaneously.
4. Power supply condition $V_{CC} \geqq V1 \geqq V2 \geqq V3 \geqq GND$ should be maintained.

- **ELECTRICAL CHARACTERISTICS – 1 (V_{CC} = 2.5 to 5.5V, T_a = –40 to +85°C)**

Item	Symbol	Test Conditions	Value min	Value max	Unit	Note
Input "Low" Voltage	V_{IL}		–0.3	0.15·Vcc	V	
Input "High" Voltage	V_{IH}		0.85·Vcc	Vcc + 0.3	V	(11)
Output "Low" Voltage	V_{OL}	I_{OL} = 0.4 mA	–	0.4	V	
Output "High" Voltage (1)	V_{OH1}	$-I_{OH}$ = 0.08 mA	Vcc–0.5	–	V	(1)
Output "High" Voltage (2)	V_{OH2}	$-I_{OH}$ = 0.01 mA	Vcc–0.4	–	V	(2)
Driver Voltage Descending (COM)	Vd1	Id = 0.05 mA	–	0.5	V	(15)
Driver Voltage Descending (SEG)	Vd2	Id = 0.01 mA	–	0.5	V	(15)
Dividing Resistor of LCD Power Supply	Rwell		25	300	kΩ	
Interrupt Input Hold Time	tINT		2·T_{inst}	–	μs	(13)
Output "High" Current	I_{OH}	V_{OH} = Vcc	–	4	μA	(3)
Input Leakage Current	I_{IL}	V_{in} = 0 to Vcc	–	2	μA	(4), (11)
Pull up MOS Current	$-I_P$	Vcc = 3V	10	100	μA	
Supply Current	I_{CC}	V_{in} = Vcc, Vcc = 3V R_f Oscillation (f_{osc} = 200 kHz) External Clock Operation (f_{cp} = 200 kHz)	–	0.3	mA	(5)
Standby I/O Leakage Current	I_{LS}	$\overline{HLT}$ = 0.5V, Vin = 0 to Vcc	–	1	μA	(6), (11)
Standby Supply Current (1)	I_{CCS1}	Vin = Vcc, $\overline{HLT}$ = 0.1V, Vcc = 2.5 to 3.5V	–	6	μA	(14)
Standby Supply Current (2)	I_{CCS2}	Vin = Vcc, $\overline{HLT}$ = 0.1V, Vcc = 3.0V	–	21	μA	(7)
LCD Display Voltage	V_{LCD}	Vcc–V_3	2.5	Vcc	V	(10)
Frame Frequency of LCD Drive	f_F	n = 1 (static) n = 2 (1/2 Duty) n = 3 (1/3 Duty) n = 4 (1/4 Duty)	$\frac{1}{256 \times n \times T_{inst}}$		Hz	(12)
External Clock Operation; System Clock						
External Clock Frequency	f_{cp}		130	300	kHz	(8), (12)
External Clock Duty	Duty		45	55	%	(8)
External Clock Rise Time	t_{rcp}		0	0.2	μs	(8)
External Clock Fall Time	t_{fcp}		0	0.2	μs	(8)
Instruction Cycle Time	T_{inst}	$T_{inst} = 4/f_{cp}$	13.3	30.7	μs	(8)
Internal Clock Operation (R_f Oscillation); System Clock						
Clock Oscillation Frequency	f_{osc}	R_f=270kΩ±2%	Vcc = 2.5 to 3.5V	130	270	kHz	(9)
			Vcc = 2.5 to 5.5V	130	300		
Instruction Cycle Time	T_{inst}	$T_{inst}=4/f_{osc}$	Vcc = 2.5 to 3.5V	14.8	30.7	μs	(9)
			Vcc = 2.5 to 5.5V	13.3	30.7		
Clock Oscillation Frequency	f_{osc}	R_f = 62kΩ ± 2%	Vcc = 4.5 to 5.5V	600	1000	kHz	(9)
			Vcc = 2.5 to 5.5V	420	1000		
Instruction Cycle Time	T_{inst}	$T_{inst} = 4/f_{osc}$	Vcc = 4.5 to 5.5V	4.0	6.7	μs	(9)
			Vcc = 2.5 to 5.5V	4.0	9.5		

(NOTE) All voltages are with respect to GND.

• ELECTRICAL CHARACTERISTICS-2 (T_a = -40 to +85°C)

Item	Symbol	Test Conditions	Value		Unit	Note
			min	max		
Halt Duration Voltage	V_{DH}	$\overline{HLT}$ = 0.2V	2.3	–	V	(16)
Halt Current	I_{DH}	V_{in} = V_{CC}, $\overline{HLT}$ = 0.2V, V_{DH} = 2.3V	–	4.0	μA	(16), (18)
Halt Delay Time	t_{HD}		100	–	μs	(16)
Operation Recovery Time	t_{RC}		100	–	μs	(16)
$\overline{HLT}$ Fall Time	t_{fHLT}		–	1000	μs	(16)
$\overline{HLT}$ Rise Time	t_{rHLT}		–	1000	μs	(16)
$\overline{HLT}$ "Low" Hold Time	t_{HLT}		400	–	μs	(16)
$\overline{HLT}$ "High" Hold Time	t_{OPR}		100	–	μs	(16)
RESET Pulse Width (1)	t_{RST1}	External Reset, $\overline{HLT}$ = V_{CC}	1	–	ms	(17)
RESET Pulse Width (2)	t_{RST2}	External Reset, $\overline{HLT}$=V_{CC}, V_{CC}=2.5V to 5.5V	2·Tinst	–	μs	(17)
RESET Rise Time	t_{rRST}	External Reset, $\overline{HLT}$ = V_{CC} V_{CC} = 2.5 to 5.5V	–	100	μs	(17)
RESET Fall Time	t_{fRST}	External Reset, $\overline{HLT}$ = V_{CC} V_{CC} = 2.5 to 5.5V	–	100	μs	(17)
INT_0, INT_1 Rise Time	t_{rINT}		–	50	μs	(13)
INT_0, INT_1 Fall Time	t_{fINT}		–	50	μs	(13)

(NOTE) 1. Applied to PMOS load of CMOS output pins and CMOS I/O common pins among D and R pins.
2. Applied to CMOS output pins, CMOS I/O common pins, input pins with pull up MOS, and I/O common pins with pull up MOS among D and R pins.
3. Applied to open-drain output pins and open-drain I/O common pins among D and R pins.
4. Pull up MOS current is excluded.
5. Applied to the supply current when the LCD-IV is in the reset state and the crystal oscillation for timer doesn't operate. (Current that flows in input/output circuit and in the power supply circuit for LCD is excluded).
Test Conditions: RESET, $\overline{HLT}$ = V_{CC} (Reset State), $\overline{TEST}$ = V_{CC}
D_{14}/XO, D_{15}/XI — D_{14}/XO, D_{15}/XI = V_{CC} (Crystal oscillation for timer is not selected.)
D_{14}/XO = Open, D_{15}/XI = V_{CC} (Crystal oscillation for timer is selected.)
V_1, V_2, V_3 = V_{CC}
COM_1 to COM_4, SEG_1 to SEG_{32} = Open
When the crystal oscillation for timer operates, the standby supply current (2) I_{CCS2} flows in addition to I_{CC}.
When the LCD-IV is installed in the user's system, and in operation current increases according to the external circuitry and devices. Those are connected to the LCD-IV. User should design the power supply in consideration of this point. (The difference between the measured current in the above reset state and that measured in the operational state in the user's system is the increased part of the supply current).
6. Standby I/O leakage current is the leakage current of I/O pins in the "Halt" and "Disable" state.
7. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded. The standby supply current (2) is the supply current at V_{CC} = 3.0V in "Halt" state in the case that the crystal oscillation for timer is selected (only the crystal oscillator for timer, 5-bit divider and 6-bit prescaler are in operation).

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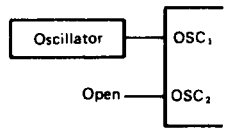
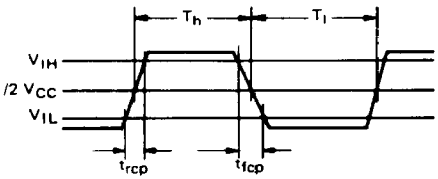
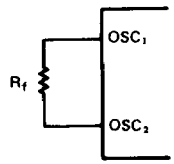
8. Applied to external clock operation. (system clock)





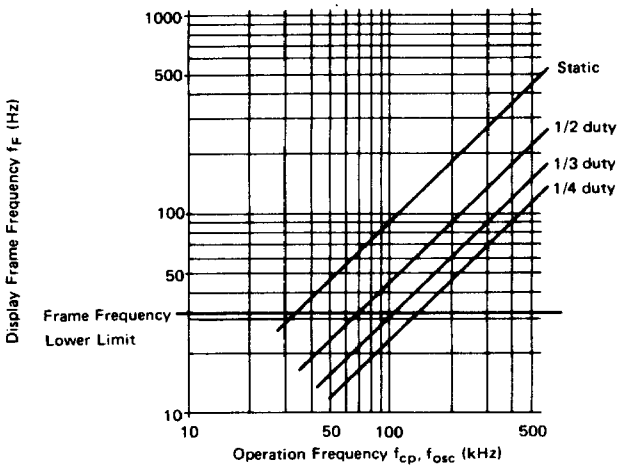
$$\text{Duty} = \frac{T_l}{T_h + T_l} \times 100\%$$

9. Applied to internal clock operation using resistor R_f. (System Clock)

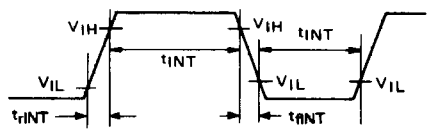


Wiring OSC_1 and OSC_2 pins should be as short as possible because the oscillation frequency is modified by capacitance of these pins.

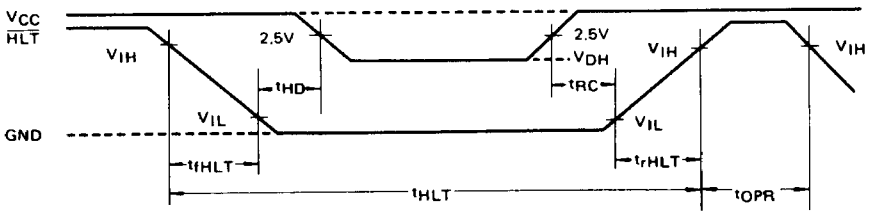
10. Power supply condition $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq GND$ should be maintained.
11. Applied to input pins, I/O common pins among D and R pins, and RESET, HLT, OSC_1, INT_0, INT_1 pins.
12. Lower limit of operation frequency is determined by liquid crystal display duty. Flutter occurs on liquid crystal display if frame frequency is under 32 Hz. Therefore operation frequency should be determined to prevent that frame frequency becomes under 32 Hz.
    The following shows the relation between liquid crystal display frame frequency and operation frequency.



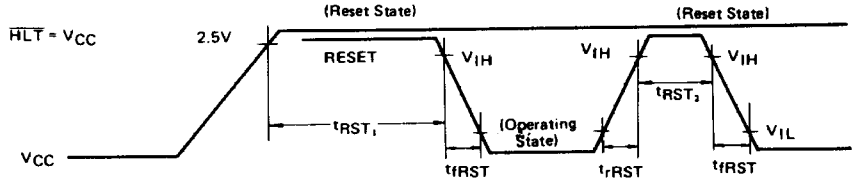
13. INT_0 and INT_1 inputs must be retained for two or more instruction cycle time at both "High" and "Low" levels.



14. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded. The standby supply current (†) is the supply at V_{CC} = 2.5 to 3.5V in "Halt" state in the case that the crystal oscillation for timer is not selected. The supply current when supply voltage fails to the Halt Duration Voltage is called "Halt Current" (I_{DH}). (shown in ELECTRICAL CHARACTERISTICS –2).
15. The voltage that drops between the power supply pins (V_{CC}, V_1, V_2, V_3) and each common or segment output pin.
16. External Halt Timing Chart

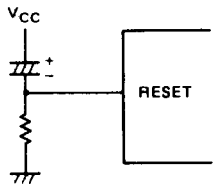


17. RESET Input Condition



- $tRST_1$ includes the time required from the power ON until the operation gets into the constant state.
- $tRST_2$ is applied when the operation is in the constant state.

Reset circuit at power on is not installed. Simple reset circuit at power on is the following.



18. The supply current at V_{CC} = V_{DH} = 2.3V in "Halt" state, in the case that the crystal oscillation for timer is not selected. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded.

■ SIGNAL DESCRIPTION

The input and output signals for the LCD-IV shown in PIN ARRANGEMENT are described in the following paragraphs.

• V_{CC} and GND

Power is supplied to the LCD-IV using these two pins. V_{CC} is power and GND is the ground connection.

• RESET

The LCD-IV can be reset by pulling RESET High.
Refer to RESET FUNCTION for additional information.

• OSC_1 and OSC_2

These pins provide control input for the on-chip clock oscillator circuit. A resistor, a ceramic filter circuit, or an external oscillator can be connected to these pins to provide a system clock with various degreeds of stability/cost trade-offs. Lead length and stray capacitance on these two pins should be minimized.

Refer to OSCILLATOR for recommendations about these pins.

• $\overline{HLT}$

This pin is used to enter the LCD-IV into the HALT state (Stand-by Mode). The LCD-IV can be moved into the halt state by pulling $\overline{HLT}$ low.

In the halt state the internal clock stops and all the internal statuses (RAM, Registers, Carry, Status, Program Counter, etc.) are maintained. Consequently power consumption is greatly reduced. By pulling $\overline{HLT}$ high, the LCD-IV starts operation from the status just before the halt state.

Refer to HALT FUNCTION for details of halt mode.

• $\overline{TEST}$

This pin is not for user application and must be connected to V_{CC}.

• INT_0 and INT_1

These pins generate interrupt request to the LCD-IV.
Refer to INTERRUPT for additional information.