



# CEP80N75/CEB80N75

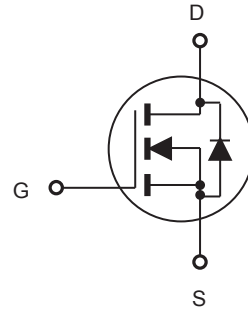
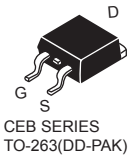
## CEF80N75

### N-Channel Enhancement Mode Field Effect Transistor

#### FEATURES

Type	V <sub>DSS</sub>	R <sub>DS(ON)</sub>	I <sub>D</sub>	@V <sub>GS</sub>
CEP80N75	75V	13mΩ	80A	10V
CEB80N75	75V	13mΩ	80A	10V
CEF80N75	75V	13mΩ	80A <sup>e</sup>	10V

- Super high dense cell design for extremely low R<sub>DS(ON)</sub>.
- High power and current handling capability.
- Lead free product is acquired.
- TO-220 & TO-263 & TO-220F full-pak for through hole.



#### ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263	TO-220F	
Drain-Source Voltage	V <sub>DS</sub>	75		V
Gate-Source Voltage	V <sub>GS</sub>	±20		V
Drain Current-Continuous	I <sub>D</sub>	80	80 <sup>e</sup>	A
Drain Current-Pulsed <sup>a</sup>	I <sub>DM</sub> <sup>f</sup>	320	320 <sup>e</sup>	A
Maximum Power Dissipation @ T <sub>C</sub> = 25°C - Derate above 25°C	P <sub>D</sub>	200	75	W
		1.3	0.5	W/°C
Single Pulsed Avalanche Energy <sup>d</sup>	E <sub>AS</sub>	880	880	mJ
Single Pulsed Avalanche Current <sup>d</sup>	I <sub>AS</sub>	45	45	A
Operating and Store Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 175		°C

#### Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	R <sub>θC</sub>	0.75	2	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θA</sub>	62.5	65	°C/W



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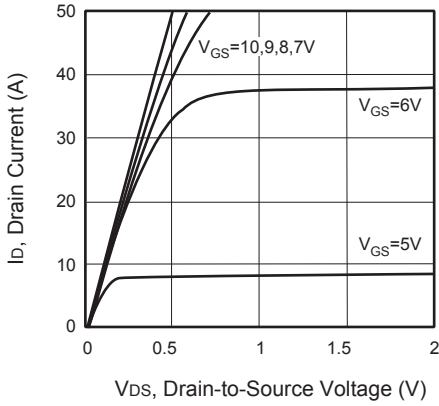
### Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	75			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60V, V_{GS} = 0V$			1	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
<b>On Characteristics <sup>b</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 40A$		10	13	m $\Omega$
<b>Dynamic Characteristics <sup>c</sup></b>						
Forward Transconductance	$g_{FS}$	$V_{DS} = 15V, I_D = 40A$		45		S
Input Capacitance	$C_{iss}$	$V_{DS} = 25V, V_{GS} = 0V, f = 1.0\text{ MHz}$		3550		pF
Output Capacitance	$C_{oss}$			580		pF
Reverse Transfer Capacitance	$C_{rss}$			40		pF
<b>Switching Characteristics <sup>c</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 37.5V, I_D = 45A, V_{GS} = 10V, R_{GEN} = 4.7\Omega$		24	48	ns
Turn-On Rise Time	$t_r$			5	10	ns
Turn-Off Delay Time	$t_{d(off)}$			61	122	ns
Turn-Off Fall Time	$t_f$			18	36	ns
Total Gate Charge	$Q_g$	$V_{DS} = 60V, I_D = 75A, V_{GS} = 10V$		79.3	105.5	nC
Gate-Source Charge	$Q_{gs}$			20.6		nC
Gate-Drain Charge	$Q_{gd}$			25.9		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S^g$				75	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = 75A$			1.5	V
<b>Notes :</b> <input type="checkbox"/> a.Repetitive Rating : Pulse width limited by maximum junction temperature . b.Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . <input type="checkbox"/> c.Guaranteed by design, not subject to production testing. <input type="checkbox"/> d.L = 0.87mH, $I_{AS} = 45A, V_{DD} = 38V, R_G = 25\Omega$ , Starting $T_J = 25^\circ\text{C}$ . e.Limited only by maximum temperature allowed . f.Pulse width limited by safe operating area . g.Full package $I_{S(max)} = 51A$ .						

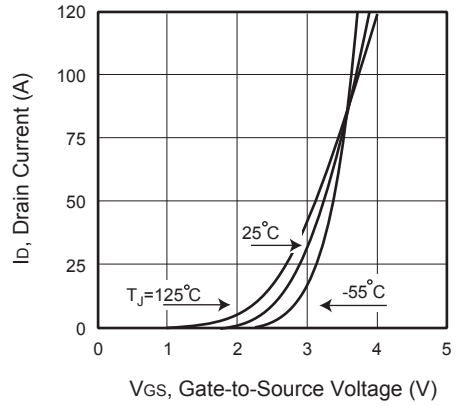


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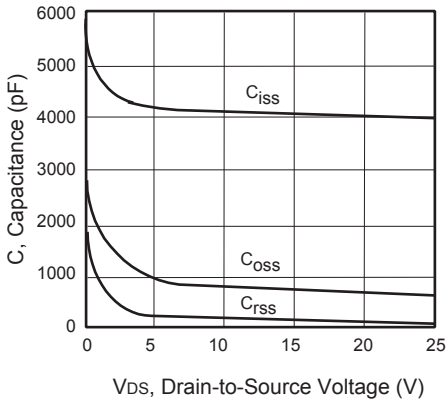
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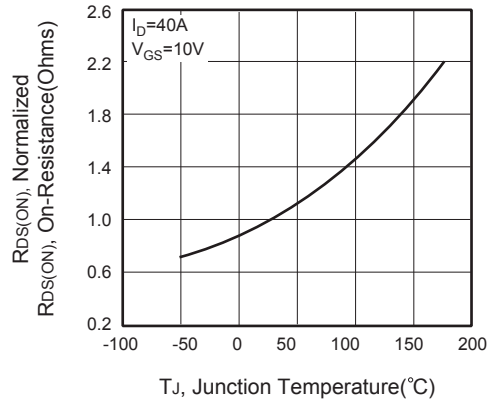
**Figure 1. Output Characteristics**



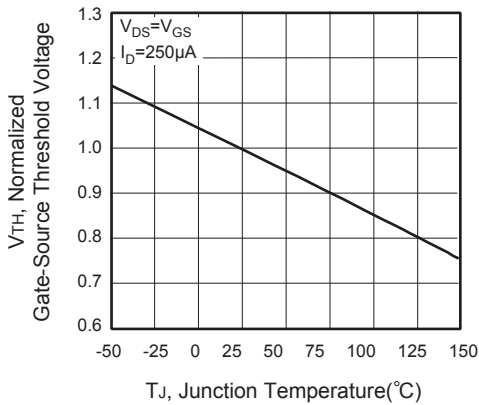
**Figure 2. Transfer Characteristics**



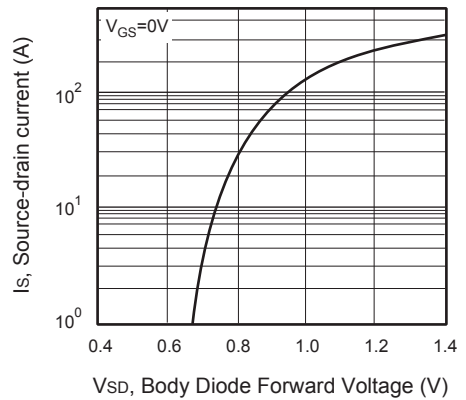
**Figure 3. Capacitance**



**Figure 4. On-Resistance Variation with Temperature**



**Figure 5. Gate Threshold Variation with Temperature**



**Figure 6. Body Diode Forward Voltage Variation with Source Current**



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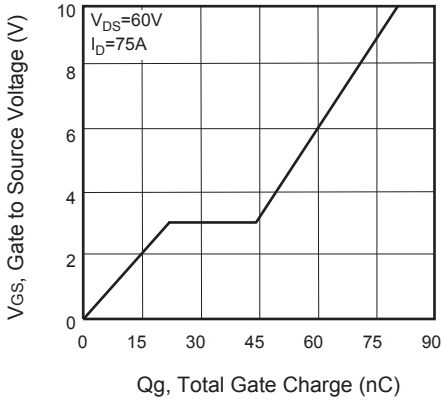


Figure 7. Gate Charge

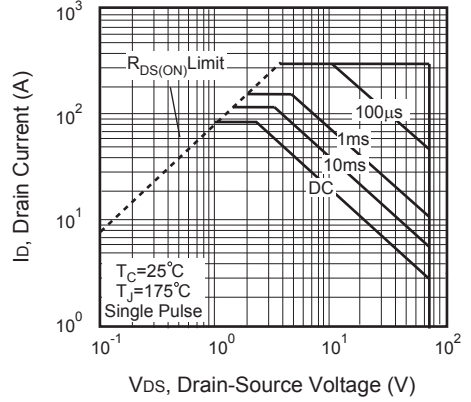


Figure 8. Maximum Safe Operating Area

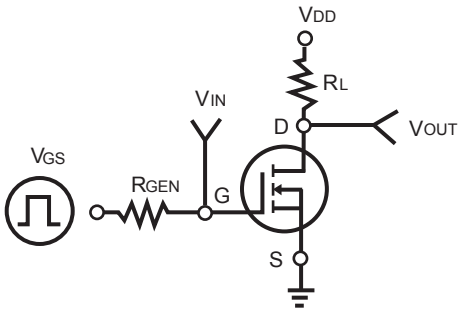


Figure 9. Switching Test Circuit



Figure 10. Switching Waveforms

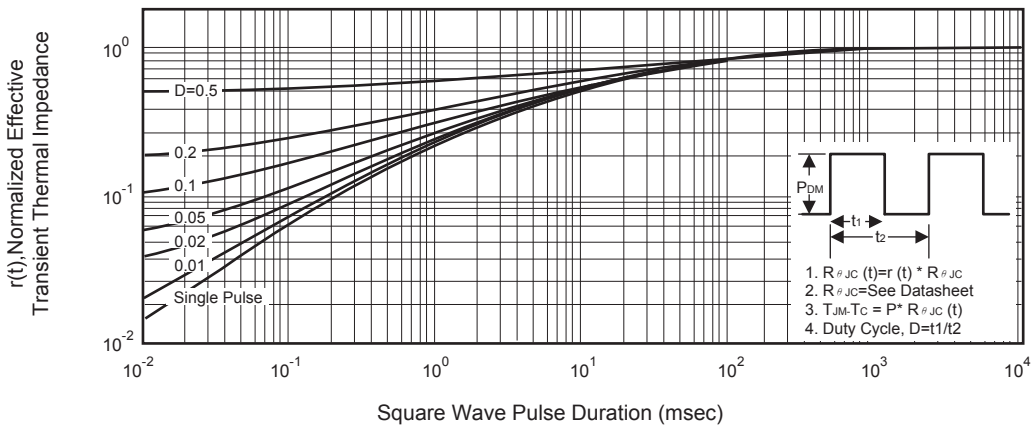


Figure 11. Normalized Thermal Transient Impedance Curve