Wide Discriminator
Monolithic IC MM1327

Outline

This IC identifies the letter box portion of wide broadcast, etc. video signals. The luminance and chroma signals are used so that the rate of identification on dark screens is increased. Output is the total of 6bit ADC data and character signal, etc. white peak signal discriminator bit, for 7bit data output.
In addition, an EDTV2 simple discrimination function is built-in.

Features

1. Signal level discrimination using composite luminance and chroma signal
2. Discrimination of video signal within horizontal scanning interval can be done every scan due to integrated output
3. Built-in white peak detection circuit for subtitles
4. Built-in EDTV2 simple discrimination function
5. 22H discrimination output (COMB-THROUGH) circuit built-in
6. Built-in window limiter circuit
7. Data output is 7bit serial output format : 6bit ADC + peak detection
8. Operates on +5V single power supply

Package

SDIP-30

Applications

Wide TV

Block Diagram

Pin Assignment

SDIP-30
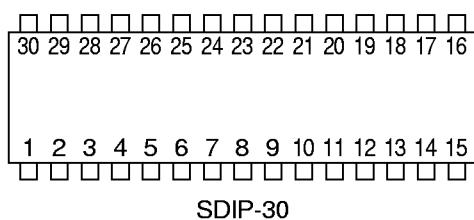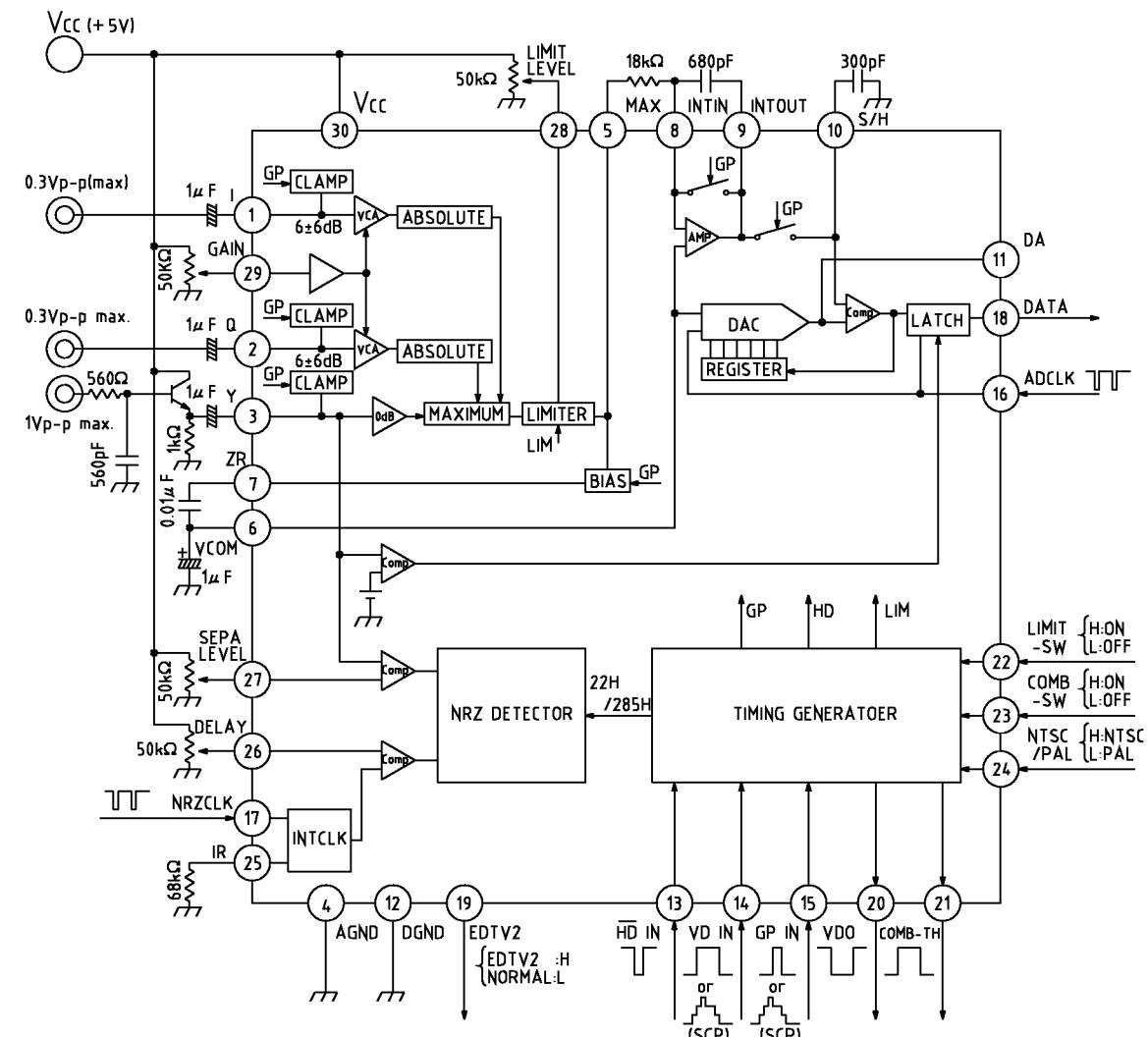
1	I	16	ADCLK
2	Q	17	NRZCLK
3	Y	18	DATA
4	AGND	19	EDTV2
5	MAX	20	VDO
6	VCOM	21	COMB–TH
7	ZR	22	LIMIT–SW
8	INT IN	23	COMB–SW
9	INT OUT	24	NTSC/PAL
10	S/H	25	IR
11	DA	26	DELAY
12	DGND	27	SEPA–LEVEL
13	HD	28	LIMIT–LEVEL
14	VD	29	GC
15	GP	30	Vcc

Pin Description

Pin no.	Pin name	Function	Internal equivalent circuit diagram
1	I	Video signal input pin	
2	Q		
3	Y		
4	AGND		
12	DGND		
5	MAX	Composite output of input video signal maximum value	
6	VCOM	Internal reference voltage output Connect 1μF between this pin and GND.	
7	ZR	Connection pin for MAX output clamp capacitor	
8	INT IN	Integrated circuit input pin Integrated reset done at GP timing.	
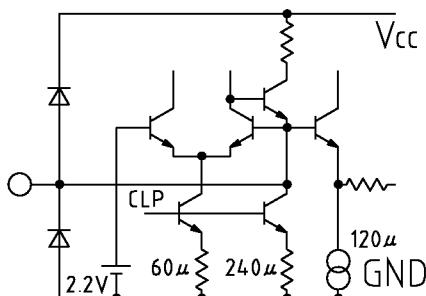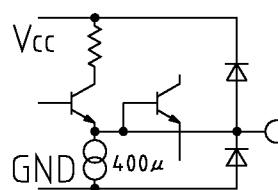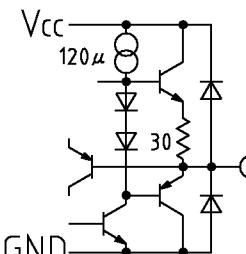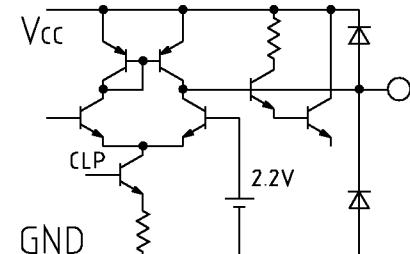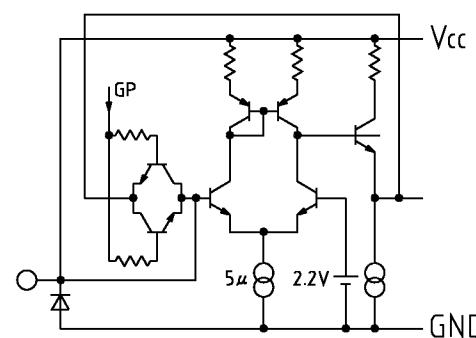
Pin no.	Pin name	Function	Internal equivalent circuit diagram
9 10	INT OUT S/H	Integrated output pin and sample and hold pins S/H of integration results at HD timing	
11	DA	DAC output for consecutive comparison ADC	
13 15	$\overline{\text{HD}}$ IN GP IN	Timing pulse input pins GP operates even on SCP input (5V$_{\text{P-P}}$).	
14	VD IN	Timing pulse input pin VD operates even on SCP input (5V$_{\text{P-P}}$).	
16	ADCLK	Clock input pin for consecutive ADC	
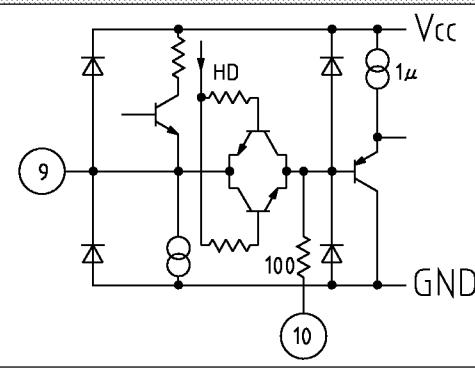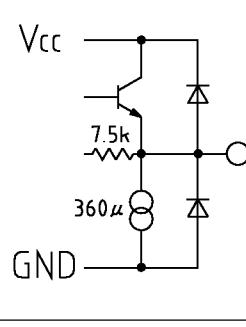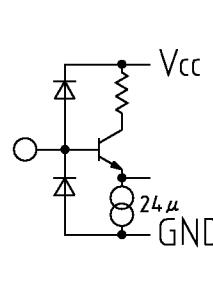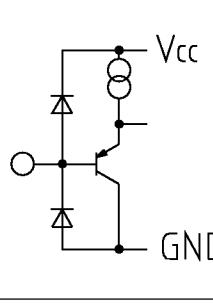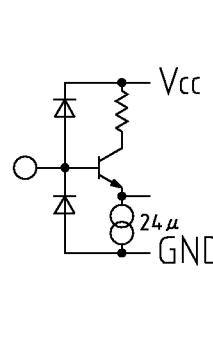
Pin no.	Pin name	Function	Internal equivalent circuit diagram
17 25 26	NRZCLK IR DELAY	Clock input pins for NRZ discrimination Input CLK is integrated by resistor connected between Pin 25 and GND and internal 20pF, and delay is set by Pin 26 voltage.	
18 19 20 21	DATA EDTV2 VDO COMB–TH	Data output pins	
22 23 24	LIMIT–SW COMB–SW NTSC/PAL	Switching pins	
27	SEPA LEVEL	NRZ discrimination luminance signal SEPA level adjustment pin	
28	LIMIT LEVEL	MAX composite output limit level adjustment pin Limit area: NTSC : 42~241H PAL : 46~291H	
29	GAIN	I, Q gain adjustment pin	
30	Vcc		

Absolute Maximum Ratings

Item	Symbol	Ratings	Units
Operating temperature	T_{OPR}	–20~+75	°C
Storage temperature	T_{STG}	–40~+125	°C
Power supply voltage	V_{CC} max.	7.0	V
Input voltage	V_{IN} max.	$GND \le V_{IN} \le V_{CC}$	V
Allowable loss	Pd	800	mW

Recommended Operating Conditions

| Item	Symbol	Ratings	Units
Operating temperature	T_{OPR}	–20~+75	°C
Operating voltage	V_{OPR}	4.5~5.5	V

Electrical Characteristics (Except where noted otherwise, Ta=25°C, Vcc=5.0V)

Item			Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Consumption current			I_{CC}			20	30	mA
MAX amp								
Clamping level		Y	V_{YIN}	∗1	2.0	2.2	2.4	V
		I	V_{IIN}	∗1	2.0	2.2	2.4	
		Q	V_{QIN}	∗1	2.0	2.2	2.4	
MAX output pin voltage			V max.	∗1	2.0	2.2	2.4	V
Maximum input level		Y	V max.$_Y$		1.0			V_{P-P}
		I	V max.$_I$		0.6			
		Q	V max.$_Q$		0.6			
Y input voltage gain			G_Y	∗2	–0.5	0.0	0.5	dB
VCA	Maximum gain	I	G max.$_I$	V_{GC}=1.2V ∗3	+11.5	+12.0	+12.5	dB
		Q	G max.$_Q$	V_{GC}=1.2V ∗3	+11.5	+12.0	+12.5	
	Minimum gain	I	G min.$_I$	V_{GC}=3.6V ∗3	–0.5	0.0	0.5	dB
		Q	G min.$_Q$	V_{GC}=3.6V ∗3	–0.5	0.0	0.5	
	I, Q gain difference		$\triangle G_{IQ}$	$\triangle G_{IQ}=G_I-G_Q$	–0.5	0.0	0.5	dB
EDTV Ⅱ discrimination								
NRZ detection level		L	V_{YSL}			5	7	IRE
		H	V_{YSH}		27	30		
NRZ detection readout timing		L	V_{CSL}			0.4	0.7	μS
		H	V_{CSH}		1.5	1.8		
NRZCLK pin input current		L	I_{NRZCL}	V_{NRZCLK}=0.4V			1	μA
		H	I_{NRZCH}	V_{NRZCLK}=4.5V			1	
IR pin voltage			V_{IR}		2.2	2.4	2.6	V
EDTV Ⅱ output voltage L			V_{NL}	I_{NL}=1mA			0.4	V
Trigger signal								
Sync signal separation level		HD$_{IN}$	V_{THD}	HD	2.30	2.50	2.70	V
		VD$_{IN}$	V_{TVD}	VD or SCP	0.63	0.83	1.03	
		GP$_{IN}$	V_{TGP}	GP or SCP	3.69	3.89	4.09	
HD pin input current		L	I_{HDL}	V_{HD}=0.4V			1	μA
		H	I_{HDH}	V_{HD}=4.5V			1	
VD pin input current		L	I_{VDL}	V_{VD}=0.4V			1	μA
		H	I_{VDH}	V_{VD}=4.5V			1	
GP pin input current		L	I_{GPL}	V_{GP}=0.4V			1	μA
		H	I_{GPH}	V_{GP}=4.5V			1	
COMB-SW switching voltage		L	V_{TCOSL}				0.7	V
		H	V_{TCOSH}		2.1			
COMB-TH output voltage L			V_{OCOMB}	I_{COMB}=1mA			0.4	V
VDO output voltage L			V_{OVDO}	I_{VDO}=1mA			0.4	V

Note 1 : *1 Clamp level and MAX output pin voltage

Measure voltage on each pin when GPIN and HDIN are connected to V$_{CC}$.

Note 2 : *2 Y input voltage gain

Input a sweep signal to Y input, input a clamp pulse synchronized to H$_{SYNC}$ to GPIN pin, and measure voltage gain at MAX pin for 100kHz.

Note 3 : *3 I, Q max/min gain

Input a square wave signal as shown below and a GPIN signal to I input (or Q input) and GPIN pin, and measure voltage gain at MAX pin.

```
                                  _____        _____   0.3V
   I or Q signal         _____|       |_____|       |
                                                      ---- 0V
                                 _                _    ------ 5V
   GP pin                       | |_____| |_____ 0V

                          2μS

                              63.5μS
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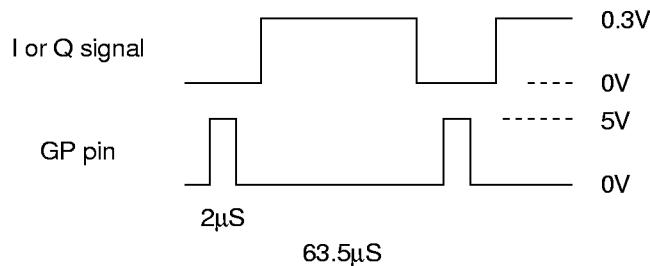
Note 4 : *4 MAX amp limit level

Measure limit level at MAX pin when LIMIT-SW pin is high. However, the limit range is as follows for the NTSC/PAL pin.

Note 5 : *5 Offset voltage for reset

Connect GPIN pin to V$_{CC}$ and measure potential difference between INT IN pin and INT OUT pin.

Note 6 : *6 Integrated limit voltage

Input a 100% white signal to Y input and a clamp pulse synchronized to H$_{SYNC}$ to GPIN pin. Measure INT OUT pin voltage at integration end at this time.

```
                            _____      ____
   Y input          _      |      |    |    |      100IRE
                   | |_____|      |____|    |____
                                              
   INT OUT output    X\_
                        \____
                             |_____       V$_{INTL}$
```

Timing Chart

Timing chart (1st diagram): Signals Composite, SCP, GP, VB, RB, VDO, COMB-TB over 1st field (259H, 260H, 261H, 262H) and 2nd field (1H–25H). Voltage levels for SCP: −5V, −2.8V, −1.7V, −0V; GP: −5V, −0V; VB: −5V, −0V; RB: −5V, −0V.

Timing chart (2nd diagram): Signals Composite, SCP, GP, VB, RB, VDO, COMB-TB over 1st field (260H, 261H, 262H, 263H) and 2nd field (1H–25H). Voltage levels for SCP: −5V, −2.8V, −1.7V, −0V; GP: −5V, −0V; VB: −5V, −0V; RB: −5V, −0V.

Timing Chart 2

1. The largest of Y, I and Q video input signals is output on MAX output pin.
2. MAX output date is integrated during horizontal scanning.
3. Integration results are sampled and held at HD pulse timing.
4. Consecutive comparison ADC outputs data as serial data.
   (Serial data is 1H delayed from video signal input.)
5. Output data configuration is as shown in the table below.

Data configuration

Y input	PEAK
Peak of more than 50IRE	1
No peak of more than 50IRE	0

Video	DATA
White scanning	00
	⇕
Black scanning	3F

Timing Chart 3
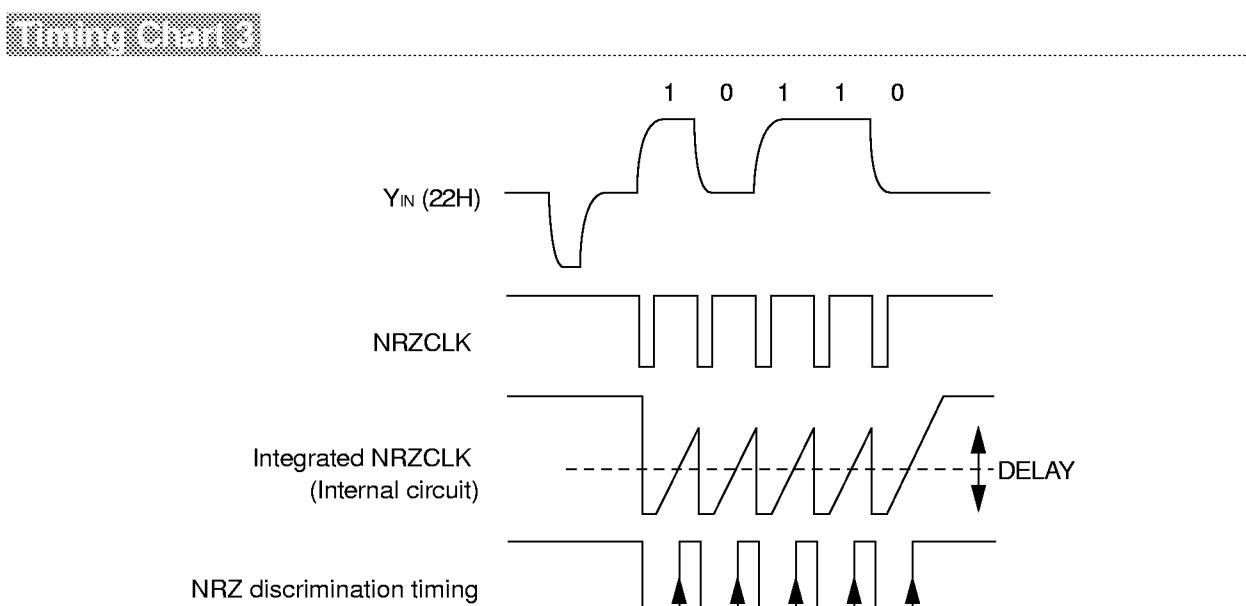
1. When Y$_{IN}$ input signal matches "10110" at NRZ discrimination timing, it is identified as an EDTV2 signal.
   EDTV2 pin is high for EDTV2 identification.

Measuring Circuit