TurboSPARC

Highly Integrated 32-bit RISC Microprocessor

FUJITSU

DATASHEET

January 1997

DESCRIPTION

The Fujitsu TurboSPARC Microprocessor is a high frequency, highly integrated single-chip CPU providing balanced integer and floating point performance. The TurboSPARC microprocessor is an implementation of the SPARC V.8 architecture and is ideally suited for low-cost uniprocessor applications.

The TurboSPARC microprocessor derives its high performance from a number of design techniques. A 170 MHz operating frequency, large 16 KByte instruction and 16 KByte data caches utilizing a *streaming* architecture which helps to minimize cache miss delays, numerous dedicated address translation caches, on-chip secondary cache and DRAM control interfaces, along with an efficient 9-stage pipeline, all combine to offer a device whose performance is at the cutting-edge of today's microprocessor technology.

The TurboSPARC microprocessor contains an Integer Unit (IU), Floating Point Controller (FPC), Floating Point ALU, Multiply, and Divide/Square Root Units, Instruction and Data caches, Memory Management Unit (MMU), and Secondary cache, DRAM, SBus, and AFX bus controllers. The various on-chip controllers help to increase performance while simplifying system design.

- The cache controller supplies all necessary secondary cache signals including a dedicated address bus and is capable of supporting up to 1 MByte of secondary cache.
- The DRAM controller contains all necessary signals for interfacing to industry standard page-mode DRAM's.
- The SBus controller handles the interface between the processor and other bus masters, and provides all of the signals as defined in the Sun Microsystems SBus Specification.
- The AFX graphics bus controller supplies all necessary signals for interfacing to the Sun Microsystems compatible AFX graphics bus.

Figures 1.0 and 2.0 show block diagrams of the TurboSPARC microprocessor and 512 KByte secondary cache.

FEATURES:

- SPARC V.8 32-bit High Performance RISC Architecture
- 170 MHz Operating Frequency
- 16 KByte Direct Mapped Instruction Cache
- 16 KByte Direct Mapped Data Cache
- 8-Window, 136-word Register File
- Supports up to 1 MByte of Secondary Cache
- On-chip Memory Management Unit
- Programmable On-chip memory controllers
- Programmable System Clock Frequencies
- 0.35 micron CMOS Technology
- Compatible with SunOS and Solaris
- Compatible with Current Software Applications
- IEEE 1149.1 Boundary Scan Test Interface

PRELIMINARY

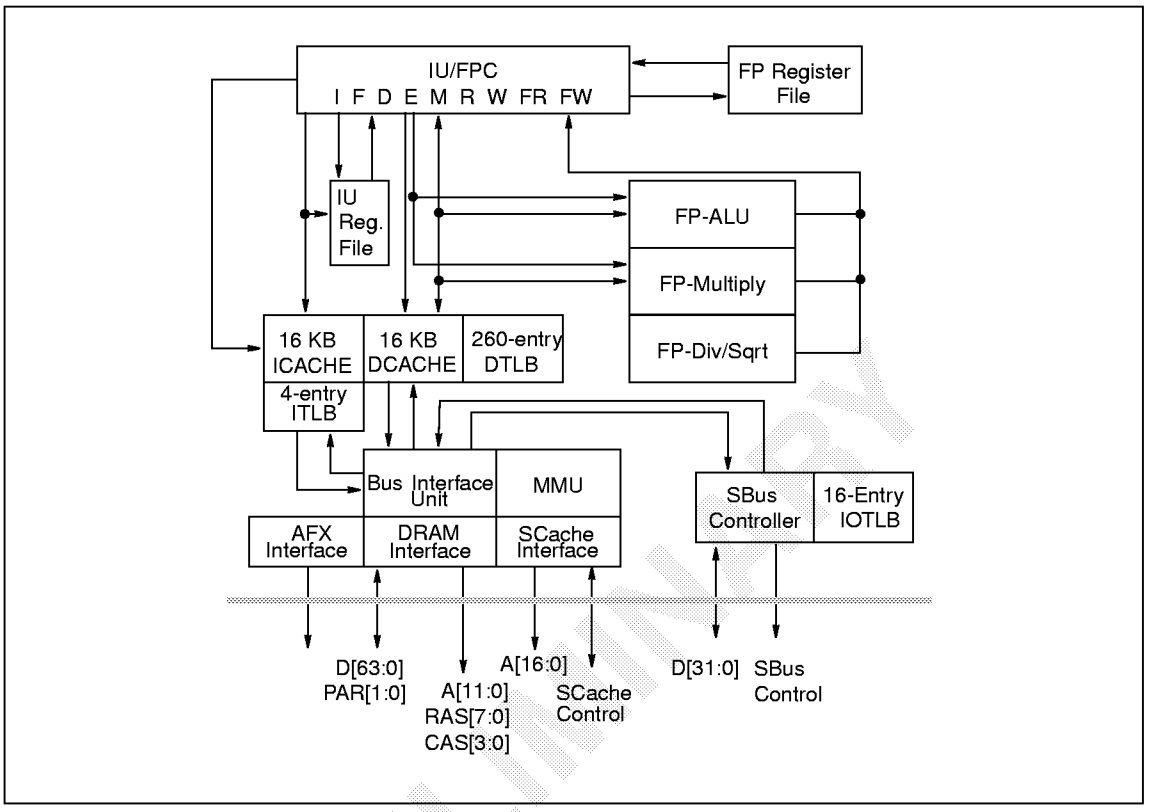

Figure 1. TurboSPARC CPU Block Diagram

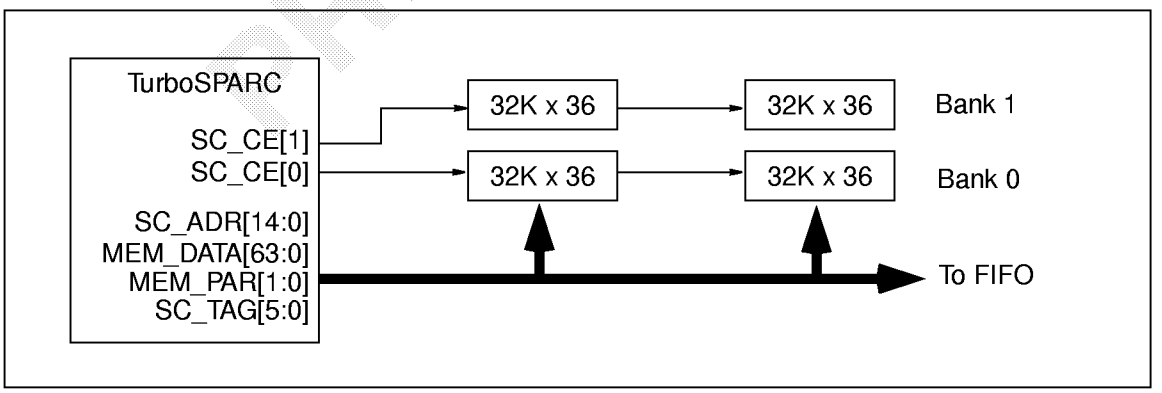

Figure 2. 512 KByte Secondary Cache Configuration

TECHNICAL OVERVIEW

Integer Unit/Floating Point Unit Controller

As shown in the block diagram, the integer unit (IU) and floating point control (FPC) are merged into a 9-stage pipeline. Below are some of the features of the IUFPC.

- 9-stage instruction pipeline.
- No branch folding. Branch instruction (taken/not-taken) execute in one cycle.
- Harvard architecture.
- IMUL and IDIV implemented using Floating Point Multiplier and Divider.
- Three read and one write port 8-Window register file.
- Single cycle store operation.
- Fully integrated pipelined FPC within IU pipeline.

The Floating Point Controller resides in stages D through FW. The floating point controller (FPC) can at most issue one floating point related instruction. All floating point ALU and MUL instructions complete in the FR stage. Floating point DIV instructions are pipelined in the M, R, and W stages, and complete in the FR stage. The floating point queue is 3-entries deep, with each instruction having a corresponding address (PC) entry. The integer multiply and divide instructions are also dispatched to FP-MUL and FP-DIV units respectively in the E-stage. The pipeline is held until the results are available and then written to integer unit register file in W stage.

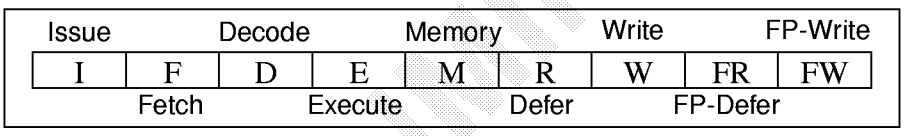

Figure 3. TurboSPARC Pipeline

Table 1. Instruction Latencies

Instruction	Cycles
Unsigned Integer Load	1
Signed Integer Load	2
Integer Single (Single)	1
Integer Load/Store (Double)	2
Atomics	3
FP Load/Store	1
CALL, Bicc, Bfcc	1
JMPL, RETT	2
Ticc (taken)	9
WRSPR	2
WRWIM, WRTBR, WRY	1
Arithmetical, Logical	1
Integer Multiply	7
Integer Divide	8-33
FP-ALU (faddx, fsubs, fxtox)	4
FP-MUL (fmulx, fsmuld)	4
FP-DIV (fdivd)	8-50 (35 Typical)
FP-DIV(fdivds)	8-27 (21 Typical)
FP-SQRT (fsqrtd)	8-50 (35 Typical)
FP-SQRT (fsqrts)	8-27 (21 Typical)
FP-CPY (fmovs, fnegs, fabs)	1

FLOATING POINT UNITS

The FP-MUL and FP-DIV/SQRT units handle both floating point and integer multiply and divide operations. The FP-ALU unit handles floating point add and subtract operations, while integer ALU operations are performed within the IU.

The floating point unit is made up of three arithmetic blocks (FALU, FMUL, FDIV) along with a fourth block (FPUIO) which serves as the interface between the three blocks and the Integer Unit/Floating Point Controller (IUFPC).

Integer and Floating Point Unit Register Files

The integer unit register file (IU-RF) unit includes the integer unit register file, which is comprised of three read ports and one write port. The floating point register file (FP-RF) unit contains the floating point register file, which consists of two read ports and one write port. Both register files contain bypass logic which provides a feedback loop on dependent operations.

Instruction Cache

The instruction cache is 16 KBytes in size and direct mapped. The cache is virtually indexed and virtually tagged. The instruction cache line size is 32 bytes. and implements a *'streaming'* cache architecture, which allows execution to resume after the first doubleword of an instruction cache line fill has been fetched. The remaining three doublewords of the line fill are fetched in the background. The result is that the cache is not blocked until the line fill is completed.

The instruction cache also includes a fully-associative 4-entry instruction TLB (ITLB) which contains only page table entries (PTE) and is accessed only on an instruction cache miss. In addition to the ITLB, an 8-bit context identifier is attached to each instruction cache entry. This identifier helps to differentiate between multiple processes within the same cache and helps to reduce cache flushing by allowing the operating system to invalidate only those lines whose process is no longer valid.

Data Cache

The data cache is also 16 KBytes in size and direct mapped. The data cache is virtually indexed, allowing data cache to be indexed at the same time as the translation lookaside buffer (TLB) is performing the virtual-to-physical address translation. If there is a hit to the primary data cache, data can be written or read in the same clock as the TLB lookup. In the case of a primary data cache miss, the virtual-to-physical address translation has already occurred and the secondary cache access can begin immediately. The data cache is physically tagged in order to maintain coherency with the secondary cache.

The data cache implements a write-back protocol and has a 32-byte fixed line size. The data cache also implements the *'streaming'* architecture, as defined in the instruction cache section above, and has a 32 byte write-back buffer. Each incoming data cache line is compared to a dirty bit RAM. Any dirty lines are written to the write-back buffer before the actual cache line can be filled. The subsequent write-back does not occur until after the line fill is completed.

The data cache has a flush mechanism by which all data cache lines can be invalidated with one operation. During a flush modified data is not written out before being invalidated.

To enhance data cache performance, a dedicated Data cache TLB is used to translate data cache addresses. This cache is divided into two sections, a 4-entry, fully associated Content Addressable Memory (CAM), and a 256-entry direct mapped RAM. In the multi-level address mapping scheme of the TurboSPARC processor, the CAM is dedicated to translating level 1 and level 2 page table entries, while the RAM translates level 3 entries.

Memory Management Unit (MMU)

The memory management unit (MMU) of the TurboSPARC microprocessor performs virtual-to-physical address translation as well as memory protection. Virtual-to-physical translation is done using a 4 KByte fixed page size. Any virtual page can be mapped to any available physical page. Memory protection is provided so that one process cannot read or write to the address space of another process. This allows multiple processes to reside in physical memory at the same time.

The MMU implements a three level virtual address mapping scheme, called a *'table walker'*. On a TLB miss, table-walking hardware generates the physical address for the requesting TLB virtual address by 'walking' through the three levels of page tables. The first and second levels contain *'Page Table Pointers'* (PTP), which are pointers to the next level down. The first level contains 256 entries, while the second and third levels each contain 64 entries. The third level is always a *'Page*

Table Entry' (PTE), which points to a physical page. Once the physical address pertaining to the virtual address of the TLB miss is determined, the address is driven out onto the bus and a secondary cache access is initiated.

Clock Interface

The TurboSPARC microprocessor provides dedicated clocks for the memory, SBus, and AFX graphics bus interfaces. Each of these clocks is derived from the internal CPU clock, which is a multiple of the input clock. The divide-by ratios for each clock is dependent on the state of certain input pins at power-up. Input pins such as IOC_RANGE, IOCLK_DIV2, and IOCLK_DIV6 allow the CPU to determine the correct divide ratio for each clock. Typically, the internal CPU clock is generated based on the output of the on-chip phase-locked-loop (PLL) circuit. However, the PLL can be bypassed by driving the PLL_BYP pin low at power-up. If PLL_BYP is sampled high at the falling edge of RESET, the EXT_CLK2 input bypasses the PLL circuitry and becomes HF_CLK.

The CPU clock, which is used by the internal circuits of the CPU, is a derivative of the High Frequency clock (HF_CLK), which in turn is a multiple of the input clock (EXT_CLK1) as shown in the table below.

The I/O clock is used for the secondary cache and main memory subsystems. As shown in the table below, the IOCLK_DIV2 input pin is used to determine the divide ratio from the HF_CLK for both the CPU clock and the I/O clock.

The SBus Clock is generated either as a divide by 4, 5 or 6 of the IO_CLK. Input pins DIV6[1:0] determine the divide ratio. The SBus clock must be within the range of 16.67 to 25 MHz.

The AFX graphics bus clock is derived from the IO_CLK based in the state of the IOC_RANGE[1:0] pins at reset. The AFX clock is divided from the IO_CLK as shown in the table below. The AFX clock must be within the range of 20 - 42 MHz in order to meet the AFX bus specification.

Table 2. CPU Clock Generation

EXT_CLK1	Multiple By	HF_CLK	Divide By	CPU_CLK	IOCLK_DIV2
25-75 MHz	8	200-600 MHz	2	100-300 MHz	1
25-75 MHz	12	300-900 MHz	2	150-450 MHz	0

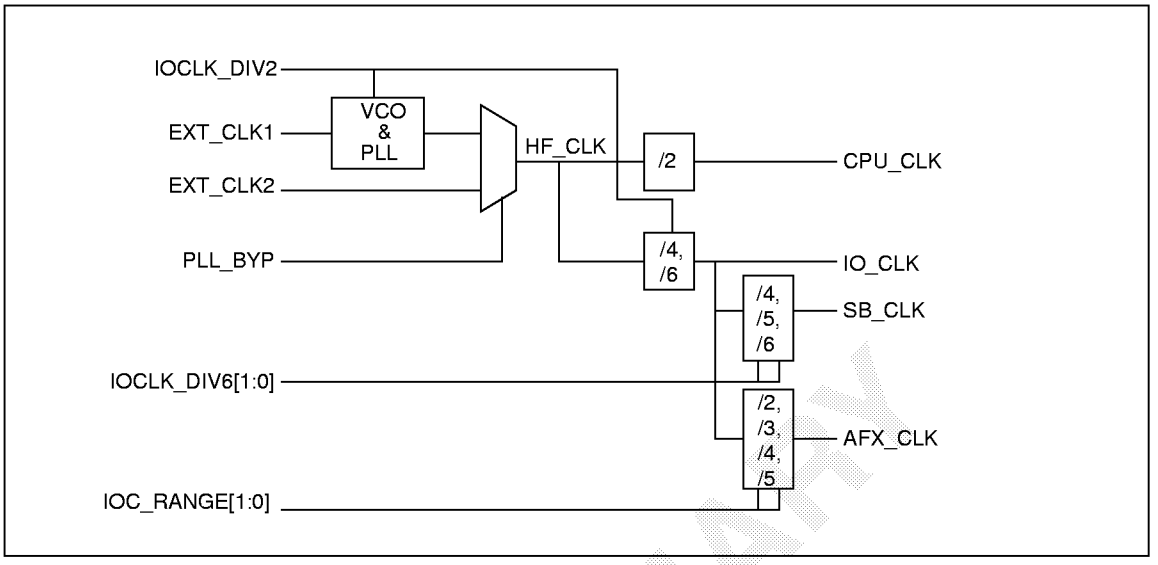

Figure 4. Clocking Scheme in the TurboSPARC Microprocessor

Table 3. I/O Clock Generation

EXT_CLK1	Multiple By	HF_CLK	Divide By	IO_CLK	IOCLK_DIV2
25-75 MHz	8	200-600 MHz	4	50-150 MHz	1
25-75 MHz	12	300-900 MHz	6	50-150 MHz	0

Table 4. SBus Clock Generation

IO_CLK	DIVISION	SB_CLK	IOCLK_DIV6[1:0]
[66.7-100]	4	[16.6-25.0]	0 x
[100.0-125.0]	5	[20.0-25.0]	1 0
[125.0-150.0]	6	[20.8-25.0]	1 1

Table 5. AFX Clock Generation

IO_CLK	AFX_CLK	DIVISION	IOC_RANGE[1:0]
[66.7-72.0]	[33.3-36.0]	2	00
[66.7-100.0]	[22.2-33.3]	3	01
[100.0-125.0]	[33.3-41.7]	3	01
[100.0-125.0]	[25.0-31.3]	4	10
[125.0-150.0]	[25.0-30.0]	5	11

Bus Interface Unit

The bus interface unit of the TurboSPARC microprocessor includes a DRAM interface, a secondary cache interface, an I/O (SBus) interface, and a graphics interface (AFX). The secondary cache interface contains a dedicated address bus and supports up to 1 MByte of SRAM memory.

The DRAM interface generates all standard DRAM control signals and can support up to 256 MBytes of memory divided into eight 32 MByte banks. A 64-bit external data bus is shared between the secondary cache and main memory interfaces and allows a cache line fill to be accomplished in four sequential memory transfers.

The Sbus interface supports up to five slots and contains a dedicated 16-entry IOTLB. The SBus supports I/O transactions between the processor and other SBus devices. The SBus has a direct virtual address memory interface and works in conjunction with the MMU to arbitrate for system and memory resources.

The AFX graphics bus contains a dedicated Sun Microsystems compatible interface which operates between 20 and 42 MHz.

SIGNAL DESCRIPTIONS

Signal	Type	Volts	Description
MEM_DATA[63:0]	I/O	3.5	64-bit memory data bus for transferring data to and from main memory.
MEM_PAR[1:0]	I/O	3.5	Bidirectional memory data parity pins. Parity is provided on a word basis (for DRAM only).
DRAM_ADDR[11:0]	Out	5	DRAM address pins. These memory address pins may require external buffering to provide the necessary drive for the memory array.
DRAM_RAS_[7:0]	Out	5	DRAM Row Address Strobe. Eight separate active low RAS signals, buffered externally to provide sufficient drive to connect directly to the DRAMs. Up to eight DRAM banks are supported.
DRAM_CAS_[3:0]	Out	5	DRAM Column Address Strobes. Four separate active low CAS signals are provided for word access. These signals may require external to provide sufficient drive to connect directly to the memory array. Two separate banks are supported by the four CAS lines.
DRAM_WE_	Out	5	DRAM Write Enable output pin. This active low signal may require external buffering to provide sufficient drive to connect directly to the memory array.
SC_CONFIG[2:0]	In	5	These bits encode the secondary cache size as well as the number of banks. The information on these pins is loaded into the SCC[2:0] field of the CPU configuration register.
SC_ADDR[16:0]	Out	3.5	Secondary cache address bus. How many bits are used depends on the size of the SRAM device being used. 32K x36 -bit SRAM devices use SC_ADDR[14:0]. 64 K x 18-bit SRAM devices use SC_ADDR[15:0]. 128K x 9-bit SRAM devices use SC_ADDR[16:0].
SC_CE[3:0]	Out	3.5	Secondary cache bank select signals select one of four possible SRAM bank s. Which bank is selected depends on the state of the SCC field in the CPU configuration register.

SIGNAL DESCRIPTIONS (continued)

Signal	Type	Volts	Description
SC_ADSC_	Out	3.5	Active low Secondary cache address strobe. Asserted along with SC_ADDR to indicate the start of a secondary cache access.
SC_ADV_	Out	3.5	Active low Secondary cache address Advance. This signal is typically asserted for 3 cycles following the assertion of SC_ADSC_, in order to read or write an entire cache line.
SC_GW_	Out	3.5	Active low Secondary cache global write. This signal is asserted for the duration of a cache line write cycle. All writes to the secondary cache are 64-bits wide.
SC_OE_	Out	3.5	Secondary cache output enable.
SC_TAG[5:0]	I/O	3.5	Secondary cache tag bits. These bits contain 5-bits (one-half) of the address tag, along with a valid bit. When paired with an adjacent cache entry, they compose a complete address tag.
SC_CLK[3:0]	Out	3.5	Secondary cache clock signals. These signals contain four duplicate copies of the same clock in order to minimize the loading on any given signal.
MF_RST_	Out	3.5	Active low memory FIFO reset.
MF_WCE_	Out	3.5	Active low memory FIFO write enable.
MF_RCE_	Out	3.5	Active low memory FIFO read enable.
MF_OEBA	Out	3.5	Memory FIFO output enable for enabling external cache data onto the CPU data bus.
MF_LE	Out	3.5	Memory FIFO latch enable.
MF_CLK[1:0]	Out	3.5	Memory FIFO clock signals.
AFX_AEN	Out	5	AFX bus address enable output. Indicates when valid address information is on the bus.
AFX_SREPLY[1:0]	Out	5	Graphics system reply. Driven by the processor and indicates that the graphics bus has been selected along with the type of access. On write cycles, the data follows in the following cycle. On read cycles, data is driven onto the bus in the same cycle as AFX_PREPLY is asserted. 00 = Idle, 01 = Idle, 10 = Single Write, 11 = Single Read
AFX_PREPLY[1:0]	In	5	Graphics bus port reply driven by the graphics bus slave. On writes cycles, assertion of this signal indicates that data has been removed from the write buffer. On read cycles, assertion indicates that read data is available in the read latch.
AFX_ADDR[15:13]	Out	5	Graphics bus address bits.
AFX_CLK	Out	5	Graphics clock output for the AFX bus. The AFX clock frequency is a derivative of the I/O clock as defined in the CPU configuration register. The frequency can range between 25 and 42 MHz. The clocks may be used in differential form to improve the common mode noise immunity at high clock rates.
SB_ADDR[27:0]	Out	5	SBus Address output pins provide the Physical Address to SBus slave devices.

SIGNAL DESCRIPTIONS (continued)

Signal	Type	Volts	Description
SB_DATA[31:0]	I/O	5	Bidirectional SBus data pins. The 32-bit SBus data pins provide SBus support for the CPU, and support DBMA cycle access via the CPU SBus controller.
SB_SEL_[4:0]	I/O	5	Output Slave Select pins. A separate active low slave select is driven to each SBus slot. The slave select pins are used in conjunction with the physical address for accessing each SBus device.
SB_SIZE[2:0]	I/O	5	Bidirectional SBus transfer Size description pins. These three pins encode the size of the data transfer of the current SBus operation.
SB_RD	I/O	5	Bidirectional SBus Read/Write pin. This pin indicates whether the current transfer is a read or a write operation.
SB_CLK[2:0]	Out	5	SBus clock frequency ranging from 16.6 MHz to 25 MHz. The actual frequency depends on the input frequency and its ratio to the I/O clock. Refer to Table 4.4.
SB_AS_	Out	5	SBus Address Strobe Output pin. This active low signal indicates that a valid address is on the SBus.
SB_ACK_[2:0]	I/O	5	SBus transfer acknowledge pins. The bidirectional ACK[2:0] pins encode the status of the current SBus transfer, from the slave.
SB_LERR_	In	5	SBus Late data Error input pin. This active low signal is driven by the current SBus slave, and aborts the current SBus transfer.
SB_BR_[5:0]	In	5	Active low Bus Request input pins. There is one pin per bus master.
SB_BG_[5:0]	Out	5	Active low Bus Grant output pins. There is one pin per bus master.
SB_CR_	Out	5	Active low SBus CPU request output. For Debug purposes only.
SB_CG_	Out	5	Active low SBus CPU grant output. For Debug purposes only.
IRL[3:0]	In	5	The four interrupt request line input pins encode the highest priority interrupt pending. These pins are driven by the external interrupt logic chip directly to the CPU.
CP_STAT_[1:0]	Out	5	Active low CP Status output pins. Used to indicate CP interrupt/trap status as follows: 11 - Normal 10 - Level 15 interrupt 01 - Trap occurred, when trap disabled 00 - Reserved
EXT_CLK1	In	5	CPU input clock pin. EXT_CLK1 is used to synchronize the phase lock loop (PLL).
EXT_CLK2	In	5	CPU input clock pin. EXT_CLK2 becomes HF_CLK when BYP_PLL = 0.
PLL_BYP_	In	5	Selects either Phase Lock Loop (when high) or the clock inputs directly (when low).
IOCLK_DIV2	In	5	Determines the divide ratio between the CPU clock and the I/O clock.

SIGNAL DESCRIPTIONS (continued)

Signal	Type	Volts	Description
IOCLK_DIV6[1:0]	In	5	Determines the divide ratio between the I/O clock and the SBus clock.
IOC_RANGE[1:0]	In	5	Determines the divide ratio between the I/O clock and the AFX clock.
RESET_	In	5	Power-up reset input pin. This signal is active low.
STANDBY	In	5	Input pin to put the CPU in Standby mode. Apply a low logic level in normal operation.
JTAG_CLK	In	5	Test (JTAG) input clock for boundary scan registers.
JTAG_TMS	In	5	Test Mode Select input pin.
JTAG_TDI	In	5	Test Data Input pin (JTAG standard).
JTAG_TRST	In	5	JTAG Reset pin (JTAG standard).
JTAG_TDO	Out	3.5	Test Data Output pin (JTAG standard).

ELECTRICAL SPECIFICATIONS

Table 6. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply Voltage	V_{DD1}, V_{DD3}, V_{DD4}	-0.5	4	V
	V_{DD2}	-0.5	6	V
Input Voltage (5v)	V_{IN}	-0.5	6	V
Input Voltage (3v)	V_{IN}	-0.5	4	V
Input Clamp Current (any pin)	I_i	-20	20	mA
Ambient Temperature	T_a	0	70	°C
Storage Temperature	T_s	-45	125	°C
Static Discharge Voltage		-	2000	V

Table 7. Recommended Operating Conditions

Parameter		Symbol	170 MHz		Units	Comments
			Min	Max		
Core Supply Voltage		V_{DD1}	3.325	3.605	V	3.5 V +3% - 5%
I/O Supply Voltage	5.0V	V_{DD2}	4.75	5.25	V	5.0 V +/- 5%
	3.5V	V_{DD3}	3.325	3.605	V	3.5 V +3% - 5%
PLL Supply Voltage		V_{DD4}	3.325	3.605	V	3.5 V +3% - 5%
PLL Ground		V_{SS4}	-0.2	+0.2	V	
Operating Case Temperature (with Fan Heatsink)		T_c	0	85	°C	

Table 8. DC Characteristics (V_{CC} = V_{DD2}, V_{DD3}) [5]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2.2		V_{cc}+0.2	V
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{OH}	Output High Voltage	I_{OH}=4.0mA,V_{CC}=Min[1]	2.4			V
		I_{OH}=5.0mA,V_{CC}=Min[2]	2.4			V
		I_{OH}=8.0mA,V_{CC}=Min[3]	2.4			V
V_{OL}	Output Low Voltage	I_{OL}=4.0mA,V_{CC}=Min[1]			0.4	V
		I_{OL}=5.0mA,V_{CC}=Min[2]			0.4	V
		I_{OL}=8.0mA,V_{CC}=Min[3]			0.4	V
I_{IN}	Input Current	V_{IN}=V_{CC} or GND, except[4]	-10		10	uA
		V_{IN}=V_{CC} or GND, [4]	-10		10	uA
I_{OZ}	Output Leakage Current	V_{OUT}=V_{CC} or GND Outputs Disabled	-10		10	uA
I_{DD}	Dynamic Supply Current	V_{CC}=Max, 50pF load, @ 170 MHz		2.3		A
I_{STBY}	Standby Supply Current	V_{CC}=Max, V_{in} =V_{CC} or GND, outputs static	-	-	600	mA
W_D	Power Dissipation	V_{DD1}, V_{DD2}, V_{DD3} = typ		7	8	W

Notes: 1. SB_CR, SB_CG, JTAG_TDO, SB_SEL, SB_BG, CP_STAT, DRAM_ADR[11:0], DRAM_RAS_[7:0], and DRAM_CAS_[7:0] outputs only.

2. For each line of SB_CLK output only.

3. MEM_PAR[1:0], MEM_DATA[63:0], SB_DATA[31:0], SB_ACK, SB_SIZE[2:0], SB_RD, SB_ADR[27:0], and SB_AS outputs only.

4. JTAG_TMS, JTAG_TRST, JTSG_TDI, JTAG_TCK, RESET_, and PLL_BYP_ only.

5. Max conditions: V_{DD2} = 5.25V (5.0V + 5%) . V_{DD3} = 3.605V (3.5V + 3%)
Min conditions: V_{DD2} = 4.75V (5.0V - 5%) . V_{DD3} = 3.325V (3.5V - 5%)

Power Consumption Estimation

The following formula estimates the power consumption for a given CPU frequency.

Power Consumption (W) = (Static Power consumed by Sense Amps) +
+ Core Power (function of frequency)
+ 5VIO Power + 3VIO Power
= 1.3W + (CPU-Clk * 0.025W/MHz) + 1.0W + 0.5W

For CPU_Clk=170 MHz,

Power Consumption (W) = 1.3 + (170*0.025) + 1.0 + 0.5 = 7.05W

Table 9. AC Characteristics (Input Pins)

Pin Name	Symbol	170 MHz		Units
		Min	Max	
AFX_PREPLY[1:0]	t_{SI} t_{HI}	3.0 1.0	- -	ns ns
SB_LERR_	t_{SI} t_{HI}	2.0 1.0	- -	ns ns
SB_BR[5:0]	t_{SI} t_{HI}	2.0 1.0	- -	ns ns
IRL[3:0]	t_{SI} t_{HI}	2.0 1.0	- -	ns ns
STANDBY	t_{SI} t_{HI}	2.0 1.0	- -	ns ns

Notes: 1. CPU_MODE[2:0], PLL_BYP, IOCLK_DIV6[1:0], IOCLK_DIV2, INPUT_RESET and IOC_RANGE[1:0] are system configuration pins and should be tied to their appropriate power or ground levels.

2. All input pins measured with a tester load of 50 pF wrt I/0 CLK.

Table 10. AC Characteristics (Output Pins)

Pin Name	Symbol	170 MHz		Units
		Min	Max	
DRAM_ADDR[11:0]	t_{DO} t_{HO}	- 4.0	6.0 -	ns
DRAM_RAS_[7:0]	t_{DO} t_{HO}	- 4.0	6.3 -	ns
DRAM_CAS_[3:0]	t_{DO} t_{HO}	- 4.0	6.1 -	ns
DRAM_WE_	t_{DO} t_{HO}	- 4.0	6.0 -	ns
SC_ADDR[16:0]	t_{DO} t_{HO}	- 3.0	5.0 -	ns
SC_CE[3:0]	t_{DO} t_{HO}	- 3.0	5.0 -	ns
SC_ADSC_	t_{DO} t_{HO}	- 3.0	5.0 -	ns
SC_GW	t_{DO} t_{HO}	- 3.0	5.0 -	ns
SC_ADV_	t_{DO} t_{HO}	- 3.0	5.0 -	ns
SC_OE_	t_{DO} t_{HO}	- 3.0	5.0 -	ns
SC_CLK[3:0]	t_{DO}	-	1.0	ns
MF_RST_	t_{DO} t_{HO}	- 3.0	4.5 -	ns
MF_WCE_	t_{DO} t_{HO}	- 3.0	5.0 -	ns
MF_RCE_	t_{DO} t_{HO}	- 3.0	5.0 -	ns
MF_OEBA	t_{DO} t_{HO}	- 3.0	5.0 -	ns
MF_OEAB	t_{DO} t_{HO}	- 3.0	5.0 -	ns
MF_LE	t_{DO} t_{HO}	- 3.0	5.0 -	ns
MF_CLK[1:0] (see footnote 2)	t_{DO}	-	7.0	ns
AFX_AEN	t_{DO}	-	6.3	ns
AFX_SREPLY[1:0]	t_{DO}	-	6.3	ns
AFX_ADDR[2:0]	t_{DO}	-	6.3	ns
AFX_CLK	t_{DO}	-	6.2	ns
SB_PA[27:0]	t_{DO} t_{HO}	- 4.0	7.7 -	ns
SB_CLK[2:0]	t_{DO}	-	6.2	ns
SB_AS_	t_{DO} t_{HO}	- 4.0	7.7 -	ns
SB_BG_[5:0]	t_{DO} t_{HO}	- 4.0	8.0 -	ns
SB_SEL[4:0]	t_{DO} t_{HO}	- 4.0	8.0 -	ns

Notes: 1. All input pins measured with a tester load of 50 pF
2. MFCLK is measured wrt EXT_CLK1 and the remaining signals are referenced to I/O CLK (=MFCLK).

Table 11. AC Characteristics (Bi-Directional Pins)

Pin Name	Symbol	170 MHz		Units
		Min	Max	
MEM_DATA[63:0]	t_{SI} t_{HI} t_{DO} t_{HO}	2.0 1.0 - 3.0	- - 5.5 -	ns
MEM_PAR[1:0]	t_{SI} t_{HI} t_{DO} t_{HO}	2.0 1.0 - 3.0	- - 5.0 -	ns
SC_TAG[5:0]	t_{SI} t_{HI} t_{DO} t_{HO}	2.0 1.0 - 3.0	- - 4.2 -	ns
SB_DATA[31:0]	t_{SI} t_{HI} t_{DO} t_{HO}	2.0 1.0 - 4.0	- - 6.2 -	ns
SB_SIZE[2:0]	t_{SI} t_{HI} t_{DO} t_{HO}	2.0 1.0 - 4.0	- - 7.7 -	ns
SB_RD	t_{SI} t_{HI} t_{DO} t_{HO}	2.0 1.0 - 4.0	- - 7.0 -	ns
SB_ACK_[2:0]	t_{SI} t_{HI} t_{DO} t_{HO}	2.0 1.0 - 4.0	- - 6.2 -	ns

TIMING WAVEFORMS

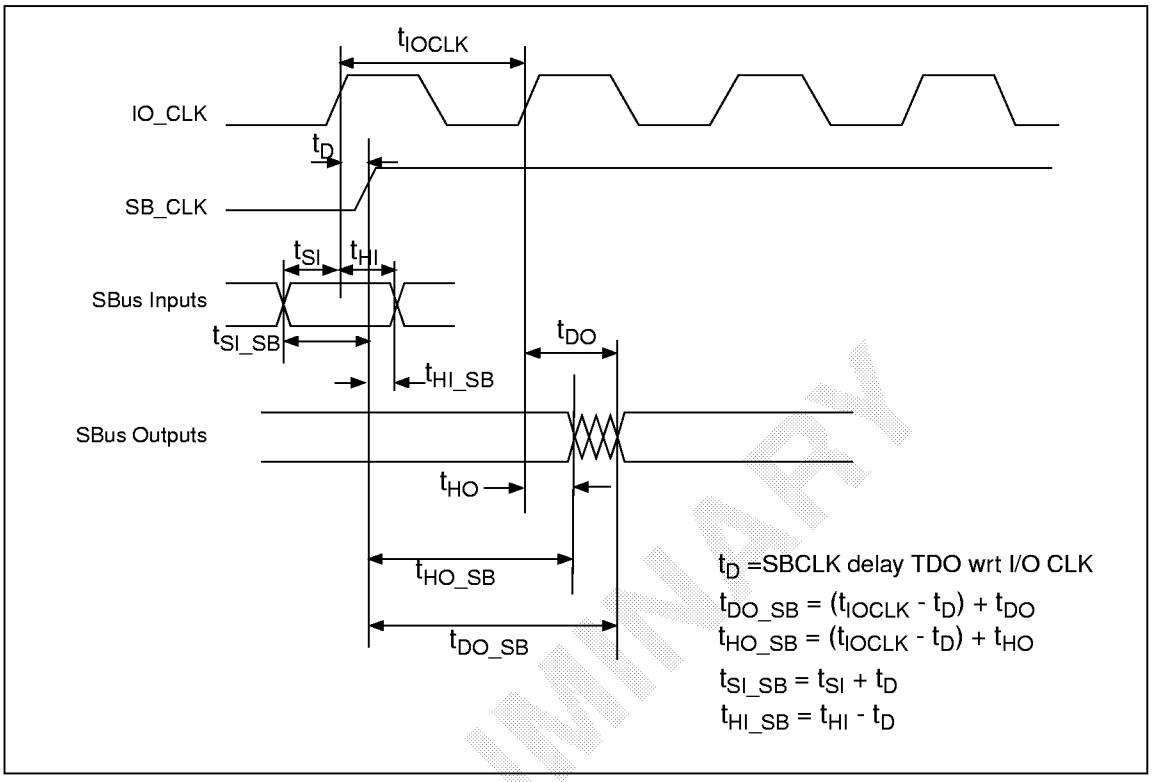

Figure 5. SBus Clock Relationships

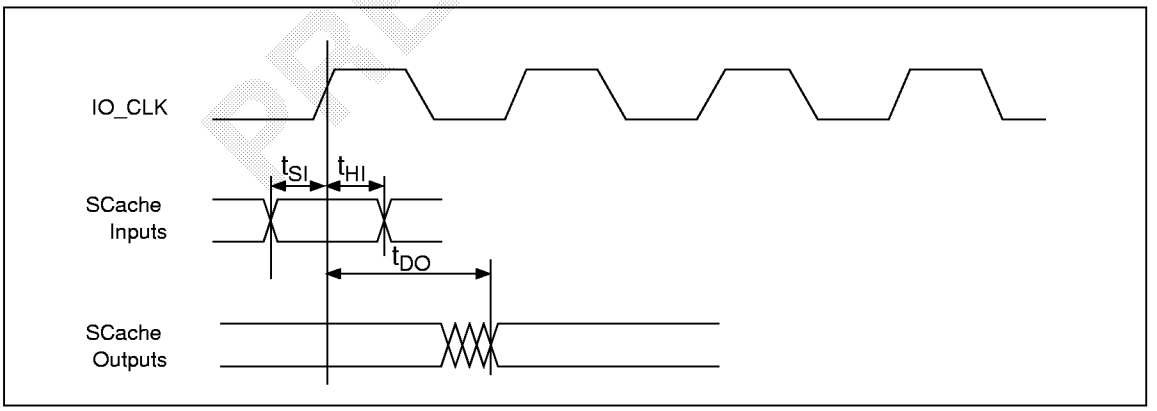

Figure 6. Secondary Cache Timing

DRAM Wait State Timings

WS The 3-bit Wait State field controls the number of DRAM wait states and other DRAM timing factors. The field is cleared (000) on power-up and can be modified by writing to the CCR (CPU Configuration Register). Table 12 shows the encoding of the WS field.

Table 12. DRAM Access Times (Unit = number of I/O_Clk cycles)

WS[2:0]	t_ASR	t_ASC	t_CAH	t_CAS	t_CP	t_RAS	t_RP	t_CSR
000	3	3	6	3	6	11	8	3
001	4	3	7	3	7	11	8	4
010	5	4	9	4	9	13	9	5
011	6	5	11	5	11	13	9	6
100	1	1	2	1	2	7	5	1
101	2	1	3	1	3	7	6	2
110	2	2	4	2	4	9	7	2
111	3	2	5	2	5	9	7	3

1. t_ASR - row address setup time
2. t_ASC - column address setup time
3. t_CAS - CAS pulse width time
4. t_RAS - RAS pulse width time
5. t_CSR - CAS setup time before refresh
6. t_CAH - column address hold time
7. t_CP - CAS precharge time (min)
8. t_RP - RAS precharge time (min)

The following timing diagram explains the above setup and hold times.

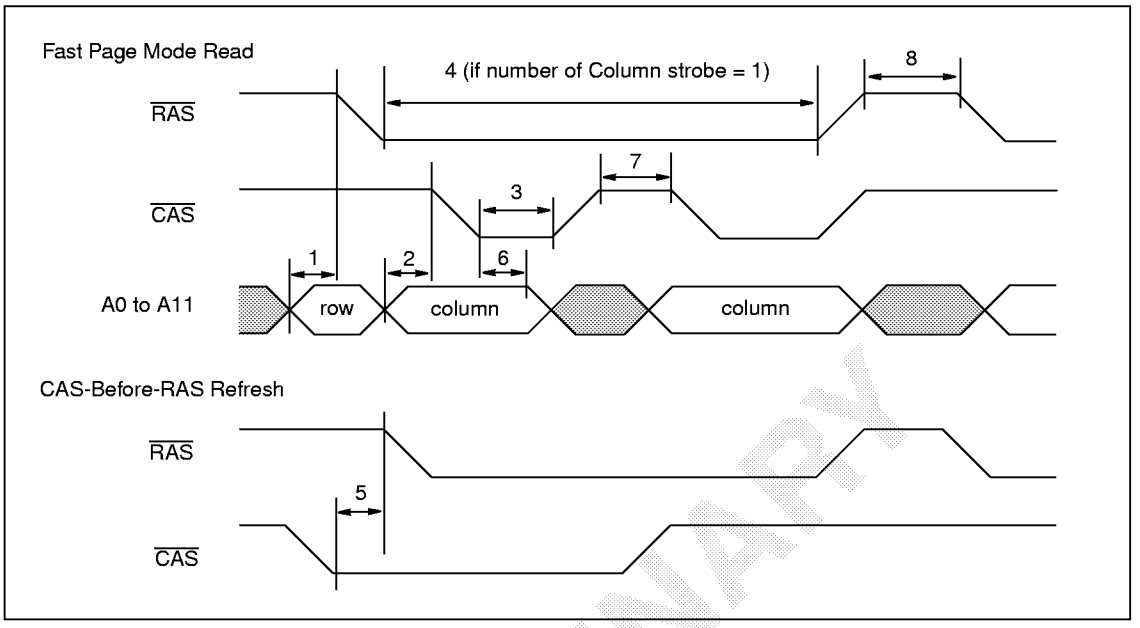

Figure 7. DRAM Timing Illustration

Table 13. DRAM Setup and Hold Times (Unit = number of I/O_Clk cycles)

WS[2:0]	t_RDS SCC=0	t_RDS SCC≠0	t_RDH SCC = 0	t_RDH SCC≠0	t_RDLS SCC = 0	t_RDLS SCC≠0	t_DS SCC = 0	t_DS SCC≠0	t_DH SCC = 0	t_DH SCC≠0
000	5	8	0	0	-	6	3	3	6	4
001	6	9	0	0	-	7	3	4	7	4
010	8	12	0	0	-	9	4	5	9	5
011	10	15	0	0	-	11	5	6	11	6
100	1	2	0	0	-	2	1	1	2	2
101	2	3	0	0	-	3	1	2	3	2
110	3	5	0	0	-	4	2	2	4	3
111	4	6	0	0	-	5	1	3	5	3

SCC - SCC field of CPU configuration register: 0 - no secondary cache,
not 0 - secondary cache

t_RDS - CPU read data setup - CAS falling edge to IO_CLK rising edge

t_RDH - CPU read data hold - CAS falling edge to IO_CLK rising edge

t_RDLS - FIFO read data setup - CAS falling edge to LE falling edge

t_DS - write data setup time

t_DH - write data hold time

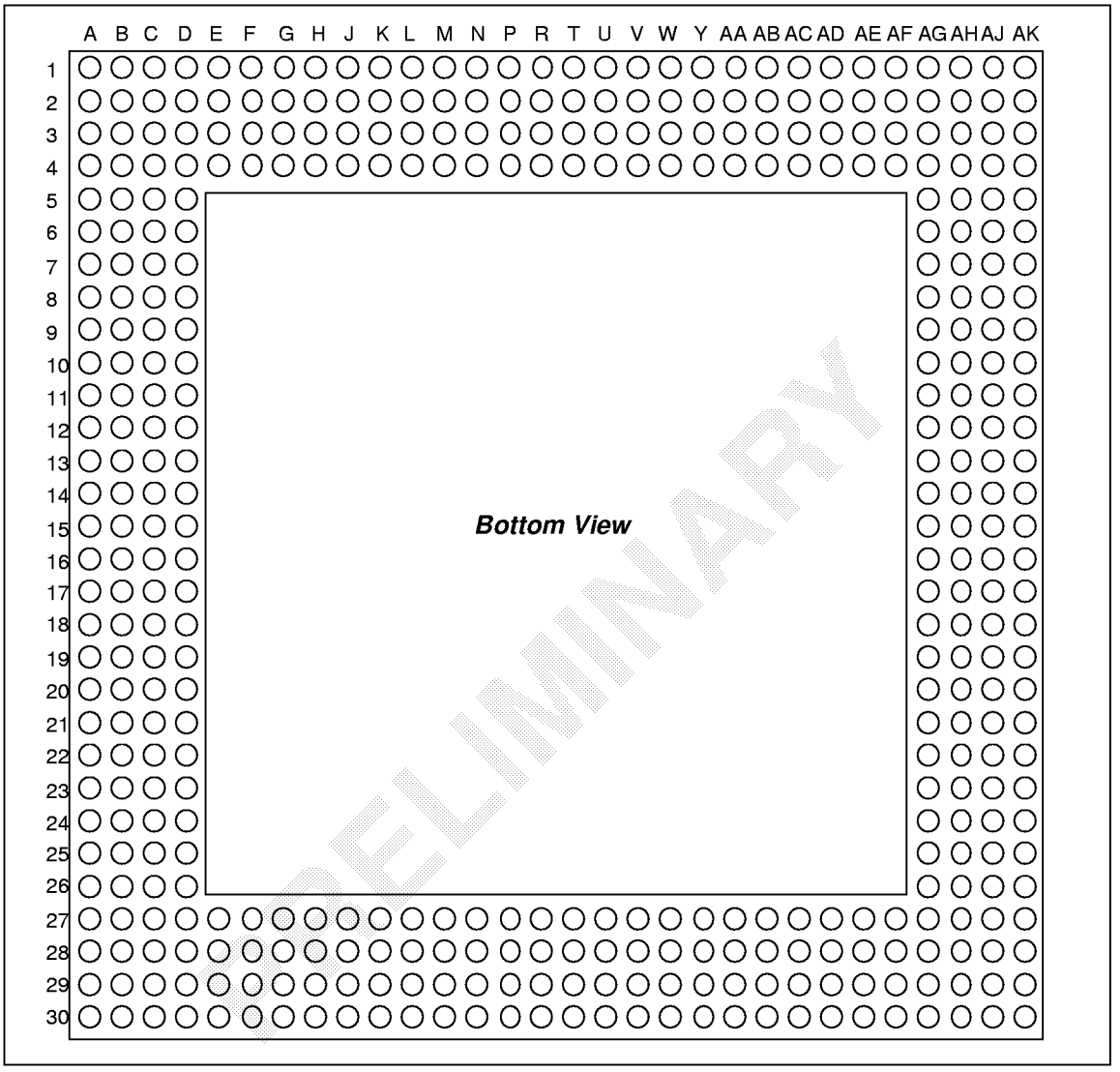

Figure 8. CBGA 416 Package Pin Assignments

Table 14. Pin Description

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	SB_CG	B5	Vss2/Vss3	C9	SB_BG[0]	D13	Vss1	G1	Vss2/Vss3
A2	Vdd2	B6	Vss2/Vss3	C10	SB_ACK[1]	D14	SB_DATA[31]	G2	DRAM_ADDR[2]
A3	SB_BR[4]	B7	SB_BG[5]	C11	SB_SIZE[1]	D15	SB_DATA[27]	G3	DRAM_ADDR[1]
A4	SB_CLK[2]	B8	Vdd2	C12	SB_RD	D16	Vdd1	G4	AFX_PREPLY[1]
A5	Vss2/Vss3	B9	SB_BG[1]	C13	SB_SEL[1]	D17	SB_DATA[23]	G27	SB_PA[12]

Table 14. Pin Description (Continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A6	Vss2/Vss3	B10	SB_ACK[0]	C14	SB_SEL[0]	D18	SB_DATA[19]	G28	SB_PA[13]
A7	SB_BG[4]	B11	Vss2/Vss3	C15	SB_DATA[28]	D19	Vss1	G29	SB_PA[14]
A8	Vdd2	B12	SB_LERR	C16	Vdd1	D20	SB_DATA[15]	G30	SB_PA[15]
A9	Vdd2	B13	SB_SEL[2]	C17	SB_DATA[24]	D21	SB_DATA[13]	H1	DRAM_ADDR[4]
A10	SB_SIZE[2]	B14	Vdd2	C18	SB_DATA[20]	D22	Vdd1	H2	DRAM_ADDR[3]
A11	Vss2/Vss3	B15	SB_DATA[29]	C19	Vss1	D23	SB_DATA[8]	H3	Vdd1
A12	SB_AS	B16	SB_DATA[25]	C20	SB_DATA[16]	D24	SB_DATA[5]	H4	Vdd1
A13	SB_SEL[3]	B17	Vss2/Vss3	C21	SB_DATA[12]	D25	Vss1	H27	Vss1
A14	Vdd2	B18	SB_DATA[21]	C22	Vdd1	D26	SB_DATA[1]	H28	Vss1
A15	SB_DATA[30]	B19	SB_DATA[17]	C23	SB_DATA[9]	D27	SB_PA[2]	H29	Vss2/Vss3
A16	SB_DATA[26]	B20	Vdd2	C24	SB_DATA[4]	D28	Vdd1	H30	Vss2/Vss3
A17	Vss2/Vss3	B21	SB_DATA[14]	C25	Vss1	D29	SB_PA[7]	J1	DRAM_ADDR[8]
A18	SB_DATA[22]	B22	SB_DATA[10]	C26	SB_DATA[3]	D30	SB_PA[10]	J2	DRAM_ADDR[7]
A19	SB_DATA[18]	B23	Vss2/Vss3	C27	SB_PA[0]	E1	AFX_AEN	J3	DRAM_ADDR[6]
A20	Vdd2	B24	SB_DATA[6]	C28	SB_PA[4]	E2	AFX_CLK	J4	DRAM_ADDR[5]
A21	Vdd2	B25	Vdd2	C29	SB_PA[5]	E3	Vss1	J27	SB_PA[17]
A22	SB_DATA[11]	B26	Vdd2	C30	SB_PA[6]	E4	Vss1	J28	SB_PA[16]
A23	Vss2/Vss3	B27	SB_DATA[0]	D1	Vss1	E27	Vdd1	J29	Vss2/Vss3
A24	SB_DATA[7]	B28	SB_PA[3]	D2	AFX_ADDR[1]	E28	SB_PA[8]	J30	Vss2/Vss3
A25	Vdd2	B29	Vss2/Vss3	D3	AFX_ADDR[0]	E29	Vdd2	K1	Vdd2
A26	Vdd2	B30	Vss2/Vss3	D4	Vdd1	E30	Vdd2	K2	Vdd2
A27	SB_DATA[2]	C1	Vss1	D5	SB_CLK[1]	F1	DRAM_ADDR[0]	K3	DRAM_ADDR[10]
A28	SB_PA[1]	C2	THERM_DIODE	D6	SB_BR[2]	F2	AFX_SREPLY	K4	DRAM_ADDR[9]
A29	Vss2/Vss3	C3	SB_CR	D7	Vss1	F3	AFX_PREPLY[0]	K27	SB_PA[21]
A30	Vss2/Vss3	C4	Vdd1	D8	SB_BG[2]	F4	AFX_ADDR[2]	K28	SB_PA[19]
B1	CP_STAT[1]	C5	SB_CLK[0]	D9	SB_ACK[2]	F27	SB_PA[9]	K29	SB_PA[20]
B2	Vdd2	C6	SB_BR[1]	D10	Vdd1	F28	SB_PA[11]	K30	SB_PA[18]
B3	SB_BR[5]	C7	SB_BR[0]	D11	SB_SIZE[0]	F29	Vdd2	L1	DRAM_RAS_[0]
B4	SB_BR[3]	C8	SB_BG[3]	D12	SB_SEL[4]	F30	Vdd2	L2	DRAM_ADDR[11]
L3	Vss1	R29	IRL[1]	Y3	Vdd1	AD29	STANDBY	AG19	MF_OEBA
L4	Vss1	R30	IRL[0]	Y4	Vdd1	AD30	JTAG_TRST	AG20	MEM_DATA[62]
L27	Vdd1	T1	Vdd3	Y27	Vss1	AE1	Vss2/Vss3	AG21	MEM_DATA[60]
L28	Vdd1	T2	MEM_DATA[1]	Y28	Vss1	AE2	Vss2/Vss3	AG22	Vdd1
L29	Vdd2	T3	MEM_DATA[2]	Y29	EXT_CLK[2]	AE3	MEM_DATA[24]	AG23	MEM_DATA[53]
L30	Vdd2	T4	MEM_DATA[0]	Y30	EXT_CLK[1]	AE4	MEM_DATA[23]	AG24	MEM_DATA[51]
M1	DRAM_RAS_[4]	T27	Vdd4	AA1	MEM_DATA[14]	AE27	JTAG_TDO	AG25	Vss1
M2	DRAM_RAS_[3]	T28	IRL[3]	AA2	MEM_DATA[13]	AE28	MEM_PAR[1]	AG26	MEM_DATA[44]
M3	DRAM_RAS_[2]	T29	Vss2/Vss3	AA3	MEM-DATA[12]	AE29	Vdd3	AG27	MEM_DATA[40]
M4	DRAM_RAS_[1]	T30	Vss2/Vss3	AA4	MEM_DATA[11]	AE30	Vdd3	AG28	Vdd1

Table 14. Pin Description (Continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
M27	SB_PA[23]	U1	Vdd3	AA27	IOC_RANGE[0]	AF1	MEM_DATA[25]	AG29	MEM_DATA[35]
M28	SB_PA[22]	U2	Vdd3	AA28	INPUT_RESET	AF2	MEM_DATA[26]	AG30	Vss2/Vss3
M29	Vdd2	U3	Vss1	AA29	Vss2/Vss3	AF3	Vdd1	AH1	MEM_DATA[29]
M30	Vdd2	U4	Vss1	AA30	Vss2/Vss3	AF4	Vdd1	AH2	Vdd1
N1	Vss2/Vss3	U27	Vdd1	AB1	Vdd3	AF27	Vss1	AH3	SC_ADDR[0]
N2	Vss2/Vss3	U28	Vdd1	AB2	Vdd3	AF28	MEM_DATA[34]	AH4	SC_ADDR[1]
N3	DRAM_RAS_[6]	U29	PLL_BYP	AB3	MEM_DATA[16]	AF29	MEM_DATA[33]	AH5	Vss1
N4	DRAM_RAS_[5]	U30	CPU_MODE[0]	AB4	MEM_DATA[15]	AF30	MEM_DATA[32]	AH6	SC_ADDR[6]
N27	Vss4	V1	MEM_DATA[6]	AB27	JTAG_TDI	AG1	MEM_DATA[27]	AH7	SC_ADDR[11]
N28	SB_PA[24]	V2	MEM_DATA[5]	AB28	JTAG_CLK	AG2	Vdd1	AH8	SC_ADDR[13]
N29	Vdd2	V3	MEM_DATA[4]	AB29	Vss2/Vss3	AG3	MEM_DATA[28]	AH9	SC_ADDR[15]
N30	Vdd2	V4	MEM_DATA[3]	AB30	Vss2/Vss3	AG4	MEM_DATA[31]	AH10	SC_ADV
P1	DRAM_WE_	V27	IOCLK_DIV6[0]	AC1	MEM_DATA[17]	AG5	Vss1	AH11	SC_CE[2]
P2	DRAM_RAS_[7]	V28	CP_STAT[0]	AC2	MEM_DATA[18]	AG6	SC_ADDR[5]	AH12	Vss1
P3	Vdd1	V29	Vdd3	AC3	Vss1	AG7	SC_ADDR[8]	AH13	SC_TAG[4]
P4	Vdd1	V30	Vdd3	AC4	Vss1	AG8	Vdd1	AH14	MF_CLK[0]
P27	Vss1	W1	Vss2/Vss3	AC27	Vdd1	AG9	SC_ADDR[14]	AH15	Vdd1
P28	Vss1	W2	Vss2/Vss3	AC28	Vdd1	AG10	SC_CE[0]	AH16	SC_TAG[2]
P29	SB_PA[26]	W3	MEM_DATA[8]	AC29	JTAG_TMS	AG11	SC_CE[1]	AH17	MF_WCE
P30	SB_PA[25]	W4	MEM_DATA[7]	AC30	IOC_RANGE[1]	AG12	Vss1	AH18	Vss1
R1	DRAM_CAS_[3]	W27	IOCLK_DIV2	AD1	MEM_DATA[22]	AG13	SC_OE	AH19	MF_OEAB
R2	DRAM_CAS_[2]	W28	IOCLK_DIV6[1]	AD2	MEM_DATA[21]	AG14	MF_CLK[1]	AH20	MEM_DATA[61]
R3	DRAM_CAS_[1]	W29	CPU_MODE[2]	AD3	MEM_DATA[20]	AG15	Vdd1	AH21	MEM_DATA[59]
R4	DRAM_CAS_[0]	W30	CPU_MODE[1]	AD4	MEM_DATA[19]	AG16	SC_CLK[1]	AH22	MEM_DATA[56]
R27	IRL[2]	Y1	MEM_DATA[9]	AD27	MEM_PAR[0]	AG17	SC_TAG[0]	AH23	MEM_DATA[52]
R28	SB_PA[27]	Y2	MEM_DATA[10]	AD28	3_TEST	AG18	Vss1	AH24	MEM_DATA[48]
AH25	Vss1	AJ9	SC_ADDR[16]	AJ23	Vdd3	AK7	SC_ADDR[12]	AK21	MEM_DATA[57]
AH26	MEM_DATA[45]	AJ10	Vss2/Vss3	AJ24	MEM_DATA[50]	AK8	Vdd3	AK22	MEM_DATA[54]
AH27	MEM_DATA[43]	AJ11	Vss2/Vss3	AJ25	MEM_DATA[47]	AK9	SC_ADSC	AK23	Vdd3
AH28	Vdd1	AJ12	SC_CE[3]	AJ26	Vss2/Vss3	AK10	Vss2/Vss3	AK24	MEM_DATA[49]
AH29	MEM_DATA[37]	AJ13	SC_TAG[5]	AJ27	Vss2/Vss3	AK11	Vss2/Vss3	AK25	MEM_DATA[46]
AH30	MEM_DATA[36]	AJ14	Vdd3	AJ28	MEM_DATA[41]	AK12	SC_GW	AK26	Vss2/Vss3
AJ1	Vdd3	AJ15	SC_CLK[3]	AJ29	MEM_DATA[38]	AK13	SC_TAG[3]	AK27	Vss2/Vss3
AJ2	MEM_DATA[30]	AJ16	SC_CLK[0]	AJ30	Vdd3	AK14	Vdd3	AK28	MEM_DATA[42]
AJ3	SC_ADDR[2]	AJ17	Vdd3	AK1	Vdd3	AK15	SC_CLK[2]	AK29	MEM_DATA[39]
AJ4	Vss2/Vss3	AJ18	MF_RST	AK2	SC_ADDR[3]	AK16	SC_TAG[1]	AK30	Vdd3
AJ5	Vss2/Vss3	AJ19	MF_LE	AK3	SC_ADDR[4]	AK17	Vdd3		
AJ6	SC_ADDR[7]	AJ20	Vss2/Vss3	AK4	Vss2/Vss3	AK18	MF_RCE		
AJ7	SC_ADDR[10]	AJ21	MEM_DATA[58]	AK5	Vss2/Vss3	AK19	MEM_DATA[63]		
AJ8	Vdd3	AJ22	MEM_DATA[55]	AK6	SC_ADDDR[9]	AK20	Vss2/Vss3		

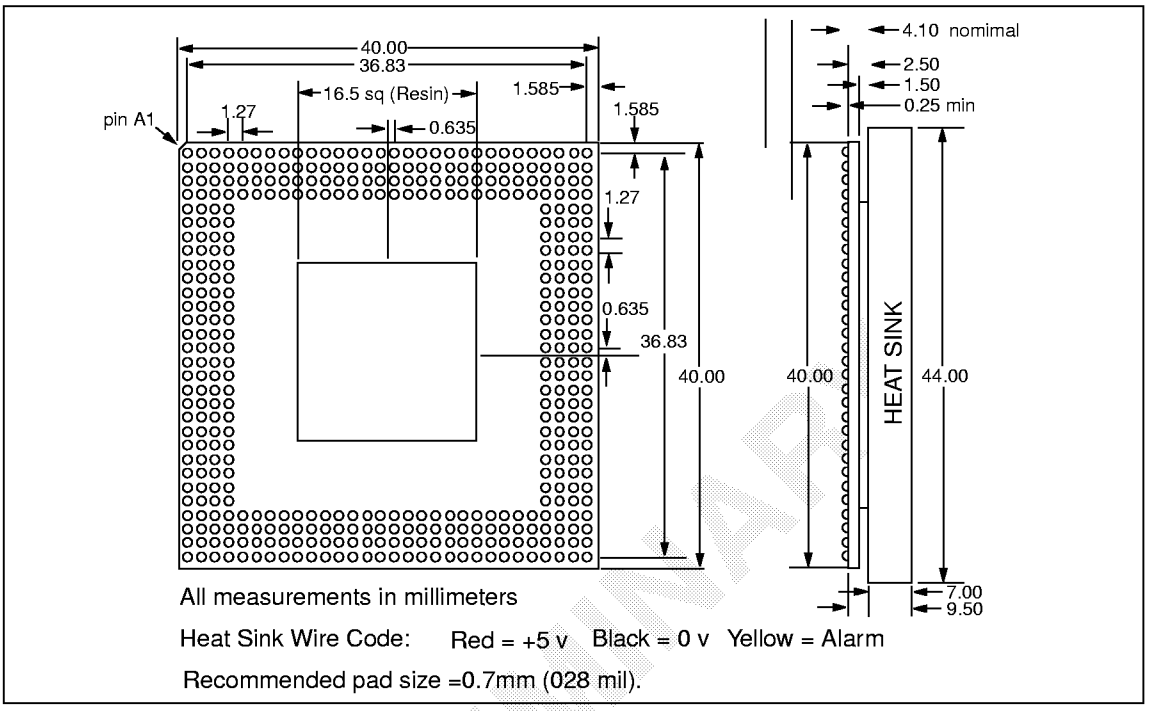

Figure 9. TurboSPARC Microprocessor Package Dimensions

The following table shows the thermal characteristics for the TurboSPARC microprocessor(PBGA416 package).

Table 15. Package Thermal Resistance

Air Flow in m/sec	0	1.01	3.04	θ_{jc} ^{0}C/W
θ_{ja} ^{0}C/W	13.1	10.5	8.5	0.6

HEAT SINK

The heatsink optimized for use with the TurboSPARC microprocessor includes a fan designed to consume 30%-60% less power than a typical off-the-shelf fan. The heatsink is slightly larger than the microprocessor package and is 7 mm in height.

In addition to the voltage and ground wires, the heatsink fan also includes a rotation abnormality detection mechanism. If the fan should fail, or the revolutions per minute should decrease significantly due to a loss of power supply current, a signal is generated through the alarm wire, alerting the motherboard. The heatsink specifications are listed below.

Table 16. Heatsink Specifications

Parameter	Value	Unit
Rated Voltage	5	Volts
Nominal Current	0.11	Amps
Acoustic Noise	27	Decibels
Operating Voltage	4.5 - 5.5	Volts
Operating Temperature	-10 - 60	^{o}C
Weight	20	Grams
Dimensions	44 x44 x7	Millimeters
Power Consumption	0.3	Watts
Rotation Speed	7500	RPM

Table 17. Rotational Speed vs. Thermal Resistance

Speed (RPM)	6,000	7,000	8,000	9,000
Thermal Resistance (^{o}C/W)	2.31	2.12	1.96	1.83

The following figure shows a graph of the above table.

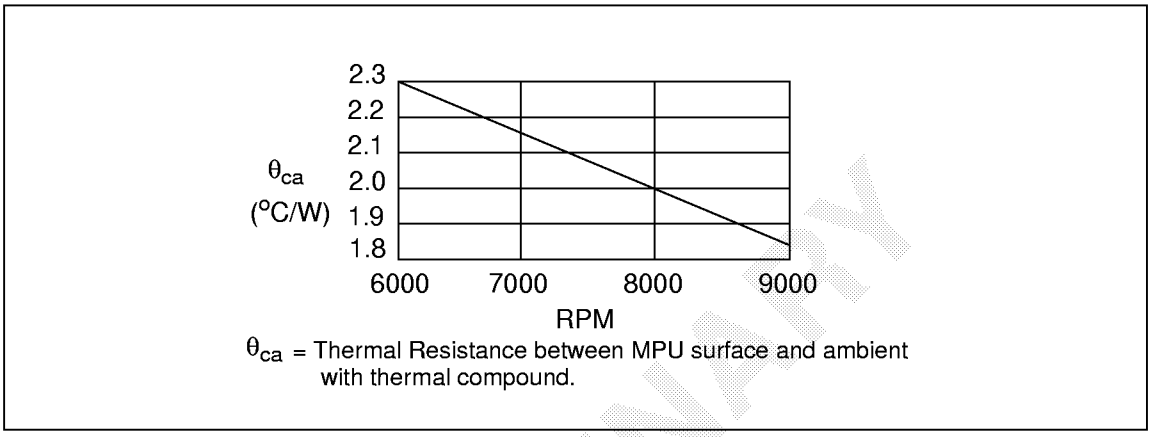

Figure 10. Graph of Rotational Speed vs. Thermal Resistance

The following table shows the thermal characteristics for the TurboSPARC microprocessor heat-sink. The air gap is described as shown in the figure below.

Table 18. Thermal Resistance

Package	Air Gap	θ_{ja} ^{0}C/W		θ_{jc} ^{0}C/W
		Airflow 0 (m/sec)	Airflow 0.5 (m/sec)	
HFB44A12	Open	3.44	3.37	1.20
	46.8 mm	3.50	3.40	1.20
	36.8 mm	3.47	3.44	1.20
	26.8 mm	3.45	3.46	1.22
	16.8 mm	3.41	3.71	1.23
	11.8 mm	3.97	4.11	1.25

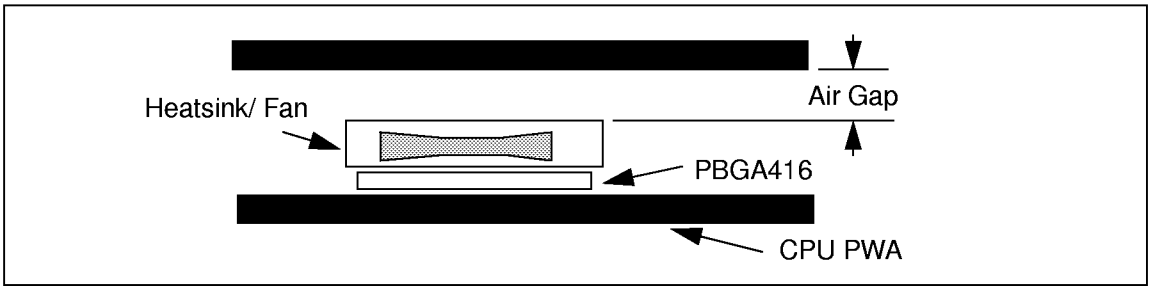

Figure 11. Description of the Air Gap

PRODUCT ORDERING INFORMATION

Part Number	Description
MB86907DCR-ES	TurboSPARC Microprocessor
FM80101-01-17	170 MHz TurboSPARC Microprocessor with Heatsink/Fan
FM80102-01-17	321-pin PGA Adapter Board with 170 MHz TurboSPARC Microprocessor*
FM80103-01-17	321-pin PGA Adapter Board with 170 MHz TurboSPARC Microprocessor and Heatsink/ Fan*
FM80104-01-16-SA	321-pin PGA Daughterboard with 512 KByte of Secondary Cache, 160 MHz TurboSPARC Microprocessor and Heatsink/Fan Starter Kit*
FM80104-01-16-SB	321-pin PGA Daughterboard with 512 KByte of Secondary Cache, 160 MHz TurboSPARC Microprocessor and Heatsink/Fan Basic Kit*

* A more detailed description of these parts is available in the appendices of the TurboSPARC Reference Manual.

FUJITSU

Worldwide Headquarters

Japan

Fujitsu Limited

Tel: +81 44 754 3753
Fax +81 44 754 3332

1015 Kamiodanaka
Nakaharaku
Kawasaki 211
Japan

http://www.fujitsu.co.jp/

Asia

Fujitsu Microelectronics Asia PTE Limited

Tel: +65 336 1600
Fax +65 336 1609
:

No. 51 Bras Basah Road
Plaza by the Park
#06-04/07
Singapore 0718

http://www.fsl.com.sg/

USA

Tel: +1 408 922 9000
Fax +1 408 922 9179

Fujitsu Microelectronics Inc
3545 North First Street
San José CA 95134-1804
USA

Tel: +1 800 866 8608
Fax: +1 408 922 9179

Customer Response Center
Mon-Fri: 7am-5pm (PST)

http://www.fujitsumicro.com/

Europe

Tel: +49 6103 6900
Fax +49 6103 690122
:

Fujitsu Mikroelektronik GmbH
Am Siebenstein 6-10
D-63303 Dreieich-Buchschlag
Germany

http://www.fujitsu.ede.com/

FMI Document Control #05933-001 Rev 05

PP-DS-20339-01/97