

SHARP

2.6 1991

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TO: _____

REFERENCE

DEVICE SPECIFICATION FOR

64K bit STATIC RAM (8,192 X 8bit)
 MODEL NO.
L H 5 1 6 0 H N - 1 0 L
 (LH5160N8)

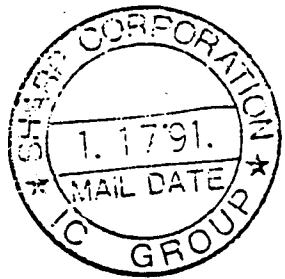
SPEC NO.: EL02Y011

ISSUE: Dec. 13. 1990

CUSTOMERS APPROVAL

DATE: _____

BY: _____



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 Integrated Circuit Group
 SHARP CORPORATION

EL-02-2966

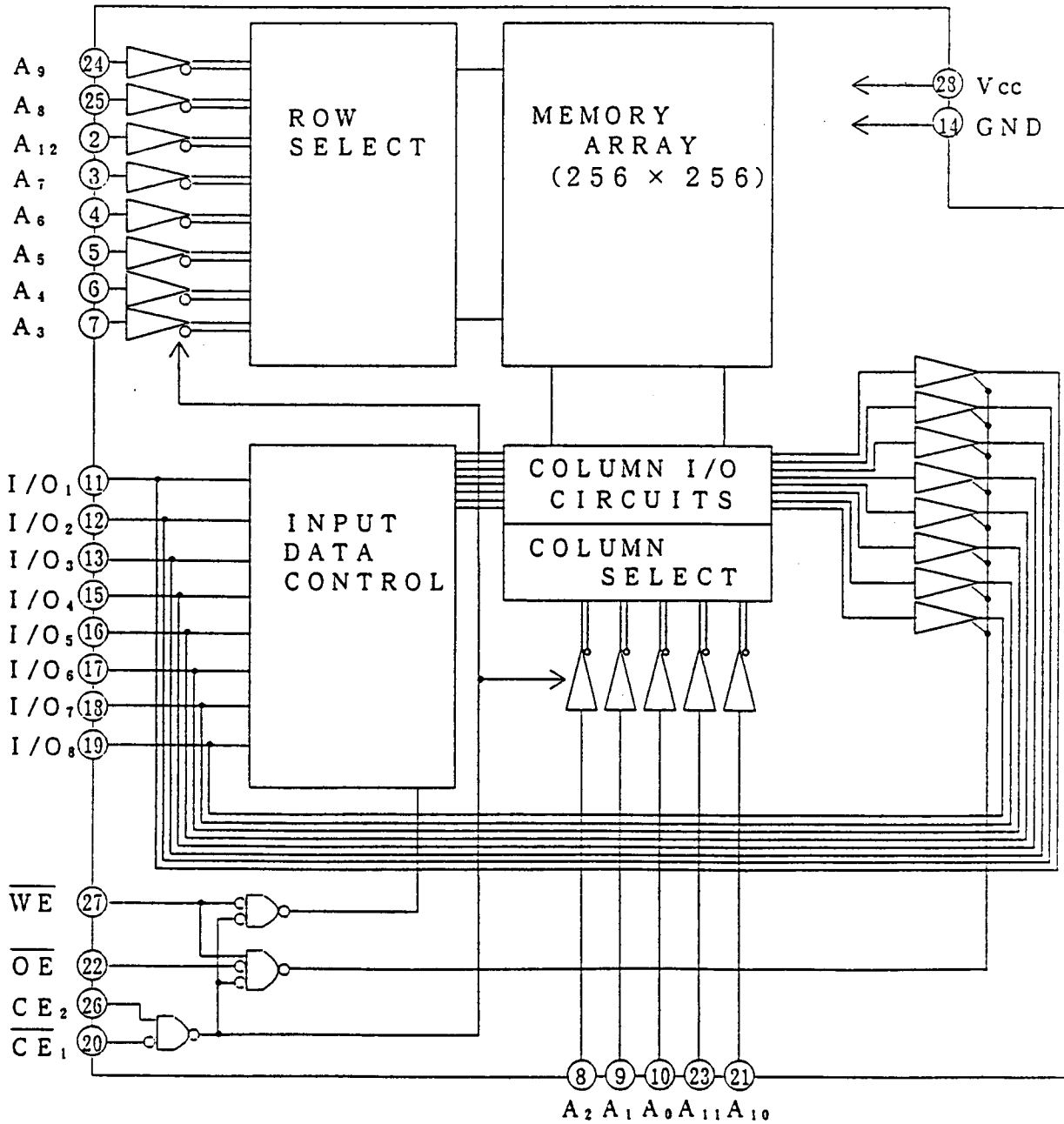
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3. Operating Mode

\overline{CE}_1	CE_2	\overline{WE}	\overline{OE}	Mode	I/O ₁ ~I/O ₈	Supply current
H	X	X	X	Deselect	High Z	Standby (I _{cc1})
X	L	X	X			
L	H	L	X	Write	D _{IN}	Operating (I _{cc})
L	H	H	L	Read	D _{OUT}	Operating (I _{cc})
L	H	H	H	Output disable	High Z	Operating (I _{cc})

X : H or L

4. Block Diagram



5. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage*	V _{CC}	-0.3~+7.0	V
Input voltage *	V _{IN}	-0.3~V _{CC} +0.3	V
Operating temperature	T _{opt}	-40~+85	°C
Storage temperature	T _{stg}	-55~+150	°C

* Maximum applicable voltage on any pin with respect to GND

6. Recommended DC Operating Conditions

(T_a = -40~+85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input voltage	V _{IH}	2.2		V _{CC} +0.3	V
	V _{IL}	-0.3		0.8	V

7. DC Electrical Characteristics

(T_a = -40~+85°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Input leakage current	I _{LI}	V _{IN} = 0 ~ V _{CC}		1.0	μA
Output leakage current	I _{LO}	$\overline{CE}_1 = V_{IH}$ or $CE_2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ V _{I/O} = 0 ~ V _{CC}		1.0	μA
Operating Supply current	I _{CC}	$\overline{CE}_1 = V_{IL}$, V _{IN} = V _{IL} or V _{IH} CE ₂ = V _{IH} , Output open		40	mA
Standby current	I _{CC1}	$\overline{CE}_1 = V_{IH}$ or CE ₂ = V _{IL}		10	mA
		I _{CC2}	CE ₂ ≤ 0.2V or $\overline{CE}_1 ≥ V_{CC} - 0.2V$ *	~+70°C	1.0
	~+85°C			3.0	μA
Output voltage	V _{OL}	I _{OL} = 2.1mA		0.4	V
	V _{OH}	I _{OH} = -1mA	2.4		V

* CE₂ ≥ V_{CC} - 0.2V or CE₂ ≤ 0.2V

8. Test Condition of AC Characteristics

Input pulse level	0.6~2.4 V
Input rise/fall time	10 ns
Input/Output timing level	1.5 V
Output load	1 TTL + C _L = 100pF

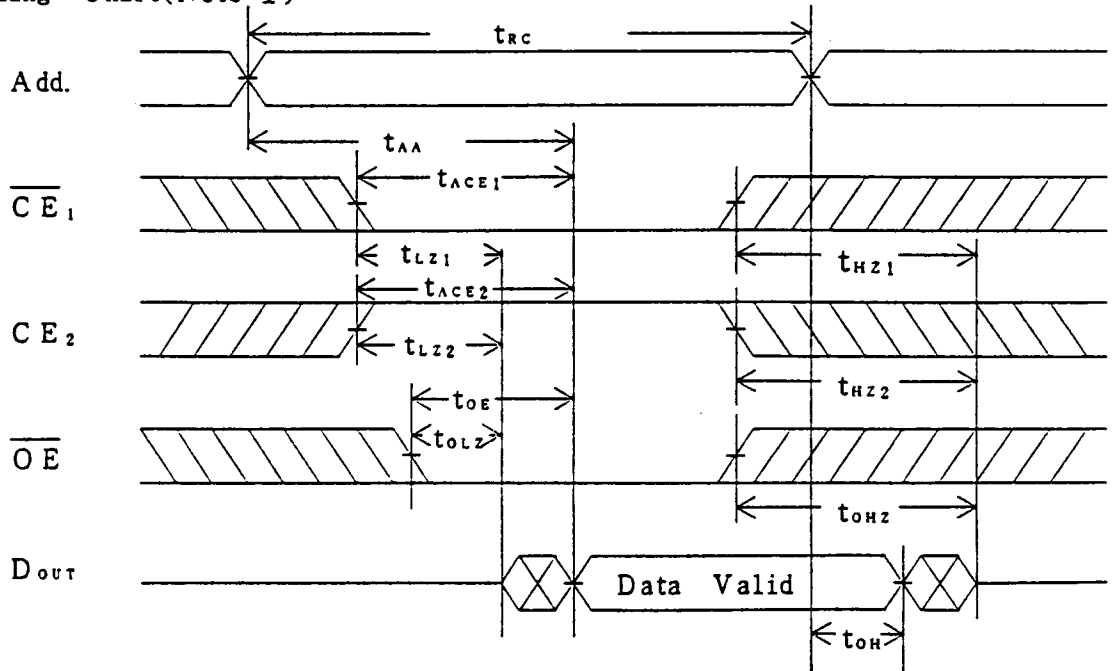
9. AC Characteristics

Read cycle

($T_a = -40 \sim 85^\circ\text{C}$, $V_{cc} = 5\text{V} \pm 10\%$)

Parameter	Symbol	Min.	Max.	Unit
Read cycle time	t_{RC}	100		ns
Address access time	t_{AA}		100	ns
Chip enable access time with respect to \overline{CE}_1	t_{ACE1}		100	ns
Chip enable access time with respect to \overline{CE}_2	t_{ACE2}		100	ns
Output enable access time	t_{OE}		40	ns
Output hold time	t_{OH}	10		ns
Output floating hold time with respect to \overline{CE}_1	t_{LZ1}	10		ns
Output floating hold time with respect to \overline{CE}_2	t_{LZ2}	10		ns
Output floating time with respect to \overline{OE}	t_{OLZ}	5		ns
Output floating time with respect to \overline{CE}_1	t_{HZ1}	0	30	ns
Output floating time with respect to \overline{CE}_2	t_{HZ2}	0	30	ns
Output floating time with respect to \overline{OE}	t_{OHZ}	0	20	ns

Timing Chart(Note 1)

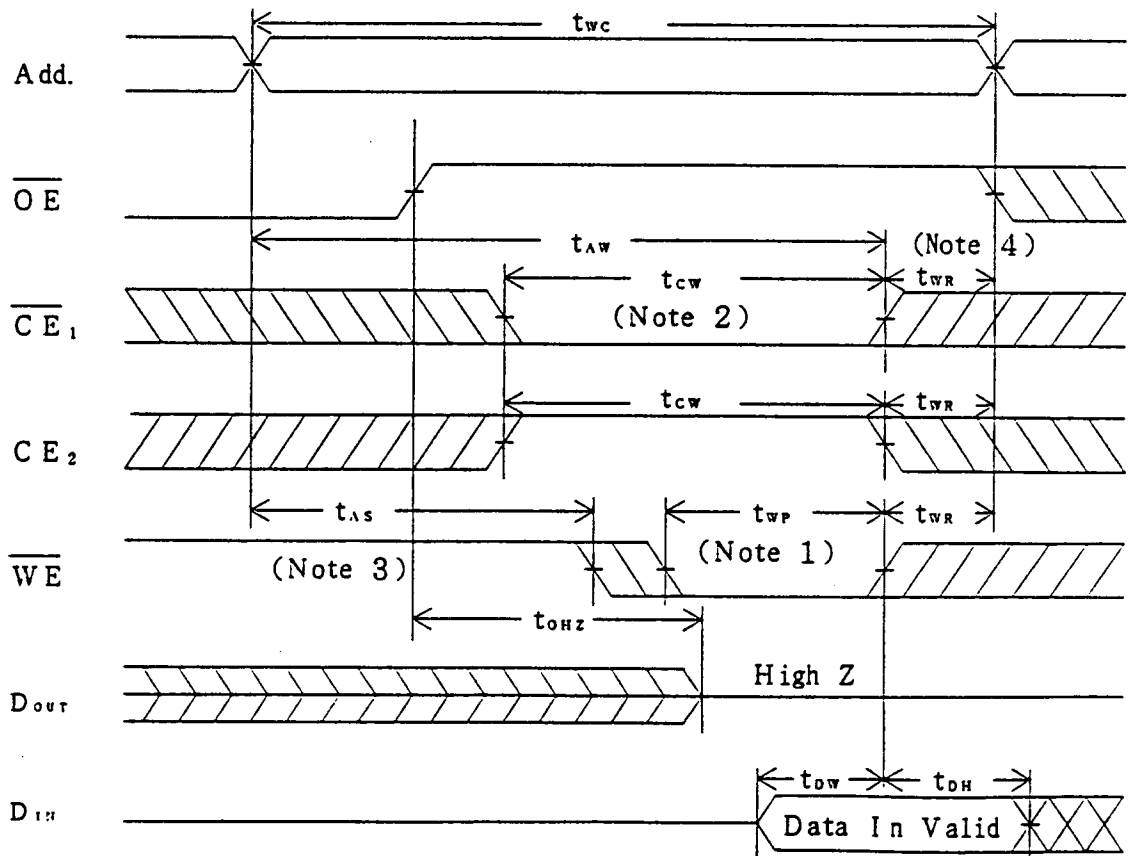


Note 1) \overline{WE} is "High" level during the read cycle

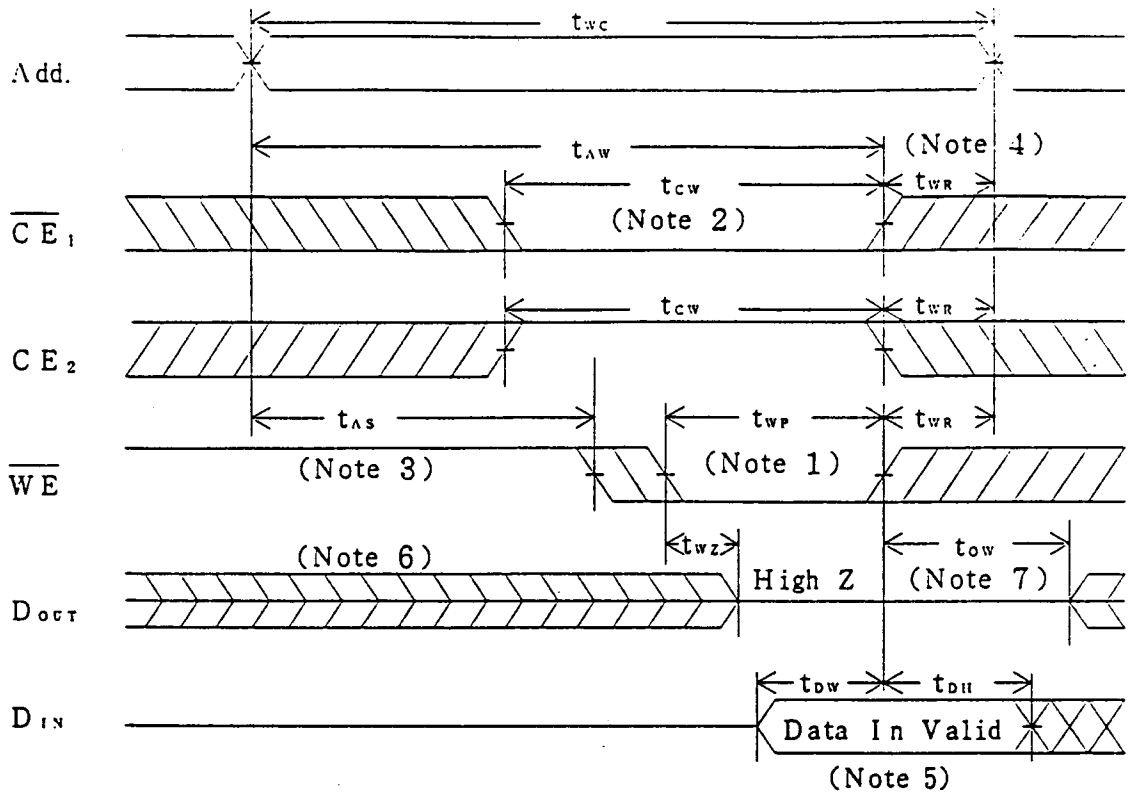
Write cycle

($T_a = -40 \sim 85^\circ\text{C}$, $V_{cc} = 5\text{V} \pm 10\%$)

Parameter	Symbol	Min.	Max.	Unit
Write cycle time	t_{wc}	100		ns
Chip enable time to write	t_{cw}	90		ns
Address valid time	t_{AW}	90		ns
Address setup time	t_{AS}	20		ns
Write pulse width	t_{WP}	60		ns
Write recovery time	t_{WR}	10		ns
Input data set time	t_{DW}	50		ns
Input data hold time	t_{DH}	0		ns
Output floating hold time with respect to \overline{WE}	t_{OW}	10		ns
Output floating time with respect to \overline{WE}	t_{WZ}	0	30	ns
Output floating time with respect to \overline{OE}	t_{OHZ}	0	20	ns



Timing Chart - (\overline{OE} Low fixed)



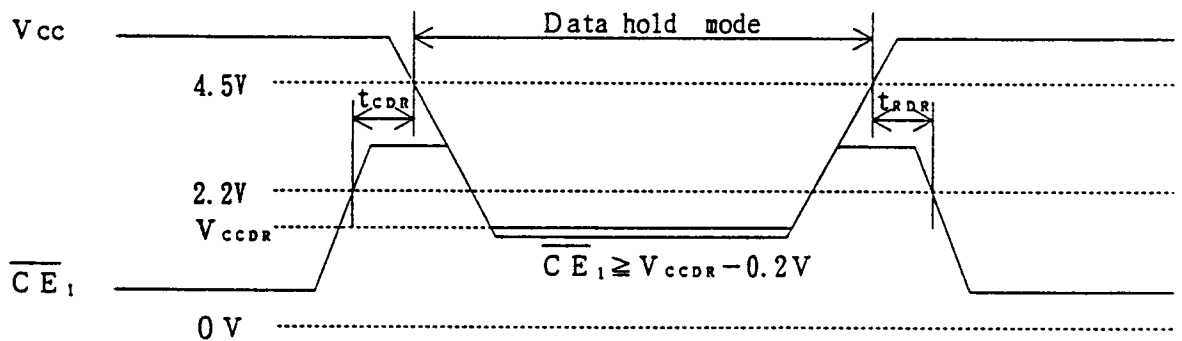
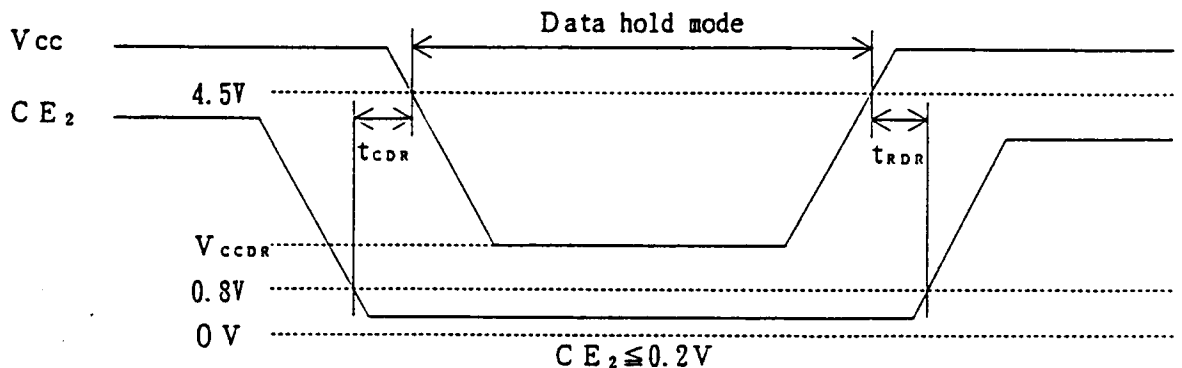
- Note) 1. The writing occurs during a overlapping period of $\overline{CE}_1 = 'Low'$, $CE_2 = 'High'$ and $\overline{WE} = 'Low'$ (t_{WP}).
2. t_{CW} is defined as the time from the last occurring transit, either \overline{CE}_1 Low transit or CE_2 High transit, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. Since during this period, I/O pins assume output state, no input signal 180° out of phase with an output signal admitted.
6. If \overline{CE}_1 Low transit or CE_2 High transit occurs at the same time or after \overline{WE} Low transit the output will remain High Z.
7. If CE_1 High transit or CE_2 Low transit occurs at the same time or before \overline{WE} High transit, the output remain High Z.

10. Low Voltage Data Hold Characteristics

(Ta = -40 ~ +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Data hold supply voltage	V_{CCDR}	$CE_2 \leq 0.2V$ or $\overline{CE}_1 \geq V_{CCDR} - 0.2V$ *	2.0		V
Data hold supply current	I_{CCDR}	$V_{CCDR} = 3V$ $CE_2 \leq 0.2V$ or $\overline{CE}_1 \geq V_{CCDR} - 0.2V$ *		0.2 0.4 0.6	μA
Chip enable setup time	t_{CDR}		0		ns
Chip enable hold time	t_{RDR}		** t_{RC}		ns

 * $CE_2 \geq V_{CCDR} - 0.2V$ or $CE_2 \leq 0.2V$ ** Read cycle time

 Timing Chart - (\overline{CE}_1 Control) Note)1

 Timing Chart - (CE_2 Control)


Note)1 To control the data hold mode at \overline{CE}_1 , fix the input level of CE_2 between $V_{CCDR} \sim V_{CCDR} - 0.2V$ or $0.0V \sim 0.2V$ during the data hold mode.

11. Pin Capacitance

($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	$V_{IN} = 0\text{ V}$			7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O} = 0\text{ V}$			10	pF

Note) Parameter is sample value, not all tested.

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PACKAGE AND PACKING SPECIFICATION

1. Package Outline Specification

Refer to drawing No. AA 9 3 1

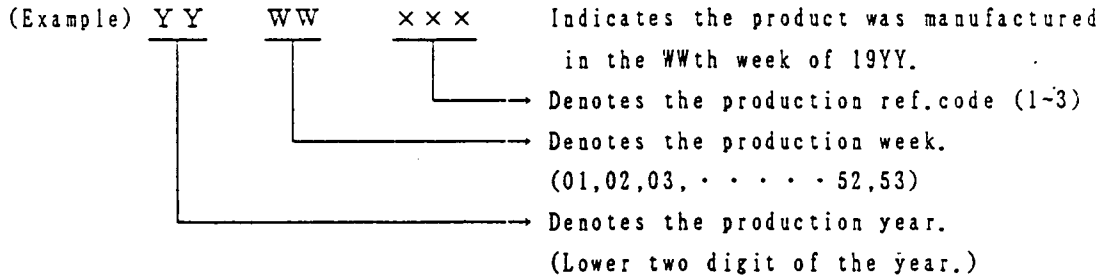
2. Markings

2-1. Marking contents

(1) Product name : LH5160HN-10L

(2) Company name : SHARP

(3) Date code



(4) The marking of "JAPAN" indicates the country of origin.

2-2. Marking layout

Refer drawing No. AA 9 3 1

(This layout do not define the dimensions of marking character and marking position.)

3. Surface Mount Conditions

The conditions below are recommended when mounting ICs not to deteriorate IC quality.

3-1. Soldering conditions

Mounting Method	Temperature and Duration	Measurement Point
Infrared reflow soldering	Peak temperature of 240°C, duration less than 15 seconds above 230°C, temperature increase rate of 1~4°C/second	IC surface
Solder dipping	245°C or less, duration less than 3 seconds/dip, total of 5 seconds	Solder bath
Vapor phase solderring	215°C or less, duration less than 40 seconds above 200°C	Steam
Manual soldering (soldering iron)	260°C or less, duration less than 10 seconds	IC outer lead surface

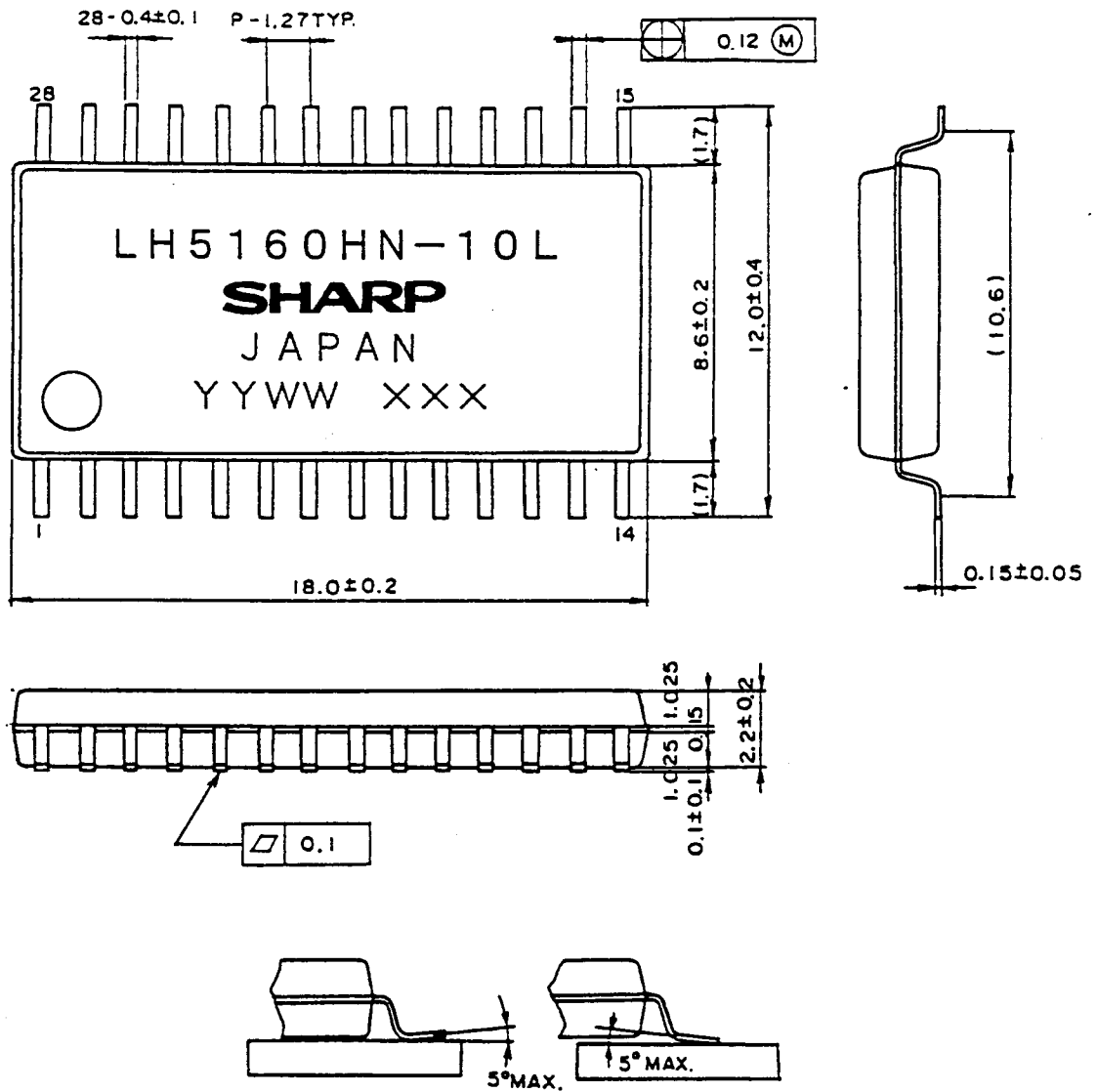
3-2. Conditions for removal of residual flux

(1) Ultrasonic washing power : 25 Watts/liter or less

(2) Washing time : Total 1 minute maximum

(3) Solvent temperature : 15~40°C

ISSUE DATE	'90.12.03	APPROVE	CHECK	DESIGN	DESIGN	(NOTE)
ISSUE NUMBER	H01203-03	<i>T. Tsuda</i>	<i>F. Kurosaki</i>	<i>T. Kimura</i>	<i>T. Awan</i>	
S/C NUMBER	LH5160N8					



名称	リード仕上	TIN-LEAD	単位	備考
NAME SOP28-P-450	LEAD FINISH	PLATING	UNIT mm	プラスチックパッケージ外形寸法は、バリを含まないものとする。
シャープ株式会社 IC事業本部		DRAWING NO.	AA931	NOTE Plastic body dimensions do not include burr of resin.
SHARP CORP. IC GROUP				

4. Packing Specification (Embossed Carrier Taping Specification)

This standard apply to the embossed carrier taping specification for ICs to be delivered from SHARP CORPORATION. SHARP's embossed carrier taping specification are, in principle, based on those set forth by the EIAJ (Electronic Industries Association of Japan (RC-1009B)) and the EIA (Electronic Industries Association (EIA481A)).

4 - 1. Tape Structure

- Embossed carrier tape is made of conductive plastic. The embossed portions of the carrier tape are filled with IC packages and covered with a top covering tape to enclose them.

4 - 2. Taping Reel and Embossed Carrier Tape Size

- For the taping reel and embossed carrier tape sizes, refer to the attached drawings (NO. CV524 and CV521)

4 - 3. IC Package Enclosure in Embossed Carrier Tape

- The IC package enclosure direction in the embossed portion as it compares to the direction in which the tape is pulled is indicated by an index mark on package (Index mark indicate the NO.1 pin on package) in the attached drawing (NO. CV522).

4 - 4. Missing IC Packages inside Embossed Carrier Tape

- The number of missing IC packages inside the embossed carrier tape should not exceed 0.1% of the total enclosed in the tape per reel, or 1, whichever may be larger. There should never be more than two consecutive missing IC package.

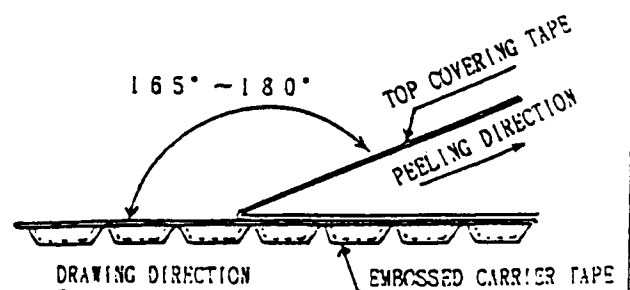
4 - 5. Tape Joints

- The embossed carrier tape should not have more than one joint per reel.

4 - 6. Peeling Strength of the Top Covering Tape

- Peeling strength must meet the following conditions.

- 1) Peeling angle
at 165° to 180°
- 2) Peeling speed
at 300mm/min.
- 3) Peeling strength
at 0.2 to 0.7N (20 to 70gf)



4 - 7. Packing

- The top covering tape (leader side) at the leading edge of the embossed carrier tape, and the trailing edge of the embossed carrier tape, shall be held in place with paper adhesive tape exceeding 30mm in length.
- The leading and trailing edges of the embossed carrier tape shall be left empty (with embossed portions not filled with IC packages), in the attached drawing (NO. CV522).
- The number of IC packages enclosed in the embossed carrier tape per reel shall, in principle, be as listed below.

Package Type	Number of IC Packages/Reel
SOP14PIN, SOP16PIN	3,000 pcs
SOP24PIN	1,500 pcs
SOP28PIN	1,000 pcs

4 - 8. Indications

- The following shall be indicated on the taping reel and the packing case.
 - 1) Part Number (Product Name)
 - 2) Storage Quantity
 - 3) Production Date
 - 4) Manufacture's Name (SHARP)

Note : The IC taping direction shall be indicated by "E1" or "E2" suffixed to the part number.

E1 : Equivalent to "f" of the EIAJ (RC-1009B) standard.
E2 : Equivalent to "B" of the EIAJ (RC-1009B) standard.

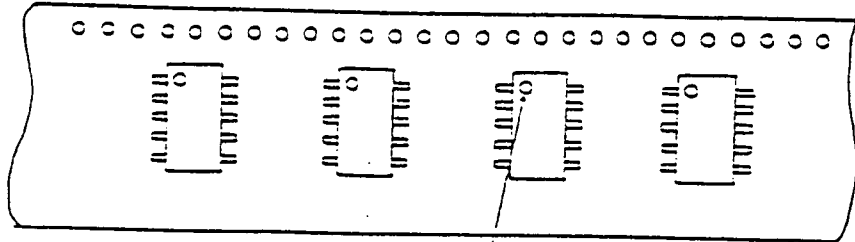
4 - 9. Protection While in Transit

Embossed carrier tape should be free from deformed IC leads and deterioration in electrical characteristics.

EMBOSS TAPING TYPE (E2)

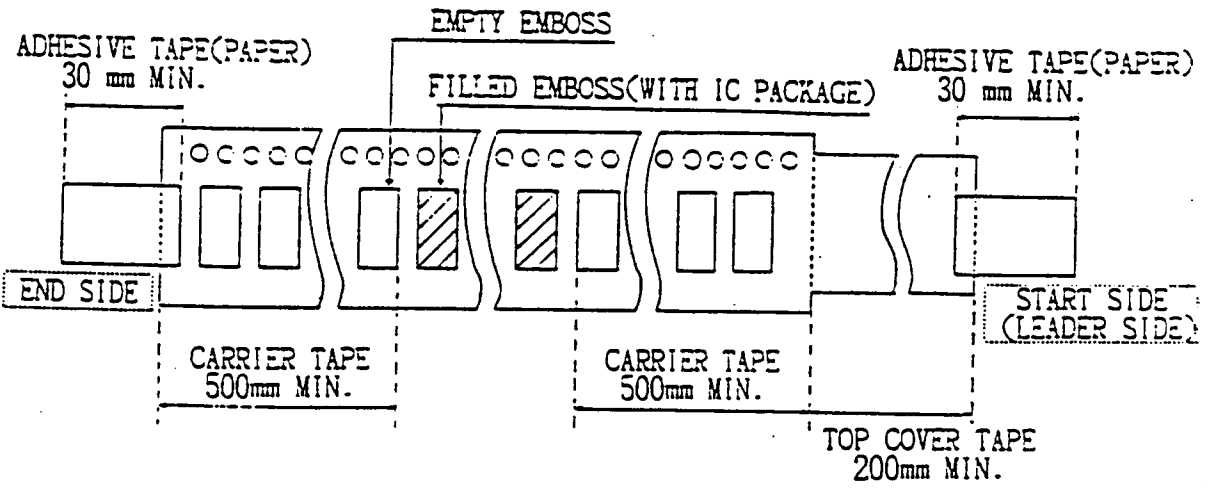
IC TAPING DIRECTION

THE DRAWING DIRECTION OF TAPE

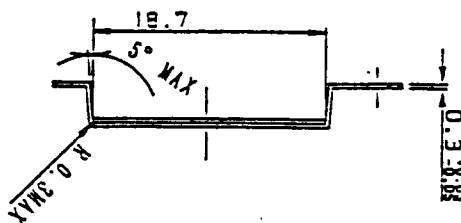
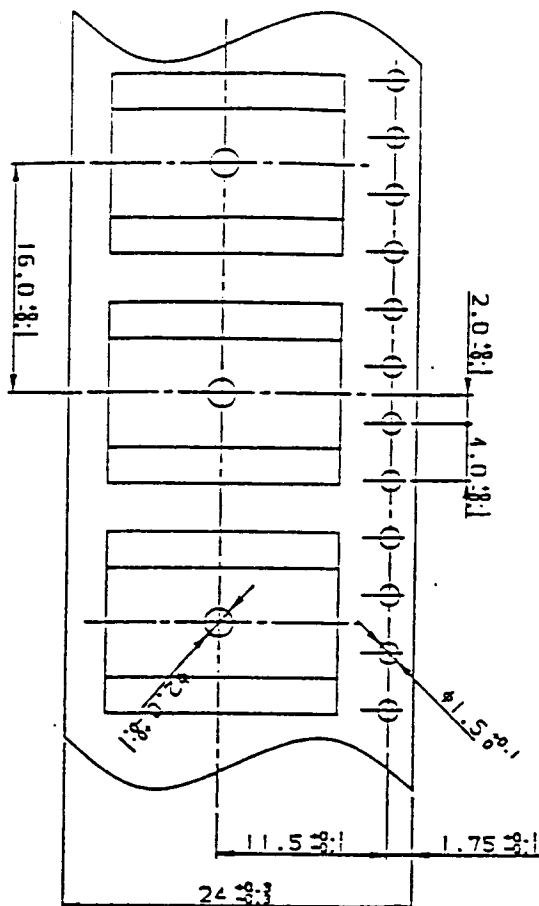
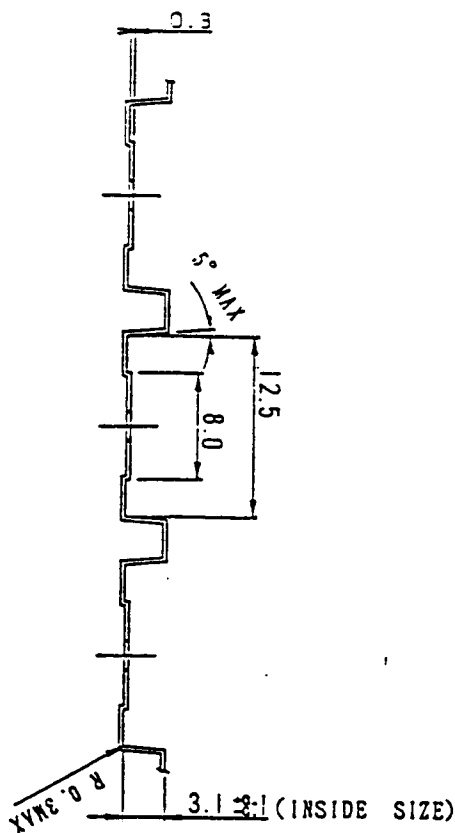


INDEX OF IC PACKAGE
(Indicate the NO.1 pin of IC package)

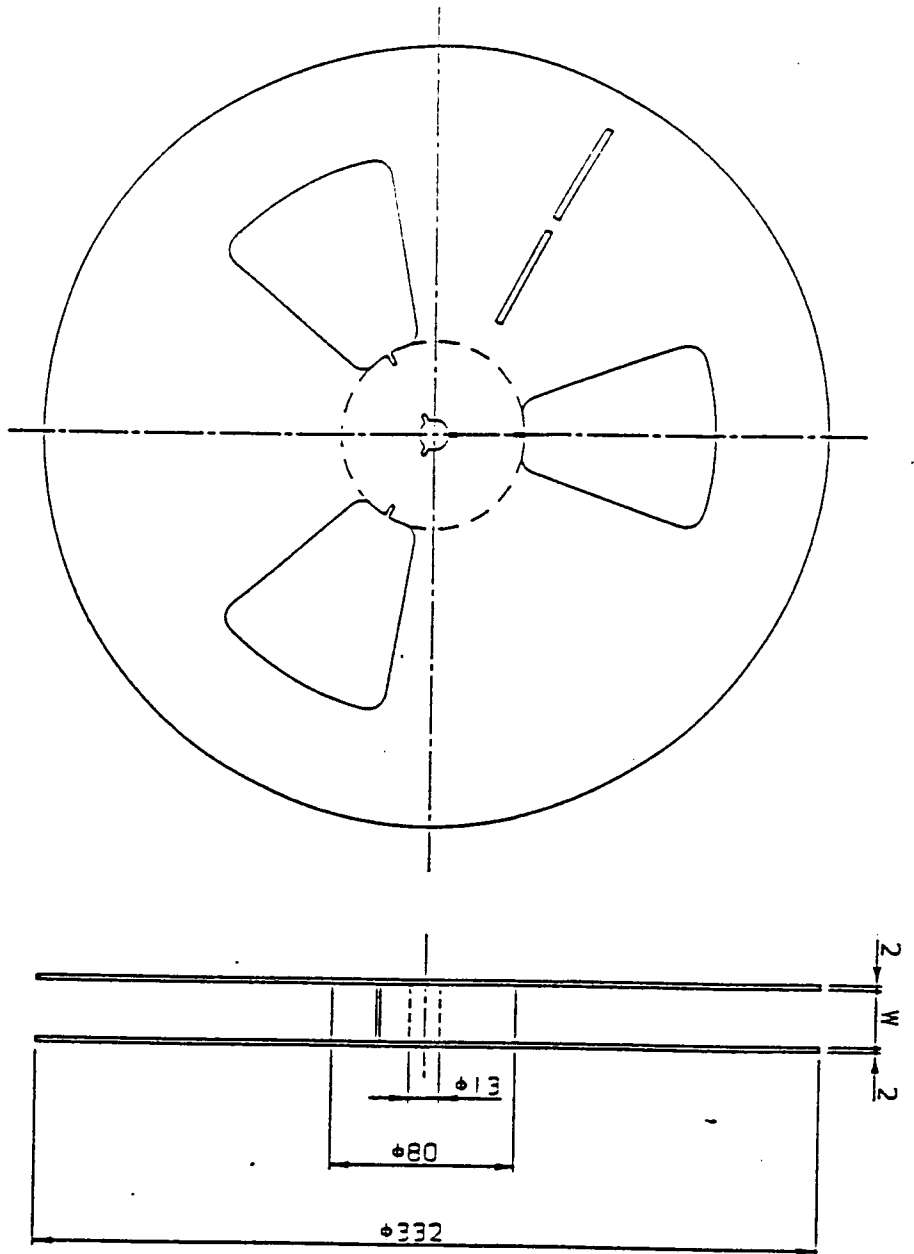
LEADER SIDE AND END SIDE OF TAPE



尺 度 SCALE	单 位 UNIT	△	
/	1 = /	△	
材 質 MATERIAL	仕 上 FINISH	改 訂 日 期 DATE	改 訂 記 事 REVISE
		名 称 NAME	EMBOSS TAPING TYPE (E2)
SHARP CORPORATION		编 号 CODE	
		图 号 DRAWING No	CV 5 2 2



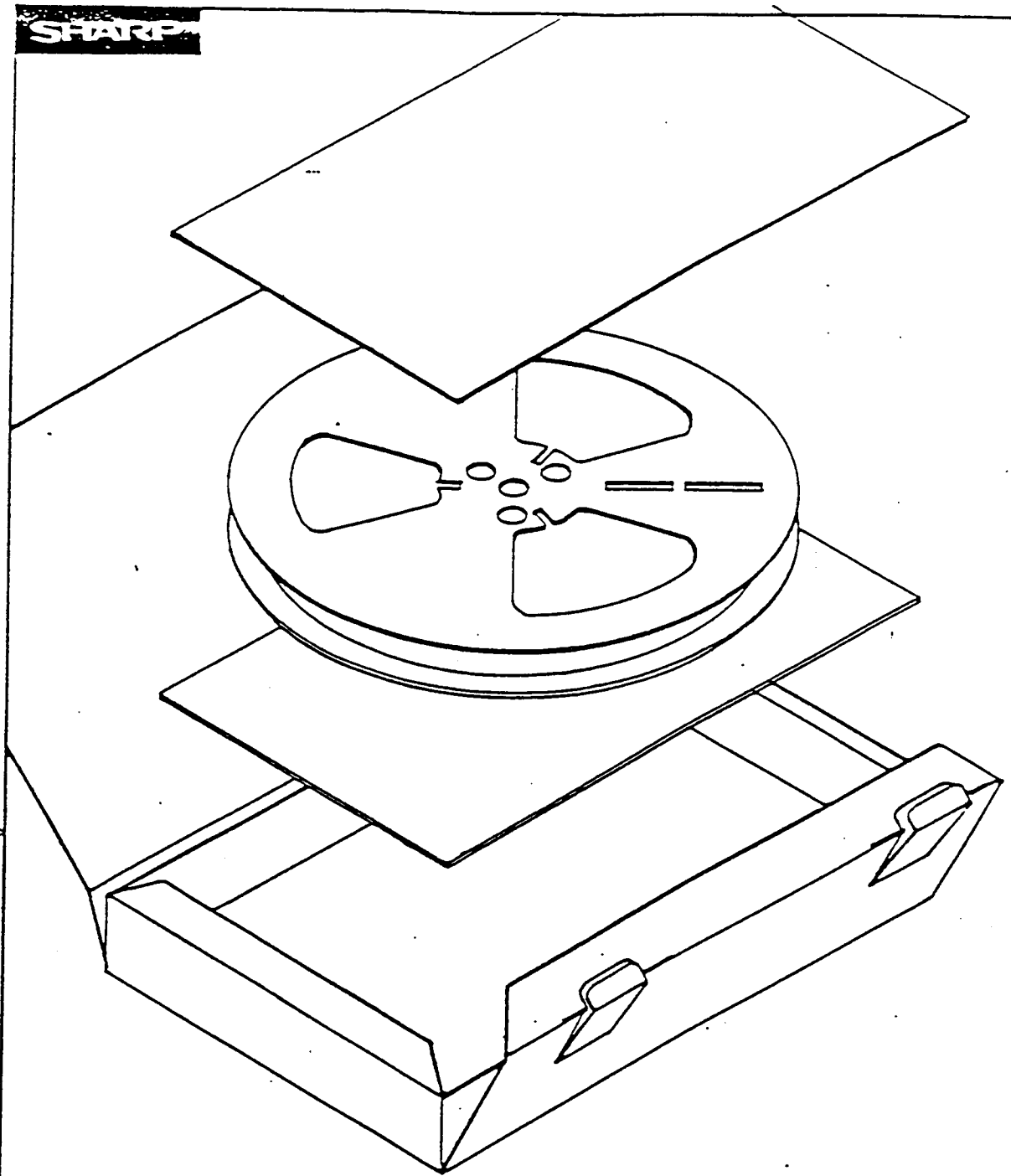
尺度 SCALE	単位 UNIT	△			
1/2	1 = mm/mm	△			
材質 MATERIAL	仕上 FINISH	改訂日 DATE	改訂記事 REVISION	担当者 CHARGE	
CONDUCTIVE PVC					名称 NAME EC28SPS
SHARP CORPORATION		コード CODE			
SHARP CORPORATION		図番 DRAWING No.	CV524		



PKG	W (mm)	TAPE NUMBER
SOP14-P-225	16.4	ECR16
SOP16-P-225	"	"
SOP24-P-450	24.4	ECR24
SOP28-P-450	"	"

尺度 SCALE	単位 UNIT	△ . . .	
/	1 = m/m	△ . . .	
材質 MATERIAL	仕上 FINISH	改訂日 DATE	改訂記事 REVISION
CONDUCTIVE PS		名 称 NAME	REEL FOR EMOSS CARRIER TAPING
シャープ株式会社 IC事業部		ニ 下 CODE	
SHARP CORPORATION		図 号 DRAWING No.	C.V.521
		担当 CHARGE	

SHARP



CASE, SIZE : 350 × 342 × 56 (mm)

尺 度 SCALE	单 位 UNIT	△			
/	1 = /	△			
材 質 MATERIAL	仕 上 FINISH	改 訂 DATE	改 訂 記 号 REVISION	再 査 査 査 CHARGE	
		名 称 NAME	EXTERNAL APPEARANCE OF PACKING CASE FOR EMBOSS CARRIER TAPING		
SHARP CORPORATION		品 番 CODE			
SHARP CORPORATION		図 号 DRAWING No	B.1	246	

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