

KS54AHCT 160/161
KS74AHCT 162/163

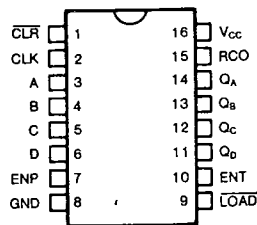
**Synchronous 4-Bit Decade
and Binary Counters**

T-45-23-05

FEATURES

- Internal Look Ahead for Fast Counting
- Carry Output for n-bit cascading
- Synchronous Counting
- Synchronously Programmable
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74AHCT: -40°C to $+85^{\circ}\text{C}$
 KS54AHCT: -55°C to $+125^{\circ}\text{C}$
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

PIN CONFIGURATION



FUNCTION TABLES

'160, '161

CLK	CLR	ENP	ENT	LOAD	Function
X	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

'162, '163

CLK	CLR	ENP	ENT	LOAD	Function
↑	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment counter

DESCRIPTION

These are synchronous, presettable 4-bit binary counters featuring internal carry-look-ahead for high-speed counting. The '160 and '162 are decade counters, and the '161 and '163 are 4-bit binary counters. The buffered clock input triggers all flip-flops simultaneously on the rising edge of the input waveform. This eliminates the output counting spikes normally associated with asynchronous counters.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

The clear function for the '160 and '161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load or enable inputs.

The clear function for the '162 and '163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter.

Two enable inputs and a ripple carry output allow easy cascading of the counters. Both count-enable inputs (ENP and ENT) must be high to count, and ENT is fed forward to enable the ripple carry output. The ripple carry output (RCO) thus enabled will produce a high-level pulse while the count is maximum (9 or 15 with Q_A high). This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that will modify the operating model have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

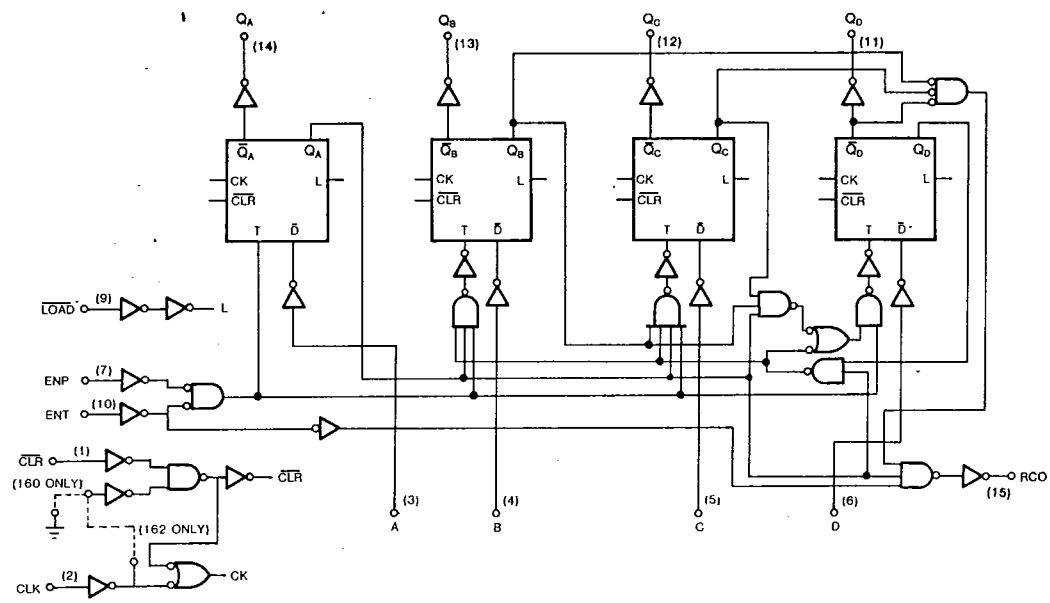
KS54AHCT 160/161
KS74AHCT 162/163

**Synchronous 4-Bit Decade
 and Binary Counters**

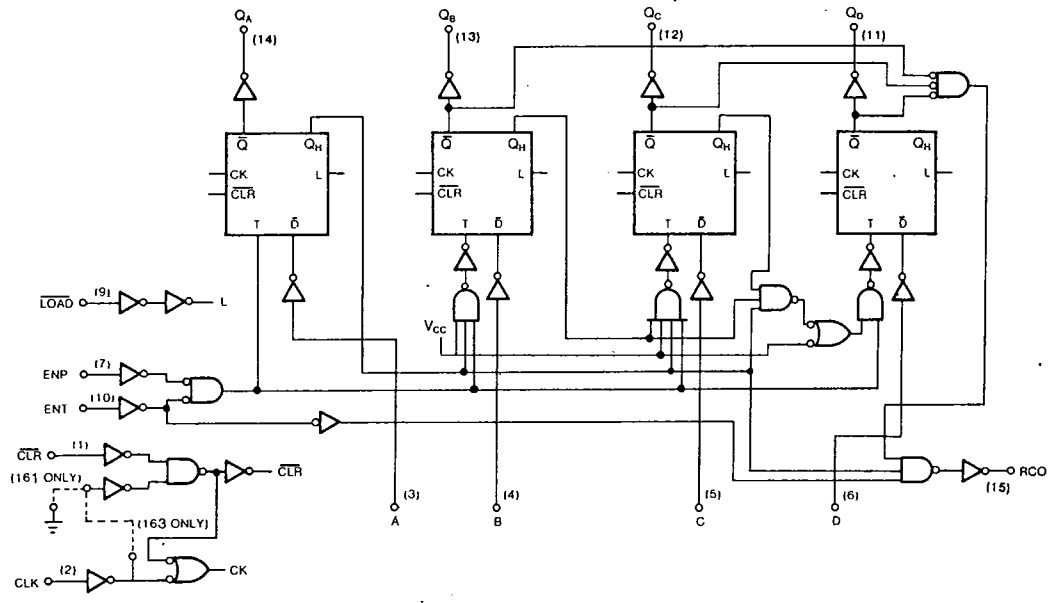
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LOGIC DIAGRAMS

'160 or '162



'161 or '163

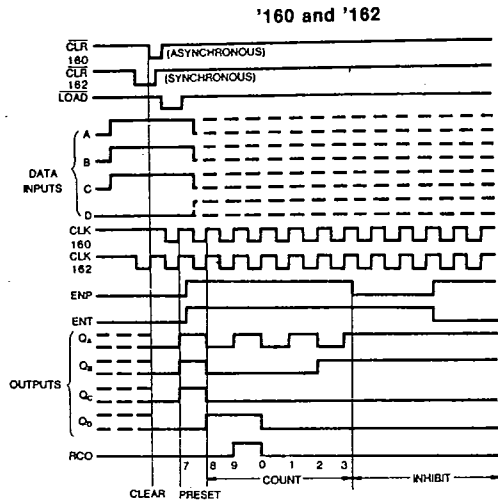


KS54AHCT 100/101
KS74AHCT 162/163

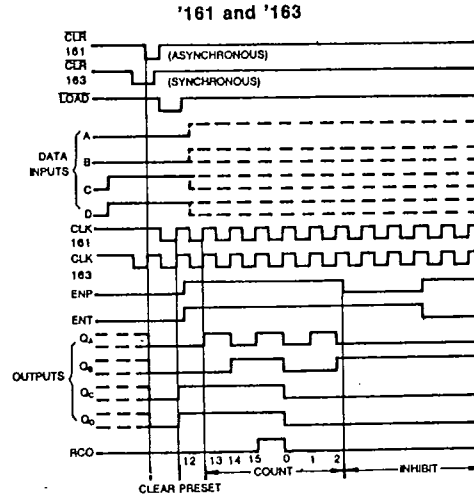
**Synchronous 4-Bit Decade
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Typical Clear, Preset, Count and Inhibit Sequences



- Sequence:**
- (1) Clear outputs to zero
 - (2) Preset to BCD seven
 - (3) Count to eight, nine, zero, one, two, and three
 - (4) Inhibit



- Sequence:**
- (1) Clear outputs to zero
 - (2) Preset to binary twelve
 - (3) Count to thirteen, fourteen, fifteen, zero, one and two
 - (4) Inhibit

Absolute Maximum Ratings*

- Supply Voltage Range V_{CC} -0.5V to +7V
- DC Input Diode Current, I_{IK}
 $(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ ± 20 mA
- DC Output Diode Current, I_{OK}
 $(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ± 20 mA
- Continuous Output Current Per Pin, I_O
 $(-0.5V < V_O < V_{CC} + 0.5V)$ ± 35 mA
- Continuous Current Through
 V_{CC} or GND pins ± 125 mA
- Storage Temperature Range, T_{stg} -65°C to +150°C
- Power Dissipation Per Package, P_d † 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

- † Power Dissipation temperature derating:
 Plastic Package (N): -12mW/°C from 65°C to 85°C
 Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating Conditions

- Supply Voltage, V_{CC} 4.5V to 5.5V
- DC Input & Output Voltages*, V_{IN}, V_{OUT} . . . 0V to V_{CC}
- Operating Temperature
 Range KS74AHCT: -40°C to +85°C
 KS54AHCT: -55°C to +125°C
- Input Rise & Fall Times, t_r, t_f Max 500 ns
- * Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

KS74AHCT **160/161**
 KS74AHCT **162/163**

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**Synchronous 4-Bit Decade
 and Binary Counters**

DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$			KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$		KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$		Unit
			Typ	Guaranteed Limits		Guaranteed Limits		Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0			V	
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8			V	
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O = -20\mu A$ $I_O = -4mA$	V_{CC} 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7			V	
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4			V	
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		± 0.1	± 1.0	± 1.0			μA	
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0			μA	
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I = 2.4V$ other inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0			mA	

AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 2$ ns, AHCT160, AHCT161)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ C$ $V_{CC} = 5.0V$		KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max		
Maximum Clock Frequency	f_{max}		50	40		35		MHz	
Propagation Delay, CLK to RCO	t_{PLH}	$C_L = 50pF$	15		20		24	ns	
	t_{PHL}		15		20		24		
Propagation Delay, CLK to any Q	t_{PLH}		10		16		19	ns	
	t_{PHL}		10		16		19		
Propagation Delay, ENT to RCO	t_{PLH}		8		13		16	ns	
	t_{PHL}		8		13		16		
Propagation Delay, CLR to any Q	t_{PHL}		15		24		29	ns	
Propagation Delay, CLR to RCO	t_{PHL}		17		23		33	ns	
Pulse Width	CLK High or Low		t_w	10	15		20		ns
	CLR Low			10	15		20		
Setup Time before CLK†	A, B, C, D	t_{su}	10	15		20	ns		
	LOAD		10	15		20			
	ENP, ENT		10	15		20			
	CLR inactive		6	10		10			
Hold time, All Synchronous Inputs after CLK†	t_h		-3	0		0	ns		
Input Capacitance	C_{IN}		5				pF		
Power Dissipation Capacitance*	C_{PD}		80				pF		

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
 † For AC switching test circuits and timing waveforms see section 2.



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RESISTANT
KS74AHCT **160/161**
162/163

**Synchronous 4-Bit Decade
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AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 2$ ns), AHCT162, AHCT163

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ	Min	Max	Min	Max	
Maximum Clock Frequency	f_{max}		50	40		35		MHz
Propagation Delay, CLK to RCO	t_{PLH}	$C_L = 50\text{pF}$	15		20		24	ns
	t_{PHL}		15		20		24	
Propagation Delay, CLK to any Q	t_{PLH}		10		16		20	ns
	t_{PHL}		10		16		20	
Propagation Delay, ENT to RCO	t_{PLH}		9		15		18	ns
	t_{PHL}		9		15		18	
Pulse Width, CLK High or Low	t_w		8	12.5		20	ns	
Setup Time before CLK†	A, B, C, D	t_{su}	10	15		20	ns	
	$\overline{\text{LOAD}}$		10	15		20		
	ENP, ENT		15	15		20		
	$\overline{\text{CLR}}$ inactive		6	10		10		
	$\overline{\text{CLR}}$ Low		6	15		20		
Hold time, All Synchronous Inputs after CLK†	t_h		-3	0		0	ns	
Input Capacitance	C_{IN}		5				pF	
Power Dissipation Capacitance*	C_{PD}		80				pF	

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

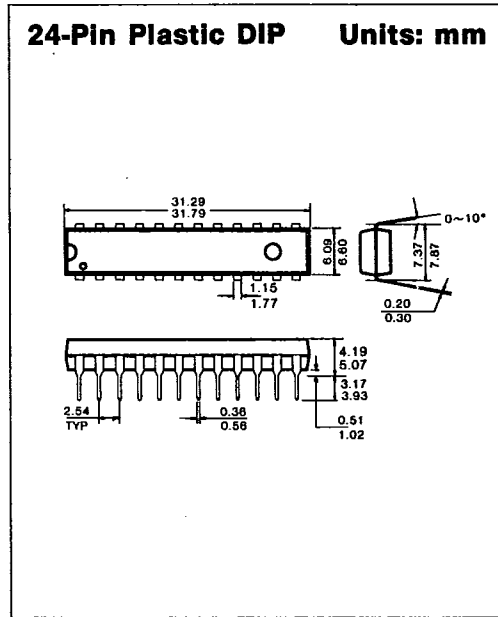
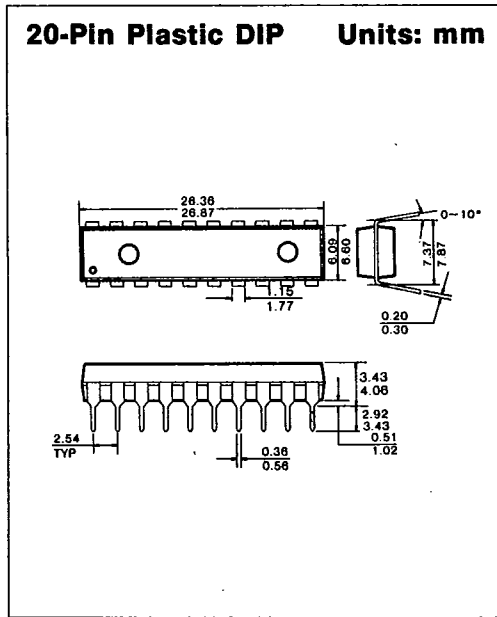
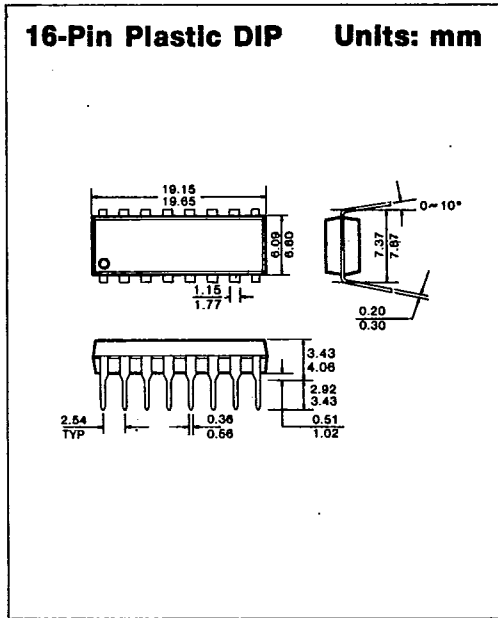
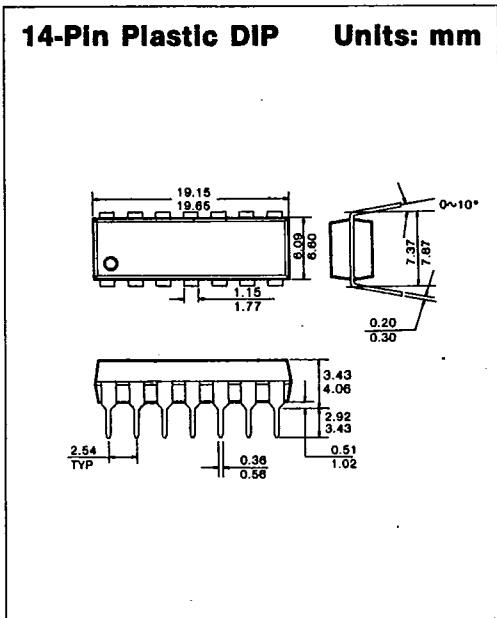
† For AC switching test circuits and timing waveforms see section 2.



PACKAGE DIMENSIONS

T-90-20

1. PLASTIC PACKAGES



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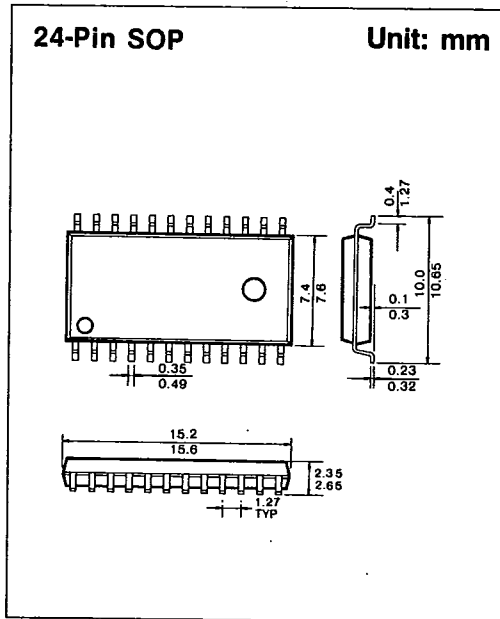
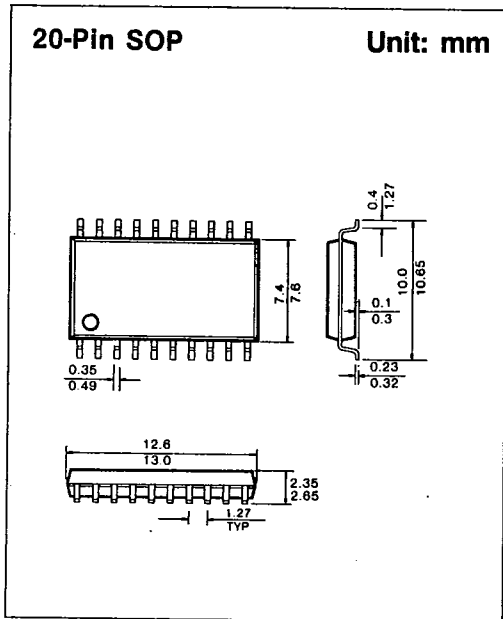
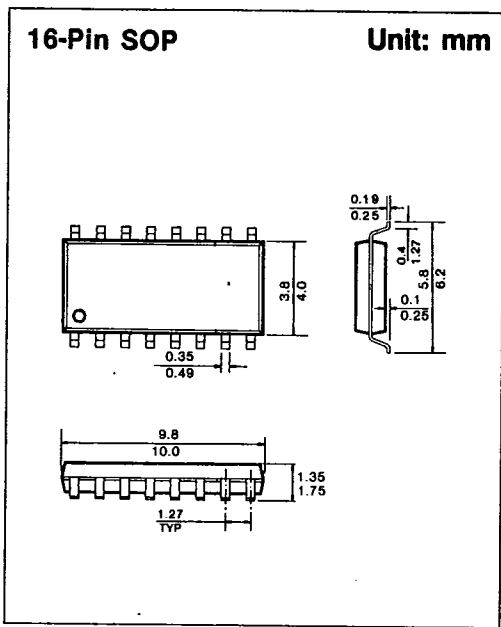
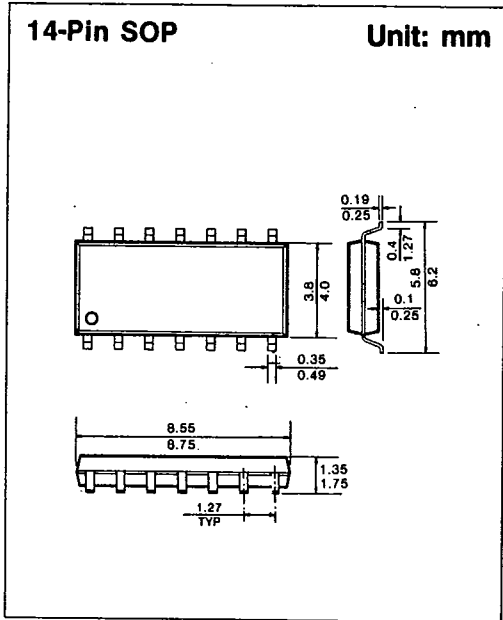
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PACKAGE DIMENSIONS

T-90-20

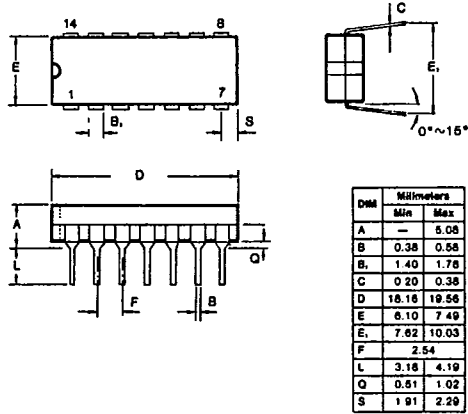


PACKAGE DIMENSIONS

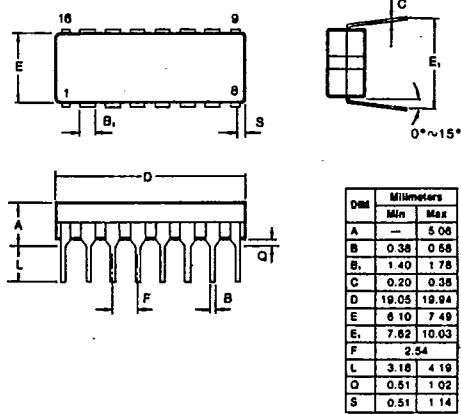
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2. CERAMIC PACKAGES

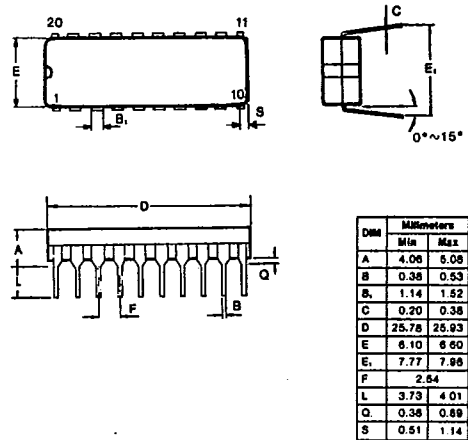
14-Pin Ceramic DIP Units: mm



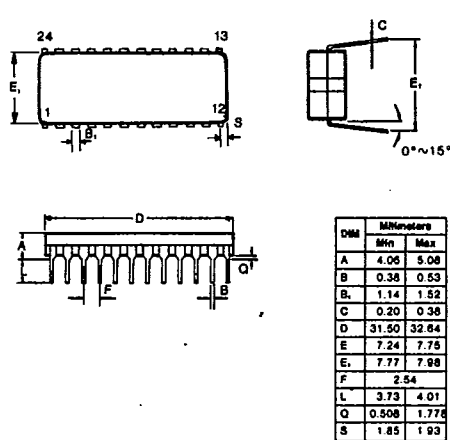
16-Pin Ceramic DIP Units: mm



20-Pin Ceramic DIP Units: mm



24-Pin Ceramic DIP Units: mm



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