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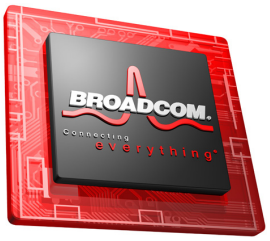
BCM3520 PRODUCT Brief



ATSC/NTSC/QAM DIGITAL CABLE READY DTV RECEIVER

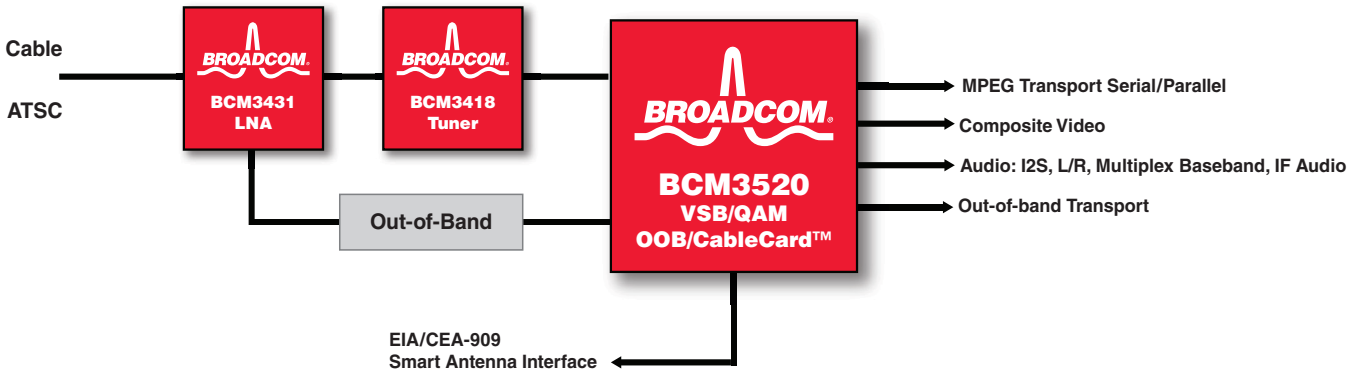
FEATURES

- **Integrated VSB/QAM QAMLink® receiver**
  - 12-bit A/D converter with internal AGC amplifier
  - Full equalizer architecture spans up to –35 to 49 µs delays
  - Direct IF sampled architecture reduces system cost
  - Single IF signal path for QAM/VSB/NTSC to reduce system costs
  - ITU-T J.83 Annex A/B/C FEC modes
  - MPEG-2 transport output (serial/parallel)
  - All-digital clock and carrier recovery
  - Integrated PLLs to minimize external components
  - All acquisition times typically less than 50 ms
- **QPSK out-of-band receiver**
  - 100–200-MHz receiver LO with input AGC and 6-bit A/D
  - Variable symbol rate QPSK receiver
  - Digital demodulator, Nyquist filters, tracking loops, and four-tap adaptive equalizer
  - DVS-167 (Davic™)/DVS-178 (DigiCipherII™) FEC decoder
- **NTSC/PAL IF Demodulator**
  - Adjacent channel rejection filters
  - Programmable digital audio trap filter
  - Programmable group delay compensation filter
  - Analog Composite Video Baseband Signal (CVBS) output
  - FM demod output supports internal BTSC stereo decoder, external BTSC stereo decoder (baseband or IF input), or external Zweiton M decoder
- **Integrated acquisition controller**
- **EIA/CEA-909 antenna interface**
- **144-pin LQFP package**

SUMMARY OF BENEFITS

- **Complete DTV single chip receiver solution**
- **FCC VSB and Digital Cable Ready**
- **Superior performance under both static and dynamic multi-path channel conditions**
- **Integrated NTSC demodulator**
- **BTSC decoder on chip**
- **Direct interface to CMOS and discrete DTV tuners**
- **Reduces system costs through direct IF sampling**
- **Single IF path for QAM/VSB/NTSC simplifies board design**
- **Smart antenna support**
- **Automatic NTSC co-channel interference and RFI rejection filters**
- **Integrated de-interleaver RAM for VSB FEC, and QAM for modes up to J=4 reduces system costs**
- **Analog stereo, mono, or SAP outputs**
- **I^2S or baseband multiplexed audio output**
- **On-chip stereo audio DACs**
- **BSC master to control peripherals**

Plug and Play DTV System Solution



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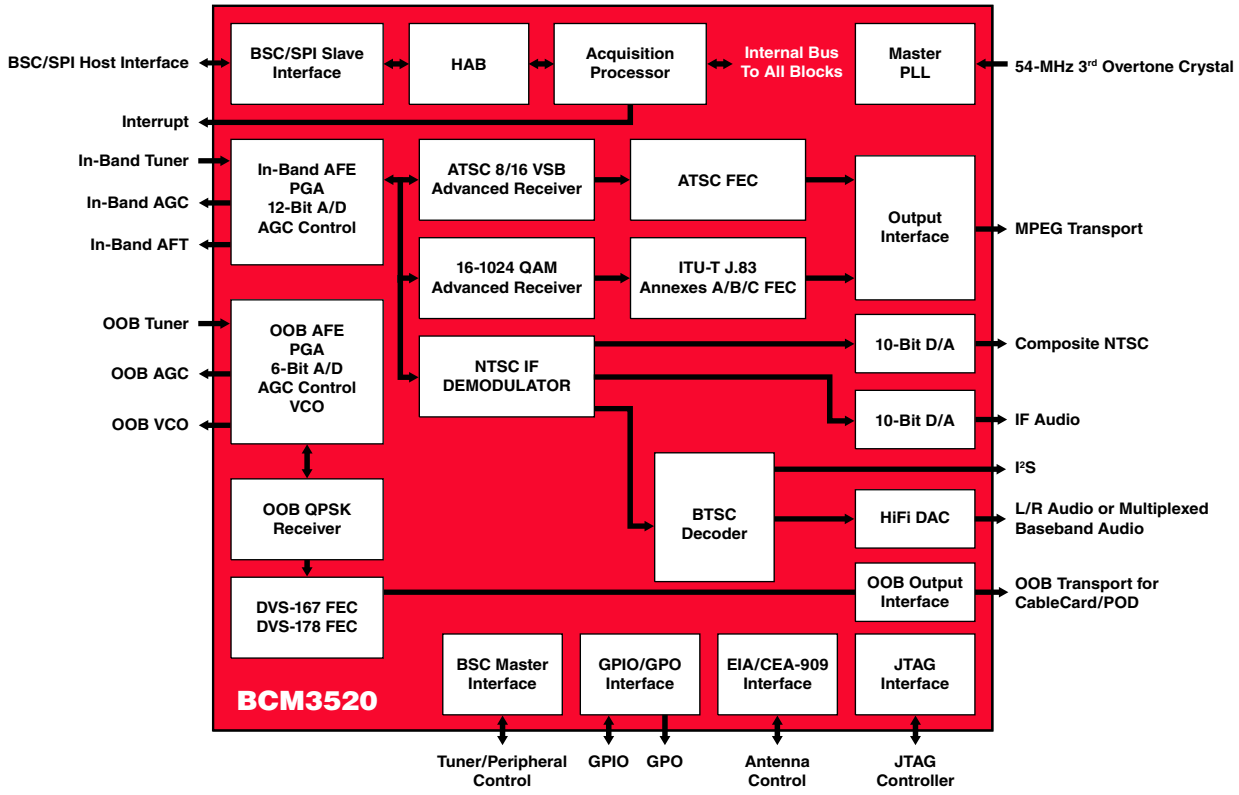
OVERVIEW



BCM3520 Block Diagram

The BCM3520 is a ATSC/NTSC/QAM Digital Cable Ready DTV receiver that contains a digital receiver that is compatible with both North American digital cable television and digital terrestrial broadcast television standards. This receiver is capable of receiving all standard-definition and high-definition digital formats (SDTV/HDTV). It also contains an IF demodulator compatible with the NTSC video standard. The output of the IF demodulator can be directed to an external BTSC or Zweiton M decoder, or can be sent to an on-chip audio decoder. The on-chip audio decoder is fully compliant with the BTSC audio standard. An out-of-band QPSK receiver is also contained to meet the needs of the CableCard specification.

The BCM3520's digital receiver and NTSC demodulator accepts an analog signal centered at the standard television IF frequencies, and amplifies and digitizes this signal with an integrated programmable gain amplifier and 12-bit A/D converter. The output of the A/D is sent to the receiver and demodulator. The digital receiver consists of a QAM demodulator and a VSB demodulator. Each demodulator contains adaptive filters that remove multi-path propagation effects, NTSC co-channel interference, and RFI interference. The output of the VSB demodulator goes to an ATSC A/53 coding forward error corrector (FEC), with integrated trellis and Reed-Solomon decoder. The output of the QAM demodulator goes to an ITU-T J.83 Annex A/B/C coding FEC. The output of either QAM or VSB FEC is delivered in either parallel or serial MPEG-2 transport format. The NTSC demodulator filters and demodulates the analog NTSC and FM audio signals and delivers a composite output via an on-chip 10-bit DAC. An IF modulated audio output is also provided via a second on-chip 10-bit DAC. An on-chip BTSC decoder handles the decoding of the base-band multiplexed audio from the IF demod, providing an stereo left/right, mono, or SAP output via a pair of high precision HiFiDACs.

All gain, clock, and carrier, acquisition, and tracking loops are integrated on-chip as are the necessary phase-locked loops, referenced to a single external crystal.

Chip configuration, channel acquisition, and performance monitoring functions are conducted by the on-chip acquisition processor using Broadcom-provided software.

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