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80220/80221
100BASE-TX/10BASE-T Ethernet
Media Interface Adapter

98184

Features

- **Single Chip 100Base-TX/10Base-T Physical Layer Solution**
- **Dual Speed - 100/10 Mbps**
- **Half And Full Duplex**
- **MII Interface To Ethernet Controller**
- **MI Interface For Configuration & Status**
- **Optional Repeater Interface**
- **AutoNegotiation: 10/100, Full/Half Duplex**
- **Meets All Applicable IEEE 802.3, 10Base-T, 100Base-TX Standards**
- **On Chip Wave Shaping - No External Filters Required**
- **Adaptive Equalizer**
- **Baseline Wander Correction**
- **Interface to External 100Base-T4 PHY**
- **LED Outputs**
  - **- Link**
  - **- Activity**
  - **- Collision**
  - **- Full Duplex**
  - **- 10/100**
  - **- User Programmable**
- **Many User Features And Options**
- **Few External Components**
- **Pin configuration**
  - **- 44L PLCC - 80220**
  - **- 64L LQFP - 80221**

Note: Check for latest Data Sheet revision before starting any designs.

SEEQ Data Sheets are now on the Web, at www.lsilogic.com.

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Description

The 80220/80221 are highly integrated analog interface IC's for twisted pair Ethernet applications. The 80220/80221 can be configured for either 100 Mbps (100Base-TX) or 10 Mbps (10Base-T) Ethernet operation. The 80220 is packaged in a 44L package, while the 80221 is packaged in a 64L package and contains a few more features.

The 80220/80221 consist of 4B5B/Manchester encoder/decoder, scrambler/descrambler, 100Base-TX/10Base-T twisted pair transmitter with wave shaping and output driver, 100Base-TX/10Base-T twisted pair receiver with on chip equalizer and baseline wander correction, clock and data recovery, AutoNegotiation, controller interface (MII), and serial port (MI).

The addition of internal output waveshaping circuitry and on-chip filters eliminates the need for external filters normally required in 100Base-TX and 10Base-T applications.
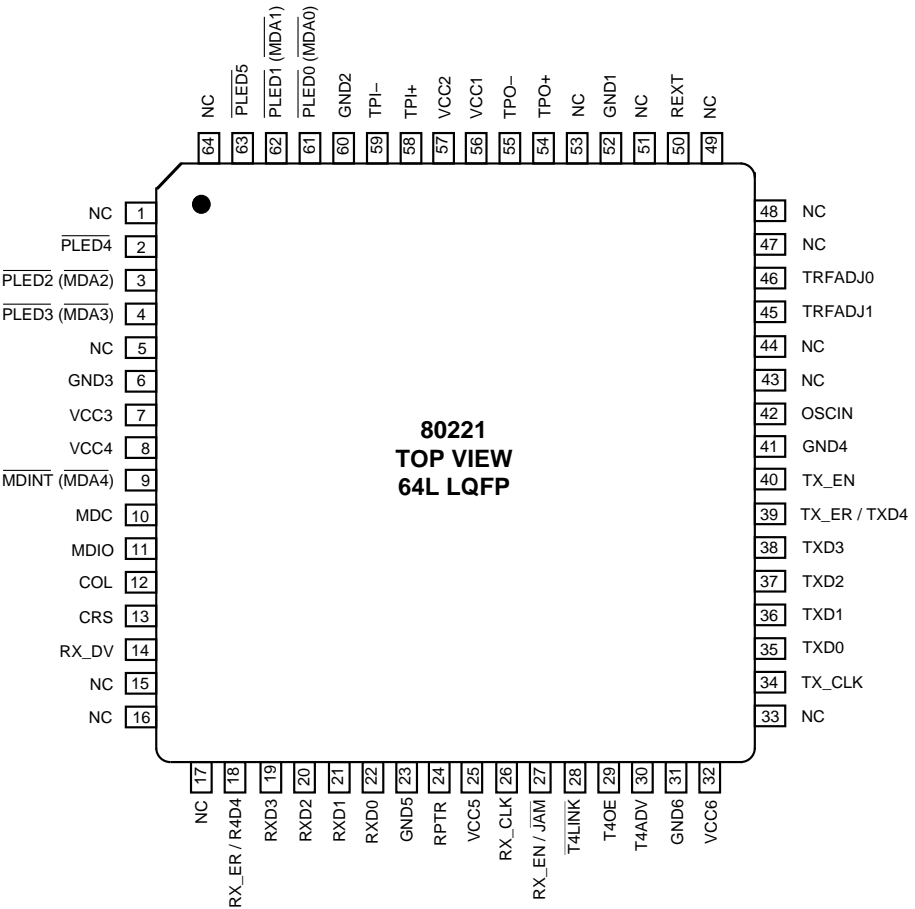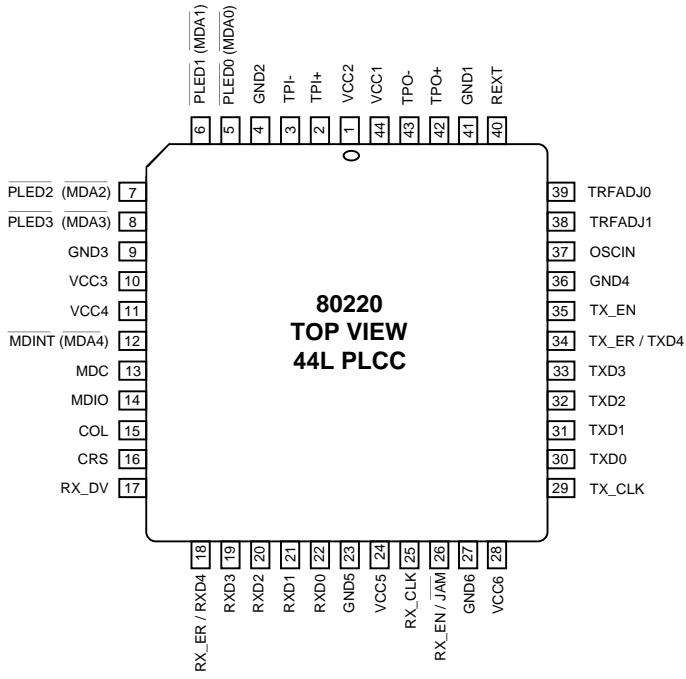
The 80220/80221 can automatically configure itself for 100 or 10 Mbps and Full or Half Duplex operation with the on-chip AutoNegotiation algorithm.

The 80220/80221 can access eleven 16-bit registers though the Management Interface (MI) serial port. These registers contain configuration inputs, status outputs, and device capabilities.

The 80220/80221 are ideal as media interfaces for 100Base-TX/10Base-T adapter cards, motherboards, repeaters, switching hubs, and external PHY's.

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Pin Configuration

**80220
TOP VIEW
44L PLCC**

Top pins (left to right): 6 PLED1 (MDA1), 5 PLED0 (MDA0), 4 GND2, 3 TPI-, 2 TPI+, 1 VCC2, 44 VCC1, 43 TPO-, 42 TPO+, 41 GND1, 40 REXT

Left pins (top to bottom):
PLED2 (MDA2) 7
PLED3 (MDA3) 8
GND3 9
VCC3 10
VCC4 11
MDINT (MDA4) 12
MDC 13
MDIO 14
COL 15
CRS 16
RX_DV 17

Right pins (top to bottom):
39 TRFADJ0
38 TRFADJ1
37 OSCIN
36 GND4
35 TX_EN
34 TX_ER / TXD4
33 TXD3
32 TXD2
31 TXD1
30 TXD0
29 TX_CLK

Bottom pins (left to right): 18 RX_ER / RXD4, 19 RXD3, 20 RXD2, 21 RXD1, 22 RXD0, 23 GND5, 24 VCC5, 25 RX_CLK, 26 RX_EN / JAM, 27 GND6, 28 VCC6

**80221
TOP VIEW
64L LQFP**

Top pins (left to right): 64 NC, 63 PLED5, 62 PLED1 (MDA1), 61 PLED0 (MDA0), 60 GND2, 59 TPI–, 58 TPI+, 57 VCC2, 56 VCC1, 55 TPO–, 54 TPO+, 53 NC, 52 GND1, 51 NC, 50 REXT, 49 NC

Left pins (top to bottom):
NC 1
PLED4 2
PLED2 (MDA2) 3
PLED3 (MDA3) 4
NC 5
GND3 6
VCC3 7
VCC4 8
MDINT (MDA4) 9
MDC 10
MDIO 11
COL 12
CRS 13
RX_DV 14
NC 15
NC 16

Right pins (top to bottom):
48 NC
47 NC
46 TRFADJ0
45 TRFADJ1
44 NC
43 NC
42 OSCIN
41 GND4
40 TX_EN
39 TX_ER / TXD4
38 TXD3
37 TXD2
36 TXD1
35 TXD0
34 TX_CLK
33 NC

Bottom pins (left to right): 17 NC, 18 RX_ER / R4D4, 19 RXD3, 20 RXD2, 21 RXD1, 22 RXD0, 23 GND5, 24 RPTR, 25 VCC5, 26 RX_CLK, 27 RX_EN / JAM, 28 T4LINK, 29 T4OE, 30 T4ADV, 31 GND6, 32 VCC6

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80220 / 80221 TABLE OF CONTENTS continued

1.0 Pin Description

Pin#		Pin Name	I/O	Description
44L	64L			
28 24 11 10 1 44	32 25 8 7 57 56	VCC6 VCC5 VCC4 VCC3 VCC2 VCC1	—	**Positive Supply.** 5 ± 5% Volts
27 23 36 9 4 41	31 23 41 6 60 52	GND6 GND5 GND4 GND3 GND2 GND1	—	**Ground.** 0 Volts
42	54	TPO+	O	**Twisted Pair Transmit Output, Positive.**
43	55	TPO -	O	**Twisted Pair Transmit Output, Negative.**
2	58	TPI+	I	**Twisted Pair Receive Input, Positive.**
3	59	TPI -	I	**Twisted Pair Receive Input, Negative.**
40	50	REXT	—	**Transmit Current Set.** An external resistor connected between this pin and GND will set the output current level for the twisted pair outputs.
37	42	OSCIN	I	**Clock Oscillator Input.** There must be either a 25 Mhz crystal between this pin and GND or a 25 Mhz clock applied to this pin. TX_CLK output is generated from this input.
29	34	TX_CLK	O	**Transmit Clock Output.** This controller interface output provides a clock to an external controller. Transmit data from the controller on TXD, TX_EN, and TX_ER is clocked in on rising edges of TX_CLK and OSCIN.
35	40	TX_EN	I	**Transmit Enable Input.** This controller interface input has to be asserted active high to indicate that data on TXD and TX_ER is valid, and it is clocked in on rising edges of TX_CLK and OSCIN.
33 32 31 30	38 37 36 35	TXD3 TXD2 TXD1 TXD0	I	**Transmit Data Input.** These controller interface inputs contain input nibble data to be transmitted on the TP outputs, and they are clocked in on rising edges of TX_CLK and OSCIN when TX_EN is asserted.
34	39	TX_ER / TXD4	I	**Transmit Error Input.** This controller interface input causes a special pattern to be transmitted on the twisted pair outputs in place of normal data, and it is clocked in on rising edges of TX_CLK when TX_EN is asserted. If the device is placed in the Bypass 4B5B Encoder mode, this pin is reconfigured to be the fifth TXD transmit data input, TXD4.
25	26	RX_CLK	O	**Receive Clock Output.** This controller interface output provides a clock to an external controller. Receive data on RXD, RX_DV, and RX_ER is clocked out on falling edges of RX_CLK.
16	13	CRS	O	**Carrier Sense Output.** This controller interface output is asserted active high when valid data is detected on the receive twisted pair inputs, and it is clocked out on falling edges of RX_CLK.
17	14	RX_DV	O	**Receive Data Valid Output.** This controller interface output is asserted active high when valid decoded data is present on the RXD outputs, and it is clocked out on falling edges of RX_CLK.
19 20 21 22	19 20 21 22	RXD3 RXD2 RXD1 RXD0	O	**Receive Data Output.** These controller interface outputs contain receive nibble data from the TP input, and they are clocked out on falling edges of RX_CLK.

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Pin Description continued

Pin#		Pin Name	I/O	Description
44L	64L			
18	18	RX_ER / RXD4	O	**Receive Error Output.** This controller interface output is asserted active high when a coding or other specified errors are detected on the receive twisted pair inputs and it is clocked out on falling edges of RX_CLK.
				If the device is placed in the Bypass 4B5B Decoder mode, this pin is reconfigured to be the fifth RXD receive data output, RXD4.
15	12	COL	O	**Collision Output.** This controller interface output is asserted active high when a collision between transmit and receive data is detected.
13	10	MDC	I	**Management Interface (MI) Clock Input.** This MI clock shifts serial data into and out of MDIO on rising edges.
14	11	MDIO	I/O	**Management Interface (MI) Data Input/Output.** This bidirectional pin contains serial MI data that is clocked in and out on rising edges of the MDC clock.
12	9	MDINT (MDA4)	I/O O.D. Pullup	**Management Interface Interrupt Output/Management Interface Address Input.** This pin is an interrupt output and is asserted active low whenever there is a change in certain MI serial port register bits, and deasserted after all changed bits have been read out.
				During powerup or reset, this pin is high impedance and the value on this pin is latched in as the physical device address MDA4 for the MI serial port
8	4	PLED3 (MDA3)	I/O O.D. Pullup	**Programmable LED Output/Management Interface Address Input.** The default function of this pin is to be a 100 Mbps Link Detect output. This pin can also be programmed through the MI serial port to indicate other events or be user controlled. This pin can drive an LED from VCC.
				When programmed as 100 Mbps Link Detect Output (default): 1= No Detect 0 = 100 Mbps Link Detected
				During powerup or reset, this pin is high impedance and the value on this pin is latched in as the physical device address MDA3 for the MI serial port.
7	3	PLED2 (MDA2)	I/O O.D. Pullup	**Programmable LED Output/Management Interface Address Input.** The default function of this pin is to be an Activity Detect output. This pin can also be programmed through the MI serial port to indicte other events or be user controlled. This pin can drive an LED from VCC.
				When programmed as an Activity Detect Output (default): 1 = No Activity 0 = Transmit Or Receive Packet Occurred, Hold Low for 100 mS
				During powerup or reset, this pin is high impedance and the value on this pin is latched in as the physical device address MDA2 for the MI serial port.
6	62	PLED1 (MDA1)	I/O Pullup	**Programmable LED Output/Management Interface Address Input.** The default function of this pin is to be a Full Duplex Detect output. This pin can also be programmed through the MI serial port to indicate other events or be user controlled. This pin can drive an LED from both VCC and GND.
				When programmed as Full Duplex Detect Output (default). 1 = Half Duplex 0 = Full Duplex
				During powerup or reset, this pin is high impedance and the value on this pin is latched in as the physical address device address MDA1 for the MI serial port.

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Pin Description continued

Pin# 44L	Pin# 64L	Pin Name	I/O	Description
5	61	PLED0 (MDA0)	I/O Pullup	**Programmable LED Output/Management Interface Address Input.** The default function of this pin is to be a 10 Mbps Link Detect output. This pin can also be programmed through the MI serial port to indicate other events or be user controlled. This pin can drive an LED from both VCC and GND. When programmed as 10 Mbps Link Detect Output (default): 1 = No Detect 0 = 10 Mbps Link Detected During powerup or reset, this pin is high impedance and the value on this pin is latched in as the address MDA0 for the MI serial port.
38 39	45 46	TRFADJ1 TRFADJ0	I Pullup Pulldown	**Twisted Pair Output Rise/Fall Time adjust Input.** These digital inputs adjust the rise/fall time on the TPO± outputs. 11 = Rise/Fall Time Changed -0.25 nS 10 = Rise/Fall Time Changed in MI Serial Port (Default = 0.0 nS) 01 = Rise/Fall Time Changed +0.25 nS 00 = Rise/Fall Time Changed +0.50 nS
26	27	RX_EN/ JAM	I	**Receive Enable Input** 1 = All Outputs Enabled 0 = Receive Controller Outputs are High Impedance (RX_CLK, RXD[3:0], RX_DV, RX_ER, COL).
			I	**Automatic Jam Input** 1 = Normal 0 = Jam Packet Transmitted when Receive Activity Detected
—	63	PLED5	O O.D. Pullup	**Receive LED Output.** The function of this pin is to be a Receive Activity Detect output and this pin can drive an LED from VCC. 1 = No Receive Activity 0 = Receive Packet Occurred, Hold Low for 100 mS
—	2	PLED4	O O.D. Pullup	**Transmit LED Output.** The function of this pin is to be a Transmit Activity Detect output and this pin can drive an LED from VCC. 1 = No Transmit Activity 0 = Transmit Packet Occurred, Hold Low for 100 mS
—	30	T4ADV	I Pulldown	**100Base-T4 AutoNegotiation Advertise Input.** This input causes the AutoNegotiation algorithm to advertise 100Base-T4 as one of the operating modes. 1 = Advertise 100Base-T4 Capability During AutoNegotiation 0 = No Advertise
—	29	T4OE	O	**100Base-T4 Output Enable.** This output indicates that the AutoNegotiation algorithm has selected 100Base-T4 as the operating mode and can be used to enable and external 100Base-T4 PHY. When asserted, the TP outputs are high impedance.
—	24	RPTR	I Pulldown	**Repeater Mode Enable Input.** 1 = Repeater Mode Enabled 0 = Normal Operation

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Pin Description continued

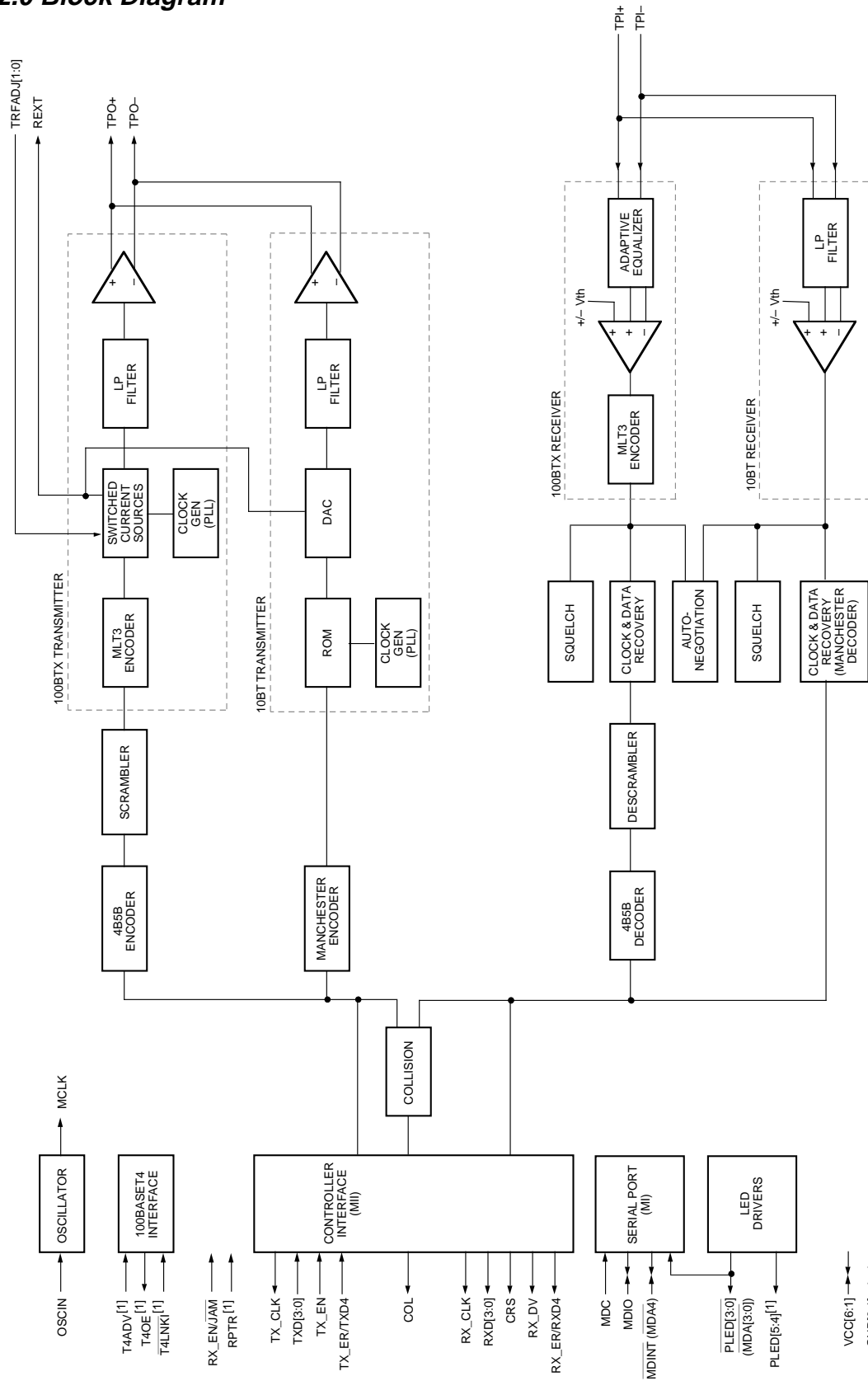| Pin# 44L	Pin# 64L	Pin	I/O	Description

—	28	T̄4̄L̄N̄K̄	I Pullup	**100Base-T4 Link Detect Input.** This input indicates to the device the link status of an external 100Base-T4 PHY.
				
				  1 = No Detect
				  0 = 100Base-T4 link Detected from external PHY

—	1 5 15 16 17 33 43 44 47 48 49 51 53 64	NC		**No Connect.**

2.0 Block Diagram

Figure 1. 80220 / 80221 Block Diagram

Note 1: These pins available on 64L 80221 version only.

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3.0 FUNCTIONAL DESCRIPTION

3.1 GENERAL

The 80220/80221 is a complete 100/10 Mbps Ethernet Media Interface IC. The 80220/80221 has ten main sections: controller interface, encoder, decoder, scrambler, descrambler, clock and data recovery, twisted pair transmitter, twisted pair receiver, MI serial port, and AutoNegotiation. A block diagram is shown in Figure 1.

The 80220/80221 can operate as a 100Base-TX device (hereafter referred to as 100 Mbps mode) or as a 10Base-T device (hereafter referred to as 10 Mbps mode). The difference between the 100 Mbps mode and the 10 Mbps mode is data rate, signalling protocol, and allowed wiring. The 100 Mbps mode uses two pairs of category 5 or better UTP or STP twisted pair cable with 4B5B encoded, scrambled, and MLT-3 coded 62.5 MHz ternary data to achieve a thruput of 100 Mbps. The 10 Mbps mode uses

two pairs of category 3 or better UTP or STP twisted pair cable with Manchester encoded, 10 MHz binary data to achieve a 10 Mbps thruput. The data symbol format on the twisted pair cable for the 100 and 10 Mbps modes are defined in IEEE 802.3 specifications and shown in Figure 2.

On the transmit side for 100 Mbps operation, data is received on the controller interface from an external Ethernet controller per the format shown in Figure 3. The data is then sent to the 4B5B encoder for formatting. The encoded data is then sent to the scrambler. The scrambled and encoded data is then sent to the TP transmitter. The TP transmitter converts the encoded and scrambled data into MLT-3 ternary format, preshapes the output, and drives the twisted pair cable.

ETHERNET MAC FRAME

INTERFRAME GAP	PREAMBLE	SFD	DA	SA	LN	LLC DATA	FCS	INTERFRAME GAP

100 BASE-TX TP DATA SYMBOLS

IDLE	SSD	PREAMBLE	SFD	DA	SA	LN	LLC DATA	FCS	ESD	IDLE

```
            IDLE = [ 1 1 1 1 ...]
             SSD = [ 1 1 0 0 0 1 0 0 0 1 ]
        PREAMBLE = [ 1 0 1 0 ...] 62 BITS LONG        BEFORE / AFTER
             SFD = [ 1 1 ]                             4B5B ENCODING,
DA, SA, LN, LLC DATA, FCS = [ DATA ]                   SCRAMBLING, AND
             ESD = [ 0 1 1 0 1 0 0 1 1 1 ]             MLT3 CODING
```

10 BASE-T TP DATA SYMBOLS

IDLE	PREAMBLE	SFD	DA	SA	LN	LLC DATA	FCS	SOI	IDLE

```
            IDLE = [ NO TRANSITIONS ]
        PREAMBLE = [ 1 0 1 0 ... ] 62 BITS LONG        BEFORE / AFTER
             SFD = [ 1 1 ]                             MANCHESTER
DA, SA, LN, LLC DATA, FCS = [ DATA ]                   ENCODING
             SOI = [ 1 1 ] WITH NO MID BIT
                           TRANSITION
```

Figure 2. Twisted Pair Frame Format

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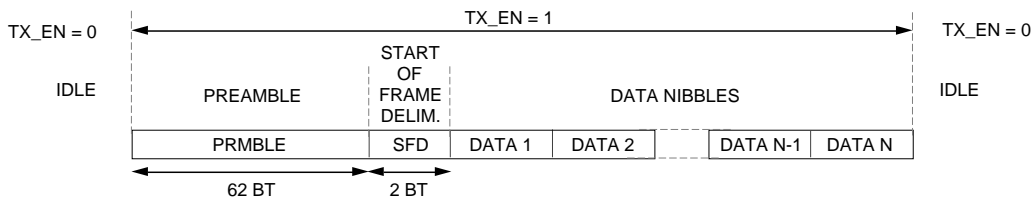
PREAMBLE = [1 0 1 0 ...] 62 BITS LONG
SFD = [1 1]
DATAn = [BETWEEN 64-1518 DATA BYTES]
IDLE = TX_EN = 0

a.) MII Frame Format
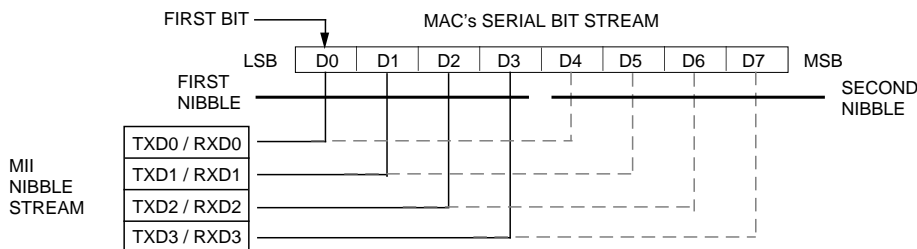
b.) MII Nibble Order

Signals	Bit Value																			
TXDO	X	X	1[1]	1	1	1	1	1	1	1	1	1	1	1	1	1	1[2]	1	D0[3]	D4[4]
TXD1	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D1	D5
TXD2	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D2	D6
TXD3	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	D3	D7
TX_EN	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

1. 1st preamble nibble transmitted.
2. 1st sfd nibble transmittted.
3. 1st data nibble transmitted.
4. D0 thru D7 are the first 8 bits of the data field.

c.) Transmit Preamble and SFD bits

Signals	Bit Value																		
RXDO	X	1[1]	1	1	1	1	1	1	1	1	1	1	1	1	1	1[2]	1	D0[3]	D4[4]
RXD1	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D1	D5
RXD2	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D2	D6
RXD3	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	D3	D7
RX_DV	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

1. 1st preamble nibble received. Depending on mode, device may eliminate
   either all or some of the preamble nibbles, up to 1st SFD nibble.
2. 1st sfd nibble received.
3. 1st data nibble received.
4. D0 thru D7 are the first 8 bits of the data field.

d.) Receive Preamble and SFD Bits

Figure 3. MII Frame Format

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On the receive side for 100 Mbps operation, the twisted pair receiver receives incoming encoded and scrambled MLT-3 data from the twisted pair cable, remove any high frequency noise, equalizes the input signal to compensate for the effects of the cable, qualifies the data with a squelch algorithm, and converts the data from MLT-3 coded twisted pair levels to internal digital levels. The output of the twisted pair receiver then goes to a clock and data recovery block which recovers a clock from the incoming data, uses the clock to latch in valid data into the device, and converts the data back to NRZ format. The NRZ data is then unscrambled and decoded by the 4B5B decoder and descrambler, respectively, and outputted to an external Ethernet controller by the controller interface.

10 Mbps operation is similar to the 100 Mbps operation except, (1) there is no scrambler/descrambler, (2) the encoder/decoder is Manchester instead of 4B5B, (3) the data rate is 10 Mbps instead of 100 Mbps, and (4) the twisted pair symbol data is two level Manchester instead of ternary MLT-3.

The AutoNegotiation block automatically configures the device for either 100Base-TX or 10Base-T, and for either Full or Half Duplex. This configuration is based on the capabilities selected for this device and the capabilities detected from a remote device.

The Management Interface, (hereafter referred to as the MI serial port), is a two pin bidirectional link through which configuration inputs can be set and status outputs can be read.

Each block plus the operating modes are described in more detail in the following sections. Since the 80220/80221 can operate either as a 100Base-TX or a 10Base-T device, each of the following sections describes the performance of the respective section in both the 100 and 10 Mbps modes.

3.2 DIFFERENCES BETWEEN 80220 AND 80221

The differences between the 80220 and 80221 are summarized in Table 1. For more information on each of these features, refer to the appropriate sections where these features are described.

Table 1. 80220 vs. 80221

Feature	80220	80221
Package	44L PLCC	64L LQFP
# LED Outputs	4	6
External 100Base-T4 Interface	No	Yes
Repeater Mode Pin	No	Yes

3.3 CONTROLLER INTERFACE

3.3.1 General

The 80220/80221 has two interfaces to an external controller: Media Independent Interface (referred to as the MII) and Five Bit interface (referred to as the FBI).

3.3.2 MII - 100 Mbps

The MII is a nibble wide packet data interface defined in IEEE 802.3 and shown in Figure 3. The 80220/80221 meets all the MII requirements outlined in IEEE 802.3. The 80220/80221 can directly connect, without any external logic, to any Ethernet controllers or other devices which also complies with the IEEE 802.3 MII specifications. The MII frame format is shown in Figure 3.

The MII consists of eighteen signals: four transmit data bits (TXD[3:0]), transmit clock (TX_CLK), transmit enable (TX_EN), transmit error (TX_ER), four receive data bits (RXD[3:0]), receive clock (RX_CLK), carrier sense (CRS), receive data valid (RX_DV), receive data error (RX_ER), and collision (COL). The transmit and receive clocks operate at 25 MHz in 100 Mbps mode.

On the transmit side, the TX_CLK output runs continuously at 25 Mhz. When no data is to be transmitted, TX_EN has to be deasserted. While TX_EN is deasserted, TX_ER and TXD[3:0] are ignored and no data is clocked into the device. When TX_EN is asserted on the rising edge of TX_CLK, data on TXD[3:0] is clocked into the device on rising edges of the TX_CLK output clock. TXD[3:0] input data is nibble wide packet data whose format needs to be the same as specified in IEEE 802.3 and shown in Figure 3. When all data on TXD[3:0] has been latched into the device, TX_EN has to be deasserted on the rising edge of TX_CLK.

TX_ER is also clocked in on rising edges of the TX_CLK clock. TX_ER is a transmit error signal which, when asserted, will substitute an error nibble in place of the normal data nibble that was clocked in on TXD[3:0]. The error nibble is defined to be the /H/ symbol which is defined in IEEE 802.3 and shown in Table 2.

Since OSCIN input clock generates the TX_CLK output clock, TXD[3:0], TX_EN, and TX_ER are also clocked in on rising edges of OSCIN.

On the receive side, as long as a valid data packet is not detected, CRS and RX_DV are deasserted and RXD[3:0] is held low. When the start of packet is detected, CRS and RX_DV are asserted on falling edge of RX_CLK. The assertion of RX_DV indicates that valid data is clocked out on RXD[3:0] on falling edges of the RX_CLK clock. The RXD[3:0] data has the same frame structure as the TXD[3:0] data and is specified in IEEE 802.3 and shown in Figure 3.

When the end of packet is detected, CRS and RX_DV are deasserted, and RXD[3:0] is held low. CRS and RX_DV also stay deasserted if the device is in the Link Fail State.

RX_ER is a receive error output which is asserted when certain errors are detected on a data nibble. RX_ER is asserted on the falling edge of RX_CLK for the duration of that RX_CLK clock cycle during which the nibble containing the error is being outputted on RXD[3:0].

The collision output, COL, is asserted whenever the collision condition is detected.

3.3.3 MII - 10 Mbps

10 Mbps operation is identical to the 100 Mbps operation except, (1) TX_CLK and RX_CLK clock frequency is reduced to 2.5 MHZ, (2) TX_ER is ignored, (3) RX_ER is disabled and always held low, and (4) receive operation is modified as follows: On the receive side, when the squelch circuit determines that invalid data is present on the TP inputs, the receiver is idle. During idle, RX_CLK follows TX_CLK, RXD[3:0] is held low, and CRS and RX_DV are deasserted. When a start of packet is detected on the TP receive inputs, CRS is asserted and the clock recovery process starts on the incoming TP input data. After the receive clock has been recovered from the data, the RX_CLK is switched over to the recovered clock and the data valid signal RX_DV is asserted on a falling edge of RX_CLK. Once RX_DV is asserted, valid data is clocked out on RXD[3:0] on falling edges of the RX_CLK clock. The RXD[3:0] data has the same packet structure as the TXD[3:0] data and is formatted on RXD[3:0] as specified in IEEE 802.3 and shown in Figure 3. When the end of packet is detected, CRS and RX_DV are deasserted. CRS and RX_DV also stay deasserted as long as the device is in the Link Fail State.

3.3.4 FBI - 100 Mbps

The Five Bit Interface (also referred to as the FBI) is a five bit wide interface that is produced when the 4B5B encoder/decoder is bypassed. The FBI is primarily used for repeaters or Ethernet controllers which have integrated encoder/decoders.

The FBI is identical to the MII except, (1) the FBI data path is five bits wide, not nibble wide like the MII, (2) TX_ER pin is reconfigured to be the fifth transmit data bit, TXD4, and (3) RX_ER pin is reconfigured to be the fifth receive data bit RXD4, (4) CRS is asserted as long as the device is in the Link Pass State, (5) COL is not valid, (6) RX_DV is not valid, and (7) TX_EN is ignored.

3.3.5 FBI - 10 Mbps

The FBI is not available in 10 Mbps mode.

3.3.6 Selection Of MII Or FBI

The FBI is automatically enabled when the 4B5B encoder/decoder is bypassed. Bypassing the encoder/decoder passes the 5B symbols between the receiver/transmitter directly to the FBI without any alteration or substitutions noted in the Encoder and Decoder sections. The 4B5B encoder/decoder can be bypassed by setting the bypass encoder bit in the MI serial port Configuration 1 register.

When the FBI is enabled, it may also be desirable to bypass the scrambler/descrambler and disable the internal CRS loopback function. The scrambler/descrambler can be bypassed by setting the bypass scrambler bit in the MI serial port Configuration 1 register. The internal CRS loopback can be disabled by setting the TX_EN to CRS loopback disable bit in the MI serial port Configuration 1 register.

3.3.7 MII Disable

The MII and FBI inputs and outputs can be disabled by setting the MII disable bit in the MI serial port Control register. When the MII is disabled, the MII/FBI inputs are ignored, the MII/FBI outputs are placed in high impedance state, and the TP output is high impedance.

If the MI address lines, $\overline{MDA[4:0]}$, are pulled high during reset or powerup, the 80220/80221 powers up and resets with the MII and FBI disabled. Otherwise, the 80220/80221 powers up and resets with the MII and FBI enabled.

3.3.8 Receive Output High Impedance Control

The $\overline{RX\_EN/JAM}$ pin can be configured to be RX_EN, a high impedance control for the receive controller output signals, by setting the R/J Configuration select bit in the MI serial port Configuration 2 register. When this pin is configured to be RX_EN and is deasserted active low, the following outputs will be placed in the high impedance state: RX_CLK, RXD[3:0], RX_DV, RX_ER, and COL.

3.3.9 TX_EN to CRS Loopback Disable

The internal TX_EN to CRS loopback can be disabled by appropriately setting the TXEN to CRS loopback disable bit in the MI serial port Configuration 1 register.

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3.4 ENCODER

3.4.1 4B5B Encoder - 100 Mbps

100Base-TX requires that the data be 4B5B encoded. 4B5B coding converts the 4-Bit data nibbles into 5-Bit date code words. The mapping of the 4B nibbles to the 5B code words is specified in IEEE 802.3 and shown in Table 2. The 4B5B encoder on the 80220/80221 takes 4B nibbles from the controller interface, converts them into 5B words according to Table 2, and sends the 5B words to the scrambler. The 4B5B encoder also substitutes the first 8 bits of the preamble with the SSD delimiters (a.k.a. /J/K/ symbols) and adds an ESD delimiter (a.k.a /T/R/ symbols) to the end of every packet, as defined in IEEE 802.3 and shown in Figure 2. The 4B5B encoder also fills the period between packets, called the idle period, with the a continuous stream of idle symbols, as shown in Figure 2.

3.4.2 Manchester Encoder - 10 Mbps

The Manchester encoding process combines clock and NRZ data such that the first half of the data bit contains the complement of the data, and the second half of the data bit contains the true data, as specified in IEEE 802.3. This guarantees that a transition always occurs in the middle of the bit cell. The Manchester encoder on the 80220/80221 converts the 10 Mbps NRZ data from the controller interface into a Manchester Encoded data stream for the TP transmitter and adds a start of idle pulse (SOI) at the end of the packet as specified in IEEE 802.3 and shown in Figure 2. The Manchester encoding process is only done on actual packet data, and the idle period between packets is not Manchester encoded and filled with link pulses.

Table 2. 4B/5B Symbol Mapping

Symbol Name	Description	5B Code	4B Code
0	Data 0	11110	0000
1	Data 1	01001	0001
2	Data 2	10100	0010
3	Data 3	10101	0011
4	Data 4	01010	0100
5	Data 5	01011	0101
6	Data 6	01110	0110
7	Data 7	01111	0111
8	Data 8	10010	1000
9	Data 9	10011	1001
A	Data A	10110	1010
B	Data B	10111	1011
C	Data C	11010	1100
D	Data D	11011	1101
E	Data E	11100	1110
F	Data F	11101	1111
I	Idle	11111	0000
J	SSD #1	11000	0101
K	SSD #2	10001	0101
T	ESD #1	01101	0000
R	ESD #2	00111	0000
H	Halt	00100	Undefined
---	Invalid codes	All others*	0000*

* These 5B codes are not used. For decoder, these 5B codes are decoded to 4B 0000. For encoder, 4B 0000 is encoded to 5B 11110, as shown in symbol Data 0.

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3.4.3 Encoder Bypass

The 4B5B encoder can be bypassed by setting the bypass encoder/decoder bit in the MI serial port Configuration 1 register. When this bit is set to bypass the encoder/ decoder, 5B code words are passed directly from the controller interface to the scrambler without any of the alterations described in the 4B5B Encoder section. Setting this bit automatically places the device in the FBI mode as described in the Controller Interface section.

3.4 DECODER

3.4.1 4B5B Decoder - 100 Mbps

Since the TP input data is 4B5B encoded on the transmit side, it must also be decoded by the 4B5B decoder on the receive side. The mapping of the 5B nibbles to the 4B code words is specified in IEEE 802.3 and shown in Table 2. The 4B45 decoder on the 80220/80221 takes the 5B code words from the descrambler, converts them into 4B nibbles per Table 2, and sends the 4B nibbles to the controller interface. The 4B5B decoder also strips off the SSD delimiter (a.k.a. /J/K/ symbols) and replaces them with two 4B Data 5 nibbles (a.k.a /5/ symbol), and strips off the ESD delimiter (a.k.a /T/R/ symbols) and replaces it with two 4B Data 0 nibbles (a.k.a /I/ symbol), per IEEE 802.3 specifications and shown in Figure 2.

The 4B5B decoder detects SSD, ESD and, codeword errors in the incoming data stream as specified in IEEE 802.3. These errors are indicated by asserting RX_ER output while the errors are being transmitted across RXD[3:0], and they are also indicated in the serial port by setting SSD, ESD, and codeword error bits in the MI serial port Status Output register.

3.4.2 Manchester Decoder - 10 Mbps

In Manchester coded data, the first half of the data bit contains the complement of the data, and the second half of the data bit contains the true data. The Manchester decoder in the 80220/80221 converts the Manchester encoded data stream from the TP receiver into NRZ data for the controller interface by decoding the data and stripping off the SOI pulse. Since the clock and data recovery block has already separated the clock and data from the TP receiver, the Manchester decoding process to NRZ data is inherently performed by that block.

3.4.3 Decoder Bypass

The 4B5B decoder can be bypassed by setting the bypass encoder/decoder bit in the MI serial port Configuration 1 register. When this bit is set to bypass the encoder/ decoder, (1) 5B code words are passed directly to the controller interface from the descrambler without any of the alterations described in the 4B5B Decoder section,

and (2) CRS is continuously asserted whenever the device is in the Link Pass state. Setting this bit automatically places the device in the FBI mode as described in the Controller Interface section.

3.5 CLOCK AND DATA RECOVERY

3.5.1 Clock Recovery - 100 Mbps

Clock recovery is done with a PLL. If there is no valid data present on the TP inputs, the PLL is locked to the 25 MHz TX_CLK. When valid data is detected on the TP inputs with the squelch circuit and when the adaptive equalizer has settled, the PLL input is switched to the incoming data on the TP input. The PLL then recovers a clock by locking onto the transitions of the incoming signal from the twisted pair wire. The recovered clock frequency is a 25 MHz nibble clock, and that clock is outputted on the controller interface signal RX_CLK.

3.5.2 Data Recovery - 100 Mbps

Data recovery is performed by latching in data from the TP receiver with the recovered clock extracted by the PLL. The data is then converted from a single bit stream into nibble wide data word according to the format shown in Figure 3.

3.5.3 Clock Recovery - 10 Mbps

The clock recovery process for 10 Mbps mode is identical to the 100 Mbps mode except, (1) the recovered clock frequency is 2.5 MHz nibble clock, (2) the PLL is switched from TX_CLK to the TP input when the squelch indicates valid data, (3) The PLL takes up to 12 transitions (bit times) to lock onto the preamble, so some of the preamble data symbols are lost, but the clock recovery block recovers enough preamble symbols to pass at least 6 nibbles of preamble to the receive controller interface as shown in Figure 3.

3.5.4 Data Recovery - 10 Mbps

The data recovery process for 10 Mbps mode is identical to the 100 Mbps mode. As mentioned in the Manchester Decoder section, the data recovery process inherently performs decoding of Manchester encoded data from the TP inputs.

3.6 SCRAMBLER

3.6.1 100 Mbps

100Base-TX requires scrambling to reduce the radiated emissions on the twisted pair. The 80220/80221 scrambler takes the encoded data from the 4B5B encoder, scrambles it per the IEEE 802.3 specifications, and sends it to the TP transmitter.

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3.6.2 10 Mpbs

A scrambler is not used in 10 Mbps mode.

3.6.3 Scrambler Bypass

The scrambler can be bypassed by setting the bypass scrambler/descrambler bit in the MI serial port Configuration 1 register. When this bit is set, the 5B data bypasses the scrambler and goes directly from the 4B5B encoder to the twisted pair transmitter.

3.7 DESCRAMBLER

3.7.1 100 Mbps

The 80220/80221 descrambler takes the scrambled data from the data recovery block, descrambles it per the IEEE 802.3 specifications, aligns the data on the correct 5B word boundaries, and sends it to the 4B5B decoder.

The algorithm for synchronization of the descrambler is the same as the algorithm outlined in the IEEE 802.3 specification. Once the descrambler is synchronized, it will maintain synchronization as long as enough descrambled idle pattern 1's are detected within a given interval. To stay in synchronization, the descrambler needs to detect at least 25 consecutive descrambled idle pattern 1's in a 1 mS interval. If 25 consecutive descrambled idle pattern 1's are not detected within the 1 mS interval, the descrambler goes out of synchronization and restarts the synchronization process.

If the descrambler is in the unsynchronized state, the descrambler loss of synchronization detect bit is set in the MI serial port Status Output register to indicate this condition. Once this bit is set, it will stay set until the descrambler achieves synchronization.

3.7.2 10 Mpbs

A descrambler is not used in 10 Mbps mode.

3.7.3 Descrambler Bypass

The descrambler can be bypassed by setting the bypass scrambler/descrambler bit in the MI serial port Configuration 1 register. When this bit is set, the data bypasses the descrambler and goes directly from the TP receiver to the 4B5B decoder.

3.8 TWISTED PAIR TRANSMITTER

3.8.1 Transmitter - 100 Mbps

The transmitter consists of a MLT-3 encoder, waveform generator and line driver.

The MLT-3 encoder converts the NRZ data from the scrambler into a three level MLT-3 code required by IEEE 802.3. MLT-3 coding uses three levels and converts 1's to transitions between the three levels, and converts 0's to no transitions or changes in level.

The purpose of the waveform generator is to shape the transmit output pulse. The waveform generator takes the MLT-3 three level encoded waveform and uses an array of switched current sources to control the rise/fall time and level of the signal at the output. The output of the switched current sources then goes through a low pass filter in order to "smooth" the current output and remove any high frequency components. In this way, the waveform generator preshapes the output waveform transmitted onto the twisted pair cable to meet the pulse template requirements outlined in IEEE 802.3. The waveform generator eliminates the need for any external filters on the TP transmit output.

The line driver converts the shaped and smoothed waveform to a current output that can drive 100 meters of category 5 unshielded twisted pair cable or 150 Ohm shielded twisted pair cable.

3.8.2 Transmitter - 10 Mbps

The transmitter operation in 10 Mbps mode is much different than the 100 Mbps transmitter. Even so, the transmitter still consists of a waveform generator and line driver.

The purpose of the waveform generator is to shape the output transmit pulse. The waveform generator consists of a ROM, DAC, clock generator, and filter.   The DAC generates a stair-stepped representation of the desired output waveform. The stairstepped DAC output then goes through a low pass filter in order to "smooth" the DAC output and remove any high frequency components. The DAC values are determined from the ROM outputs; the ROM contents are chosen to shape the pulse to the desired template and are clocked into the DAC at high speed by the clock generator. In this way, the waveform generator preshapes the output waveform to be transmitted onto the twisted pair cable to meet the pulse template requirements outlined in IEEE 802.3 Clause 14 and also shown in Figure 4. The waveshaper replaces and eliminates external filters on the TP transmit output.

The line driver converts the shaped and smoothed waveform to a current output that can drive 100 meters of category 3/4/5 100 Ohm unshielded twisted pair cable or 150 Ohm shielded twisted pair cable tied directly to the TP output pins without any external filters. During the idle period, no output signal is transmitted on the TP outputs (except link pulse).

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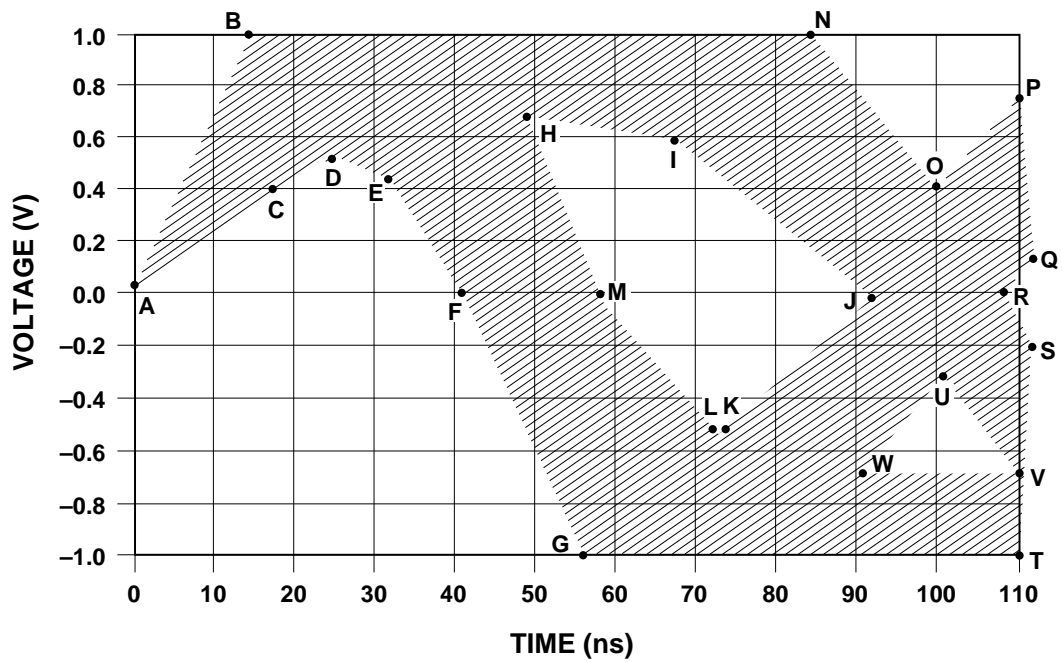
Figure 4. TP Output Voltage Template-10 Mbps

Voltage Template Values for Figure 4

Reference	Time (ns) Internal MAU	Voltage (V)
A	0	0
B	15	1.0
C	15	0.4
D	25	0.55
E	32	0.45
F	39	0
G	57	-1.0
H	48	0.7
I	67	0.6
J	89	0
K	74	-0.55
L	73	-0.55
M	61	0
N	85	1.0
O	100	0.4
P	110	0.75
Q	111	0.15
R	111	0
S	111	-0.15
T	110	-1.0
U	100	-0.3
V	110	-0.7
W	90	-0.7

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3.8.3 Transmit Level Adjust

The transmit output current level is derived from an internal reference voltage and the external resistor on REXT pin. The transmit level can be adjusted with either (1) the external resistor on the REXT pin, or (2) the four transmit level adjust bits in the MI serial port Configuration 1 register as shown in Table 3. The adjustment range is approximately -14% to +16% in 2% steps.

Table 3. Transmit Level Adjust

TLVL[3:0]	Gain
0000	1.16
0001	1.14
0010	1.12
0011	1.10
0100	1.08
0101	1.06
0110	1.04
0111	1.02
1000	1.00
1001	0.98
1010	0.96
1011	0.94
1100	0.92
1101	0.90
1110	0.88
1111	0.86

3.8.4 Transmit Rise And Fall Time Adjust

The transmit output rise and fall time can be adjusted with either (1) the two pins TRFADJ[1:0], or (2) the two transmit rise/fall time adjust bits in the MI serial port Configuration 1. The adjustment range is -0.25 nS to +0.5 nS in 0.25 nS steps. When the TRFADJ[1:0] pins are set to 1 and 0, respectively, the rise and fall times are set with the register bits (with 0 ns as the default). When TRFADJ[1:0] pin are set to anything other than 10, then the pins control the transmit rise and fall time as shown in the Pin Description and the TRFADJ[1:0] bits are disabled.

3.8.5 STP (150 Ohm) Cable Mode

The transmitter can be configured to drive 150 Ohm shielded twisted pair cable. The STP mode can be selected by appropriately setting the cable type select bit in the MI serial port Configuration 1 register. When STP

mode is enabled, the output current is automatically adjusted to comply with IEEE 802.3 levels.

3.8.6 Transmit Activity Indication

Transmit activity can be programmed to appear on some of the PLED[5:0] pins by appropriately setting the programmable LED output select bits in the MI serial port LED Configuration 2 register as described in Table 5. When one or more of the PLED[5:0] pins is programmed to be an activity or transmit activity detect output, that pin is asserted low for 100 mS every time a transmit packet occurs. The PLED[5:0] output is open drain with pullup resistor and can drive an LED from VCC or can drive another digital input.

3.8.7 Transmit Disable

The TP transmitter can be disabled by setting the transmit disable bit in the MI serial port Configuration 1 register. When the transmit disable bit is set, the TP transmitter is forced into the idle state, no data is transmitted, no link pulses are transmitted, and internal loopback is disabled.

3.8.8 Transmit Powerdown

The TP transmitter can be powered down by setting the transmit powerdown bit in the MI serial port Configuration 1 register. When the transmit powerdown bit is set, the TP transmitter is powered down, the TP transmit outputs are high impedance, and the rest of the 80220/80221 operates normally.

3.9 TWISTED PAIR RECEIVER

3.9.1 Receiver - 100 Mbps

The TP receiver detects input signals from the twisted pair input and convert it to a digital data bit stream ready for clock and data recovery. The receiver can reliably detect data from a 100Base-TX compliant transmitter that has been passed through 0-100 meters of 100 Ohm category 5 UTP or 150 Ohm STP.

The 100 Mbps receiver consists of an adaptive equalizer, baseline wander correction circuit, comparators, and MLT-3 decoder. The TP inputs first go to an adaptive equalizer. The adaptive equalizer compensates for the low pass characteristic of the cable, and it has the ability to adapt and compensate for 0-100 meters of category 5,100 Ohm UTP or 150 Ohm STP twisted pair cable. The baseline wander correction circuit restores the DC component of the input waveform that was removed by external transformers. The comparators convert the equalized signal back to digital levels and are used to qualify the data with the squelch circuit. The MLT-3 decoder takes the three

level MLT-3 digital data from the comparators and converts it to back to normal digital data to be used for clock and data recovery.

3.9.2 Receiver - 10 Mbps

The 10 Mbps receiver is able to detect input signals from the twisted pair cable that are within the template shown in Figure 5. The inputs are biased by internal resistors. The TP inputs pass through a low pass filter designed to eliminate any high frequency noise on the input. The output of the receive filter goes to two different types of comparators, squelch and zero crossing. The squelch comparator determines whether the signal is valid, and the zero crossing comparator is used to sense the actual data transitions once the signal is determined to be valid. The output of the squelch comparator goes to the squelch circuit and is also used for link pulse detection, SOI detection, and reverse polarity detection; the output of the zero crossing comparator is used for clock and data recovery in the Manchester decoder.
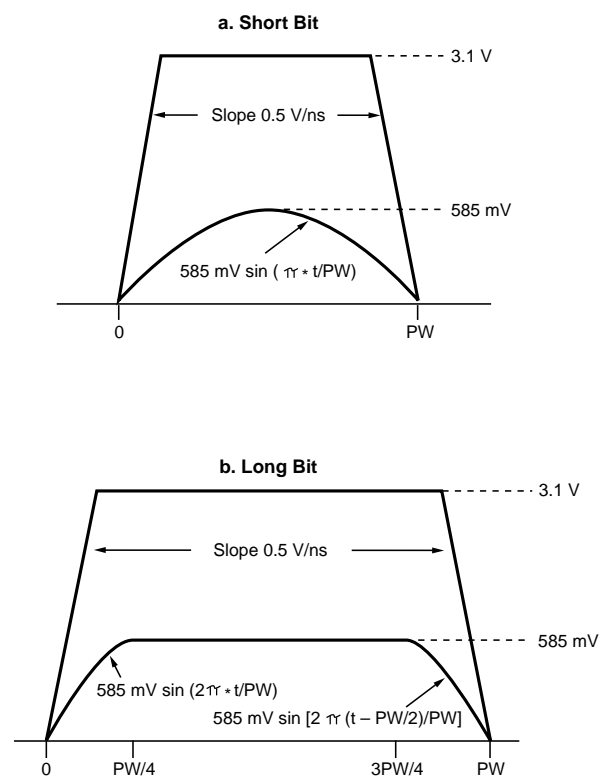
a. Short Bit

- - - - - 3.1 V

Slope 0.5 V/ns

- - - - 585 mV

585 mV sin ($\pi * t$/PW)

0   PW

b. Long Bit

- - - - - 3.1 V

Slope 0.5 V/ns

- - - - 585 mV

585 mV sin (2$\pi * t$/PW)

585 mV sin [2 π (t – PW/2)/PW]

0   PW/4   3PW/4   PW

Figure 5. TP Input Voltage Template-10Mbps

3.9.3 TP Squelch - 100 Mbps

The squelch block determines if the TP input contains valid data. The 100 Mbps TP squelch is one of the criteria used to determine link intergrity. The squelch comparators compare the TP inputs against fixed positive and negative thresholds, called squelch levels. The output from the squelch comparator goes to a digital squelch circuit which determines if the receive input data on that channel is valid. If the data is invalid, the receiver is in the squelched state. If the input voltage exceeds the squelch levels at least 4 times with alternating polarity within a 10 µS interval, the data is considered to be valid by the squelch circuit and the receiver now enters into the unquelch state.   In the unsquelch state, the receive threshold level is reduced by approximately 30% for noise immunity reasons and is called the unsquelch level. When the receiver is in the unsquelch state, then the input signal is deemed to be valid. The device stays in the unsquelch state until loss of data is detected. Loss of data is detected if no alternating polarity unsquelch transitions are detected during any 10 µS interval. When the loss of data is detected, the receive squelch is turned on again.

3.9.4 TP Squelch, 10 Mbps

The TP squelch algorithm for 10 Mbps mode is identical to the 100 Mbps mode except, (1) the 10 Mbps TP squelch algorithm is not used for link integrity but to sense the beginning of a packet, (2) the receiver goes into the unsquelch state if the input voltage exceeds the squelch levels for three bit times with alternating polarity within a 50-250 nS interval, (3) the receiver goes into the squelch state when idle is detected, (4) unsquelch detection has no affect on link integrity, link pulses are used for that in 10 Mbps mode, (5) start of packet is determined when the receiver goes into the unsquelch state and CRS is asserted, and (6) the receiver meets the squelch requirements defined in IEEE 802.3 Clause 14.

3.9.5 Equalizer Disable

The adaptive equalizer can be disabled by setting the equalizer disable bit in the MI serial port Configuration 1 register. When disabled, the equalizer is forced into the response it would normally have if zero cable length was detected.

3.9.6 Receive Level Adjust

The receiver squelch and unsquelch levels can be lowered by 4.5 dB by setting the receive level adjust bit in the MI serial port Configuration 1 register. By setting this bit, the device may be able to support longer cable lengths.

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3.9.7 Receive Activity Indication

Receive activity can be programmed to appear on some of the PLED[5:0] pins by appropriately setting the programmable LED output select bits in the MI serial port LED Configuration 2 register as shown in Table 5. When one or more of the PLED[5:0] pins is programmed to be an receive activity or activity detect output, that pin is asserted low for 100 mS every time a receive packet occurs. The PLED[5:0] outputs are open drain with pullup resistor and can drive an LED from VCC or can drive another digital input.

3.10 COLLISION

3.10.1 100 Mbps

Collision occurs whenever transmit and receive occur simultaneously while the device is in Half Duplex.

Collision is sensed whenever there is simultaneous transmission (packet transmission on TPO±) and reception (non idle symbols detected on TP input). When collision is detected, the COL output is asserted, TP data continues to be transmitted on twisted pair outputs, TP data continues to be received on twisted pair inputs, and internal CRS loopback is disabled. Once collision starts, CRS is asserted and stays asserted until the receive and transmit packets that caused the collision are terminated.

The collision function is disabled if the device is in the Full Duplex mode, is in the Link Fail state, or if the device is in the diagnostic loopback mode.

3.10.2 10 Mbps

Collision in 10 Mbps mode is identical to the 100 Mbps mode except, (1) reception is determined by the 10 Mbps squelch criteria, (2) RXD[3:0] outputs are forced to all 0's, (3) collision is asserted when the SQE test is performed, (4) collision is asserted when the jabber condition has been detected.

3.10.3 Collision Test

The controller interface collision signal, COL, can be tested by setting the collision test register bit in the MI serial port Control register. When this bit is set, TX_EN is looped back onto COL and the TP outputs are disabled.

3.10.4 Collision Indication

Collision can be programmed to appear on the PLED2 pin by appropriately setting the programmable LED output select bits in the MI serial port Configuration 2 register, as shown in Table 5. When the PLED2 pin is programmed to be a collision detect output, this pin is asserted low for 100 mS every time a collision occurs. The PLED2 output

is open drain with pullup resistor and can drive an LED from VCC or can drive another digital input.

3.11 START OF PACKET

3.11.1 100 Mbps

Start of packet for 100 Mbps mode is indicated by a unique Start of Stream Delimiter (referred to as SSD). The SSD pattern consists of the two /J/K/ 5B symbols inserted at the beginning of the packet in place of the first two preamble symbols, as defined in IEEE 802.3 Clause 24 and shown in Figure 2.

The transmit SSD is generated by the 4B5B encoder and the /J/K/ symbols are inserted by the 4B4B encoder at the beginning of the transmit data packet in place of the first two 5B symbols of the preamble, as shown in Figure 2.

The receive pattern is detected by the 4B5B decoder by examining groups of 10 consecutive code bits (two 5B words) from the descrambler. Between packets, the receiver will be detecting the idle pattern, which is 5B /I/ symbols. While in the idle state, CRS and RX_DV are deasserted.

If the receiver is in the idle state and 10 consecutive code bits from the receiver consist of the /J/K/ symbols, the start of packet is detected, data reception is begun, CRS and RX_DV are asserted, and /5/5/ symbols are substituted in place of the /J/K/ symbols.

If the receiver is in the idle state and 10 consecutive code bits from the receiver consist of a pattern that is neither /I/I/ nor /J/K/ symbols but contains at least 2 non contiguous 0's, then activity is detected but the start of packet is considered to be faulty and a False Carrier Indication (also referred to as bad SSD) is signalled to the controller interface. When False Carrier is detected, then CRS is asserted, RX_DV remains deasserted, RXD[3:0]=1110 while RX_ER is asserted, and the bad SSD bit is set in the MI serial port Status Output register. Once a False Carrier Event is detected, the idle pattern (two /I/I/ symbols) must be detected before any new SSD's can be sensed.

If the receiver is in the idle state and 10 consecutive code bits from the receiver consist of a pattern that is neither /I/I/ nor /J/K/ symbols but does not contain at least 2 non-contiguous 0's, the data is ignored and the receiver stays in the idle state.

3.11.2 10 Mbps

Since the idle period in 10 Mbps mode is defined to be the period when no data is present on the TP inputs, then the

start of packet for 10 Mbps mode is detected when valid data is detected by the TP squelch circuit. When start of packet is detected, CRS is asserted as described in the Controller Interface section. Refer to the TP squelch section for 10 Mbps mode for the algorithm for valid data detection.

3.12 END OF PACKET

3.12.1 100 Mbps

End of packet for 100 Mbps mode is indicated by a the End of Stream Delimiter (referred to as ESD). The ESD pattern consists of the two /T/R/ 4B5B symbols inserted after the end of the packet, as defined in IEEE 802.3 Clause 24 and shown in Figure 2.

The transmit ESD is generated by the 4B5B encoder and the /T/R/ symbols are inserted by the 4B5B encoder after the end of the transmit data packet, as shown in Figure 2.

The receive ESD pattern is detected by the 4B5B decoder by examining groups of 10 consecutive code bits (two 5B words) from the descrambler during valid packet reception to determine if there is an ESD.

If the 10 consecutive code bits from the receiver during valid packet reception consist of the /T/R/ symbols, the end of packet is detected, data reception is terminated, CRS and RX_DV are asserted, and /I/I/ symbols are substituted in place of the /T/R/ symbols.

If 10 consecutive code bits from the receiver during valid packet reception do not consist of /T/R/ symbols but consist of /I/I/ symbols instead, then the packet is considered to have been terminated prematurely and abnormally. When this premature end of packet condition is detected, RX_ER is asserted for the nibble associated with the first /I/ symbol detected and then CRS and RX_DV are deasserted. Premature end of packet condition is also indicated by setting the bad ESD bit in the MI serial port Status Output register.

3.12.2 10 Mbps

The end of packet for 10 Mbps mode is indicated with the SOI (Start of Idle) pulse. The SOI pulse is a positive pulse containing a Manchester code violation inserted at the end of every packet .

The transmit SOI pulse is generated by the TP transmitter and inserted at the end of the data packet after TX_EN is deasserted. The transmitted SOI output pulse at the TP output is shaped by the transmit waveshaper to meet the pulse template requirements specified in IEEE 802.3 Clause 14 and shown in Figure 6.

The receive SOI pulse is detected by the TP receiver by sensing missing data transitions. Once the SOI pulse is detected, data reception is ended and CRS and RX_DV are deasserted.
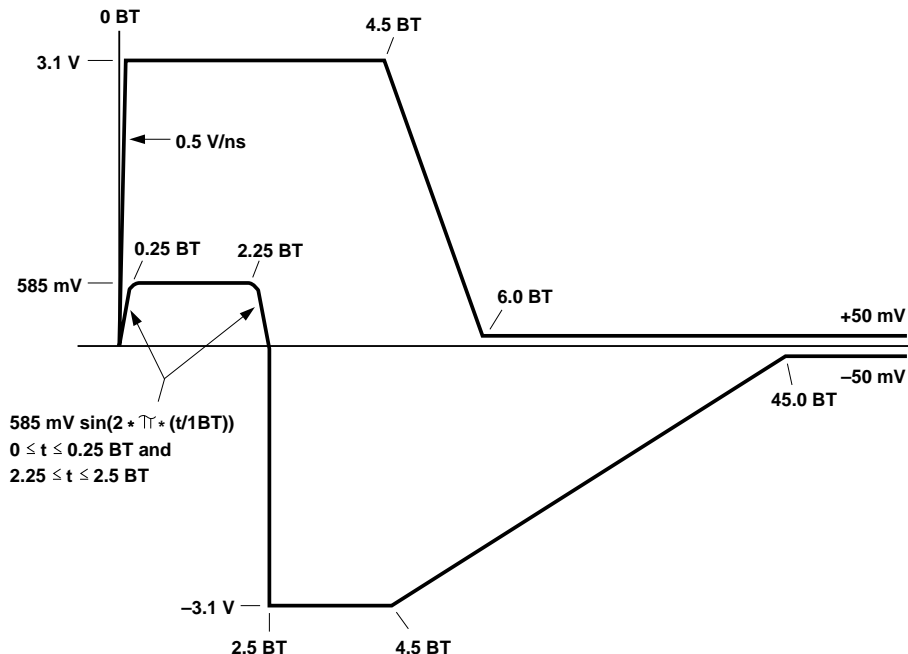
Figure 6. SOI Output Voltage Template - 10 Mbps

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3.13 LINK INTEGRITY & AUTONEGOTIATION

3.13.1 General

The 80220/80221 can be configured to implement either the standard link integrity algorithms or the AutoNegotiation algorithm.

The standard link integrity algorithms are used solely to establish an active link to and from a remote device. There are different standard link integrity algorithms for 10 and 100 Mbps modes. The AutoNegotiation algorithm is used for two purposes: (1) To automatically configure the device for either 10/100 Mbps and Half/Full Duplex modes, and (2) to establish an active link to and from a remote device. The standard link integrity and AutoNegotiation algorithms are described below.

3.13.2 10Base-T Link Integrity Algorithm - 10Mbps

The 80220/80221 uses the same 10Base-T link intergrity algorithm that is defined in IEEE 802.3 Clause 14. This algorithm uses normal link pulses, referred to as NLP's and transmitted during idle periods, to determine if a device has successfully established a link with a remote device (called Link Pass state). The transmit link pulse meets the template defined in IEEE 802.3 Clause 14 and shown in Figure 7. Refer to IEEE 802.3 Clause 14 for more details if needed.

3.13.3 100Base-TX Link Integrity Algorithm -100Mbps

Since 100Base-TX is defined to have an active idle signal, then there is no need to have separate link pulses like those defined for 10Base-T. The 80220/80221 uses the squelch criteria and descrambler synchronization algorithm on the input data to determine if the device has successfully established a link with a remote device (called Link Pass state). Refer to IEEE 802.3 for both of these algorithms for more details.

3.13.4 AutoNegotiation Algorithm

As stated previously, the AutoNegotiation algorithm is used for two purposes: (1) To automatically configure the device for either 10/100 Mbps and Half/Full Duplex modes, and (2) to establish an active link to and from a remote device. The AutoNegotiation algorithm is the same algorithm that is defined in IEEE 802.3 Clause 28. AutoNegotiation uses a burst of link pulses, called fast link pulses and referred to as FLP's, to pass up to 16 bits of signaling data back and forth between the 80220/80221 and a remote device. The transmit FLP pulses meet the templated specified in IEEE 802.3 and shown in Figure 7. A timing diagram contrasting NLP's and FLP's is shown in Figure 8.
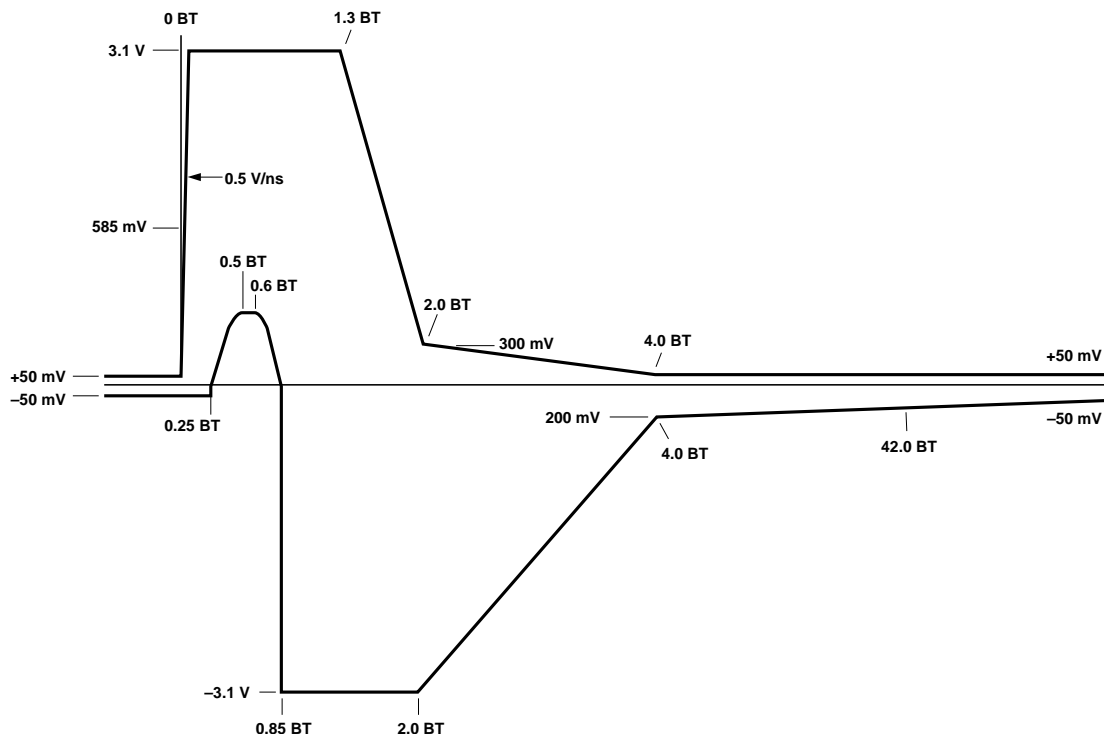
Figure 7. Link Pulse Output Voltage Template _ NLP, FLP

The AutoNegotiation algorithm is initiated by any of the following events: (1) Powerup, (2) device reset, (3) AutoNegotiation reset, (4) AutoNegotiation enabled, or (5) a device enters the Link Fail State. Once a negotiation has been initiated, the 80220/80221 first determines if the remote device has AutoNegotiation capability. If the remote device is not AutoNegotiation capable and is just transmitting either a 10Base-T or 100Base-TX signal, the 80220/80221 will sense that and place itself in the correct mode. If the 80220/80221 detects FLP's from the remote device, then the remote device is determined to have AutoNegotiation capability and the device then uses the contents of the MI serial port AutoNegotiation Advertisement register and FLP's to advertise its capabilities to a remote device. The remote device does the same, and the capabilities read back from the remote device are stored in the MI serial port AutoNegotiation Remote End Capability register. The 80220/80221 negotiation algorithm then matches it's capabilities to the remote device's capabilities and determines what mode the device should be configured to according to the priority resolution algorithm defined in IEEE 802.3 Clause 28. Once the negotiation process is completed, the 80220/80221 then configures itself for either 10 or 100 Mbps mode and either Full or Half Duplex modes (depending on the outcome of the negotiation process), and it switches to either the 100Base-TX or 10Base-T link integrity algorithms (depending on which mode was enabled by AutoNegotiation). Refer to IEEE 802.3 Clause 28 for more details.

3.13.5 AutoNegotiation Outcome Indication

The outcome or result of the AutoNegotiation process is stored in the speed detect and duplex detect bits in the MI serial port Status Output register.

3.13.6 AutoNegotiation Status

The status of the AutoNegotiation process can be monitored by reading the AutoNegotiation status bits in the MI serial port Status register. The MI serial port Status register contains a single AutoNegotiation acknowledgement bit which indicates when an AutoNegotiation has been initiated and successfully completed.
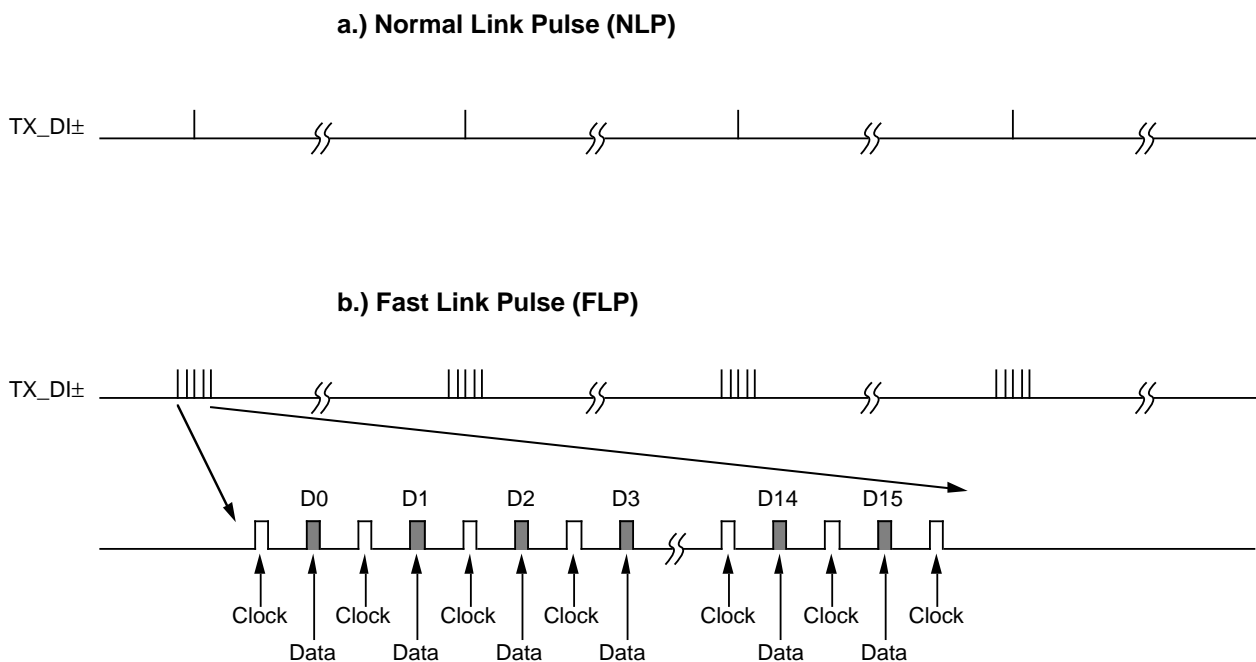
Figure 8. NLP vs. FLP Link Pulse

3.13.7 AutoNegotiation Enable

The AutoNegotiation algorithm can be enabled (or re-started) by setting the AutoNegotiation enable bit in the MI serial port Control register. When the AutoNegotiation algorithm is enabled, the device halts all transmissions including link pulses for 1200-1500 mS, enters the Link Fail State, and restarts the negotiation process. When the AutoNegotiation algorithm is disabled, the selection of 100 Mbps or 10 Mbps modes is determined by the speed select bit in the MI serial port Control register, and the selection of Half or Full Duplex is determined by the duplex select bit in the MI serial port Control register.

3.13.8 AutoNegotiation Reset

The AutoNegotiation algorithm can be initiated at any time by setting the AutoNegotiation reset bit in the MI serial port Control register.

3.13.9 Link Indication

Receive link detect activity can be monitored through the link detect bit in the MI serial port Status and Status Output registers or it can also be programmed to appear on the $\overline{PLED3}$ or $\overline{PLED0}$ pin by appropriately setting the programmable LED output select bits in the MI serial port Configuration 2 register as shown in Table 5. When either the $\overline{PLED3}$ or $\overline{PLED0}$ pins are programmed to be a link detect output, these pins are asserted low whenever the device is in the Link Pass State. The $\overline{PLED3}$ output is open drain with pullup resistor and can drive an LED from VCC; The $\overline{PLED0}$ output has both pullup and pulldown driver transistors in addition to a weak pullup resistor, so it can drive an LED from either VCC or GND. Both $\overline{PLED3}$ and $\overline{PLED0}$ can also drive another digital input. Refer to the LED Driver Section (3.23) for a description on how to program the PLED[3:0] pins and their defaults.

3.13.10 Link Disable

The link integrity function can be disabled by setting the link disable bit in the MI serial port Configuration 1 register. When the link integrity function is disabled, the device is forced into the Link Pass state, configures itself for Half/Full Duplex based on the value of the duplex bit in the MI serial port Control register, configures itself for 100/10 Mbps operation based on the values of the speed bit in the MI serial port Control register, and continues to transmit NLP's or TX idle patterns, depending on whether the device is in 10 or 100 Mbps mode.

3.13.11 100Base-T4 Capability

The 80221 has the ability to advertise and detect 100Base-T4 capability in addition to 100Base-TX Full/Half Duplex and 10Base-T Full/Half Duplex capability. Refer to the 100Base-T4 Interface section for more details.

3.14 JABBER

3.14.1 100 Mbps

Jabber function is disabled in the 100 Mbps mode.

3.14.2 10 Mbps

Jabber condition occurs when the transmit packet exceeds a predetermined length. When jabber is detected, the TP transmit outputs are forced to the idle state, collision is asserted, and register bits in the MI serial port Status and Status Output registers are set.

3.14.3 Jabber Disable

The jabber function can be disabled by setting the jabber disable bit in the MI serial port Configuration 2 register.

3.15 RECEIVE POLARITY CORRECTION

3.15.1 100 Mbps

No polarity detection or correction is needed in 100 Mbps mode.

3.15.2 10 Mbps

The polarity of the signal on the TP receive input is continuously monitored. If either 3 consecutive link pulses or one SOI pulse indicates incorrect polarity on the TP receive input, the polarity is internally determined to be incorrect, and a reverse polarity bit is set in the MI serial port Status Output register.

The 80220/80221 will automatically correct for the reverse polarity condition provided that the autopolarity feature is not disabled.

3.15.3 Autopolarity Disable

The autopolarity feature can be disabled by setting the autopolarity disable bit in the MI serial port Configuration 2 register.

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3.16 FULL DUPLEX MODE

3.16.1 100 Mbps

Full Duplex mode allows transmission and reception to occur simultaneously. When Full Duplex mode is enabled, collision is disabled and internal TX_EN to CRS loopback is disabled.

The device can be either forced into Half or Full Duplex mode, or the device can detect either Half or Full Duplex capability from a remote device and automatically place itself in the correct mode.

The device can be forced into the Full or Half Duplex modes by setting the duplex bit in the MI serial port Control register.

The device can automatically configure itself for Full or Half Duplex modes by using the AutoNegotiation algorithm to advertise and detect Full and Half Duplex capabilities to and from a remote terminal. All of this is described in detail in the Link Integrity and AutoNegotiation section.

3.16.2 10 Mbps

Full Duplex in 10 Mbps mode is identical to the 100 Mbps mode.

3.16.3 Full Duplex Indication

Full Duplex detection can be monitored through the duplex bit in the MI serial port Status Output register, or it can also be programmed to appear on the $\overline{PLED1}$ pin by appropriately setting the programmable LED output select bits in the MI serial port Configuration 2 register as described in Table 5. When the $\overline{PLED1}$ pin is programmed to be a Full Duplex detect output, this pin is asserted low when the device is configured for Full Duplex operation. The $\overline{PLED1}$ output has both pullup and pulldown driver transistors and a weak pullup resistor, so it can drive an LED from either VCC or GND and can also drive a digital input.

3.17 100/10 MBPS SELECTION

3.17.1 General

The device can be forced into either the 100 or 10 Mbps mode, or the device also can detect 100 or 10 Mbps capability from a remote device and automatically place itself in the correct mode.

The device can be forced into either the 100 or 10 Mbps mode by setting the speed select bit in the MI serial port Control register.

The device can automatically configure itself for 100 or 10 Mbps mode by using the AutoNegotiation algorithm to advertise and detect 100 and 10 Mbps capabilities to and from a remote terminal. All of this is described in detail in the Link Integrity & AutoNegotiation section.

3.17.2 10/100 Mbps Indication

The device speed (100/10 Mbps) can be determined through the speed bit in the MI serial port Status Output register, or it can also be programmed to appear on the PLED0 pin by setting the programmable LED output select bits in the MI serial port Configuration 2 register. When the PLED0 pin is programmed to be speed detect output, this pin is asserted low when the device is configured for 100 Mbps operation. The $\overline{PLED0}$ output has both pullup and pulldown driver transistors and a weak pullup resistor, so it can drive an LED from either VCC or GND and can also drive a digital input.

3.18 LOOPBACK

3.18.1 Internal CRS Loopback

TX_EN is internally looped back onto CRS during every transmit packet. This internal CRS loopback is disabled during collision, in Full Duplex mode, in Link Fail State, and when the transmit disable bit is set in the MI serial port Configuration 1 register. In 10 Mbps mode, internal CRS loopback is also disabled when jabber is detected.

The internal CRS loopback can be disabled by setting the TX_EN to CRS loopback disable bit in the MI serial port Configuration 1 register. When this bit is set, TX_EN is no longer looped back to CRS.

3.18.2 Diagnostic Loopback

A diagnostic loopback mode can also be selected by setting the loopback bit in the MI serial port Control register. When diagnostic loopback is enabled, TXD[3:0] data is looped back onto RXD[3:0], TX_EN is looped back onto CRS, RX_DV operates normally, the TP receive and transmit paths are disabled, the transmit link pulses are halted, and the Half/Full Duplex modes do not change. Diagnostic loopback mode can not be enabled when the FBI interface is selected.

3.19 AUTOMATIC JAM

3.19.1 100 Mbps

The 80220/80221 has an automatic JAM feature which will cause the device to automatically transmit a JAM packet if receive activity is detected. If automatic JAM is enabled, then the following $\overline{JAM}$ packet will be transmitted on TPO± when the JAM pin is asserted active low and receive activity is detected on TP inputs (expressed in 5B code words):

/J/K/5/5/5/5/5/5/5/5/5/5/5/5/D/H/H/H/H/H/H/H/T/R/

This automatic JAM feature is enabled when the RX_EN/$\overline{JAM}$ pin is programmed to be a $\overline{JAM}$ input. RX_EN/$\overline{JAM}$ can be configured to be a $\overline{JAM}$ input by appropriately setting the R/J configuration bit in the MI serial port Configuration 2 register.

3.19.2 10 Mbps

The JAM feature for 10 Mbps mode is identical to 100 Mbps mode except: (1) the JAM packet transmitted on TPO± is composed of standard 62 bit preamble (alternating 1,0) followed by SFD (11) followed by 32 bits of alternating 1,0 pattern.

3.20 RESET

The 80220/80221 is reset when either (1) VCC is applied to the device, or (2) the reset bit is set in the MI serial port Control register. When reset is initiated, an internal power-on reset pulse is generated which resets all internal circuits, forces the MI serial port bits to their default values, and latches in new values for the MI address. After the power-on reset pulse has finished, the reset bit in the MI serial port Control register is cleared and the device is ready for normal operation. The device is guaranteed to be ready for normal operation 500 mS after the reset was initiated.

3.21 POWERDOWN

The 80220/80221 can be powered down by setting the powerdown bit in the MI serial port Control register. In powerdown mode, the TP outputs are in high impedance state, all functions are disabled except the MI serial port, and the power consumption is reduced to a minimum. The device is guaranteed to be ready for normal operation 500 mS after powerdown is deasserted.

3.22 OSCILLATOR

The 80220/80221 requires a 25 Mhz reference frequency for internal signal generation. This 25 Mhz reference frequency is generated by either connecting an external 25 MHz crystal between OSCIN and GND or by applying an external 25Mhz clock to OSCIN.

3.23 LED DRIVERS

The $\overline{PLED[5:2]}$ outputs are open drain with a pullup resistor and can drive LED's tied to VCC. The $\overline{PLED[1:0]}$ outputs have both pullup and pulldown driver transistors with a pullup resistor, so $\overline{PLED[1:0]}$ can drive LED's tied to either VCC or GND.

The $\overline{PLED[5:0]}$ outputs can be programmed through the MI serial port to do 4 different functions: (1) Normal Function (2) On, (3) Off, and (4) Blink. $\overline{PLED[5:0]}$ can be programmed with the LED output select bits and the LED Normal Function select bits in the MI serial port Configuration 2 register.

When $\overline{PLED[5:0]}$ are programmed for their Normal Functions, these outputs indicate specific events. There are four sets of specific events that these outputs can indicate, and they are described in Tables 5 and 6. The selection of which set of events that these outputs indicate is determined by appropriately setting the LED Normal Function select bits in the MI serial port Configuration 2 register. The default Normal Functions for $\overline{PLED[5:0]}$ are Transmit Activity, Receive Activity, Link 100, Activity, Full Duplex, and Link 10, respectively. $\overline{PLED5}$ and $\overline{PLED4}$ are only available on the 64L 80221 version.

When $\overline{PLED[3:0]}$ is programmed to be On, the LED output driver go low, thus turning on the LED under user control. When $\overline{PLED[3:0]}$ is programmed to be Off, the LED output driver will turn off, thus turning off the LED under user control. When PLED[3:0] is programmed to Blink, the LED output driver will continuously blink at a rate of 100 mS on, 100 mS off.

Table 5. LED Normal Function Definition

BITS 17.7-6	PLED5	PLED4	PLED3	PLED2	PLED1	PLED0
11	RCV ACT	XMT ACT	LINK	COL	FDX	10/100
10	RCV ACT	XMT ACT	LINK	ACT	FDX	10/100
01	RCV ACT	XMT ACT	LINK + ACT	COL	FDX	10/100
00	RCV ACT	XMT ACT	LINK 100	ACT	FDX	LINK10

Device powers up with default set to 00.

Table 6. LED Event Definition

Symbol	Definition
XMT ACT	Transmit Activity Occurred, Stretch Pulse to 100 mS
RCV ACT	Receive Activity Occurred, Stretch Pulse to 100 mS
ACT	Activity Occurred, Stretch Pulse to 100 mS
COL	Collision Occurred, Stretch Pulse to 100 mS
LINK100	100 Mb Link Detected
LINK10	10 Mb Link Detected
LINK	100 or 10 Mb Link Detected
LINK+ACT	100 or 10 Mb Link Detected or Activity Occurred, Stretch Pulse To 100 mS (Link Detect Causes LED to be On, Activity Causes LED to Blink)
FDX	Full Duplex Mode Enabled
10/100	10 Mb Mode Enabled (High), or 100 Mb Mode Enabled (Low)

3.24 100BASE-T4 INTERFACE

The 80220/80221 has a 100Base-T4 (referred to as T4) interface to an external 100Base-T4 transceiver. This interface is available only on the 80221 64L version. The T4 interface is intended to allow the 80220/80221 to be able to perform AutoNegotiation with T4 as one of the advertised capabilities, then enable an external T4 transceiver if T4 is chosen as the operating mode at the conclusion of the AutoNegotiation process, and then turn over control of the TP cable to the external T4 transceiver.

The 80220/80221 will advertise T4 as one of its capabilities if either the T4ADV pin is asserted or the T4 capability bit is set in the MI serial port AutoNegotiation Advertisement register. If the AutoNegotiation process is initiated with the T4ADV pin asserted, T4 will be advertised along with any other capabilities written into the MI serial port AutoNegotiation Advertisement register. The AutoNegotiation process will then proceed as outlined in the Link Integrity & AutoNegotiation section with the addition of factoring T4 into the AutoNegotiation algorithm along with the other advertised capabilities. If T4 is selected by the AutoNegotiation process as the mode to be enabled, then the T4OE pin is asserted to enable an external T4 transceiver and the 80220/80221 transmitter is placed in the high impedance mode. The 80220/80221 then waits to see if the external T4 transceiver goes into the Link Pass state. If the external T4 transceiver goes into link pass within the required time, it has to assert the $\overline{\text{T4LNK}}$ input to the 80220/80221. In response, the 80220/80221 keeps the T4OE pin asserted and TP transmitter stays in high impedance. If the $\overline{\text{T4LNK}}$ pin doesn't get asserted within the required time, then the AutoNegotiation process restarts with the T4OE pin deasserted and 80220/80221 transmitter activated. If the T4OE output is asserted and the $\overline{\text{T4LNK}}$ input goes from asserted to deasserted, the AutoNegotiation process restarts with the T4OE pin deasserted and 80220/80221 transmitter activated.

3.25 REPEATER MODE

The 80221 has one predefined repeater mode which can be enabled by asserting the RPTR pin. When this repeater mode is enabled with the RPTR pin, the device operation is altered as follows: (1) TX_EN to CRS loopback is disabled, (2) AutoNegotiation is disabled, (3) 100 Mbps operation is enabled, and (4) Half Duplex operation is enabled. The RPTR pin is only available on the 80221 (64L version), and not available on the 80220 (44L version). Note that the repeater mode enabled by the RPTR pin is only one of many possible repeater modes available on the device; other repeater modes are available on both the 80220 and 80221 by setting the appropriate register bits to enable or disable the desired functions for a given repeater mode type. See the Repeater Applications Section (5.10.2) for more details on other possible repeater modes.

3.26 MI SERIAL PORT

3.26.1 Signal Description

The MI serial port has eight pins, MDC, MDIO, $\overline{\text{MDINT}}$, and $\overline{\text{MDA}}$[4:0]. MDC is the serial shift clock input. MDIO is a bidirectional data I/O pin. $\overline{\text{MDINT}}$ is an interrupt output. MDA[4:0] are address pins for the MI serial port.

$\overline{\text{MDA}}$[4:0] inputs share the same pins as the $\overline{\text{MDINT}}$ and $\overline{\text{PLED}}$[3:0] outputs, respectively. At powerup or reset, the $\overline{\text{PLED}}$[3:0] and $\overline{\text{MDINT}}$ output drivers are tristated for an interval called the power-on reset time. During the power-

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on reset interval, the value on these pins is latched into the device, inverted, and used as the MI serial port physical device addresses.

3.26.2 Timing

A timing diagram for a MI serial port frame is shown in Figure 9. The MI serial port is idle when at least 32 continuous 1's are detected on MDIO and remains idle as long as continuous 1's are detected. During idle, MDIO is in the high impedance state. When the MI serial port is in the idle state, a 01 pattern on the MDIO pin initiates a serial shift cycle. Data on MDIO is then shifted in on the next 14 rising edges of MDC (MDIO is high impedance). If the register access mode is not enabled, on the next 16 rising edges of MDC, data is either shifted in or out on MDIO, depending on whether a write or read cycle was selected with the bits READ and WRITE. After the 32 MDC cycles have been completed, one complete register has been read/written, the serial shift process is halted, data is latched into the device, and MDIO goes into high impedance state. Another serial shift cycle cannot be initiated until the idle condition (at least 32 continuous 1's) is detected.

3.26.3 Multiple Register Access

Multiple registers can be accessed on a single MI serial port access cycle with the multiple register access feature. The multiple register access feature can be enabled by setting the multiple register access enable bit in the MI serial port Configuration 2 register. When multiple register access is enabled, multiple registers can be accessed on a single MI serial port access cycle by setting the register address to 11111 during the first 16 MDC clock cycles. There is no actual register residing in register address location 11111, so when the register address is then set to 11111, all eleven registers are accessed on the 176 rising edges of MDC that occur after the first 16 MDC clock cycles of the MI serial port access cycle. The registers are accessed in numerical order from 0 to 20. After all 192 MDC clocks have been completed, all the registers have been read/written, and the serial shift process is halted, data is latched into the device, and MDIO goes into high impedance state. Another serial shift cycle cannot be initiated until the idle condition (at least 32 continuous 1's) is detected.

3.26.4 Bit Types

Since the serial port is bidirectional, there are many types of bits. Write bits (W) are inputs during a write cycle and are high impedance during a read cycle. Read bits (R) are outputs during a read cycle and high impedance during a write cycle. Read/Write bits (R/W) are actually write bits which can be read out during a read cycle. R/WSC bits are R/W bits that are self clearing after a set period of time or

after a specific event has completed. R/LL bits are read bits that latch themselves when they go low, and they stay latched low until read. After they are read, they are reset high. R/LH bits are the same as R/LL bits except that they latch high. R/LT are read bits that latch themselves whenever they make a transition or change value, and they stay latched until they are read. After R/LT bits are read, they are updated to their current value. R/LT bits can also be programmed to assert the interrupt function as described in the Interrupt section. The bit type definitions are summarized in Table 7.

Table 7. MI Register Bit Type Definition

Sym.	Name	Definition	
		Write Cycle	**Read Cycle**
W	Write	Input	No Operation, Hi Z
R	Read	No Operation, Hi Z	Output
R/W	Read/ Write	Input	Ouput
R/WSC	Read/ Write Self Clearing	Input	Ouput Clears Itself After Operation Completed
R/LL	Read/ Latching Low	No Operation, Hi Z	Output When Bit Goes Low, Bit Latched. When Bit Is Read, Bit Updated.
R/LH	Read/ Latching High	No Operation, Hi Z	Output When Bit Goes High, Bit Latched. When Bit Is Read, Bit Updated.
R/LT	Read/ Latching on Transition	No Operation, Hi Z	Output When Bit Transitions, Bit Latched And Interrupt Set When Bit Is Read, Interrupt Cleared And Bit Updated.

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Figure 9. MI Serial Port Frame Timing Diagram

WRITE CYCLE

MDC

MDIO

ST[1:0]　OP[1:0]　PHYAD[4:0]　REGAD[4:0]　TA[1:0]　DATA[15:0]

WRITE BITS
PHY CLOCKS IN DATA ON RISING EDGES OF MDC

READ CYCLE

MDC

MDIO

ST[1:0]　OP[1:0]　PHYAD[4:0]　REGAD[4:0]　TA[1:0]　DATA[15:0]

WRITE BITS
PHY CLOCKS IN DATA ON RISING EDGES OF MDC

READ BITS
PHY CLOCKS OUT DATA ON RISING EDGES OF MDC

29
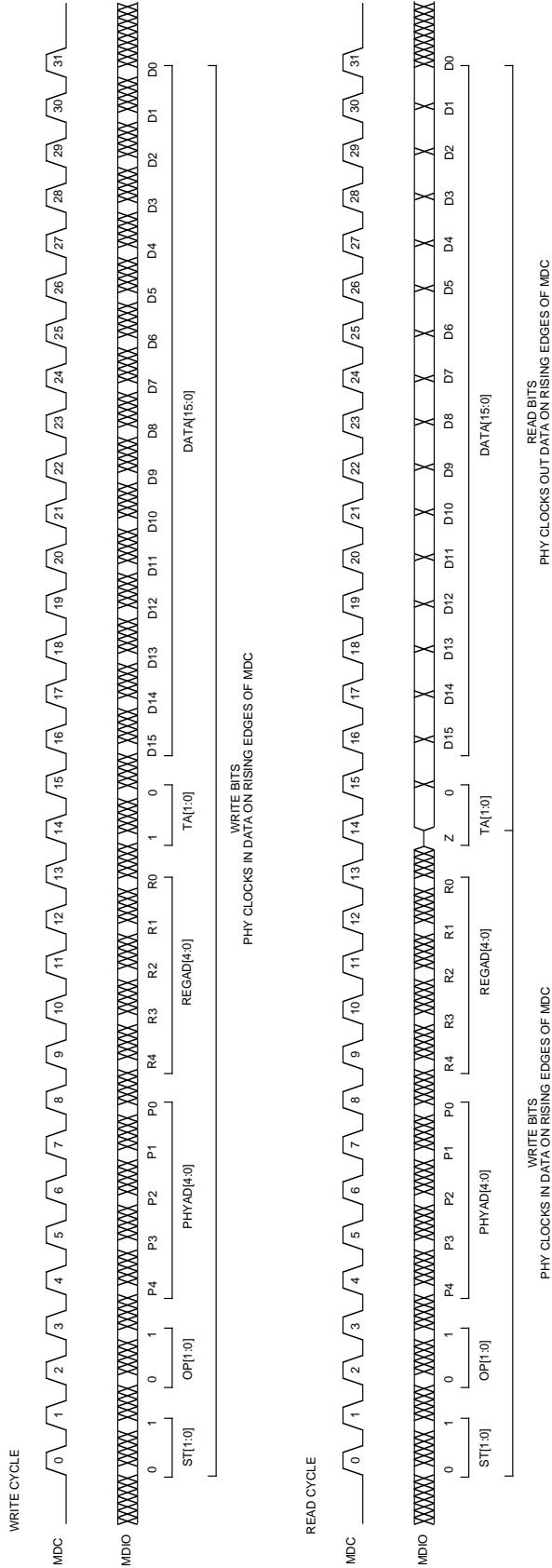
3.26.5 Frame Structure

The structure of the serial port frame is shown in Table 8 and a timing diagram of a frame is shown in Figure 9. Each serial port access cycle consists of 32 bits (or 192 bits if multiple register access is enabled and REGAD[4:0]=11111), exclusive of idle. The first 16 bits of the serial port cycle are always write bits and are used for addressing. The last 16/176 bits are from one/all of the 11 data registers.

The first 2 bits in Table 8 and Figure 9 are start bits and need to be written as a 01 for the serial port cycle to continue. The next 2 bits are a read and write bit which determine if the accessed data register bits will be read or write. The next 5 bits are device addresses and they must match the inverted values latched in from pins MDA[4:0] during the power-on reset time for the serial port access to continue. The next 5 bits are register address select bits which select one of the five data registers for access. The next 1 bit is a turnaround bit which is not an actual register bit but extra time to switch MDIO from write to read if necessary, as shown in Figure 2. The final 16 bits of the MI serial port cycle (or 176 bits if multiple register access is enabled and REGAD[4:0]=11111) come from the specific data register designated by the register address bits REGAD[4:0].

3.26.6 Register Structure

The 80220/80221 has eleven internal 16 bit registers. Ten registers are available for setting configuration inputs and reading status outputs, and one register is reserved for factory use. A map of the registers is shown in Table 9. The ten accessible registers consist of six registers that are defined by IEEE 802.3 specifications (Registers 0-5) and four registers that are unique to the 80220/80221 (Registers 16-19).

The structure and bit definition of the Control register is shown in Table 10. This register stores various configuration inputs and its bit definition complies with the IEEE 802.3 specifications.

The structure and bit definition of the Status register is shown in Table 11. This register contains device capabilities and status output information. and its bit definition complies with the IEEE 802.3 specifications.

The structure and bit definition of the PHY ID #1 and #2 registers is shown in Tables 12 and 13, respectively. These registers contain an identification code unique to the 80220/80221 and their bit definition complies with the IEEE 802.3 specifications.

The structure and bit definition of the AutoNegotiation Advertisement and AutoNegotiation Remote End Capability registers is shown in Tables 14 and 15, respectively. These registers are used by the AutoNegotiation algorithm and their bit definition complies with the IEEE 802.3 specifications.

The structure and bit definition of the Configuration 1 and Configuration 2 registers is shown in Table 16 and 17, respectively. These registers store various configuration inputs.

The structure and bit definition of the Status Output register is shown in Table 18. This register contains output status information.

The structure and bit definition of the Mask register is shown in Table 19. This register allows each R/LT bit in the Status Output register to be masked out or removed as a bit that will set interrupt.

Register 20 is reserved for factory use. All bit values must be set to the defaults for normal operation.

3.26.7 Interrupt

The 80220/80221 has hardware and software interrupt capability. The interrupt is triggered by certain output status bits (also referred to as interrupt bits) in the serial port. As indicated previously, R/LT bits are read bits that latch on transition. R/LT bits are also interrupt bits if they are not masked out with the Mask register bits. Interrupt bits automatically latch themselves into their register locations and assert the interrupt indication when they change state. Interrupt bits stay latched until they are read. When interrupt bits are read, the interrupt indication is deasserted and the interrupt bits that caused the interrupt to happen are updated to their current value. Each interrupt bit can be individually masked and subsequently be removed as an interrupt bit by setting the appropriate mask register bits in the Mask register.

Interrupt indication is done in three ways: (1) $\overline{MDINT}$ pin, (2) INT bit in the MI serial port Status Output register, and (3) interrupt pulse on MDIO. The $\overline{MDINT}$ pin is an active low interrupt output indication. The INT bit is an active high interrupt register bit that resides in the Status Output register. The interrupt pulse on MDIO also indicates interrupt and is available when the interrupt pulse select bit is set in the MI serial port Configuration 2 register. When

this bit is set, an interrupt is signalled by an low going pulse on MDIO when MDC is high and the serial port is in the idle state, as shown in the timing diagram in Figure 10. Once MDIO is forced low to indicate the interrupt condition, MDIO stays low until MDC returns low. Once MDC returns low, then MDIO goes back to high impedance state. If the interrupt occurs while the serial port is being accessed, then the MDIO interrupt pulse is delayed until one clock bit after the serial port access cycle is ended as shown in Figure 10.

a.) Interrupt Happens During Idle.

INTERNAL
INTERRUPT

MDC

MDIO

MDIO HI-Z
PULLED HIGH EXTERNALLY

INTERRUPT
PULSE

MDIO HI-Z
PULLED HIGH EXTERNALLY
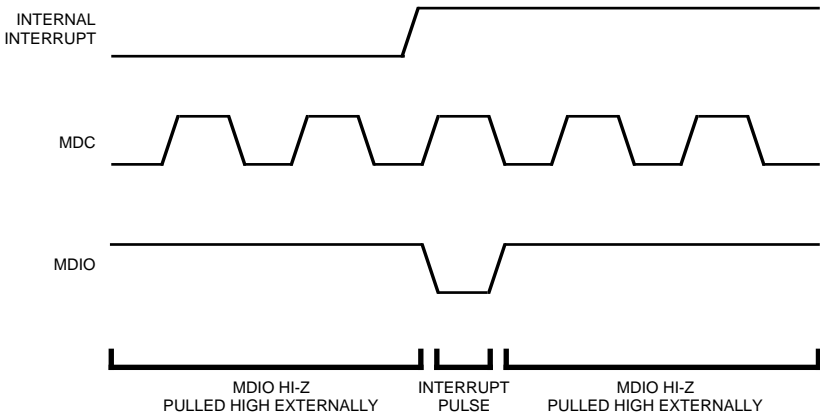
b.) Interrupt Happens During Read Cycle.

INTERNAL
INTERRUPT

MDC

MDIO

B1   B0

LAST TWO BITS
OF READ CYCLE

MDIO HI-Z
PULLED HIGH EXTERNALLY

INTERRUPT
PULSE

MDIO HI-Z
PULLED HIGH EXTERNALLY
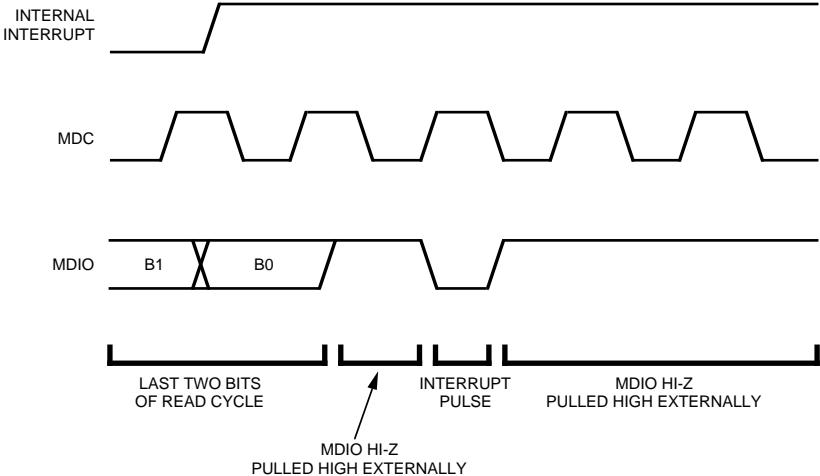
Figure 10. MDIO Interrupt Pulse

4.0 Register Description

Table 8. MI Serial Port Frame Structure

\<Idle\>	\<Start\>	\<Read\>	\<Write\>	\<PHY Addr.\>	\<Reg. Addr.\>	\<Turnaround\>	\<Data\>
IDLE	ST[1:0]	READ	WRITE	PHYAD[4:0]	REGAD[4:0]	TA[1:0]	D[15:0]....

Register 0   Control
Register 1   Status
Register 2   PHY ID #1
Register 3   PHY ID #2
Register 4   AutoNegotiation Advertisement
Register 5   AutoNegotiation Remote End Capability
Register 16   Configuration 1
Register 17   Configuration 2
Register 18   Status Output
Register 19   Mask
Register 20   Reserved
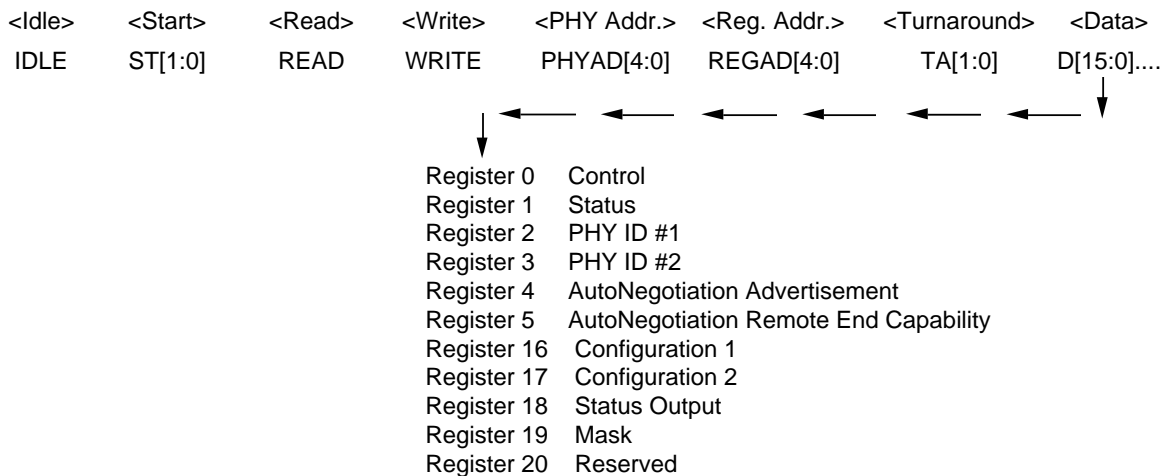
Symbol	Name	Definition	R/W
IDLE	Idle Pattern	These bits are an idle pattern. Device will not initiate an MI cycle until it detects at least 32 1's.	W
ST1 ST0	Start Bits	When ST[1:0]=01, a MI Serial Port access cycle starts.	W
READ	Read Select	1 = Read Cycle	W
WRITE	Write Select	1 = Write Cycle	W
PHYAD[4:0]	Physical Device Address	When PHYAD[4:0]=$\overline{\text{MDA[4:0]}}$ pins inverted, the MI Serial Port is selected for operation.	W
REGAD4[4:0]	Register Address	If REGAD[4:0]=00000-11110, these bits determine the specific register from which D[15:0] is read/written. If multiple register access is enabled and REGAD[4:0]=11111, all registers are read/written in a single cycle.	W
TA1 TA0	Turnaround Time	These bits provide some turnaround time for MDIO When READ=1, TA[1:0]=Z0 When WRITE=1, TA[1:0]=ZZ	R/W
D[15:0]....	Data	These 16 bits contain data to/from one of the eleven registers selected by register address bits REGAD[4:0].	Any

IDLE is shifted in first

Table 9. MI Serial Port Register Map

Register		x.15	x.14	x.13	x.12	x.11	x.10	x.9	x.8	x.7	x.6	x.5	x.4	x.3	x.2	x.1	x.0
0	Control	RST	LPBK	SPEED	ANEG_EN	PDN	MII_DIS	ANEG_RST	DPLX	COLTST							
		R/WSC	R/W	R/W	R/W	R/W	R/W	R/WSC	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		0	0	1	1	0	1 or 0	0	0	0	0	0	0	0	0	0	0
1	Status	CAP_T4	CAP_TXF	CAP_TXH	CAP_TF	CAP_TH					CAP_SUPR	ANEG_ACK	REM_FLT	CAP_ANEG	LINK	JAB	EXREG
		R	R	R	R	R	R	R	R	R	R	R	R/LH	R	R/LL	R/LH	R
		0	1	1	1	1	0	0	0	0	0	0	0	1	0	0	1
2	PHY ID #1	OUI3	OUI4	OUI5	OUI6	OUI7	OUI8	OUI9	OUI10	OUI11	OUI12	OUI13	OUI14	OUI15	OUI16	OUI17	OUI18
		R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
3	PHY ID #2	OUI19	OUI20	OUI21	OUI22	OUI23	OUI24	PART5	PART4	PART3	PART2	PART1	PART0	REV3	REV2	REV1	REV0
		R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
		1	0	1	1	1	0	0	0	0	0	0	1	0	0	1	0
4	AutoNegot. Advertisement	NP	ACK	RF				T4	TX_FDX	TX_HDX	10_FDX	10_HDX					CSMA
		R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	1
5	AutoNegot. Remote Capability	NP	ACK	RF				T4	TX_FDX	TX_HDX	10_FDX	10_HDX					CSMA
		R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16	Configuration 1	LNK_DIS	XMT_DIS	XMT_PDN	TXEN_CRS	BYP_ENC	BYP_SCR	UNSCR_DIS	EQLZR	CABLE	RLVL0	TLVL3	TLVL2	TLVL1	TLVL0	TRF1	TRF0
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17	Configuration 2	PLED3_1	PLED3_0	PLED2_1	PLED2_0	PLED1_1	PLED1_0	PLED0_1	PLED0_0	LED_DEF1	LED_DEF0	APOL_DIS	JAB_DIS	MREG	INT_MDIO	R/J_CFG	
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
18	Status Output	INT	LNK_FAIL	LOSS_SYNC	CWRD	SSD	ESD	RPOL	JAB	SPD_DET	DPLX_DET						
		R	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R	R	R	R	R	R
		0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
19	Mask	MASK_INT	MASK_LNK_FAIL	MASK_LOSS_SYNC	MASK_CWRD	MASK_SSD	MASK_ESD	MASK_RPOL	MASK_JAB	MASK_SPD_DET	MASK_DPLX_DET						
		R	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT						
		0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
20	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 10. MI Register 0 (Control) Structure And Bit Definition

0.15	0.14	0.13	0.12	0.11	0.10	0.9	0.8
RST	LPBK	SPEED	ANEG_EN	PDN	MII_DIS	ANEG_RST	DPLX
R/WSC	R/W	R/W	R/W	R/W	R/W	R/WSC	R/W

0.7	0.6	0.5	0.4	0.3	0.2	0.1	0.0
COLTST	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
0.15	RST	Reset	1 = Reset, Bit Self Clearing After Reset Completed 0 = Normal	R/W SC	0
0.14	LPBK	Loopback Enable	1 = Loopback Mode Enabled 0 = Normal	R/W	0
0.13	SPEED	Speed Select	1 = 100 Mbps Selected (100BaseTX) 0 = 10 Mbps Selected (10BaseT)	R/W	1
0.12	ANEG_EN	AutoNegotiation Enable	1 = AutoNegotiation Enabled 0 = Normal	R/W	1
0.11	PDN	Powerdown Enable	1 = Powerdown 0 = Normal	R/W	0
0.10	MII_DIS	MII Interface Disable	1 = MII Interface Disabled 0 = Normal	R/W	1[1]
0.9	ANEG_RST	AutoNegotiation Reset	1 = Restart AutoNegotiation Process, Bit Self Clearing After Reset Completed 0 = Normal	R/W SC	0
0.8	DPLX	Duplex Mode Select	1 = Full Duplex 0 = Half Duplex	R/W	0
0.7	COLTST	Collision Test Enable	1 = Collision Test Enabled 0 = Normal	R/W	0
0.6 thru 0.0			Reserved	R/W	0

x.15 Bit Is Shifted First

Note 1: if $\overline{MDA[4:0]}$ not = 11111, then the MII_DIS default value is changed to 0

Table 11. MI Register 1 (Status) Structure And Bit Definition

1.15	1.14	1.13	1.12	1.11	1.10	1.9	1.8
CAP_T4	CAP_TXF	CAP_TXH	CAP_TF	CAP_TH	0	0	0
R	R	R	R	R	R	R	R

1.7	1.6	1.5	1.4	1.3	1.2	1.1	1.0
0	CAP_SUPR	ANEG_ACK	REM_FLT	CAP_ANEG	LINK	JAB	EXREG
R	R	R	R/LH	R	R/LL	R/LH	R

Bit	Symbol	Name	Definition	R/W	Def.
1.15	CAP_T4	100Base-T4 Capable	0 = Not Capable of 100Base-T4 Operation	R	0
1.14	CAP_TXF	100Base-TX Full Duplex Capable	1 = Capable Of 100Base-TX Full Duplex	R	1
1.13	CAP_TXH	100Base-TX Half Duplex Capable	1 = Capable Of 100Base-TX Half Duplex	R	1
1.12	CAP_TF	10Base-T Full Duplex Capable	1 = Capable Of 10Base-T Full Duplex	R	1
1.11	CAP_TH	10Base-T Half Duplex Capable	1 = Capable Of 10Base-T Half Duplex	R	1
1.10 thru 1.7			Reserved	R	0
1.6	CAP_SUPR	MI Preamble Suppression Capable	0 = Not Capable of Accepting MI Frames with MI Preamble Suppressed	R	0
1.5	ANEG_ACK	AutoNegotiation Acknowledgment	1 = AutoNegotiation Acknowledgement Process Complete 0 = Normal	R	0
1.4	REM_FLT	Remote Fault Detect	1 = Remote Fault Detected. This bit is set when Either Interrupt Detect Bit 18.15 or AutoNegotiation Remote Fault Bit 5.13 is set. 0 = No Remote Fault	R/LH	0
1.3	CAP_ANEG	AutoNegotiation Capable	1 = Capable of AutoNegotiation Operation	R	1
1.2	LINK	Link Status	1 = Link Detected (Same As Bit 18.14 Inverted) 0 = Link Not Detected	R/LL	0
1.1	JAB	Jabber Detect	1 = Jabber Detected (Same As Bit 18.8) 0 = Normal	R/LH	0
1.0	EXREG	Extended Register Capable	1 = Extended Registers Exist	R	1

x.15 Bit Is Shifted First

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Table 12. MI Register 2 (PHY ID #1) Structure And Bit Definition

2.15	2.14	2.13	2.12	2.11	2.10	2.9	2.8
OUI3	OUI4	OUI5	OUI6	OUI7	OUI8	OUI9	OUI10
R	R	R	R	R	R	R	R

2.7	2.6	2.5	2.4	2.3	2.2	2.1	2.0
OUI11	OUI12	OUI13	OUI14	OUI15	OUI16	OUI17	OUI18
R	R	R	R	R	R	R	R

Bit	Symbol	Name	Definition	R/W	Def.
2.15	OUI3	Company ID,	SEEQ OUI = 00-A0-7D	R	0
2.14	OUI4	Bits 3-18			0
2.13	OUI5				0
2.12	OUI6				0
2.11	OUI7				0
2.10	OUI8				0
2.9	OUI9				0
2.8	OUI10				0
2.7	OUI11				0
2.6	OUI12				0
2.5	OUI13				0
2.4	OUI14				1
2.3	OUI15				0
2.2	OUI16				1
2.1	OUI17				1
2.0	OUI18				0

x.15 Bit Is Shifted First

Table 13. MI Register 3 (PHY ID #2) Structure And Bit Definition

3.15	3.14	3.13	3.12	3.11	3.10	3.9	3.8
OUI19	OUI20	OUI21	OUI22	OUI23	OUI24	PART5	PART4
R	R	R	R	R	R	R	R

3.7	3.6	3.5	3.4	3.3	3.2	3.1	3.0
PART3	PART2	PART1	PART0	REV3	REV2	REV1	REV0
R	R	R	R	R	R	R	R

Bit	Symbol	Name	Definition	R/W	Def.
3.15	OUI19	Company ID,	SEEQ OUI = 00-A0-7D	R	1
3.14	OUI20	Bits 19-24			1
3.13	OUI21				1
3.12	OUI22				1
3.11	OUI23				1
3.10	OUI24				0
3.9	PART5	Manufacturer's	03_H	R	0
3.8	PART4	Part Number			0
3.7	PART3				0
3.6	PART2				0
3.5	PART1				1
3.4	PART0				1
3.3	REV3	Manufacturer's		R	–
3.2	REV2	Revision Number			–
3.1	REV1				–
3.0	REV0				–

x.15 Bit Is Shifted First Table

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Table 14. MI Register 4 (AutoNegotiation Advertisement) Structure

4.15	4.14	4.13	4.12	4.11	4.10	4.9	4.8
NP	ACK	RF	0	0	0	T4	TX_FDX
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

4.7	4.6	4.5	4.4	4.3	4.2	4.1	4.0
TX_HDX	10_FDX	10_HDX	0	0	0	0	CSMA
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
4.15	NP	Next Page Enable	1 = Next Page Exists [1] 0 = No Next Page	R/W	0
4.14	ACK	Acknowledge	1 = Received AutoNegotiation Word Recognized 0 = Not Recognized	R	0
4.13	RF	Remote Fault Enable	1 = AutoNegotiation Remote Fault Detected 0 = No Remote Fault	R/W	0
4.12 4.11 4.10			Reserved	R/W	0 0 0
4.9	T4	100Base-T4 Capable	1 = Capable Of 100Base-T4 0 = Not Capable	R/W	0
4.8	TX_FDX	100Base-TX Full Duplex Capable	1 = Capable of 100Base-TX Full Duplex 0 = Not Capable	R/W	1
4.7	TX_HDX	100Base-TX Half Duplex Capable	1 = Capable Of 100Base-TX Half Duplex 0 = Not Capable	R/W	1
4.6	10_FDX	10Base-T Full Duplex Capable	1 = Capable Of 10Base-T Full Duplex 0 = Not Capable	R/W	1
4.5	10_HDX	10Base-T Half Duplex Capable	1 = Capable Of 10Base-T Half Duplex 0 = Not Capable	R/W	1
4.4 thru 4.1			Reserved	R/W	0 0 0 0
4.0	CSMA	CSMA 802.3 Capable	1 = Capable of 802.3 CSMA Operation 0 = Not Capable	R/W	1

x.15 Bit Is Shifted First

Note 1. Next Page currently not supported.

Table 15. MI Register 5 (AutoNegotiation Remote End Capability) Structure

5.15	5.14	5.13	5.12	5.11	5.10	5.9	5.8
NP	ACK	RF	0	0	0	T4	TX_FDX
R	R	R	R	R	R	R	R

5.7	5.6	5.5	5.4	5.3	5.2	5.1	5.0
TX_HDX	10_FDX	10_HDX	0	0	0	0	CSMA
R	R	R	R	R	R	R	R

Bit	Symbol	Name	Definition	R/W	Def.
5.15	NP	Next Page Enable	1 = Next Page Exists 0 = No Next Page	R	0
5.14	ACK	Acknowledge	1 = Received AutoNegotiation Word Recognized 0 = Not Recognized	R	0
5.13	RF	Remote Fault Enable	1 = AutoNegotiation Remote Fault Detected 0 = No Remote Fault	R	0
5.12 5.11 5.10			Reserved	R	0 0 0
5.9	T4	100Base-T4 Capable	1 = Capable Of 100Base-T4 0 = Not Capable	R	0
5.8	TX_FDX	100Base-TX Full Duplex Capable	1 = Capable of 100Base-TX Full Duplex 0 = Not Capable	R	0
5.7	TX_HDX	100Base-TX Half Duplex Capable	1 = Capable Of 100Base-TX Half Duplex 0 = Not Capable	R	0
5.6	10_FDX	10Base-T Full Duplex Capable	1 = Capable Of 10Base-T Full Duplex 0 = Not Capable	R	0
5.5	10_HDX	10Base-T Half Duplex Capable	1 = Capable Of 10Base-T Half Duplex 0 = Not Capable	R	0
5.4 thru 5.1			Reserved	R	0 0 0 0
5.0	CSMA	CSMA 802.3 Capable	1 = Capable of 802.3 CSMA Operation 0 = Not Capable	R	0

x.15 Bit Is Shifted First

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Table 16. MI Register 16 (Configuration 1) Structure And Bit Definition

16.15	16.14	16.13	16.12	16.11	16.10	16.9	16.8
LNK_DIS	XMT_DIS	XMT_PDN	TXEN_CRS	BYP_ENC	BYP_SCR	0	EQLZR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

16.7	16.6	16.5	16.4	16.3	16.2	16.1	16.0
CABLE	RLVL0	TLVL3	TLVL2	TLVL1	TLVL0	TRF1	TRF0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
16.15	LNK_DIS	Link Disable	1 = Receive Link Detect Function Disabled (Force Link Pass) 0 = Normal	R/W	0
16.14	XMT_DIS	TP Transmit Disable	1 = TP Transmitter Disabled 0 = Normal	R/W	0
16.13	XMT_PDN	TP Transmit Powerdown	1 = TP Transmitter Powered Down 0 = Normal	R/W	0
16.12	TXEN_CRS	TXEN to CRS Loopback Disable	1 = TX_EN to CRS Loopback Disabled 0 = Enabled	R/W	0
16.11	BYP_ENC	Bypass Encoder/Decoder Select	1 = Bypass 4B5B Encoder/Decoder 0 = No Bypass	R/W	0
16.10	BYP_SCR	Bypass Scrambler/Descr-ambler Select	1 = Bypass Scrambler/Descrambler 0 = No Bypass	R/W	0
16.9	UNSCR_DIS	Unscrambled Idle Reception Disable	1 = Disable AutoNegotiation with devices that transmit unscrambled idle on powerup and various instances 0 = Enables AutoNegotiation with devices that transmit unscramblled idle on powerup and various instances	R/W	0
16.8	EQLZR	Receive Equalizer Select	1 = Receive Equalizer Disabled, Set To 0 Length 0 = Receive Equalizer On (For 100Mb Mode Only)	R/W	0
16.7	CABLE	Cable Type Select	1 = STP (150 Ohm) 0 = UTP (100 Ohm)	R/W	0
16.6	RLVL0	Receive Input Level Adjust	1 = Receive Squelch Levels Reduced By 4.5 dB 0 = Normal	R/W	0
16.5 16.4 16.3 16.2	TLVL3 TLVL2 TLVL1 TLVL0	Transmit Output Level Adjust	See Table 3	R/W	1 0 0 0
16.1 16.0	TRF1 TRF0	Transmitter Rise/Fall Time Adjust	11 = -0.25 nS 10 = +0.0 nS 01 = +0.25 nS 00 = +0.50 nS	R/W	1 0

x.15 Bit Is Shifted First

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Table 17. MI Register 17 (Configuration 2) Structure And Bit Definition

17.15	17.14	17.13	17.12	17.11	17.10	17.9	17.8
PLED3_1	PLED3_0	PLED2_1	PLED2_0	PLED1_1	PLED1_0	PLED0_1	PLED0_0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

17.7	17.6	17.5	17.4	17.3	17.2	17.1	17.0
LED_DEF1	LED_DEF0	APOL_DIS	JAB_DIS	MREG	INT_MDIO	P26_CFG	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition		R/W	Def.
17.15 17.14	PLED3_1 PLED3_0	Programmable LED Output Select, Pin PLED3	11 = Normal 10 = LED Blink 01 = LED On 00 = LED Off	(PLED3 Is Determined By Bits 17.7-17.6 And Table 5. Default is LINK100) (PLED3 Is Toggling 100 mS Low, 100 mS High) (PLED3 Is Low) (PLED3 Is High)	R/W	11
17.13 17.12	PLED2_1 PLED2_0	Programmable LED Output Select, Pin PLED2	11 = Normal 10 = LED Blink 01 = LED On 00 = LED Off	(PLED2 Is Determined By Bits 17.7-17.6 And Table 5. Default is Activity) (PLED2 Is Toggling 100 mS Low, 100 mS High) (PLED2 Is Low) (PLED2 Is High)	R/W	11
17.11 17.10	PLED1_1 PLED1_0	Programmable LED Output Select, Pin PLED1	11 = Normal 10 = LED Blink 01 = LED On 00 = LED Off	(PLED1 Is Determined By Bits 17.7-17.6 And Table 5. Default is Full Duplex) (PLED1 Is Toggling 100 mS Low, 100 mS High) (PLED1 Is Low) (PLED1 Is High)	R/W	11
17.9 17.8	PLED0_1 PLED0_0	Programmable LED Output Select, Pin PLED0	11 = Normal 10 = LED Blink 01 = LED On 00 = LED Off	(PLED0 Is Determined By Bits 17.7-17.6 And Table 5. Default is LINK10) (PLED0 Is Toggling 100 mS Low, 100 mS High) (PLED0 Is Low) (PLED0 Is High)	R/W	11
17.7 17.6	LED_DEF1 LED_DEF0	LED Normal Function Select	See Table 5		R/W	0
17.5	APOL_DIS	Auto Polarity Disable	1 = Auto Polarity Correction Function Disabled 0 = Normal		R/W	0
17.4	JAB_DIS	Jabber Disable Select	1 = Jabber Disabled 0 = Enabled		R/W	0
17.3	MREG	Multiple Register Access Enable	1 = Multiple Register Access Enabled 0 = No Multiple Register Access		R/W	0
17.2	INT_MDIO	Interrupt Scheme Select	1 = Interrupt Signaled With MDIO Pulse During Idle 0 = Interrupt Not Signalled On MDIO		R/W	0
17.1	R/J_CFG	R/J Configuration Select	1 = RX_EN/JAM Pin Is Configured To Be JAM 0 = RX_EN/JAM Pin Is Configured To Be RX_EN		R/W	0
17.0			Reserved		R/W	0

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Table 18. MI Register 18 (Status Output) Structure And Bit Definition

18.15	18.14	18.13	18.12	18.11	18.10	18.9	18.8
INT	LNK_FAIL	LOSS_SYNC	CWRD	SSD	ESD	RPOL	JAB
R	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT

18.7	18.6	18.5	18.4	18.3	18.2	18.1	18.0
SPD_DET	DPLX_DET	0	0	0	0	0	0
R/LT	R/LT	R	R	R	R	R	R

Bit	Symbol	Name	Definition	R/W	Def.
18.15	INT	Interrupt Detect	1 = Interrupt Bit(s) Have Changed Since Last Read Operation. 0 = No Change	R	0
18.14	LNK_FAIL	Link Fail Detect	1 = Link Not Detected 0 = Normal	R/LT	0
18.13	LOSS_SYNC	Descrambler Loss of Synchronization Detect	1 = Descrambler Has Lost Synchronization 0 = Normal	R/LT	0
18.12	CWRD	Codeword Error	1 = Invalid 4B5B Code Detected On Receive Data 0 = Normal	R/LT	0
18.11	SSD	Start Of Stream Error	1 = No Start Of Stream Delimiter Detected on Receive Data 0 = Normal	R/LT	0
18.10	ESD	End Of Stream Error	1 = No End Of Stream Delimiter Detected on Receive Data 0 = Normal	R/LT	0
18.9	RPOL	Reverse Polarity Detect	1 = Reverse Polarity Detected 0 = Normal	R/LT	0
18.8	JAB	Jabber Detect	1 = Jabber Detected 0 = Normal	R/LT	0
18.7	SPD_DET	100/10 Speed Detect	1 = Device in 100 Mbps Mode (100Base-TX) 0 = Device in 10 Mbps Mode (10Base-T)	R/LT	1
18.6	DPLX_DET	Duplex Detect	1 = Device In Full Duplex 0 = Device In Half Duplex	R/LT	0
18.5 18.4 18.3 18.2 18.1 18.0			Reserved for Factory Use	R	0 0 0 0 0 0

x.15 Bit Is Shifted First

Table 19. MI Register 19 (Mask) Structure And Bit Definition

19.15	19.14	19.13	19.12	19.11	19.10	19.9	19.8
MASK_ INT	MASK_ LNK_FAIL	MASK_ LOSS_SYNC	MASK_ CWRD	MASK_ SSD	MASK_ ESD	MASK_ RPOL	MASK_ JAB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

19.7	19.6	19.5	19.4	19.3	19.2	19.1	19.0
MASK_ SPD_DET	MASK_ DPLX_DET	1	1	0	0	0	0
R/W	R/W	R/W	R/W	R	R	R	R

Bit	Symbol	Name	Definition	R/W	Def.
19.15	MASK_ INT	Interrupt Mask - Interrupt Detect	1 = Mask Interrupt For INT In Register 18 0 = No Mask	R/W	1
19.14	MASK_ LNK_FAIL	Interrupt Mask - Link Fail Detect	1 = Mask Interrupt For LNK_FAIL In Register 18 0 = No Mask	R/W	1
19.13	MASK_ LOSS_SYNC	Interrupt Mask - Descrambler Loss of Synchronization Detect	1 = Mask Interrupt For LOSS_SYNC In Register 18 0 = No Mask	R/W	1
19.12	MASK_ CWRD	Interrupt Mask - Codeword Error	1 = Mask Interrupt For CWRD In Register 18 0 = No Mask	R/W	1
19.11	MASK_ SSD	Interrupt Mask - Start Of Stream Error	1 = Mask Interrupt For SSD In Register 18 0 = No Mask	R/W	1
19.10	MASK_ ESD	Interrupt Mask -End Of Stream Error	1 = Mask Interrupt For ESD In Register 18 0 = No Mask	R/W	1
19.9	MASK_ RPOL	Interrupt Mask - Reverse Polarity Detect	1 = Mask Interrupt For RPOL In Register 18 0 = No Mask	R/W	1
19.8	MASK_ JAB	Interrupt Mask - Jabber Detect	1 = Mask Interrupt For JAB In Register 18 0 = No Mask	R/W	1
19.7	MASK_ SPD_DET	Interrupt Mask - 100/10 Speed Detect	1 = Mask Interrupt For SPD_DET In Register 18 0 = No Mask	R/W	1
19.6	MASK_ DPLX_DET	Interrupt Mask - Duplex Detect	1 = Mask Interrupt For DPLX_DET In Register 18 0 = No Mask	R/W	1
19.5 19.4			Reserved. Must be Written to 1 or Left at Default for Normal Operation	R/W	1
19.3 19.2 19.1 19.0			Reserved	R	0 0 0 0

x.15 Bit Is Shifted First

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Table 20. MI Register 20 (Reserved) Structure And Bit Definition

20.15	20.14	20.13	20.12	20.11	20.10	20.9	20.8
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

20.7	20.6	20.5	20.4	20.3	20.2	20.1	20.0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
20.15			Reserved for Factory Use. Must Be Written to 0 for Normal Operation	R/W	0
20.14					0
20.13					0
20.12					0
20.11					0
20.10					0
20.9					0
20.8					0
20.7					0
20.6					0
20.5					0
20.4					0
20.3					0
20.2					0
20.1					0
20.0					0

x.15 Bit Is Shifted First

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5.0 APPLICATION INFORMATION

5.1 EXAMPLE SCHEMATICS

A typical example schematic of the 80220/80221 used in an adapter card application is shown in Figure 11, a hub application is shown in Figure 12, and an external PHY application is shown in Figure 13.

5.2 TP TRANSMIT INTERFACE

The interface between the TP outputs on TPO± and the twisted pair cable is typically transformer coupled and terminated with the two resistors as shown in Figures 11-13.

The transformer for the transmitter is recommended to have a winding ration of 2:1 with a center tap on the 2x winding tied to VCC, as shown in Figures 11-13. The specifications for such a transformer are shown in Table 21. Sources for the transformer are listed in Table 22.

The transmit output needs to be terminated with two external termination resistors in order to meet the output impedance and return loss requirements of IEEE 802.3. It is recommended that these two external resistors be connected from VCC to each of the TPO± outputs, and their value should be chosen to provide the correct termination impedance when looking back through the transformer from the twisted pair cable, as shown in Figures 11-13. The value of these two external termination resistors depends on the type of cable driven by the device. Refer to the Cable Selection section for more details on choosing the value of these resistors.

To minimize common mode output noise and to aid in meeting radiated emissions requirements, it may be necessary to add a common mode choke on the transmit outputs as well as add common mode bundle termination. The qualified transformers mentioned in Table 22 all contain common mode chokes along with the transformers on both the transmit and receive sides, as shown in Figures 11-13. Common mode bundle termination may be needed and can be achieved by tying the unused pairs in the RJ45 to chassis ground through 75 Ohm resistors and a 0.01 uF capacitor, as shown in Figures 11-13.

To minimize noise pickup into the transmit path in a system or on a PCB, the loading on TPO± should be minimized and both outputs should always be loaded equally.

5.3 TP RECEIVE INTERFACE

Receive data is typically transformer coupled into the receive inputs on TPI± and terminated with external resistors as shown in Figures 11-13.

The transformer for the receiver is recommended to have a winding ration of 1:1, as shown in Figures 11-13. The specifications for such a transformer are shown in Table 21. Sources for the transformer are listed in Table 22.

The receive input needs to be terminated with the correct termination impedance meet the input impedance and return loss requirements of IEEE 802.3. In addition, the receive TP inputs need to be attenuated. It is recommended that both the termination and attenuation be accomplished by placing four external resistors in series across the TPI± inputs as shown in Figures 11-13. The resistors should be 15%/35%/35%/15% of the total series resistance, and the total series resistance should be equal to the characteristic impedance of the cable (100 Ohms for UTP, 150 Ohms for STP). It is also recommended that a 0.01µF capacitor be placed between the center of the series resistor string and VCC in order to provide an AC ground for attenuating common mode signal at the input. This capacitor is also shown in Figures 11-13.

To minimize common mode input noise and to aid in meeting susceptibility requirements, it may be necessary to add a common mode choke on the receive input as well as add common mode bundle termination. The qualified transformers mentioned in Table 22 all contain common mode chokes along with the transformers on both the transmit and receive sides, as shown in Figures 11-13. Common mode bundle termination may be needed and can be achieved by tying the receive secondary center tap and the unused pairs in the RJ45 to chassis ground through 75 Ohm resistors and a 0.01 µF capacitor, as shown in Figures 11-13.

In order to minimize noise pickup into the receive path in a system or on a PCB, loading on TPI± should be minimized and both inputs should be loaded equally.

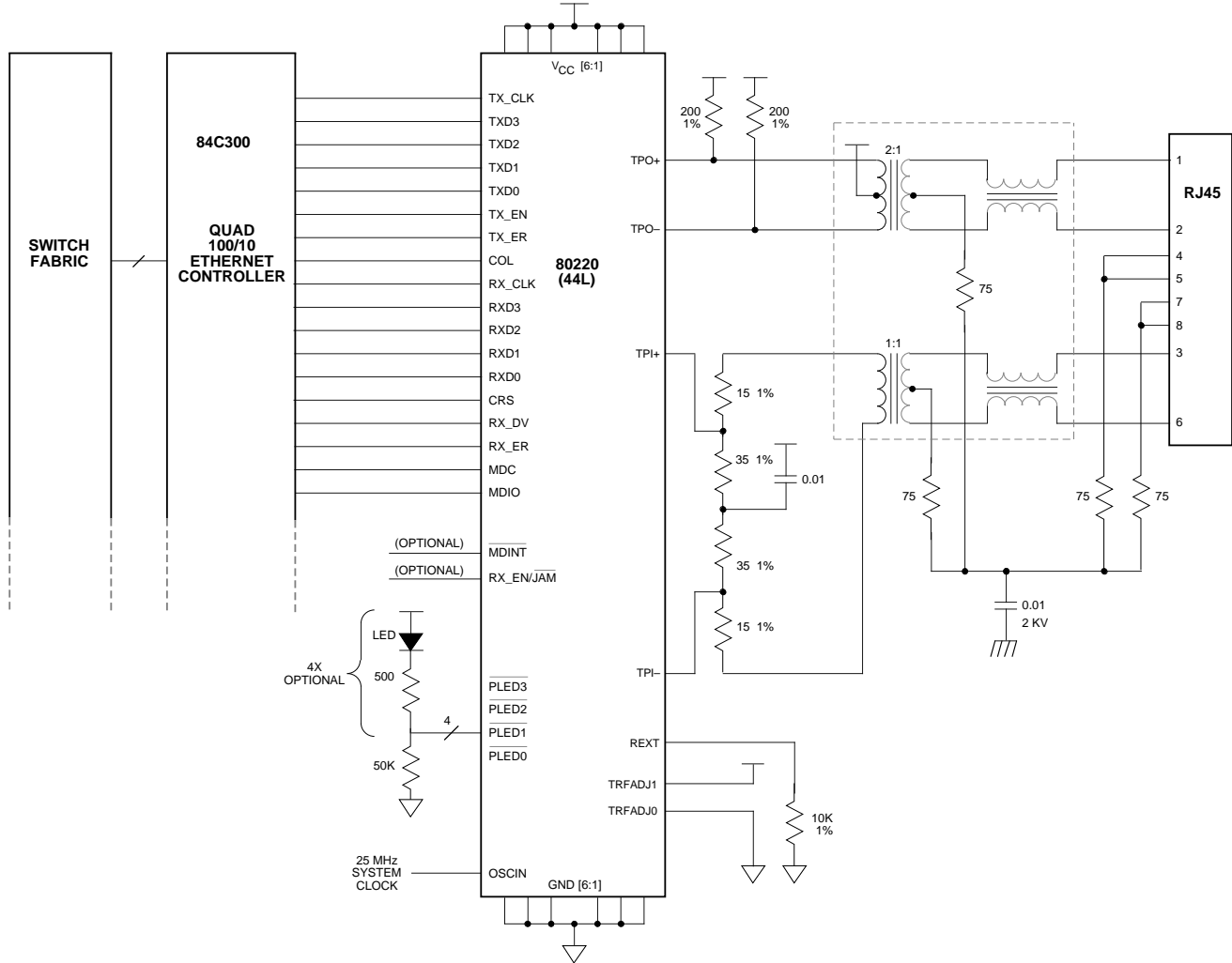**LSI LOGIC**®

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Figure 11. Typical Network Interface Card Schematic Using 80220

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Figure 12. Typical Switching Port Schematic Using 80220

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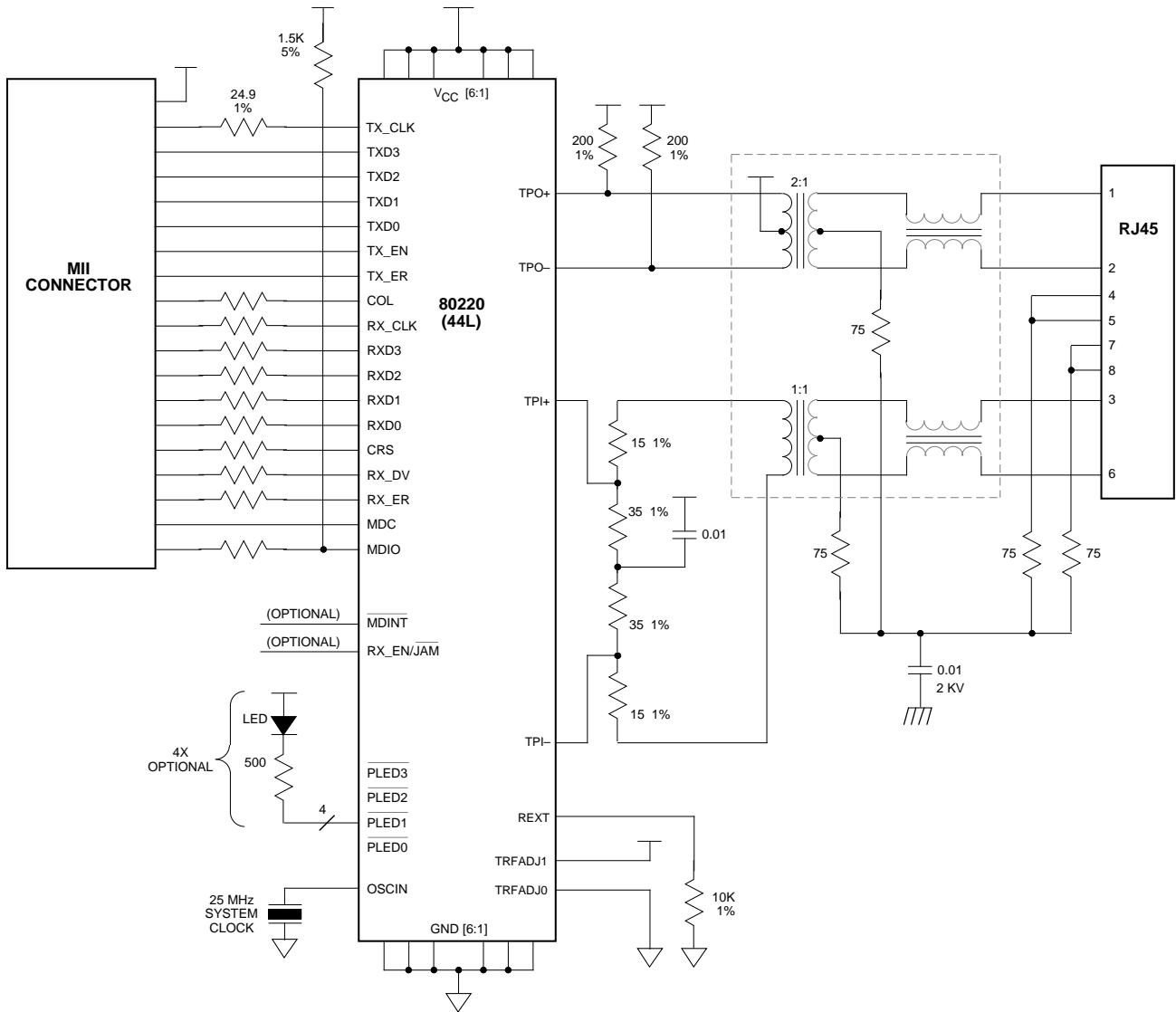
Figure 13. Typical External PHY Schematic Using 80220

Table 21. TP Transformer Specification

Parameter	Specification	
	Transmit	**Receive**
Turns Ratio	2:1 CT	1:1
Inductance, (µH Min)	350	350
Leakage Inductance, (µH)	0.05-0.15	0.0-0.2
Capacitance (pF Max)	15	15
DC Resistance (Ohms Max)	0.4	0.4

Table 22. TP Transformer Sources

Vendor	Part Number
Valor	ST6129
NanoPulse	NPI 6254-30
PCA	EPF 8025G
Belfuse	S558-5999-96 or S558-5999-98
Pulse Engineering	H1038/H1039
YCL	PT 163042

5.4 TP TRANSMIT OUTPUT CURRENT SET

The TPO± output current level is set by an external resistor tied between REXT and GND. This output current is determined by the following equation where R is the value of REXT:

$$I_{out} = (10K/R) * I_{ref}$$

Where I_{ref} *= 20   mA (100 Mbps, UTP)*
= 16.3 mA (100 Mbps, STP)
= 50   mA (10 Mbps, UTP)
= 40.8 mA (10 Mbps, STP)

For 100 Ohm UTP (unshielded twisted pair cable), REXT should be typically set to 10K Ohms and REXT should be a 1% resistor in order to meet IEEE 802.3 specified levels. Once REXT is set for the 100 Mbps and UTP modes as shown by the equation above, I_{ref} *is then automatically changed inside the device when the 10 Mbps mode or UTP120/STP150 modes are selected.*

Keep REXT close to the REXT and GND pins as possible in order to reduce noise pickup into the transmitter.

Since the TP output is a current source, capacitive and inductive loading can reduce the output voltage level from the ideal.   Thus, in actual application, it might be neces-sary to adjust the value of the output current to compen-sate for external loading. One way to adjust the TP output level is to change the value of the external resistor tied to REXT. A better way to adjust the TP output level is to use the transmit level adjust register bits accessed through the MI serial port. These four bits can adjust the output level by -14% to +16% in 2% steps as described in Table 3.

5.5 CABLE SELECTION

The 80220/80221 can drive two different cable types: (1) 100 Ohm unshielded twisted pair, Category 5, or (2) 150 Ohm shielded twisted pair.

The 80220/80221 must be properly configured for the type of cable in order to meet the return loss specifications in IEEE 802.3. This configuration requires setting a bit in the serial port and setting the value of some external resistors, as described in Table 23. The Cable Type Select bit in Table 23 is a bit in the MI serial port Configuration 1 register that sets the output current level for the cable type. R_{TERM} *in Table 23 is the value of the termination resistors needed to meet the level and return loss requirements. The value for* R_{TERM} *on the TPO± outputs is for the two external termination resistors connected between VCC to TPO±; the value for* R_{TERM} *on the TPI± inputs is for the sum of the four series resistors across TPI±, as shown in Figures 11-13. These resistors should be 1% tolerance. Also note that some output level adjustment may be necessary due to parasitics as described in the TP Output Current section.*

Table 23. Cable Configuration

Cable Type	Cable Type Select Bit (16.7)	R_{TERM} (Ohms)	
		TPO±	**TPI±**
100 Ohm UTP, Cat. 5	UTP	200	100
150 Ohm STP	STP	300	150

5.6 TRANSMITTER DROOP

The IEEE 802.3 specification has a transmit output droop requirement for 100BaseTX. Since the 80220/80221 TP output is a current source, it has no perceptible droop by itself. However, the inductance of the transformer added to the device transmitter output as shown in Figures 11-13 will cause droop to appear at the transmit interface to the TP wire. If the transformer connected to the 80220/80221 outputs meets the requirements in Table 21, the transmit interface to the TP cable will meet the IEEE 802.3 droop requirements.

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5.7 MII CONTROLLER INTERFACE

5.7.1 General

The MII controller interface allows the 80220/80221 to connect to any external Ethernet controller without any glue logic provided that the external Ethernet controller has a MII interface that complies with IEEE 802.3, as shown in Figures 11-12.

5.7.2 Clocks

Standard Ethernet controllers with a MII use TX_CLK to clock data in on TXD[3:0]. TX_CLK is specified in IEEE 802.3 and on the 80220/80221 to be an output. If a nonstandard controller or other digital device is used to interface to the 80220/80221, there might be a need to clock TXD[3:0] into the 80220/80221 on the edges of an external master clock. The master clock, in this case, would be an input to the 80220/80221. This can be done by using OSCIN as the master clock input; since OSCIN generates TX_CLK inside the 80220/80221, data on TXD[3:0] can be clocked into the 80220/80221 on edges of output clock TX_CLK or input clock OSCIN. In the case

where OSCIN is used as the input clock, a crystal is no longer needed on OSCIN, and TX_CLK can be left open or used for some other purpose.

5.7.3 Output Drive

The digital outputs on the 80220/80221 controller signals meet the MII driver characteristics specified in IEEE 802.3 and shown in Figure 14 if external 24.9 ohm 1% termination resistors are added. These termination resistors are only needed if the outputs have to drive a MII cable or other transmission line type load, such as in the external PHY application shown in Figure 13. If the 80220/80221 is used in embedded applications, such as adapter cards and switching hubs shown in Figure 11 and 12, then these terminations resistors are not needed.

5.7.4 MII Disable

The MII outputs can be placed in the high impedance state and inputs disabled by setting the MII disable bit in the MI serial port Control register. When this bit is set to the disable state, the TP outputs are also disabled and trans-
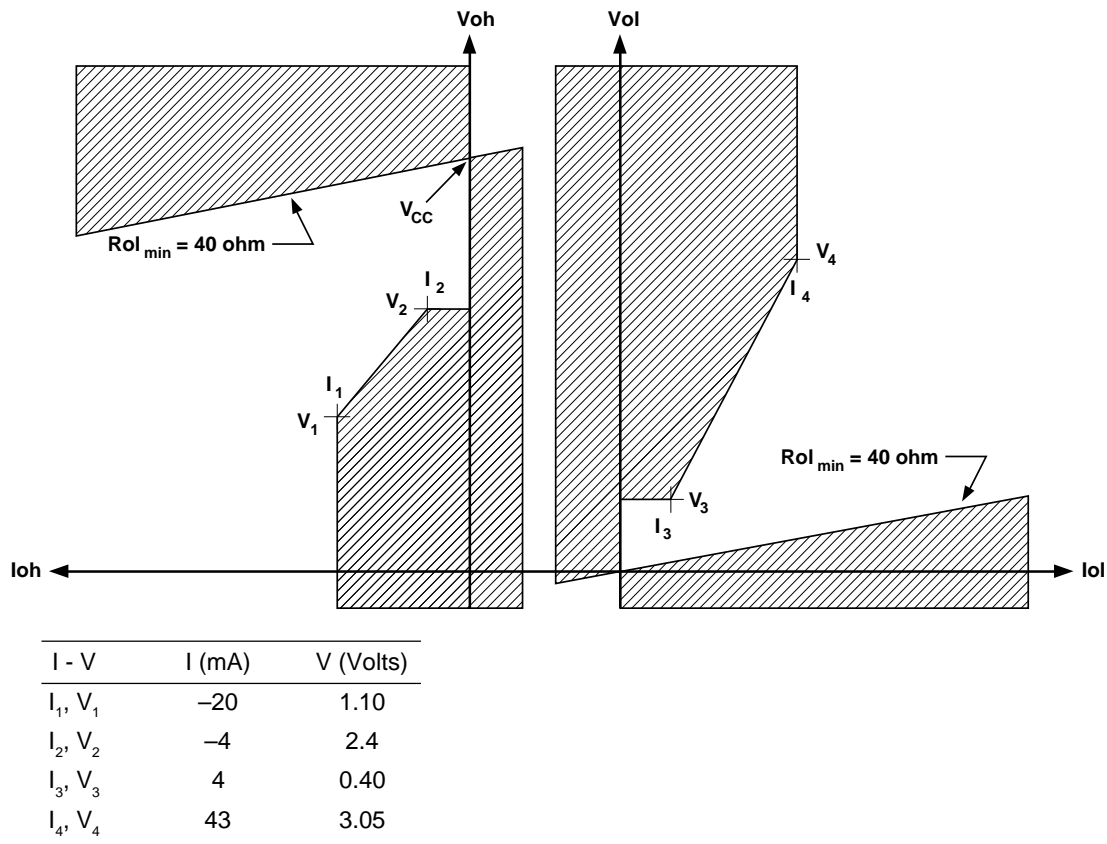

I - V	I (mA)	V (Volts)
I_1, V_1	−20	1.10
I_2, V_2	−4	2.4
I_3, V_3	4	0.40
I_4, V_4	43	3.05

Figure 14. MII Output Driver Characteristics

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mission is inhibited. The default value of this bit when the device powers up or is reset is dependent on the physical device address. If the device address latched into MDA[4:0] at reset is 11111, it is assumed that the device is being used in applications where there maybe more than one device sharing the MII bus, like external PHY's or adapter cards, so the device powers up with the MII interface disabled. If the device address latched into MDA[4:0] at reset is not 11111, it is assumed that the device is being used in application where it is the only device on the MII bus, like hubs, so the device powers up with the MII interface enabled.

5.7.5 Receive Output Enable

The receive output enable pin, RX_EN, forces the receive and collision MII/FBI outputs into the high impedance state. More specifically, when RX_EN is deasserted, RX_CLK, RXD[3:0], RX_DV, RX_ER, and COL are placed in high impedance.

RX_EN can be used to "wire OR" the outputs of many 80220/80221 devices in multiport applications where only one device may be receiving at a time, like a repeater. By monitoring CRS from each individual port, the repeater can assert only the one RX_EN to that 80220/80221 device which is receiving data. The method will reduce, by 8 per device, the number of pins and PCB traces required by a repeater core IC.

The RX_EN function can be enabled by appropriately setting the R/J Configuration select bit in the MI serial port Configuration 2 register. When this bit is set, the RX_EN/JAM pin becomes RX_EN.

5.8 FBI CONTROLLER INTERFACE

The FBI (Five Bit Interface) controller interface has the same characteristics of the MII except that the data path is five bits wide, instead of 4 bits wide per the MII. The five bit wide data path is automatically enabled when the 4B5B encoder is bypassed. Because of this encoder/decoder bypass, the FBI is used primarily for repeaters or other applications where the full PHY is not needed. For more details about the FBI, see the Repeater Applications section.

5.9 REPEATER APPLICATIONS

5.9.1 MII Based Repeaters

The 80220/80221 can be used as the physical interface for MII based repeaters by using the standard MII as the interface to the repeater core.

For most repeaters, it is necessary to disable the internal CRS loopback. This can be done be setting the TX_EN to CRS loopback disable bit in the MI serial port Configuration 1 register.

For some particular types of repeaters, it may be desirable to either enable or disable AutoNegotiation, force Half Duplex operation, and enable either 100 Mbps or 10 Mbps operation. All of these modes can be configured by setting the appropriate bits in the MI serial port Control register.

The 80221 has a RPTR pin which will automatically configure the device for one common type of repeater application. When the RPTR pin is asserted, (1) TX_EN to CRS loopback is disabled, (2) AutoNegotiation is disabled, (3) Half Duplex operation is selected, and (4) 100 Mbps operation is selected.

The MII requires 16 signals between the 80220/80221 and a repeater core. The MII signal count to a repeater core will be 16 multiplied by the number of ports, which can be quite large. The signal count between the 80220/80221 and repeater core can be reduced by 8 per device by sharing the receive output pins and using RX_EN to enable only that port where CRS is asserted. Refer to the Controller Interface section within the Applications section for more details about RX_EN.

5.9.2 Non-MII Based Repeaters

The FBI interface available on the 80220/80221 can be used to connect to non-MII based repeaters that employ the industry popular five bit wide interface.

Since the FBI is a 5 bit wide interface, it requires that the 4B5B encoder/decoder be bypassed. The FBI is automatically selected on the 80220/80221 when the 4B5B encoder/decoder is bypassed. The 4B5B encoder/decoder can be bypassed by setting the bypass encoder/decoder select bit in the MI serial port Configuration 1 register. Some applications may also require the scrambler/descrambler to be bypassed. This can be done by setting the bypass scrambler/descrambler select bit in the MI serial port Configuration 1 register.

For most repeaters, it is necessary to disable the internal CRS loopback. This can be done be setting the TX_EN to CRS loopback disable bit in the MI serial port Configuration 1 register.

For some particular types of repeaters, it may be desirable to either enable or disable AutoNegotiation, force Half Duplex operation, and enable either 100 Mbps or 10 Mbps operation. All of these modes can be configured by setting the appropriate bits in the MI serial port Control register.

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The FBI requires 16 signals between the 80220/80221 and a repeater core. The FBI signal count to a repeater core will be 16 multiplied by the number of ports, which can be quite large. The signal count between the 80220/80221 and repeater core can be reduced by 8 per device by sharing the receive output pins and using RX_EN to enable only that port where CRS is asserted. Refer to the Controller Interface section within the Applications section for more details on RX_EN.

5.9.3 Clocks

Normally, transmit data over the MII/FBI is clocked into the 80220/80221 with edges from the output clock TX_CLK. It may be desireable or necessary in some repeater applications to clock in the transmit data from a master clock from the repeater core. This would require that transmit data be clocked in on edges of an input clock. An input clock is available for clocking in data on TXD with the OSCIN pin. Notice from the timing diagrams that OSCIN generates TX_CLK, and TXD data is clocked in on TX_CLK edges. This means that TXD data is also clocked in on OSCIN edges as well. Thus, an external clock driving the OSCIN input can also be used as the clock for TXD.

5.10 SERIAL PORT

5.10.1 General

The 80220/80221 has a MI serial port to access the devices's configuration inputs and read out the status outputs. Any external device that has a IEEE 802.3 compliant MI interface can connect directly to the 80220/80221 without any glue logic, as shown in Figures 11-13.

As described earlier, the MI serial port consists of 8 lines: MDC, MDIO, $\overline{\text{MDINT}}$, and $\overline{\text{MDA[4:0]}}$. However, only 2 lines, MDC and MDIO, are needed to shift data in and out; $\overline{\text{MDINT}}$ and $\overline{\text{MDA[4:0]}}$ are not needed but are provided for convenience only.

Note that the $\overline{\text{MDA[4:0]}}$ addresses are inverted inside the 80220/80221 before going to the MI serial port block. This means that the $\overline{\text{MDA[4:0]}}$ pins would have to be pin strapped to 11111 externally in order to successfully match the MI physical address of 00000 on the PHYAD[4:0] bits internally.

5.10.2 Polling vs. Interrupt

The status output bits can be monitored by either polling the serial port or with interrupt.

If polling is used, the registers can be read at regular intervals and the status bits can be checked against their previous values to determine any changes. To make polling simpler, all the registers can be accessed in a single read or write cycle by setting the register address bits REGAD[4:0] to 11111 and adding enough clocks to read-out out all the bits, provided the multiple register access feature has been enabled.

The interrupt feature offers the ability to detect changes in the status output bits without register polling. Assertion of interrupt indicates that one or more of the status output bits has changed since the last read cycle. There are three interrupt output indicators on the 80220/80221: (1) MDINT pin, (2) INT bit in the MI serial port Status Output register, and (3) interrupt pulse on MDIO. These interrupt signals can be used by an external device to initiate a read cycle. Then when an interrupt is detected, the individual registers (or multiple registers) can be read out and the status bits compared against their previous values to determine any changes. After the interrupt its have been read out, the interrupt signals are automatically deasserted. A mask register bit exists for every status output bit in the Mask register so that the interrupt bits can be individually programmed for each application.

5.10.3 Multiple Register Access

If the MI serial port needs to be constantly polled in order to monitor changes in status output bits, or if it is desired that all registers be read or written in a singleserial port access cycle, multiple register access mode can be used. Multiple register access allows access to all registers in a single MI serial port access cycle. When multiple register access is enabled, then all the registers are read/written when the register address REGAD[4:0]=11111. This eliminates the need to read or write registers individually. Multiple register access mode is normally disabled but it can be enabled by setting the multiple register access enable bit in the MI serial port Configuration 2 register.

5.10.4 Serial Port Addressing

The device address for the MI serial port are selected by tying the $\overline{\text{MDA[4:0]}}$ pins to the desired value. $\overline{\text{MDA[4:0]}}$ share the same pins as the $\overline{\text{MDINT}}$ and PLED[3:0] outputs, respectively, as shown Figure 15a. At powerup or reset, the output drivers are tristated for an interval called the power-on reset time. During the power-on reset interval, the value on these pins is latched into the device, inverted, and used as the MI serial port address. The LED outputs are open drain with internal resistor pullup to VCC.

If an LED is desired on the LED outputs, then an LED and resistor are tied to VCC as shown in Figures 15b. If a high address is desired, then the LED to VCC automatically makes the latched address value a high. If a low value for

the address is desired, then a 50K resistor to GND must be added as shown in Figure 15b.

If no LED's are needed on the LED outputs, the selection of addresses can be done as shown in Figure 15c. If a high address is desired, the pin should be left floating and the internal pullup will pull the pin high during power-on reset time and latch in a high address value. If a low address is desired, then the $\overline{MDINT}$ and $\overline{PLED[3:0]}$ output pins should be tied either directly to GND or through an optional 50K resistor to GND. $\overline{PLED3}$ should always be tied through a 50K resistor to GND since it has both pullup and pulldown capability. The optional 50K resistor also allows the $\overline{MDINT}$ and PLED[2:0] pins to be used as digital outputs under normal conditions.

Note that the $\overline{MDA[4:0]}$ addresses are inverted inside the 80220/80221 before going to the MI serial port block. This means that the $\overline{MDA[4:0]}$ pins would have to be pin strapped to 11111 externally in order to successfully match the MI physical address bits PHYAD[4:0]=00000 internally.

a.) OUTPUT DRIVER / INPUT ADDRESS CORRESPONDENCE
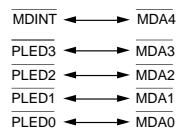
b.) SETTING ADDRESS WITH LEDs
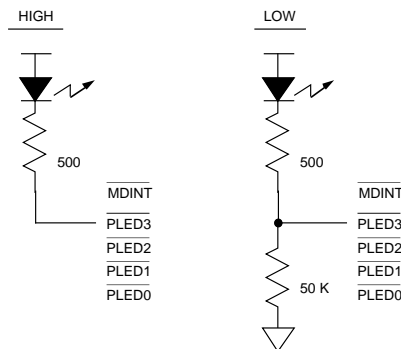
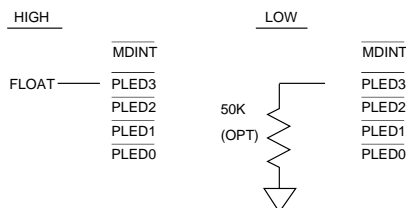**c.) SETTING ADDRESS WITHOUT LEDs**

Figure 15. Serial Device Port Address Selection

5.11 LONG CABLE

IEEE 802.3 specifies that 10BaseT and 100BaseTX operate over twisted pair cable lengths of between 0-100 meters. The squelch levels can be reduced by 4.5 dB if the receive level adjust bit is appropriately set in the MI serial port Configuration 1 register, which will allow the 80220/80221 to operate with up to 150 meters of twisted pair cable. The equalizer is already designed to accommodate between 0-125 meters of cable.

5.12 AUTOMATIC JAM

The 80220/80221 has an automatic JAM generation feature which automatically transmits a JAM packet when receive activity is detected. This feature is primarily designed to give the user a means to easily implement half duplex flow control. In a typical application, a watermark signal from a system FIFO or memory would be tied directly to the $\overline{JAM}$ pin. When the system FIFO is nearly full and more data is incoming from receiver, the device will automatically transmit a JAM packet and create a collision which will cause the far end device to backoff allowing time for the system FIFO to empty itself.

The JAM generation feature requires that the $RX\_EN/\overline{JAM}$ pin be programmed for $\overline{JAM}$. This can be done by appropriately setting the R/J configuration select bit in the MI serial port Configuration 2 register.

5.13 OSCILLATOR

The 80220/80221 requires a 25 Mhz reference frequency for internal signal generation. This 25 Mhz reference frequency can be generated by either connecting an external 25 Mhz crystal between OSCIN and GND or by applying an external 25 Mhz clock to OSCIN.

If the crystal oscillator is used, it needs only a crystal, and no other external capacitors or other components are required. The crystal must have the characteristics shown in Table 24. The crystal must be placed as close as possible to OSCIN and GND pins so that parasitics on OSCIN are kept to a minimum.

Table 24. Crystal Specifications

Parameter	Spec
Type	Parallel Resonant
Frequency	25 Mhz +/- 0.01%
Equivalent Series Resistance	25 ohms max
Load Capacitance	18 pF typ
Case Capacitance	7 pF max
Power Dissipation	1mW max

5.14 PROGRAMMABLE LED DRIVERS

The $\overline{PLED[5:0]}$ outputs can all drive LED's tied to VCC as shown in Figures 11-13. In addition, $\overline{PLED1}$ and $\overline{PLED0}$ can drive an LED tied to GND as well as VCC.

The $\overline{PLED[3:0]}$ outputs can be programmed through the MI serial port   to do 4 different functions: (1) Normal Function (2) On, (3) Off, and (4) Blink.

$\overline{PLED[3:0]}$ can be programmed to indicate 4 different sets of events with the LED Normal Function select bits in the MI serial port Configuration 2 register. In addition, $\overline{PLED[3:0]}$ can be user controlled by appropriately setting the LED output select bits in the MI serial port Configuration 2 register.

When $\overline{PLED[3:0]}$ is programmed for its Normal function, these outputs indicate the specific functions described in Table 5 and determined by the LED Normal Function select bits. When $\overline{PLED[3:0]}$ is programmed to be On, the LED output driver go low, thus turning on the LED under user control. When $\overline{PLED[3:0]}$ is programmed to be Off, the LED output driver will turn off, thus turning off the LED under user control.   When $\overline{PLED[3:0]}$ is programmed to Blink, the LED output driver will continuously blink at a rate of 100 mS on, 100 mS off.

The On and Off functions allow the LED driver to be controlled directly through the MI serial port to indicate any function that is desired under external control. The Blink function allows the same external control of the LED driver and also offers the provision to blink the LED without the need for any external timers.

The $\overline{PLED[5:0]}$ outputs can also drive other digital inputs. Thus, $\overline{PLED[5:0]}$ can also be used as digital outputs whose function can be user defined and controlled through the MI serial port.

Note that $\overline{PLED1}$ and $\overline{PLED0}$ pins have both pullup and pulldown transistors. This allows these pins to drive an LED from VCC or to GND. When $\overline{PLED0}$ is programmed to be 10/100 Mbps select, two LED's can be connected to this pin, one to VCC to indicated 100 Mbps mode is enabled, the other to GND to indicate 10 Mbps mode is enabled. Similarly, when $\overline{PLED1}$ is programmed to be a Half/Full Duplex Mode indication, two LED's can be con-nected to this pin, one to VCC to indicate Full Duplex Mode is enabled, the other to GND to indicate Half Duplex Mode is enabled.

5.15 POWER SUPPLY DECOUPLING

There are six VCC's on the 80220/80221 (VCC[6:1]) and six GND's (GND[6:1]).

All six VCC's should be connected together as close as possible to the device with a large VCC plane. If the VCC's vary in potential by even a small amount, noise and latchup can result. The VCC's should be kept to within 50 mV of each other.

All six GND's should also be connected together as close as possible to the device with a large ground plane. If the GND's vary in potential by even a small amount, noise and latchup can result. The VCC's should be kept to within 50 mV of each other.

A 0.01-0.1µF decoupling capacitor should be connected between each VCC/GND set as close as possible to the device pins, preferably within 0.5". The value should be chosen on whether the noise from VCC-GND is high or low frequency. A conservative approach would be to use two decoupling capacitors on each VCC/GND set, one 0.1µf for low frequency and one 0.001µf for high frequency noise on the power supply.

The VCC connection to the transmit transformer center tap shown in Figures 11-13 has to be well decoupled in order to minimize common mode noise injection from the supply into the twisted pair cable. And is recommended that a 0.01 µF decoupling capacitor be placed between the center tap VCC to the S004 GND plane. This decoupling capacitor should be physically placed as close as possible to the transformer center tap, preferably within 0.5"

The PCB layout and power supply decoupling discussed above should provide sufficient decoupling to achieve the following when measured at the device: (1) The resultant AC noise voltage measured across each VCC/GND set should be less than 100 mVpp, (2) All VCC's should be within 50 mVpp of each other, and (3) All GND's should be within 50 mVpp of each other.

6.0 Specifications

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are limits beyond which may cause permanent damage to the device or affect device reliability. All voltages are specified with respect to GND, unless otherwise specified.

VCC Supply Voltage ....-0.3V to 6.0V

*All Inputs and Outputs
with Respect to GND ....-0.3V to VCC+0.3V*

Package Power Dissipation, ...2.0 Watt @ 70°C
Storage Temperature ....-65 to +150°C
Temperature Under Bias ....-10 to +80°C
Lead Temperature (Soldering, 10 Sec) .... 260°C
Body Temperature (Soldering, 30 Sec) .... 220°C

DC ELECTRICAL CHARACTERISTICS

Unless otherwise noted, all test conditions are as follows:

1. T_A = 0 to +70°C
2. V_{CC} = 5V +/-5%
3. 25 MHz +/- 0.01%
4. REXT = 10K +/- 1%, no load

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
V_{IL}	Input Low Voltage			0.8	Volt	All except OSCIN, $\overline{MDA[4:0]}$
				V_{CC} -1.0	Volt	$\overline{MDA[4:0]}$
				1.5	Volt	OSCIN
V_{IH}	Input High Voltage	2			Volt	All except OSCIN, $\overline{MDA[4:0]}$
		V_{CC} - 0.5			Volt	MDA[4:0]
		3.5			Volt	OSCIN
I_{IL}	Input Low Current			±1	μA	V_{IN} = GND All Except OSCIN, $\overline{MDA[4:0]}$, TRFADJ [1:0], $\overline{T4LNK}$, TPI±
				± 10	μA	V_{IN} = GND, TRFADJ0
		-4		-25	μA	V_{IN} = GND, $\overline{MDA[4:0]}$
		-12		-120	μA	V_{IN} = GND, TRFADJ1, $\overline{T4LNK}$
				-150	μA	V_{IN} = GND, OSCIN
I_{IH}	Input High Current			±1	μA	V_{IN} = V_{CC} All Except OSCIN, TRFADJ[1:0], T4ADV, TPI±, RPTR
				± 10	μA	V_{IN} = V_{CC}, TRFADJ1
		12		120	μA	V_{IN} = V_{CC}, TRFADJ0, T4ADV, RPTR
				150	μA	V_{IN} = V_{CC}, OSCIN
V_{OL}	Output Low Voltage			0.4	Volt	I_{OL} = -4 mA All Except PLED[5:0], TPO±
				1	Volt	I_{OL} = -20 mA, $\overline{PLED[5:0]}$
V_{OH}	Output High Voltage	V_{CC}-1.0			Volt	I_{OH} = 4 mA All Except $\overline{PLED[5:0]}$, $\overline{MDINT}$, TPO±
		2.4			Volt	I_{OH} = 4 μA, $\overline{PLED[5:2]}$, $\overline{MDINT}$
		V_{CC} -1.0			Volt	I_{OH} = 10 mA, $\overline{PLED[1:0]}$
C_{IN}	Input Capacitance		5		pF	
I_{CC}	V_{CC} Supply Current		170	200	mA	Transmitting
I_{SS}	GND Supply Current			250	mA	Transmitting
				1	mA	Powerdown Mode

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TWISTED PAIR CHARACTERISTICS, TRANSMIT

Unless otherwise noted, all test conditions are as follows:

1. T_A= 0 to +70°C
2. V_{CC} = 5V +/-5%
3. 25 MHz +/- 0.01%
4. REXT = 10K +/- 1%, no load
5. TPO± loading shown in Figure 11 or equivalent.

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
T_{OV}	TP Differential Output Voltage	0.950	1.000	1.050	V pk	100 Mbps, UTP Mode, 100 Ohm Load
		1.165	1.225	1.285	V pk	100 Mbps, STP Mode, 150 Ohm Load
		2.2	2.5	2.8	V pk	10 Mbps, UTP Mode, 100 Ohm Load
		2.694	3.062	3.429	V pk	10 Mbps, STP Mode, 150 Ohm Load
T_{OVS}	TP Differential Output Voltage Symmetry	98		102	%	100 Mbps, Ratio of Positive And Negative Amplitude Peaks on TPO±
T_{ORF}	TP Differential Output Rise And Fall Time	3.0		5.0	nS	100 Mbps TRFADJ [1:0] = 10
T_{ORFS}	TP Differential Output Rise And Fall Time Symmetry			+/- 0.5	nS	100 Mbps, Difference Between Rise And Fall Times on TPO± TRFADJ [1:0] = 10
T_{ODC}	TP Differential Output Duty Cycle Distortion			+/- 0.25	nS	100 Mbps, Output Data=0101... NRZ Pattern Unscrambled, Measure At 50% Points
T_{OJ}	TP Differential Output Jitter			+/- 1.4	nS	100 Mbps, Output Data=scrambled /H/
T_{OO}	TP Differential Output Overshoot			5.0	%	100 Mbps
T_{OVT}	TP Differential Output Voltage Template	See Figure 4				10 Mbps
T_{SOI}	TP Differential Output SOI Voltage Template	See Figure 6				10 Mbps
T_{LPT}	TP Differential Output Link Pulse Voltage Template	See Figure 7				10 Mbps, NLP and FLP
T_{OIV}	TP Differential Output Idle Voltage			+/- 50	mV	10 Mbps. Measured on Secondary Side of Xfmr in Figure 11.

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TWISTED PAIR CHARACTERISTICS, TRANSMIT (continued)

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
T_{OIA}	TP Output Current	19	20	21	mA pk	100 Mbps, UTP with TLVL[3:0]=1000
		15.53	16.33	17.13	mA pk	100 Mbps, STP with TLVL[3:0]=1000
		44	50	56	mA pk	10 Mbps, UTP with TLVL[3:0]=1000
		35.93	40.82	45.72	mA pk	10 Mbps, STP with TLVL[3:0]=1000
T_{OIR}	TP Output Current Adjustment Range	0.80		1.2		V_{CC}=5V, Adjustable with REXT, relative to T_{OIA} with REXT=10K
		0.86		1.16		V_{CC}=5V, Adjustable with TLVL[3:0] See Section 5.4 Relative to Value at TLVL[3:0]=1000
T_{ORA}	TP Output Current TLVL Step Accuracy			+/-50	%	Relative to Ideal Values in Table 3. Table 3 Values Relative to Output with TLVL[3:0]=1000.
T_{OR}	TP Output Resistance		10K		Ohm	
T_{OC}	TP Output Capacitance		15		pF	

TWISTED PAIR CHARACTERISTICS, RECEIVE

Unless otherwise noted, all test conditions are as follows:

1. T_A = 0 to +70°C
2. V_{CC} = 5V +/-5%
3. 25 MHz +/- 0.01%
4. REXT = 10K +/- 1%, no load
5. 62.5/10 Mhz Square Wave on TP inputs in 100/10 Mbps

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
R_{ST}	TP Input Squelch Threshold	166		500	mV pk	100 Mbps, RLVL=0
		310		540	mV pk	10 Mbps, RLVL=0
		60		200	mV pk	100 Mbps, RLVL=1
		186		324	mV pk	10 Mbps, RLVL=1
R_{UT}	TP Input Unsquelch Threshold	100		300	mV pk	100 Mbps, RLVL=0
		186		324	mV pk	10 Mbps, RLVL=0
R_{OCV}	TP Input Open Circuit Voltage		$\frac{V_{CC}}{3} \pm 0.5$		Volt	Voltage on Either TPI+ or TPI– with Respect to GND.
R_{CMR}	TP Input Common Mode Voltage Range		$R_{OCV} \pm 0.25$		Volt	Voltage on TPI± with Respect to GND.
R_{DR}	TP Input Differential Voltage Range			V_{CC}	Volt	
R_{IR}	TP Input Resistance	5K			Ohm	
R_{IC}	TP Input Capacitance		10		pF	

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AC TEST TIMING CONDITIONS

Unless otherwise noted, all test conditions are as follows:

1. T_A = 0 to +70°C
2. V_{CC} = 5V +/-5%
3. 25 MHz +/- 0.01%
4. REXT = 10K +/- 1%, no load
5. Input conditions:
   All Inputs: tr,tf<=10nS, 20-80%
6. Output Loading
   TPO±:   Same as Figure 11 or equivalent, 10pF
   Open Drain Outputs: 1K Pullup, 50pF
   All Other Digital Outputs: 25pF
7. Measurement Points:
   TPO±, TPI±:   0.0 V During Data, ±0.3V at start/end of packet
   All other inputs and outputs: 1.5 Volts

25 Mhz INPUT / OUTPUT CLOCK TIMING CHARACTERISTICS

Refer to Figure 16 for Timing Diagram.

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_1	OSCIN Period	39.996	40	40.004	nS	Clock Applied to OSCIN
t_2	OSCIN High Time	16			nS	Clock Applied to OSCIN
t_3	OSCIN Low Time	16			nS	Clock Applied to OSCIN
t_4	OSCIN to TX_CLK Delay			10	nS	100 Mbps
				20	nS	10 Mbps
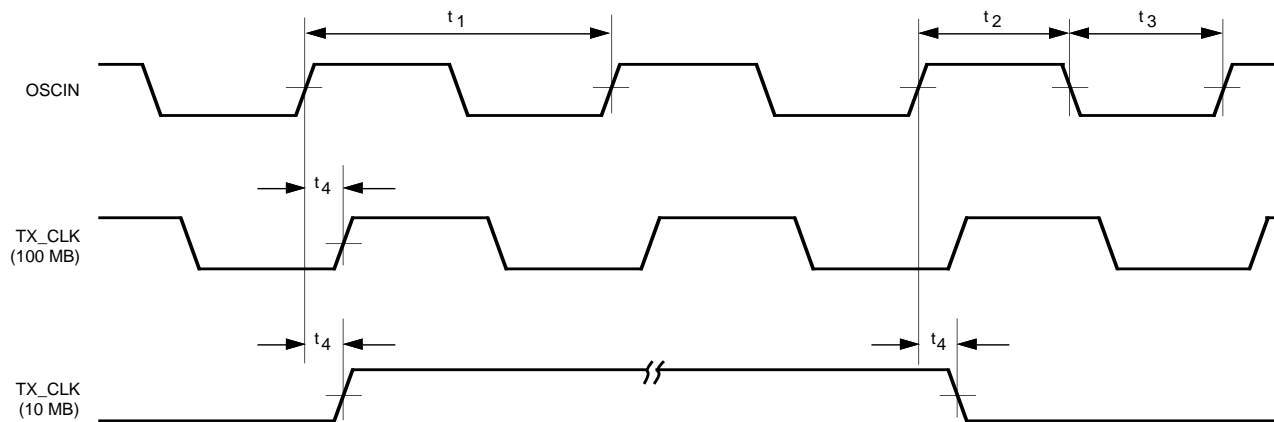
Figure 16. 25 Mhz Output Timing

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TRANSMIT TIMING CHARACTERISTICS

Refer to Figure 17-18 for Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{11}	TX_CLK Period	39.996	40	40.004	nS	100 Mbps
		399.96	400	400.04	nS	10 Mbps
t_{12}	TX_CLK Low Time	16	20	24	nS	100 Mbps
		160	200	240	nS	10 Mbps
t_{13}	TX_CLK High Time	16	20	24	nS	100 Mbps
		160	200	240	nS	10 Mbps
t_{14}	TX_CLK Rise/Fall Time			10	nS	
t_{15}	TX_EN Setup Time	15			nS	
t_{16}	TX_EN Hold Time	0			nS	
t_{17}	CRS During Transmit Assert Time			40	nS	100 Mbps
				400	nS	10 Mbps
t_{18}	CRS During Transmit Deassert Time			160	nS	100 Mbps
				900	nS	10 Mbps
t_{19}	TXD Setup Time	15			nS	
t_{20}	TXD Hold Time	0			nS	
t_{21}	TX_ER Setup Time	15			nS	
t_{22}	TX_ER Hold Time	0			nS	
t_{23}	Transmit Propagation Delay	60		140	nS	100 Mbps, MII
				140	nS	100 Mbps, FBI
				600	nS	10 Mbps
t_{24}	Transmit Output Jitter			±0.7	nS pk-pk	100 Mbps
				±5.5	nS pk-pk	10 Mbps
t_{25}	Transmit SOI Pulse Width To 0.3V	250			nS	10 Mbps
t_{26}	Transmit SOI Pulse Width to 40 mV			4500	nS	10 Mbps
t_{27}	$\overline{\text{PLEDn}}$ Delay Time			25	mS	$\overline{\text{PLEDn}}$ Programmed For Activity
t_{28}	$\overline{\text{PLEDn}}$ Pulse Width	80		105	mS	$\overline{\text{PLEDn}}$ Programmed For Activity

MII 100MBPS
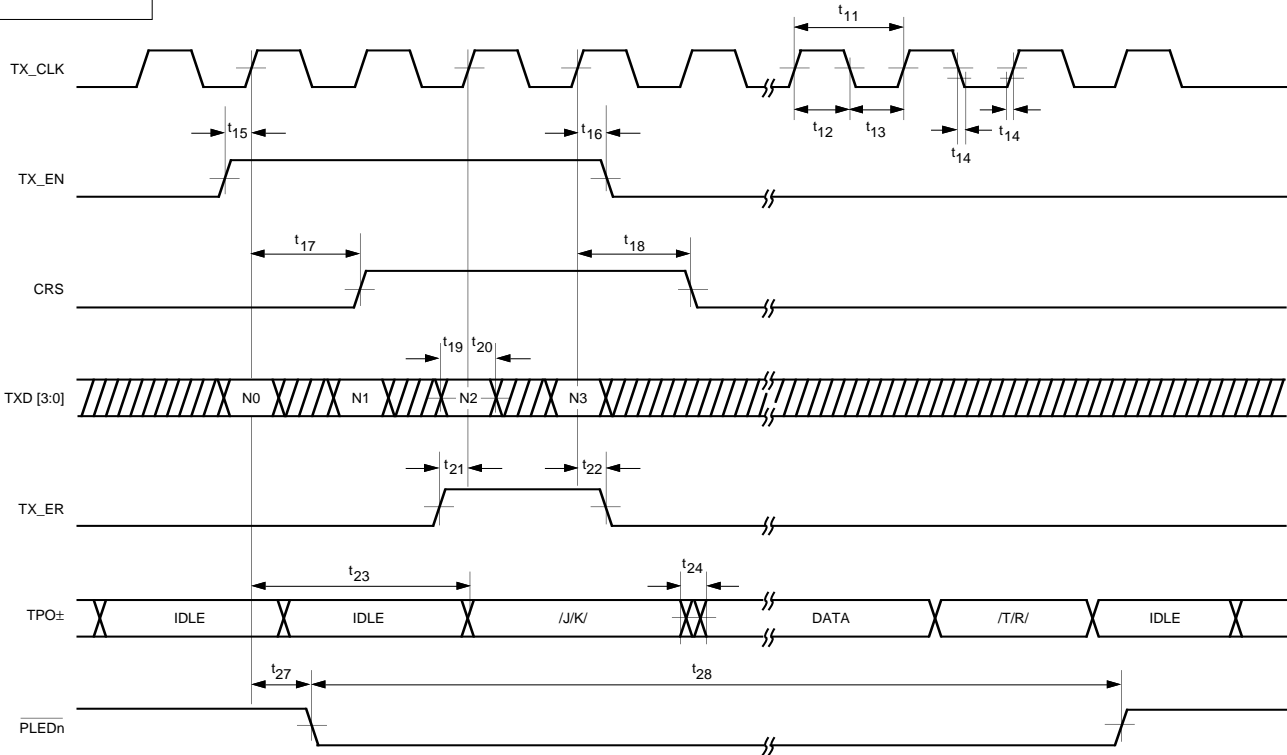
FBI 100MBPS

Same as MII 100Mbps Except:

1. TX_ER Converted to TXD4
2. RX_ER Converted to RXD4
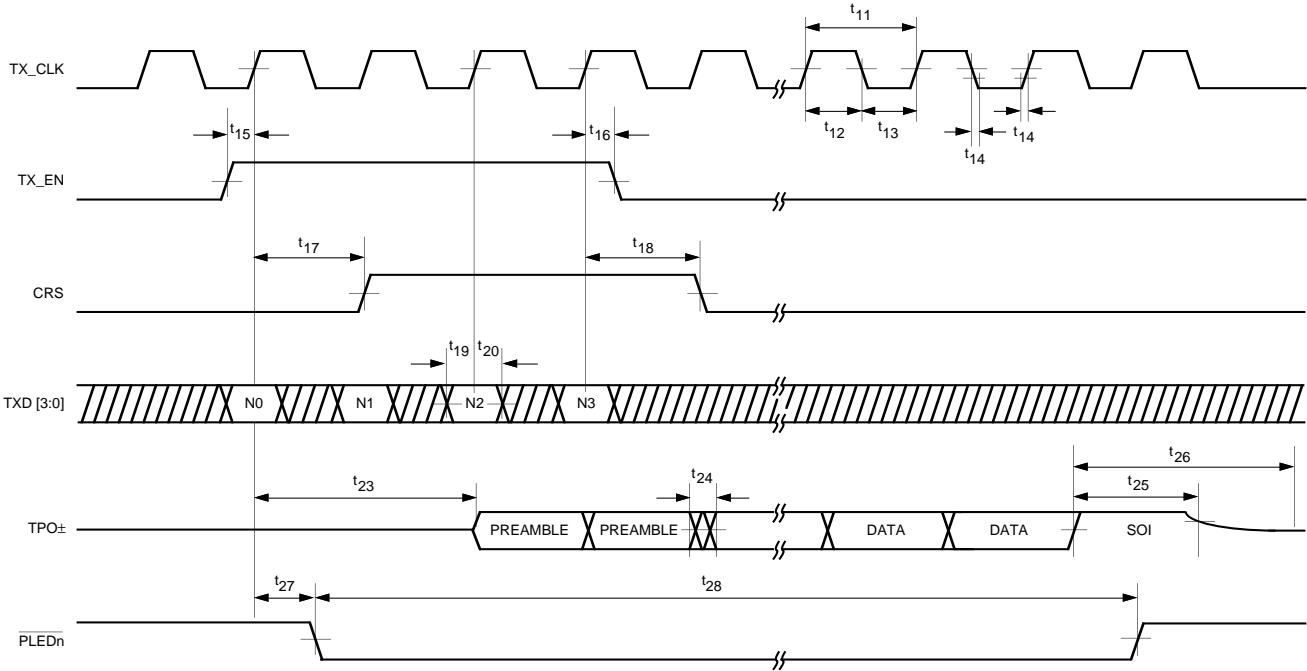
Figure 17. Transmit Timing - 100 Mbps

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MII 10MB

Figure 18. Transmit Timing - 10 Mbps

RECEIVE TIMING CHARACTERISTICS

Refer to Figures 19-23 for Timing Diagrams

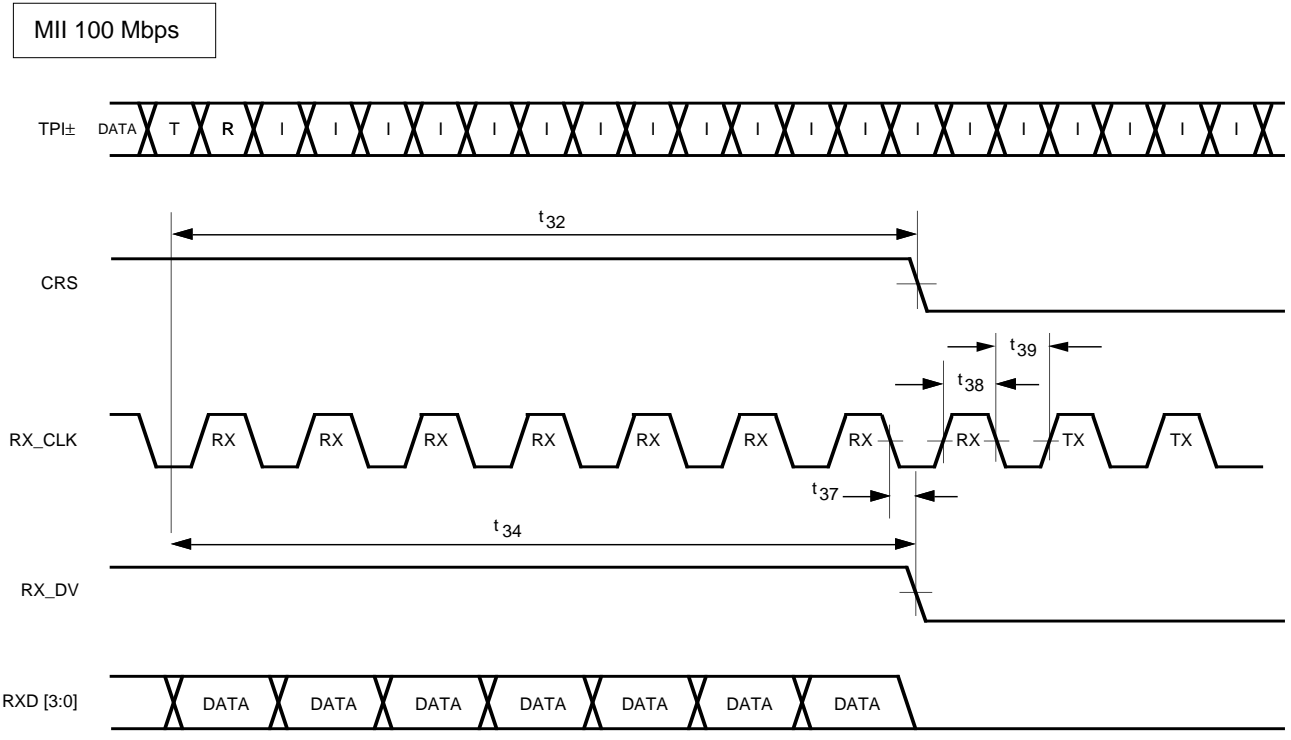| SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{31}	Start Of Packet To CRS Assert Delay			200	nS	100 Mbps, MII
				200	nS	100 Mbps, FBI
				700	nS	10 Mbps
t_{32}	End Of Packet To CRS Deassert Delay	130		240	nS	100 Mbps, MII
				240	nS	100 Mbps, FBI
				600	nS	10 Mbps. Relative To Start Of SOI Pulse
t_{33}	Start Of Packet To RX_DV Assert Delay			240	nS	100 Mbps
				3600	nS	10 Mbps
t_{34}	End Of Packet To RX_DV Deassert Delay			280	nS	100 Mbps
				1000	nS	10 Mbps. Relative To Start Of SOI Pulse
t_{37}	RX_CLK To RX_DV, RXD, RX_ER Delay	-8		8	nS	100 Mbps
		-80		80	nS	10 Mbps
t_{38}	RX_CLK High Time	18	20	22	nS	100 Mbps
		180	200	600	nS	10 Mbps
t_{39}	RX_CLK Low Time	18	20	22	nS	100 Mbps
		180	200	600	nS	10 Mbps
t_{40}	SOI Pulse Minimum Width Required for Idle Detection	125		200	nS	10 Mbps Measure TPI± from last zero cross to 0.3V point.
t_{41}	Receive Input Jitter			±3.0	nS pk - pk	100 Mbps
				±13.5	nS pk -pk	10 Mbps
t_{43}	$\overline{PLEDn}$ Delay Time			25	mS	$\overline{PLEDn}$ Programmed for Activity
t_{44}	$\overline{PLEDn}$ Pulse Width	80		105	mS	$\overline{PLEDn}$ Programmed for Activity
t_{45}	RX_CLK, RXD, CRC, RX_DV, RX_ER Output Rise and Fall Times			10	nS	
t_{46}	RX_EN Deassert to Rcv MII Output HI-Z Delay			40	nS	
t_{47}	RX_EN Assert to Rcv MII Output Active Delay			40	nS	

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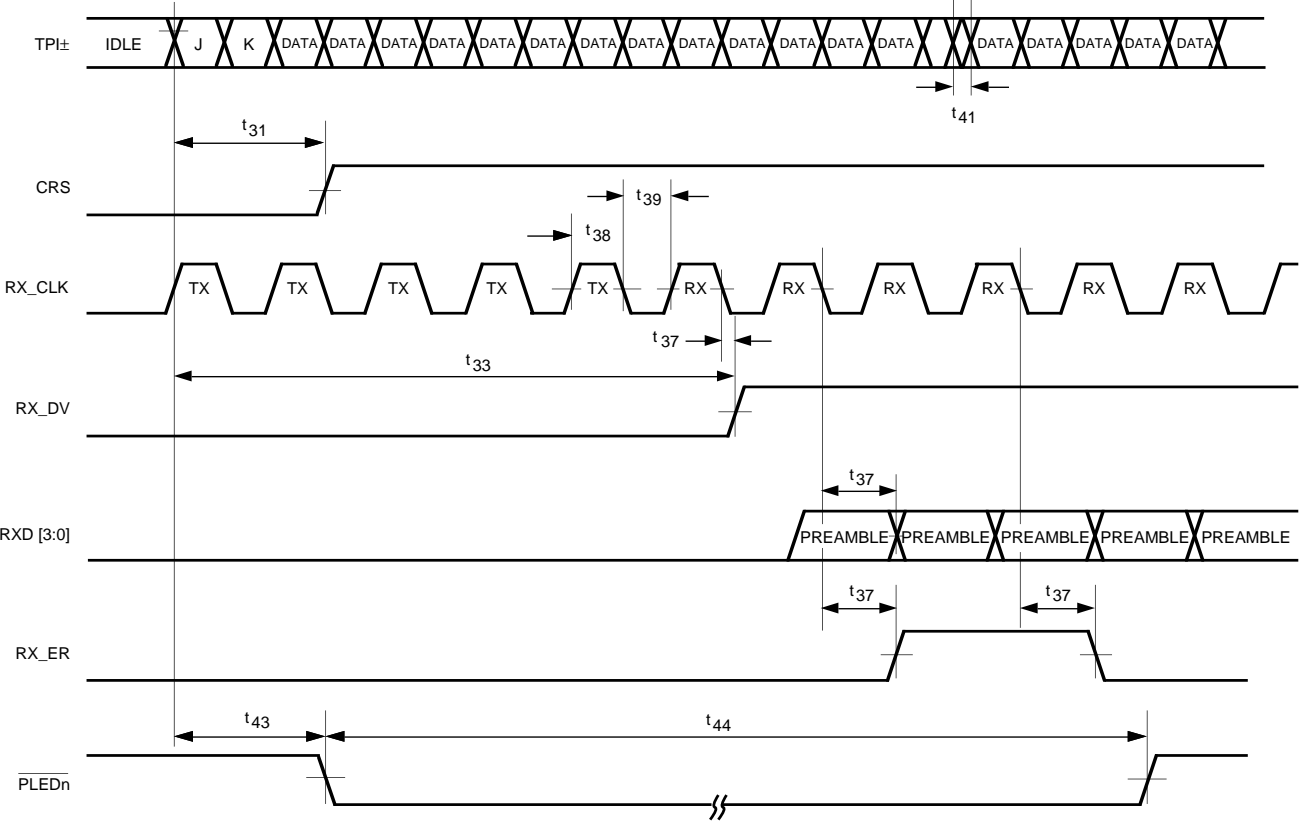
MII 100 Mbps

FBI 100 Mbps

Same as MII 100 Mbps except:
1. RX_ER Converted to RXD4
2. TX_ER Converted to TXD4

Figure 19. Receive Timing, Start of Packet - 100 Mbps

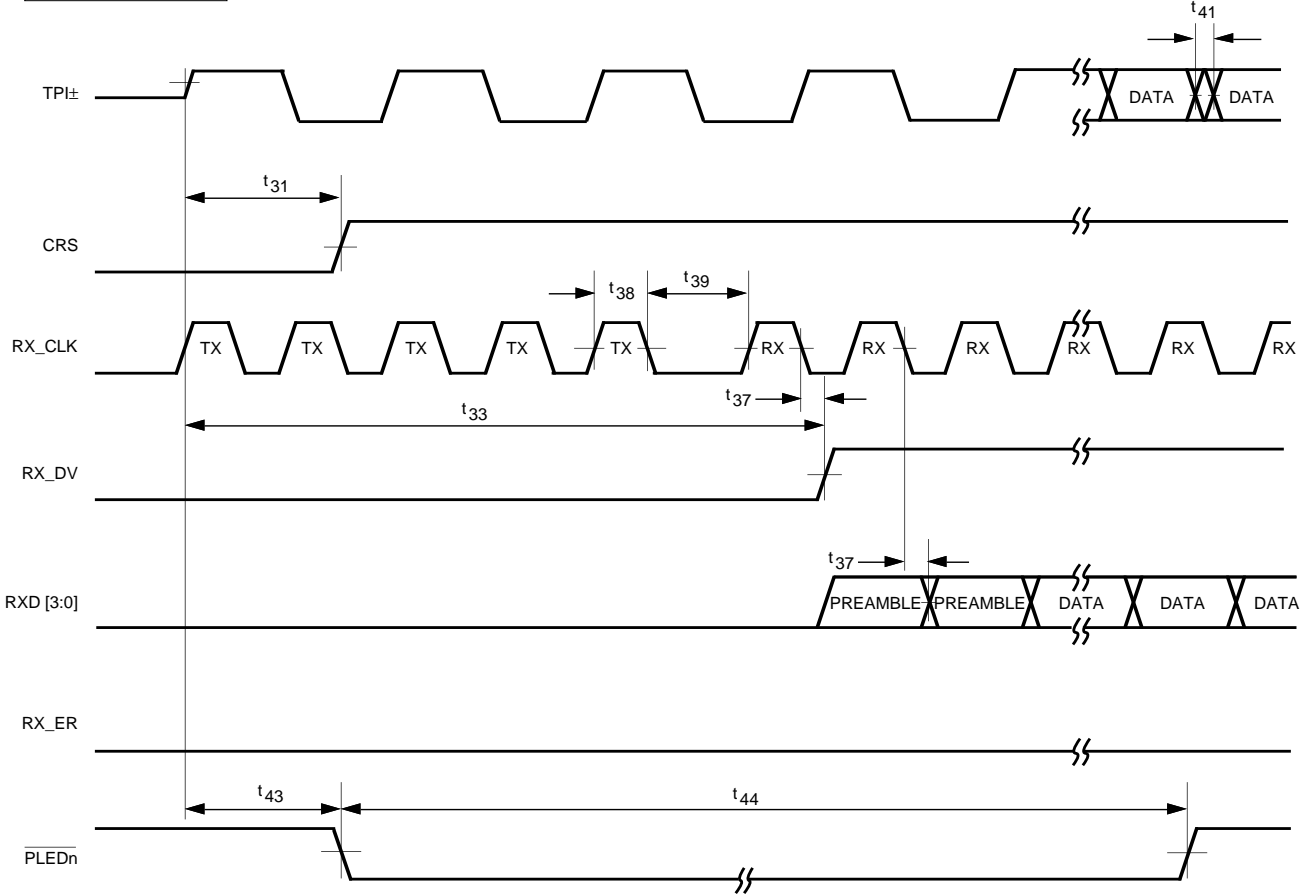LSI LOGIC®

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MII 100 Mbps

TPI± DATA | T | R | I | I | I | I | I | I | I | I | I | I | I | I | I | I | I | I | I | I | I |

t$_{32}$

CRS

t$_{39}$

t$_{38}$

RX_CLK | RX | RX | RX | RX | RX | RX | RX | RX | TX | TX

t$_{37}$

t$_{34}$

RX_DV

RXD [3:0] | DATA | DATA | DATA | DATA | DATA | DATA | DATA

FBI 100 Mbps

Same as MII 100 Mbps except:
1. TX_ER Converted to RXD4
2. RX_ER Converted to TXD4

Figure 20. Receive Timing, End of Packet - 100 Mbps

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MII 10 MB

Figure 21. Receive Timing, Start of Packet - 10 Mbps

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MII 10 MB
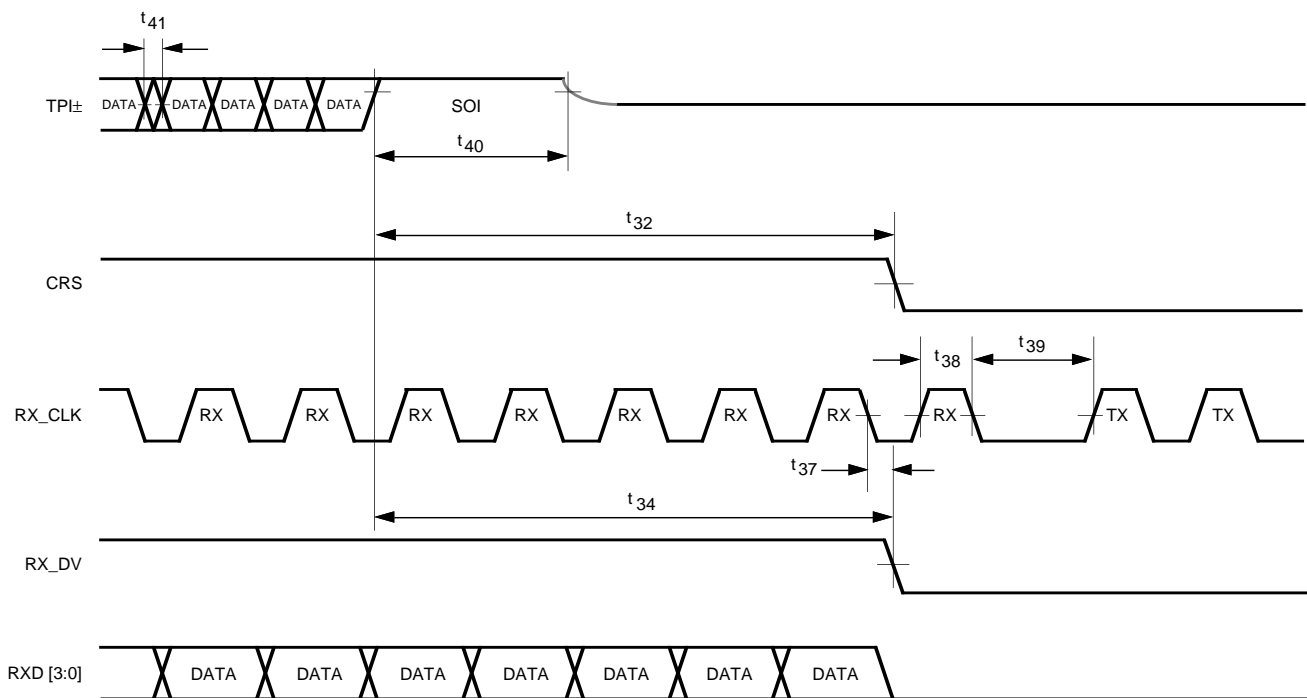
Figure 22. Receive Timing, End of Packet - 10 Mbps

Figure 23. RX_EN Timing

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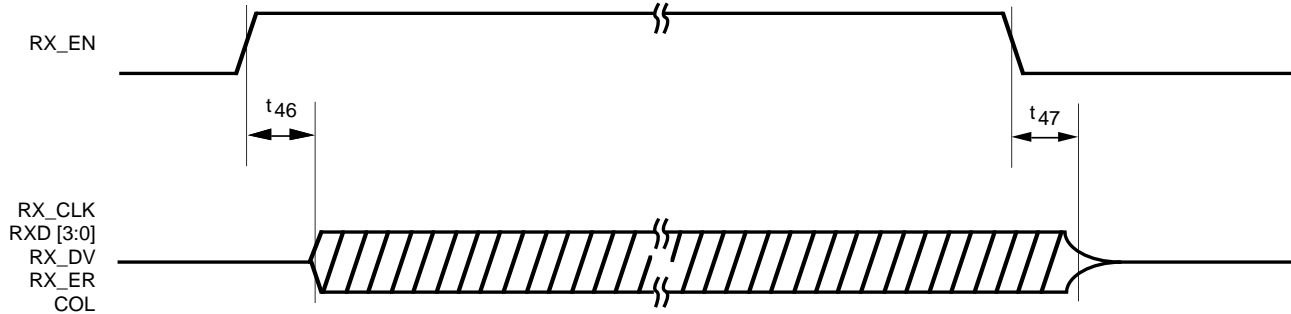
COLLISION AND JAM TIMING CHARACTERISTICS

Refer to Figures 24-27 for Timing Diagrams

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{51}	Rcv Packet Start to			200	nS	100 Mbps
	COL Assert Time			700	nS	10 Mbps
t_{52}	Rcv Packet Stop to	130		240	nS	100 Mbps
	COL Deassert Time			300	nS	10 Mbps
t_{53}	Xmt Packet Start to			200	nS	100 Mbps
	COL Assert Time			700	nS	10 Mbps
t_{54}	Xmt Packet Stop to			240	nS	100 Mbps
	COL Deassert Time			300	nS	10 Mbps.
t_{55}	$\overline{PLEDn}$ Delay Time			25	mS	$\overline{PLEDn}$ Programmed for Collision
t_{56}	$\overline{PLEDn}$ Pulse Time	80		105	mS	$\overline{PLEDn}$ Programmed for Collision
t_{57}	Collision Test Assert Time			5120	nS	
t_{58}	Collision Test Deassert Time			40	nS	
t_{59}	CRS Assert to Transmit			300	nS	100 Mbps
	JAM Packet Start During JAM			800	nS	10 Mbps
t_{60}	COL Rise and Fall Time			10	nS	

MII 100 Mbps

TPO± | I | DATA | DATA | DATA | DATA | DATA | DATA | DATA | DATA | DATA | DATA | DATA | DATA | DATA |

TPI± | I | I | I | I | J | K | DATA | DATA | DATA | DATA | T | R | I | I |

t_{51}

t_{52}

COL

t_{55}

t_{56}

$\overline{PLEDn}$

FBI 100 Mbps

Same as MII 100 Mbps

MII 100 Mbps

TPO±

TPI±

t_{51}

t_{52}

COL

t_{55}

t_{56}

$\overline{PLEDn}$
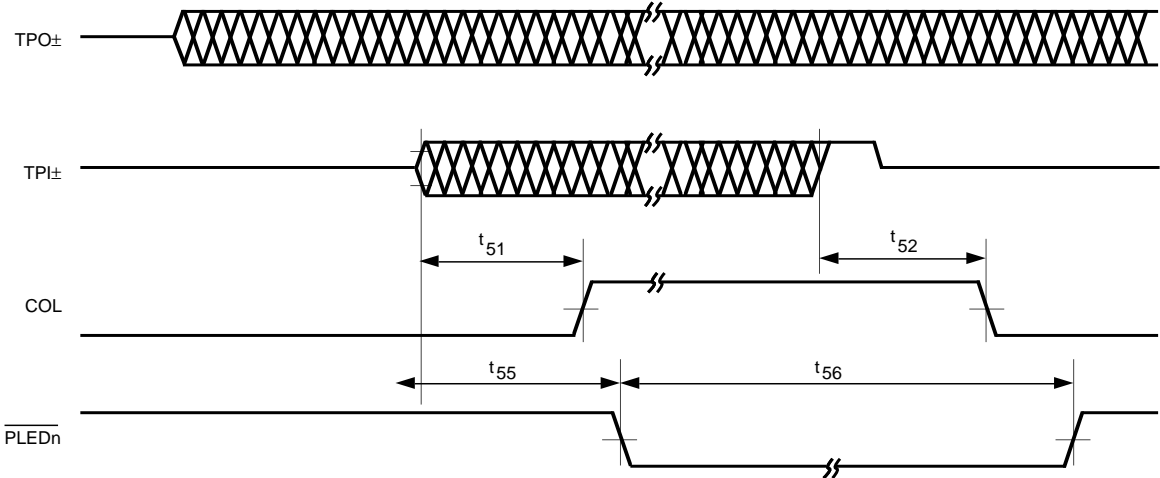
Figure 24. Collision Timing, Receive

MII 100 Mbps
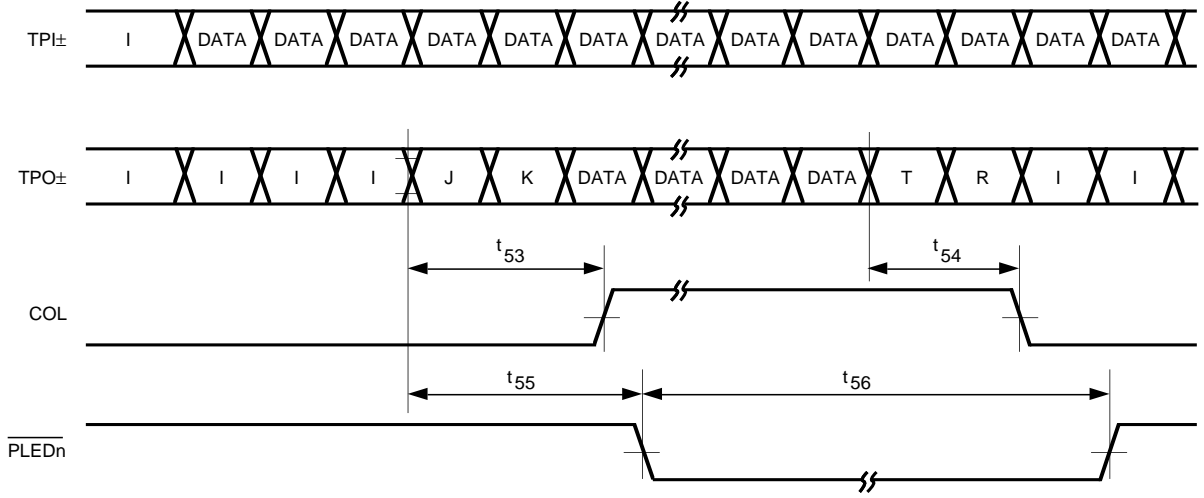
FBI 100 Mbps

Same as MII 100 Mbps
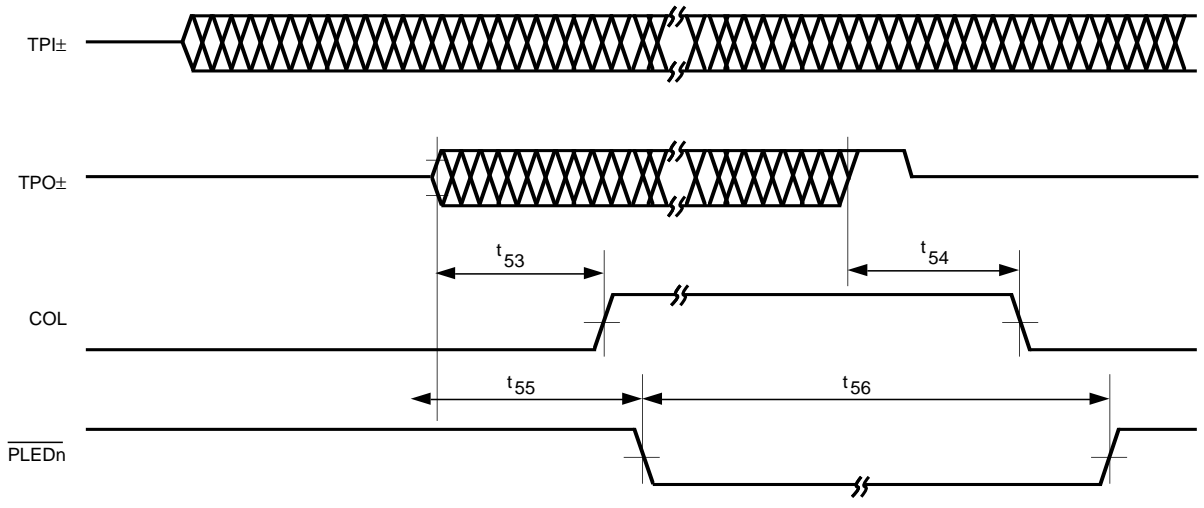
MII 100 Mbps

Figure 25. Collision Timing, Transmit

TX_EN

COL

t₅₇   t₅₈
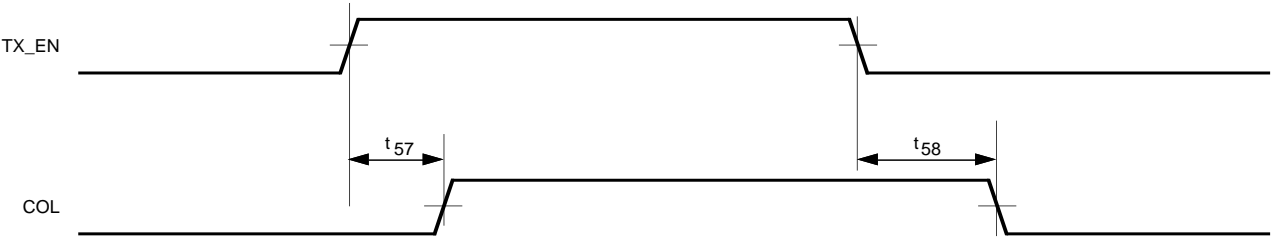
Figure 26. Collision Test Timing

MII 100 Mbps

$\overline{JAM}$ I

TPO±   I   I   J   K   DATA   DATA   DATA   DATA   DATA   DATA   DATA   DATA   DATA   DATA   DATA   DATA

t_{31}

CRS

t_{59}

TPO±   I   I   I   I   I   J   K   JAM   JAM   JAM   JAM   T   R   I   I   I

t_{53} t_{54}

COL

FBI 100 Mbps

Same as MII 100 Mbps

MII 100 Mbps

$\overline{JAM}$

TPI±

t_{31}

CRS

t_{59}

TPO±   JAM   JAM   JAM   JAM

t_{53} t_{54}

COL
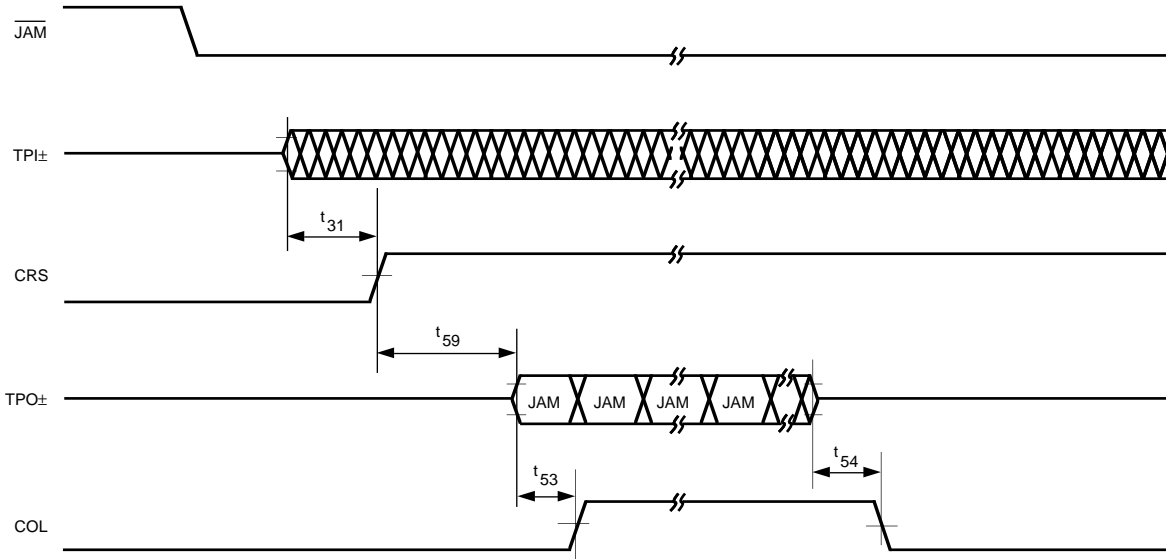
Figure 27. Jam Timing

LINK PULSE TIMING CHARACTERISTICS

Refer to Figures 28-30 for Timing Diagrams

SYM	PARAMETER	LIMIT			UNIT	CONDITION
		MIN	TYP	MAX		
t_{61}	NLP Transmit Link Pulse Width	See Figure 7			ns	
t_{62}	NLP Transmit Link Pulse Period	8		24	mS	
t_{63}	NLP Receive Link Pulse Width Required For Detection	50			nS	
t_{64}	NLP Receive Link Pulse Minimum Period Required For Detection	6		7	mS	link_test_min
t_{65}	NLP Receive Link Pulse Maximum Period Required For Detection	50		150	mS	link_test_max
t_{66}	NLP Receive Link Pulses Required To Exit Link Fail State	3	3	3	Link Pulses	lc_max
t_{63a}	T4LP Receive Link Pulse Width Required For Detection	40			nS	
t_{64a}	T4LP Receive Link Pulse Minimum Period Required For Detection	0.15		0.45	mS	
t_{65a}	T4LP Receive Link Pulse Maximum Period Required For Detection	5		6	mS	
t_{66a}	T4LP Receive Link Pulses Required To Exit Link Fail State	31			Link Pulses	31 Link Pulses Are Required To Exit Link Fail to Link Ready
t_{67}	FLP Transmit Link Pulse Width	100		150	nS	
t_{68}	FLP Transmit Clock Pulse To Data Pulse Period	55.5	62.5	69.5	μS	interval_timer
t_{69}	FLP Transmit Clock Pulse To Clock Pulse Period	111	125	139	μS	
t_{70}	FLP Transmit Link Pulse Burst Period	8		22	mS	transmit_link_burst_timer
t_{71}	FLP Receive Link Pulse Width Required For Detection	50			nS	

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LINK PULSE TIMING CHARACTERISTICS continued

SYM	PARAMETER	LIMIT			UNIT	CONDITION
		MIN	TYP	MAX		
t_{72}	FLP Receive Link Pulse Minimum Period Required For Clock Pulse Detection	5		25	µS	flp_test_min_timer
t_{73}	FLP Receive Link Pulse Maximum Period Required For Clock Pulse Detection	165		185	µS	flp_test_max_timer
t_{74}	FLP Receive Link Pulse Minimum Period Required For Data Pulse Detection	15		47	µS	data_detect_min_timer
t_{75}	FLP Receive Link Pulse Maximum Period Required For Data Pulse Detection	78		100	µS	data_detect_max_timer
t_{76}	FLP Receive Link Pulses Required To Detect Valid FLP Burst	17		17	Link Pulses	
t_{77}	FLP Receive Link Pulse Burst Minimum Period Required For Detection	5		7	mS	nlp_test_min_timer
t_{78}	FLP Receive Link Pulse Burst Maximum Period Required For Detection	50		150	mS	nlp_test_max_timer
t_{79}	FLP Receive Link Pulses Bursts Required To Detect AutoNegotiation Capability	3	3	3	Link Pulse	
t_{80}	FLP Receive Acknowledge Fail Period	1200		1500	mS	
t_{81}	FLP Transmit Renegotiate Link Fail Period	1200		1500	mS	break_link_timer
t_{82}	NLP Receive Link Pulse Maximum Period Required For Detection After FLP Negotation Has Completed	750		1000	mS	link_fail_inhibit_timer
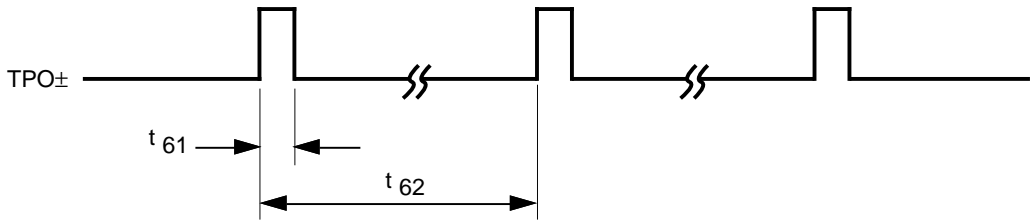
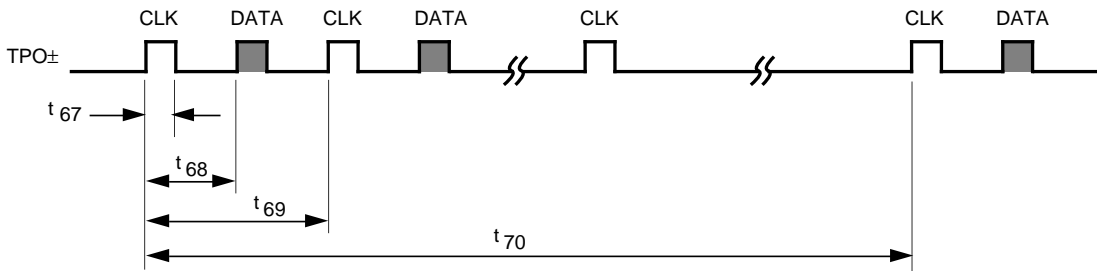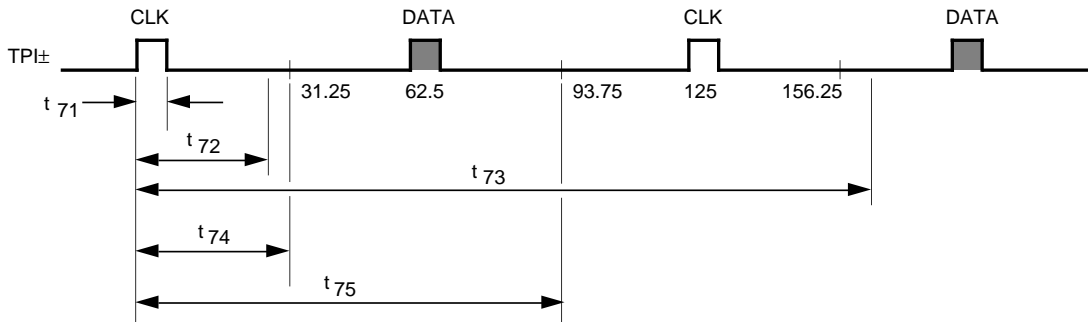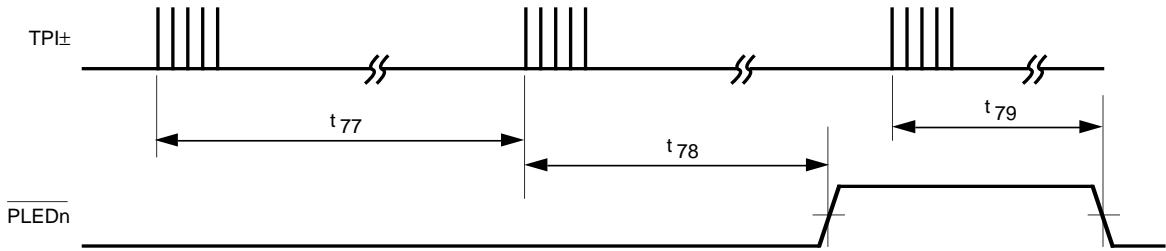a.) Transmit NLP
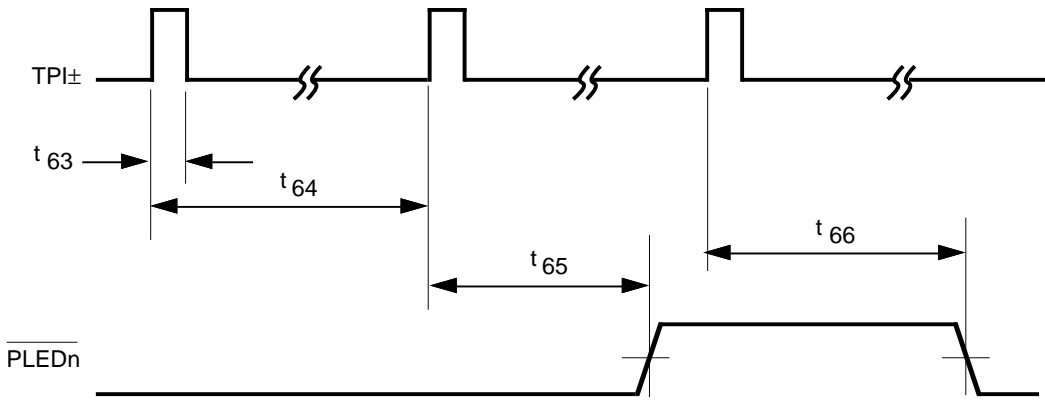
b.) Receive NLP

Figure 28. NLP Link Pulse Timing

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CLK   DATA   CLK   DATA   CLK   CLK   DATA

TPO$\pm$

t_{67}

t_{68}

t_{69}

t_{70}

a.) Transmit FLP and Transmit FLP Burst

CLK   DATA   CLK   DATA

TPI$\pm$

t_{71}

31.25   62.5   93.75   125   156.25

t_{72}

t_{73}

t_{74}

t_{75}

b.) Receive FLP

TPI$\pm$

t_{77}

t_{78}

t_{79}

$\overline{PLEDn}$

c.) Receive FLP Burst

Figure 29. FLP Link Pulse Timing

Receive T4LP
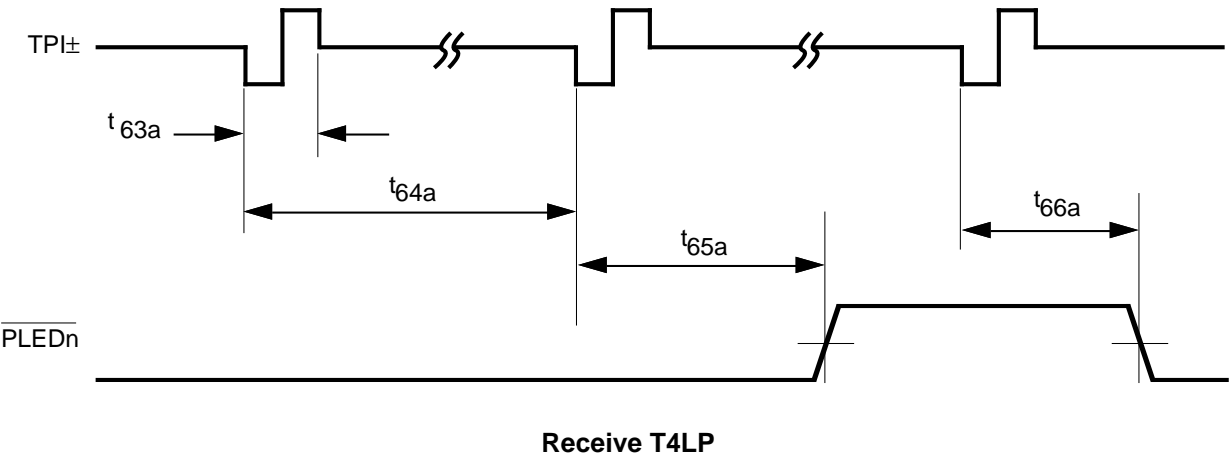
Figure 30. T4LP Link Pulse Timing

JABBER TIMING CHARACTERISTICS

Refer to Figure 31 for Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{91}	Jabber Activation Delay Time	50		100	mS	10 Mbps
t_{92}	Jabber Deactivation Delay Time	250		750	mS	10 Mbps

MII 100 Mb   Not Applicable

FBI 100 Mb   Not Applicable

MI 10 MB
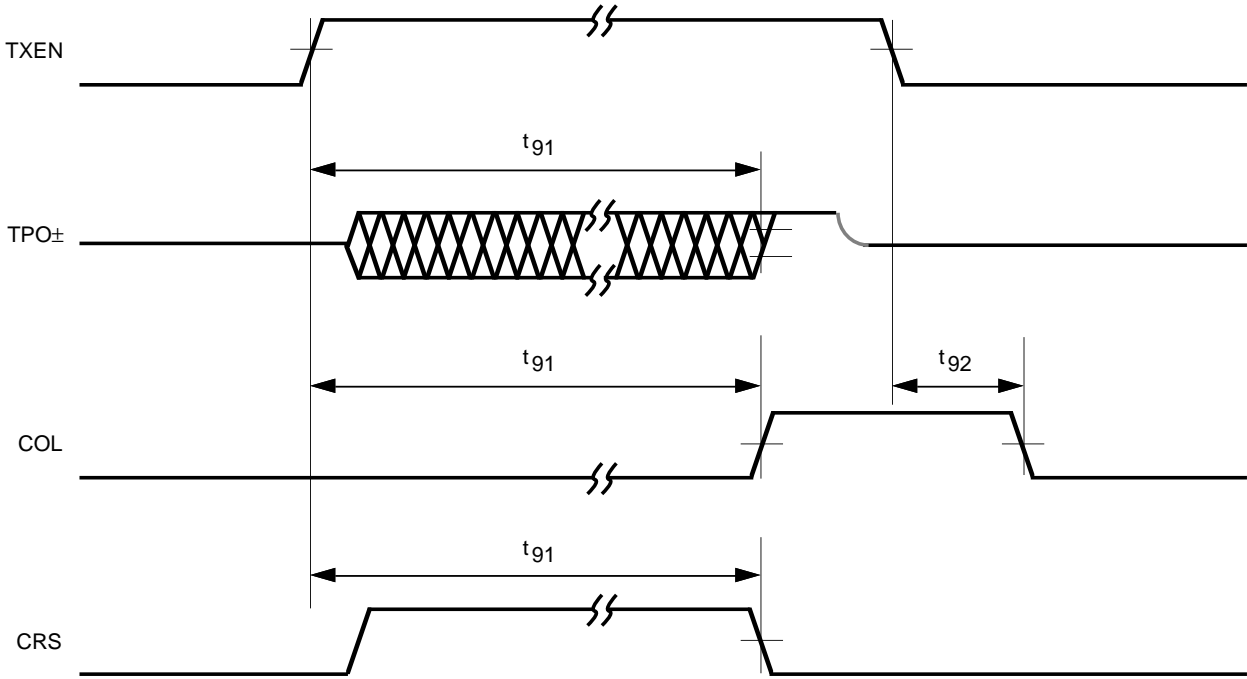
Figure 31. Jabber Timing

LED DRIVER TIMING CHARACTERISTICS

Refer to Figure 32 for Timing Diagram

		LIMIT				
SYM	**PARAMETER**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
t_{96}	$\overline{\text{PLED[5:0]}}$ On Time	80		105	mS	PLED[5:0] Programmed to Blink
t_{97}	$\overline{\text{PLED[5:0]}}$ Off Time	80		105	mS	PLED[5:0] Programmed to Blink
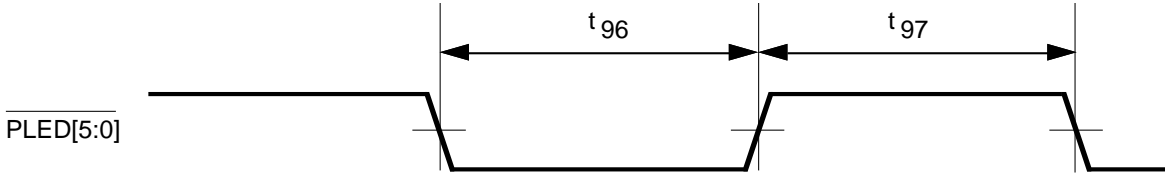
Figure 32. LED Driver Timing

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MI SERIAL PORT TIMING CHARACTERISTICS

Refer to Figures 33-34 for Timing Diagrams

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{101}	MDC High Time	20			nS	
t_{102}	MDC Low Time	20			nS	
t_{103}	MDIO Setup Time	10			nS	Write Bits
t_{104}	MDIO Hold Time	10			nS	Write Bits
t_{105}	MDC To MDIO Delay			20	nS	Read Bits
t_{106}	MDIO Hi-Z To Active Delay			20	nS	Write-Read Bit Transition
t_{107}	MDIO Active To HI-Z Delay			20	nS	Read-Write Bit Transition
t_{108}	Frame Delimiter (Idle)	32			Clocks	# of Consecutive MDC Clocks With MDIO=1
t_{109}	End Of Frame To $\overline{MDINT}$ Transition			100	nS	
t_{110}	MDC To MDIO Interrupt Pulse Assert Delay			100	nS	
t_{111}	MDC To MDIO Interrupt Pulse Deassert Delay			100	nS	

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Figure 33. MI Serial Port Timing

INTERNAL
INTERRUPT
SIGNAL

MDC

t_{110} t_{111}
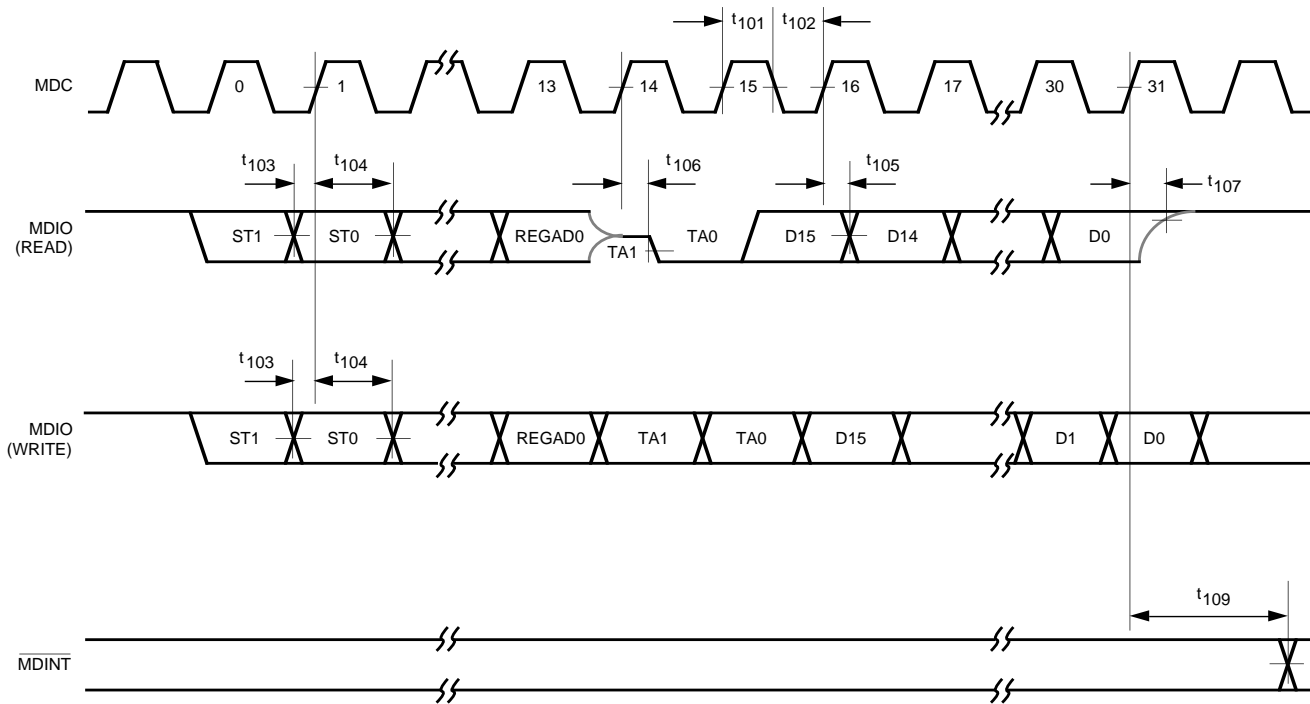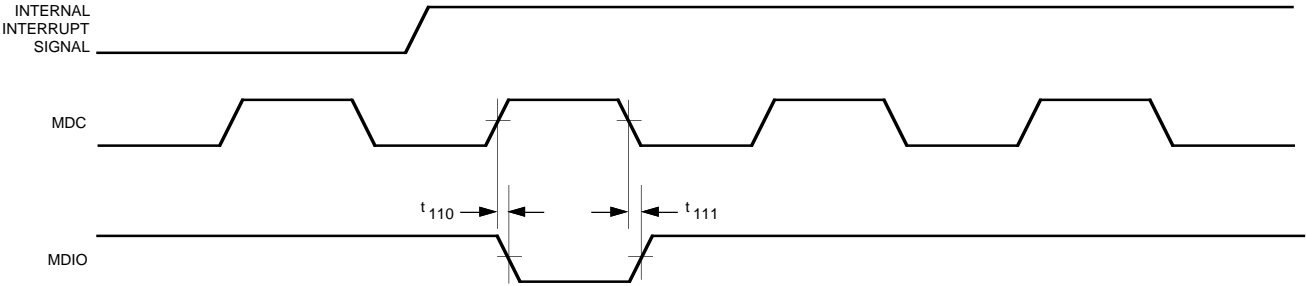
MDIO

Figure 34. MDIO Interrupt Pulse Timing

7.0 Ordering Information

7.1 44 Pin PLCC

N   Q   80220

| PACKAGE TYPE | TEMPERATURE RANGE | PART TYPE |

N = Plastic Leaded
     Chip Carrier

Q – 0°C to +70°C

100 Base-TX/10 Base-T
Ethernet Media Interface Adapter

7.2 64 Pin LQFP

L   Q   80221

| PACKAGE TYPE | TEMPERATURE RANGE | PART TYPE |

L = Low Profile Quad
     Flat Pack

Q – 0°C to +70°C

100 Base-TX/10 Base-T
Ethernet Media Interface Adapter

Revision History

2/20/97

- 2/20/97 initial release.

6/30/97

6/30/97 Document Revision changed to MD400159/B

Page 2, Pin Configuration 80221 80 PQFP:
    - Pin #30 changed from NC to RPTR

Page 4, Table of Contents:
    - 3.25 Repeater Mode, has been added to Table of Contents.
    - All previous references to 3.25 have been changed to 3.26
    - Reference to 5.7 Return Loss has been removed.
    - All references to Sections 5.8, 5.9, 5.10, 5.11 etc. have been changed to 5.7, 5.8, 5.9, 5.11 etc.

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Revision History

Page 7, Pin Configuration continued:
- Pin Name PLED5 Description, all references to Transmit have been changed to Receive.
- Pin Name PLED4 Description, all references to Receive have been changed to Transmit.
- New reference to Pin #30 including Pin name, I/O and Description, has been added.

Page 8, Pin Description continued:
- 80 PQFP reference to Pin #30 has been deleted.

Page 9, Figure 1. 80220/80221 Block Diagram:
- Reference to RPTR[1] has been added.

Page 12, Table 1 80220 vs. 80221:
- Repeater Mode Pin has been added.

Page 13, Section 3.3.4 FBI - 100 Mbps:
- Paragraph 2 copy, ...RXD4, (4) CRS is asserted as long as the device is in the Link.... has been added.

Page 19, Section 3.9.4 TP Squelch, 10 Mbps:
- Reference to 75-250 nS has been changed to 50-250 nS.

Page 24, Section 3.13.9 Link Indication:
- Copy change, copy has been changed to...The PLED3 output is open drain with resistor pullup and can drive an LED from VCC; The PLED0 output has both pullup and pulldown driver transistors in addition to a weak pullup resistor, so it can drive an LED from either VCC or GND. Both PLED3 and PLED0 can also drive another digital input. Refer...

Page 25, Section 3.15.2 10 Mbps:
- Copy change, copy has been changed to...If either 3 consecutive link pulses or one SOI pulse indicates incorrect polarity on the TP receive input, ...
Section 3.16.3 Full Duplex Indication:
- Copy change, copy has been changed to...The PLED1 output has both pullup and pulldown driver transistors and a weak pullup resistor, ...
Section 3.17.2 10/100 Mbps Indication:
- Copy change, copy has been changed to...The PLED0 output has both pullup and pulldown driver transistors and a weak pullup resistor, ...
Section 3.18.1 Internal CRS Loopback:
- Copy change, copy has been changed to... in Link Fail State, and when the transmit disable bit is set in the MI serial port Configuration 1 register. In 10 Mbps mode, ...

Page 26, Section 3.18.2 Diagnostic Loopback:
- Copy addition, copy has been changed to...do not change. Diagnostic loopback mode can not be enabled when the FBI interface is selected.
Section 3.23 LED DRIVERS:
- First paragraph has changed to ...The PLED[5:2] outputs are open drain with a pullup resistor and can drive LED's tied to VCC. The PLED[1:0] outputs have both pullup and pulldown driver transistors with a pullup resistor, so PLED[1:0] can drive LED's tied to either VCC or GND.

Page 27, Table 5. LED Normal Function Definition:
- Columns PLED5 and PLED4 references to XMT and RCV have been switched, XMT is now RCV etc.
- Section 3.25 Repeater Mode has been added.
- Reference to Sections 3.25 have been changed to 3.26.

Page 28, Reference to Sections 3.25 have been changed to 3.26.
  Table 7. MI Register Bit Type Definition:
  - R/WS C Column, Write Cycle, Clears Itself After Operation Completed is now under Column Read Cycle.

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Revision History

Page 29, Figure 9 MI Serial Port Frame Timing Diagram:
- References to ST, OP, PHYAD, REGAD, TA, DATA have been changed to ST[1:0], OP[1:0], PHYAD[4:0], REGAD[4:0], TA[1:0], DATA[15:0], for both Write Cycle and Read Cycle.

Page 30, Reference to Sections 3.25 have been changed to 3.26.

Page 38, Table 14. MI Register 4 (AutoNegotiation Advertisement) Structure:
- Bit 4.15, reference to Note 1 has been added. Note 1. Next Page currently not supported.

Page 43, Table 19. MI Register 19 (Mask) Structure and Bit Definition:
- Def. 19.3, 19.2, 19.1 19.0 have been changed from 1 to 0.
- Read Writes to 19.3, 19.2, 19.1 19.0 have been changed from R/W to R.

Page 49, Section 5.4 TP TRANSMIT OUTPUT CURRENT SET:
- Copy change ...Where I_{Ref} = 33.4 mA (10 Mbps, STP) has been changed
  to I_{Ref} = 40.8 mA (10 Mbps, STP)
General:
- Section 5.7 Return Loss has been removed, all references to 5.8 have been changed to 5.7. All following references to 5.8, 5.9, 5.10 have been changed to 5.7, 5.8, 5.9 etc.

Page 51, Section 5.9.1 MII Based Repeaters:
- Paragraph 2 copy has been changed to ...For most repeaters, it is necessary to disable the internal CRS loopback. This ...
- New paragraph 3 and paragraph 4 have been added to section.
Section 5.9.2 Non_MII Based Repeaters:
- Paragraph 3 copy has been changed to ...For most repeaters, it is necessary to disable the internal CRS loopback. This ...
- New paragraph 4 have been added to section.

Page 54, Section 5.14 PROGRAMMABLE LED DRIVERS:
- Paragraph 1 has been changed to ...The PLED[5:0] outputs can all drive LED's tied to VCC as shown in Figures 11-13. In addition, PLED1 and PLED0 can drive an LED tied to GND as well as VCC.
- Paragraph 6 references to PLED[3:0] have been changed to PLED[5:0]
- Paragraph 7, Note that PLED3... has been changed to ...Note that PLED1 and PLED0 pins have both pullup and pulldown transistors. This...

Page 55, DC Electrical Characteristics:
- I_{IL} Conditions TRFAD1, T4LNK, has been changed to TRFAD[1:0], T4LNK, TPI±.
- New I_{IL} row has been added, Conditions = TRFADJ0, Unit = µA, and LIMIT (MAX) = ±10.
- I_{IL} Conditions MDA[4:0] LIMIT (MIN) has been changed from -6 to 4.
- I_{IL} Conditions MDA[4:0] LIMIT (TYP), has been made blank.
- I_{IL} Conditions TRFADJ1, T4LNK LIMIT (TYP), has been made blank.
- I_{IL} Conditions TRFADJ1, T4LNK LIMIT (MAX), has been changed from -50 to -120
- I_{IH} Conditions, All Except OSCIN, TRFADJ0, T4ADV, has been changed to All Except OSCIN, TRFADJ[1:0], T4ADV, TPI±
- New I_{IH} row has been added Conditions = TRFADJ1, Unit = µA, and LIMIT (MAX) = ±10.
- I_{IL} Conditions TRFADJ0, T4ADV LIMIT (TYP), has been made blank.
- I_{IL} Conditions TRFADJ0, T4ADV LIMIT (MAX), has been changed from 50 to 120.
- V_{OH} Conditions I_{OH} = 6 µA PLED[5:0], MDINT has been changed to I_{OH} = 4 µA PLED[5:2], MDINT.
- New V_{OH} row has been added LIMIT (MIN) = V_{CC} - 1.0, Unit = Volt, I_{OH} = 10 mA, PLED[1:0]
- I_{IL} Conditions TRFADJ0, has been changed to V_{IN} = GND, TRFADJ0
- I_{IL} Conditions MDA[4:0], has been changed to V_{IN} = GND, MDA[4:0]
- I_{IL} Conditions TRFADJ1, T4LNK, has been changed to V_{IN} = GND, TRFADJ1, T4LNK

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Revision History

Page 55, DC Electrical Characteristics:
- I_{IL} Conditions OSCIN, has been changed to V_{IN} = GND, OSCIN
- I_{IH} Conditions TRFADJ1, has been changed to V_{IN} = V_{CC}, TRFADJ1
- I_{IH} Conditions TRFADJ0, T4ADV, RPTR, has been changed to V_{IN} = V_{CC}, TRFADJ0, T4ADV, RPTR
- I_{IH} Conditions OSCIN, has been changed to V_{IN} = V_{CC}, OSCIN
- I_{CC} LIMIT (TYP) is now 170
- I_{CC} LIMIT (MAX) has been changed form 250 to 200
- I_{CC} Conditions Powerdown Mode row has been deleted
- New I_{SS} row, Conditions, Transmitting LIMIT (MAX) = 250, UNIT = mA
- New I_{SS} row, Conditions Powerdown Mode LIMIT (MAX) = 1, UNIT = mA.

Page 56, Twisted Pair Characteristics Transmit:
- T_{OV}, LIMIT (MIN) has been changed form 2.2 to 2.694
- T_{OV}, LIMIT (TYP) has been changed form 2.5 to 3.062
- T_{OV}, LIMIT (MAX) has been changed form 2.8 to 3.429

Page 57, Twisted Pair Characteristics Transmit (continued):
- T_{OV}, LIMIT (MIN) has been changed form 29.4 to 35.93
- T_{OV}, LIMIT (TYP) has been changed form 33.4 to 40.82
- T_{OV}, LIMIT (MAX) has been changed form 37.4 to 45.72

Page 58, Twisted Pair Characteristics Receive:
- R_{OCV}, LIMIT (TYP), has been changed from V_{CC} - 0.1 to $V_{CC}/3 \pm 0.5$
- R_{CMR}, LIMIT (TYP), has been changed from $V_{CC} \pm 1.0$ to $R_{OCV} \pm 0.25$

Page 59, 25 MHz Input/Output Clock Timing Characteristics:
- t_4 LIMIT (MAX) 10, Conditions is now 100 Mbps
- t_4 new row Conditions is 10 Mbps, LIMIT (MAX) = 20, UNIT = nS.

Page 60, Transmit Timing Characteristics:
- t_{17}, LIMIT (MAX) 40, Conditions is now 100 Mbps
- t_{17}, new row Conditions is 10 Mbps, LIMIT (MAX) = 400, UNIT = nS.
- t_{18}, LIMIT (MAX) 160, Conditions is now 100 Mbps
- t_{18}, new row Conditions is 10 Mbps, LIMIT (MAX) = 400, UNIT = nS.
- t_{18}, LIMIT (MAX) has been changed from 400 to 900

Page 63, Receive Timing Characteristics:
- t_{34}, LIMIT (MAX) has changed form 900 to 1000
- t_{37}, LIMIT (MIN) has changed from -50 to -80
- t_{37}, LIMIT (MAX) has changed from 50 to 80

Page 67, Figure 23. RX_EN Timing:
- Timing TX_EN has changed to TX_EN.
- Timing TX_EN has changed

Page 79, Figure LED Driver Timing:
- t_{97} reference end of t_{97} cycle is a falling edge.

Revision History

Page 81, Figure 33. MI Serial Port Timing:
- Reference to t_{104} now extends to MDC timing.
- MDIO (Read) and MDIO (Write), Timing labels have changed.
- MDIO (Write) Data 0 rising edge is now rising falling.

9/15/97

9/15/97 Document Revision changed to MD400159/C

General: All references to 80 pin PQFP have been changed to 64 LQFP.

General: All references to Pin 26 Configuration have been changed to R/J Configuration.

Page 2, 80 Pin Configuration illustration has been changed to 64 Pin Configuration illustration.

Page 5, 1.0 Pin Description
- All Pin Number references to 80 pin PQFP has been changed to 64 pin LQFP for this table.

Page 7, 1.0 Pin Description

- Pin Name $\overline{PLED}$ 5, Description, Programmable has been changed to Receive.
- Pin Name $\overline{PLED}$ 4, Description, Programmable has been changed to Transmit.

Page 23, Section 3.13.6 AutoNegotiation Status
- The MI serial port ... inTable 4. Copy has been deleted.

Page 24, Table 4 has been deleted.

Page 33, Table 9, MI Serial Port Register Map
- 4 AutoNegot. Advertisement, Def. Bits 3,2,1,0 have been changed from 0 to –.
- 16 Configuration Bit 9 has been changed to UNSCR_DIS
- 18 Status Output, Bit 5 has been changed to 0, Bit 4 has been changed to 0.

Page 37, Table 13, MI Register 3(PHY ID #2) Structure and Bit Definition
- Name, Manufacturer's Revision Number Definition has been changed from 0H to –H, all Def, have been
  changed from 0 to –.

Page 40, Table 16. MI Register 16 (Configuration 1) Structure and Bit Definition.
- Bit 16.9 Symbol is now UNSCR_DIS, Name is now, Unscrambled Idle Reception Disable.

- Bit 16.9 Definition has been changed to:
  - 1 = Disable AutoNegotiation with devices that
    transmit unscrambled idle on powerup and
    various instances

  - 0 = Enables AutoNegotiation with devices that
    transmit unscramblled idle on powerup and
    various instances

Page 42, Table 18 MI Register 18 (Status Output) Structure and Bit Definition
- Bit 18.4, and 18.5, Symbol is now blank, Name is now blank, Definition has been changed to Reserved.

Page 55, 6.0 Specifications
- Package Power Dissipation, (80220) has been changed from 2.2 Watt @ 70° C to 2.0 Watt @ 70° C.
- Package Power Dissipation (80221) has been deleted.

Page 58, Twisted Pair Characteristics, Receive
- R_{ST}, 100 Mbps, RLVL = 1, (MIN) has been changed from 100 to 60.
- R_{ST}, 100 Mbps, RLVL = 1, (MAX) has been changed from 300 to 200.
- R_{UT}, 100 Mbps, RLVL = 1, (MIN) has been changed from 60 to 20.
- R_{UT}, 100 Mbps, RLVL = 1, (MAX) has been changed from 180 to 90.

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Revision History

Page 83, 7.0 Ordering Information
- 7.2 80 Pin PQFP, has been changed to 64 LQFP

Page 90, 8.0 Surface Mount Packages
- 80 Pin PQFP Dimension Diagram has been changed to 64 Pin LQFP Dimension Diagram.

3/15/98

3/15/98 Document Revision changed to MD400159/D

Page 1: Features List, 64 PQFP has been changed to 64 LQFP

7/2/98

7/2/98 Document Revision changed to MD400159/E

Page 23: 3.13.6 AutoNegotiation Status, Copy Change ... AutoNegotiation status bits in both the MI serial port Status and Status Output registers... has been changed to   ... AutoNegotiation status bits in the MI serial port Status register ...

Page 33: Table 9. MI Serial Port Register Map
- 1 Status, x.6, has been changed from 0 to CAP_SUPR
- 19 Mask, x.5 has been changed from MASK ANEG_ST1 to 1
- 19 Mask, x.4 has been changed from MASK ANEG_ST2 to 1
- 19 Mask, x.3, x.2, x.1, x.0 have been changed from 1 RW 1 to 0 R 0
- 18 Status Output, x.5, x.4 have been changed from R/LT to R

Page 35: Table 11. MI Register 1 (Status) Structure and Bit Definition
- Bit 1.6 has been changed from 0 to CAP_SUPR

Page 37: Table 13. MI Register 3 (PHY ID#2) Structure and Bit Definition
- Symbol, Part 6,5,4,3,2,1 has been changed to Part 5,4,3,2,1,0
- Definition, $_H$ has been deleted.

Page 42: Table 18. MI Register 18 (Status Output) Structure and Bit Definition
- Bit 18.5 Symbol is now blank.
- Bit 18.4 Symbol is now blank.
- Bit 18.5, 18.4 Definition has been changed from Reserved to Reserved for Factory Use.
- Bit 18.5 and 18.4 have been changed from R/LT to 0 R/LT

Page 43: Table 19. MI Register 19 (Mask) Structure and Bit Definition
- Bits 19.5, and 19.4 have been changed to 1
- 19.5, and 19.4 Definition has been changed to Reserved. Must be Written to 1 or Left at Default for Normal Operation.

Page 46: Figure 11. Typical Network Interface Card Schematic using 80220
- Addition of 75 ohm resistor
- Reference 2KV has been added to capacitor

Page 47: Figure 12. Typical Switching Port Schematic Using 80220
- Addition of 75 ohm resistor
- Reference 2KV has been added to capacitor

Revision History

Page 48: Figure 13. Typical external PHY Schematic Using 80220
- Addition of 75 ohm resistor
- Reference 2KV has been added to capacitor

Page 58: Twisted Pair Characteristics Receive
- R_{UT}, Row Conditions, 100 Mbps, RLVL = 1 and 10 Mbps RLVL = 1 have been deleted
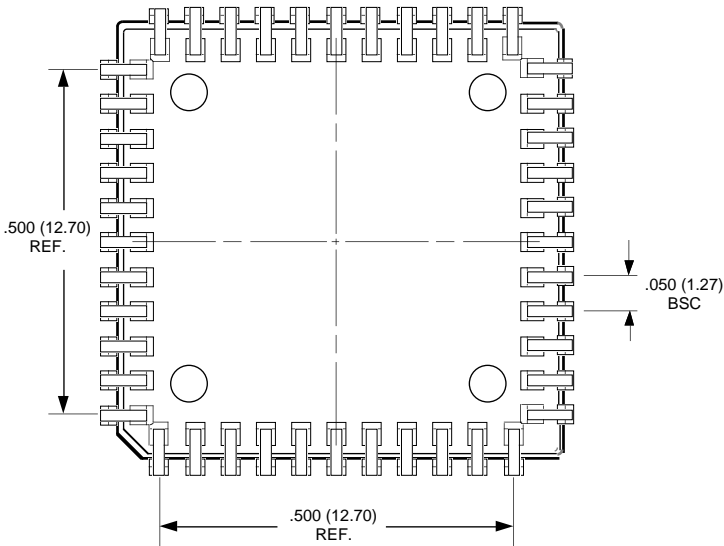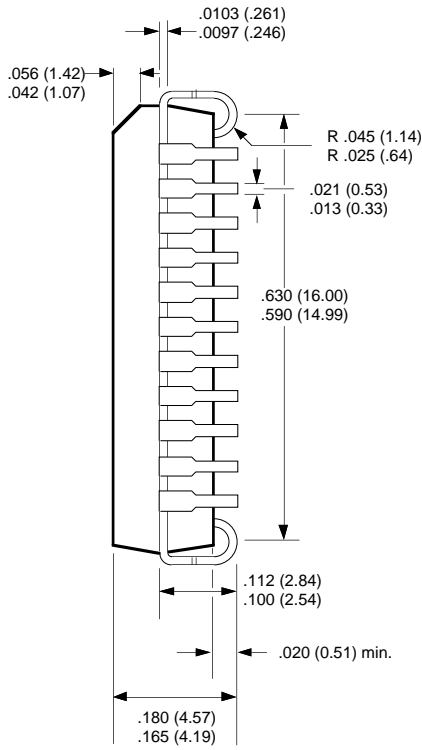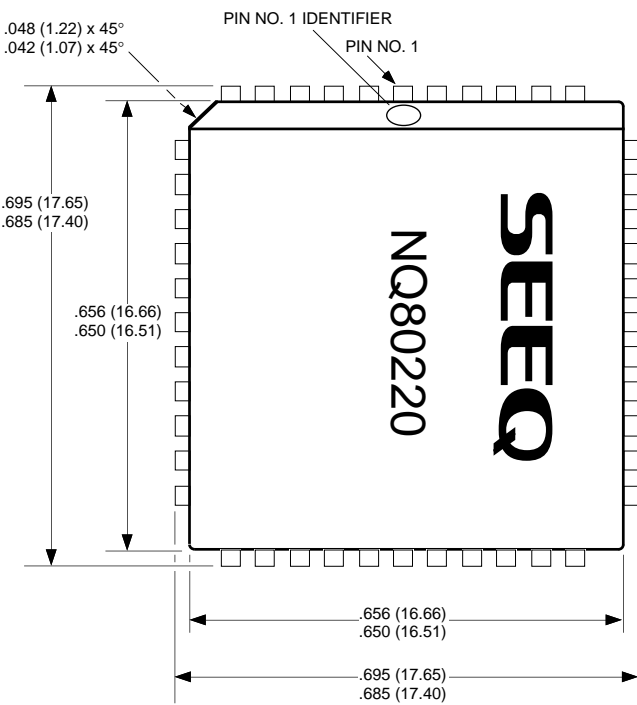
page 59: AC Test Timing Conditions
- 50 pF has been changed to 25 pF

Page 60: Transmit Timing Characteristics
- Symbol t_{15}, t_{19}, t_{21} (MIN) has been changed from 10 to 15.
- Symbol t_{15}, t_{19}, t_{21} Note 1 has been added to Conditions.

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8.0 Surface Mount Packages

8.1 44 Pin Plastic Leaded Chip Carrier

.048 (1.22) x 45°
.042 (1.07) x 45°

PIN NO. 1 IDENTIFIER
PIN NO. 1

.0103 (.261)
.0097 (.246)

.056 (1.42)
.042 (1.07)

R .045 (1.14)
R .025 (.64)

.021 (0.53)
.013 (0.33)

.695 (17.65)
.685 (17.40)

.656 (16.66)
.650 (16.51)

NQ80220

SEEQ

.630 (16.00)
.590 (14.99)

.656 (16.66)
.650 (16.51)

.695 (17.65)
.685 (17.40)

.112 (2.84)
.100 (2.54)

.020 (0.51) min.

.180 (4.57)
.165 (4.19)

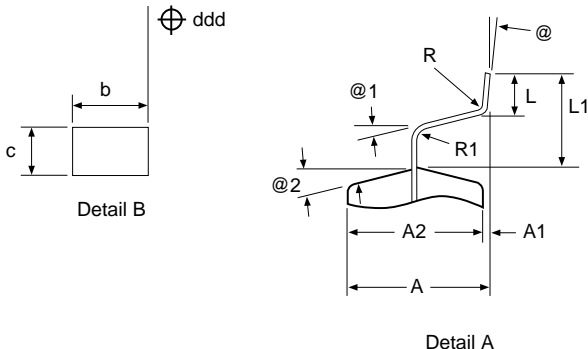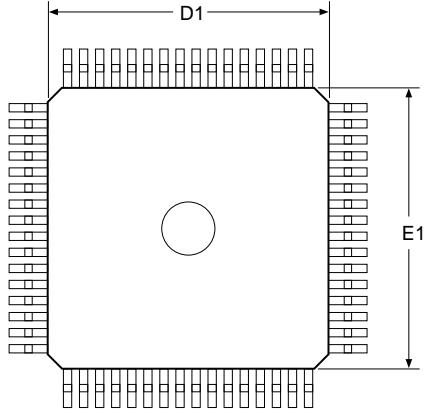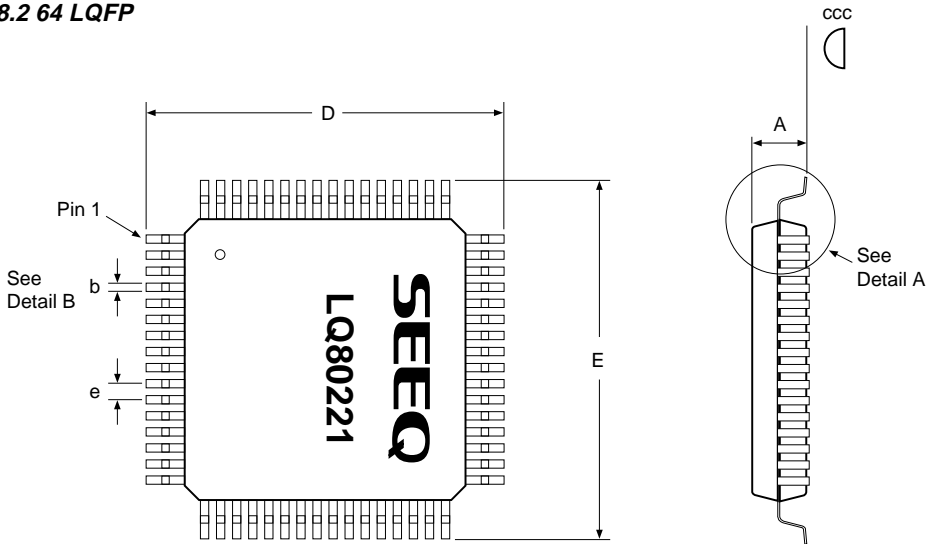.500 (12.70)
REF.

.050 (1.27)
BSC

.500 (12.70)
REF.

Notes
1. All dimensions are in inches and (millimeters).
2. Dimensions do not include mold flash. Maximum allowable flash is .008 (.20).
3. Formed leads shall be planar with respect to one another within 0.004 inches.

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8.0 Surface Mount Packages

8.2 64 LQFP

Dimension Table

Symbol	Dimensions
b	0.17 - 0.27
e	0.50 Basic
ccc	Max. 0.08
ddd	Max. 0.08
D	11.85 - 12.15
E	11.85 - 12.15
L	0.45 - 0.75
L1	1.0 Ref
R	0.08 - 0.20
R1	Min. 0.08
A	Max. 1.60
A1	0.05 - 0.15
A2	1.292 - 1.508
c	0.09 - 0.20
D1	9.90 - 10.10
E1	9.90 - 10.10
@	0° - 7°
@1	Min. 0°
@2	12°

Notes

1. All dimensions are in millimeters.
2. Dimensions do not include mold flash. Maximum allowable flash is 0.25.
3. All leads are coplanar to a tolerance of 0.08 (ccc). Bent leads to a tolerance of 0.08 (ddd).

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