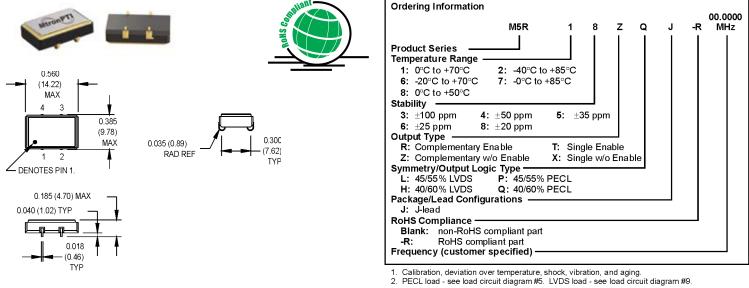
M5R Series

9x14 mm, 3.3 Volt, LVPECL/LVDS, Clock Oscillator





PARAMETER	Symbol	Min.	Тур.	Max.	Units	Condition/Notes
			1,75.			Conditional
		****			IVII IZ	
	Ts	-55	<u> </u>	+125	°C	
Ů.	∆F/F	(See Order	ina Inforn	nation)	_	See Note 1
. , ,		(
1st Year			+2	mag		
				1		
" , ,	Vicc	3 135		 	\ <u>\</u>	
		3.133	3.5		<u> </u>	0.75 to 24 MHz
1 LOL IIIpat Garrent	100					24 to 96 MHz
						96 to 800 MHz
LVDS Input Current	lcc			L		0.75 to 24 MHz
EVBO Inpat Garrent	100					24 to 800 MHz
Output Type				"	110 (PECL/LVDS
. ,,						See Note 2
		50 Ohms to Vcc -2 VDC 100 Ohm differential load				PECL Waveform
						LVDS Waveform
Symmetry (Duty Cycle)		(See Ordering Information)				@ Vcc-1.3 VDC (LVPECL)
		` '			@ 50% of waveform (LVDS)	
Output Skew				200	ps	PECL
Differential Voltage		250	340	450	mV	LVDS
Logic "1" Level	Voh	Vcc-1.02			V	PECL
Logic "0" Level	Vol			Vcc-1.63	V	PECL
Rise/Fall Time	Tr/Tf		0.35	0.55	ns	@ 20/80% LVPECL
			.50	1.0	ns	@ 20/80% LVDS
Enable Function		80% Vcc m				
		20% Vcc m	nax.: outp	ut disables to	high-Z	"R" & "T" output types
Start up Time			5		ms	
Phase Jitter	φJ					Integrated 12 kHz - 20 MHz
≥ 20 MHz			3	5	ps RMS	
	Thereafter (per year) Input Voltage PECL Input Current LVDS Input Current Output Type Load Symmetry (Duty Cycle) Output Skew Differential Voltage Logic "1" Level Logic "0" Level Rise/Fall Time Enable Function Start up Time Phase Jitter	Operating Temperature TA Storage Temperature Ts Frequency Stability ΔF/F Aging 1st Year Thereafter (per year) Input Voltage Vcc PECL Input Current Icc LVDS Input Current Icc Output Type Load Symmetry (Duty Cycle) Vol Output Skew Differential Voltage Logic "1" Level Voh Logic "0" Level Vol Rise/Fall Time Tr/Tf Enable Function Start up Time Phase Jitter φ J	Operating Temperature Storage Temperature Ts -55 Frequency Stability Aging 1st Year Thereafter (per year) Input Voltage Vcc 3.135 PECL Input Current Icc LVDS Input Current Icc Output Type Load Symmetry (Duty Cycle) Output Skew Differential Voltage Logic "1" Level Logic "0" Level Rise/Fall Time Phase Jitter VaF/F (See Order Ts -55 (See Order Ta -5 (See Order Ta -5 (See Order Ta -5 (S	Operating Temperature TA (See Ordering Information of Storage Temperature) Storage Temperature Ts -55 Frequency Stability ΔF/F (See Ordering Information of Start up Time) Aging 1st Year Thereafter (per year) ±2 ±1 Input Voltage Vcc 3.135 3.3 PECL Input Current Icc Icc LVDS Input Current Icc Icc Output Type Icc Icc Load 50 Ohms to Vcc -2 Voleton of Start up Time (See Ordering Information of Start up Time) Output Skew Icc Icc Differential Voltage 250 340 Logic "0" Level Vol Vcc-1.02 Rise/Fall Time Tr/Tf 0.35 .50 Soo Vcc min. Or N/C 20% Vcc max.: outp Start up Time 5	Operating Temperature TA (See Ordering Information) Storage Temperature Ts -55 +125 Frequency Stability ΔF/F (See Ordering Information) Aging ±2 ppm 1st Year ±1 ppm Input Voltage Vcc 3.135 3.3 3.465 PECL Input Current Icc 60 95 105 LVDS Input Current Icc 30 60 Output Type Image: Specific	Operating Temperature TA (See Ordering Information)

- 1. Calibration, deviation over temperature, shock, vibration, and aging.
- 2. PECL load see load circuit diagram #5. LVDS load see load circuit diagram #9.

MAX 4 3 0.385 (9.78) MAX 0.035 (0.89) PAD RE
0.185 (4.70) MAX 0.040 (1.02) TYP 0.018 0.018 (0.46) TYP
0.200 (5.08) TYP All dimensions in inches (mm).
SUGGESTED SOLDER PAD LAYOUT 0.200 (5.08) 0.050 (1.27) 0.346 (8.80) 0.118 (3.00)
OPTIONAL 6-PIN PACKAGE WITH TRISTATE
+ + + 0.100 (2.54) + + + +

Pin Connections

4 Pin

2

3

4

6 Pin

1

3

4

5

6

FUNCTION

Enable Ground/Cover

Output Q

N/C

+Vcc

N/C or Output Q

MtronPTI reserves the right to make changes to the product(s) and service(s) described herein without notice	ce. No liability is assumed as a	result of their use or application.
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