ASI4U

Universal Actuator-Sensor Interface IC

Datasheet

Features

- Universal application in AS-i Slave, Master, Repeater and Bus-Monitor components
- Support of AS-i Complete Specification V3.0, including all optional features
  - Synchronous Data I/O Mode
  - 4 Input / 4 Output operation in Extended Address Mode
  - User write protection for Extended ID-Code 1
  - Multiplexed Parameter Port
- Special AS-i Safety Mode
- Floating AS-i Transmitter and Receiver for high symmetrical high power applications
- On chip electronic inductor with current drive capability of 55mA
- Configurable LED outputs supporting all status indication modes defined by AS-i Complete Specification V3.0
- Several data preprocessing functions, including configurable data input filters and bit selective data inverting
- Improved additional addressing channel for easy module setup
  - IR and CMOS input mode
  - Activation by magic sequence
- Support of 8 / 16 MHz crystals by automatic frequency detection
- Clock Watchdog for high System Security
- Pin and function compatible to A²SI

Description

ASI4U is a monolithic CMOS integrated circuit certified for AS-i (Actuator Sensor Interface) networks. AS-i networks are used for industrial automation.

AS-i is designed for easy and simple interconnection of binary sensors and actuators. It uses a two-wire unshielded cable to transport power and information.

ASI4U is a direct successor of the A²SI IC and can replace the A²SI in existing board layouts.

AS-i Safety applications can use the special AS-i Safety Mode if fault reaction time is a concern.

The device is available in SSOP28 package.

Application Support

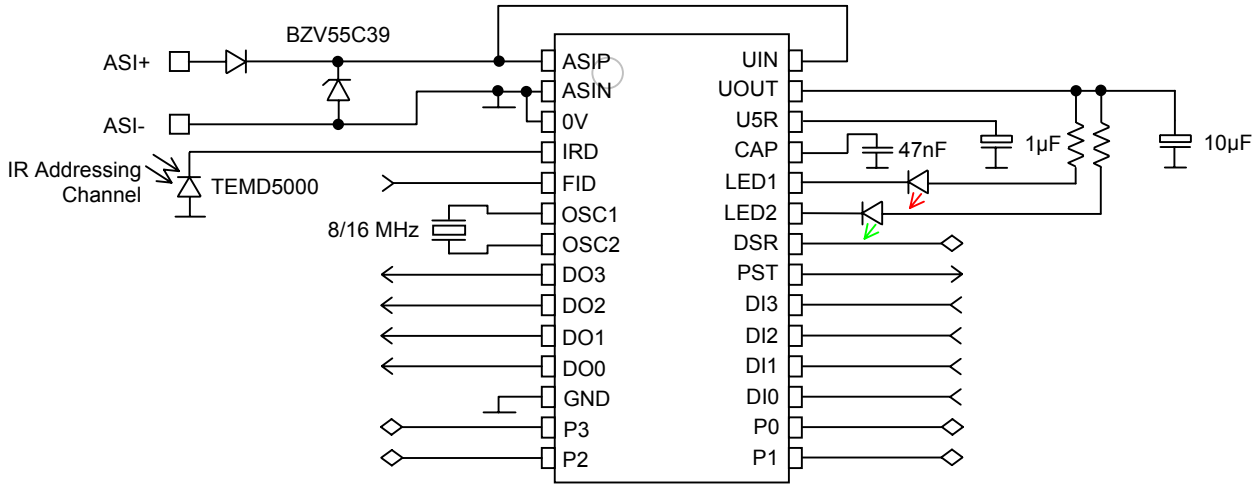
Configuration of the chip is handled through programming of the on-chip E²PROM.

ZMD provides a special

AS-Interface Programmer Tool
(Ordering Code: ZMD ASI-Programmer)

to ease product evaluation and selection of different operation modes.

Further application support is available through the e-mail hotline asi@zmd.de



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0 Read this First

SAFETY-ADVICE

0.1 Important Notice

Products sold by ZMD are covered exclusively by the warranty, patent indemnification and other provisions appearing in ZMD standard "Terms of Sale". ZMD makes no warranty (express, statutory, implied and/or by description), including without limitation any warranties of merchantability and/or fitness for a particular purpose, regarding the information set forth in the Materials pertaining to ZMD products, or regarding the freedom of any products described in the Materials from patent and/or other infringement. ZMD reserves the right to discontinue production and change specifications and prices of its products at any time and without notice. ZMD products are intended for use in commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment, are specifically not recommended without additional mutually agreed upon processing by ZMD for such applications.

ZMD reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

0.2 ASI-Safety Applications

The ASI4U is designed to allow replacement of A²SI ICs in existing board layouts and applications. However, since the ASI4U provides additional data preprocessing functions at the data input channel, the fault reaction time of an AS-i Safety module could increase by 40ms if some of the new features become activated by intention, by accident or hardware fault.

ZMD strongly recommends the use of the new ASI4U Safety-Mode, if the ASI4U shall replace the A²SI in existing ASI-Safety designs. Only then, the same fault reaction times as with the A²SI are guaranteed. For compatibility with the modified data input routing in Safety Mode, the user has to adapt the safety code table stored in the external micro controller. Only such Safety Code Sequences that contain the value **1110** are permitted.

If the IC is operated in Safety Mode, the user must pay special attention that the *Synchronous Data I/O Mode* as well as the *Data Input Filters* remain disabled by appropriate E²PROM configuration.

Application of the ASI4U in Standard Mode (no Safety Mode enabled) for AS-i Safety products is basically possible, if an additional Fault Reaction Time of 40ms is taken into account.

The user shall also obey the additional security advice regarding "Production and Repair of AS-i Safety Slaves" that is available as an additional document form the ZMD web page www.zmd.biz .

0.3 Repair of ASI-Safety Modules

If an A²SI based ASI-Safety Module shall be repaired, it is **explicitly prohibited** to replace the A²SI IC with the newer ASI4U IC. This is to exclude safety relevant deviations of module properties that can result from the different data input paths an the above mentioned possible increase in Fault Reaction Time.

The user shall also obey the additional security advice regarding "Production and Repair of AS-i Safety Slaves" that is available as an additional document form the ZMD web page www.zmd.biz .

1 General Device Specification

1.1 Absolute Maximum Ratings (Non Operating)

Table 1: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
V_{0V}, V_{GND}	Voltage reference	0	0	V	
$V_{ASIP-ASIN}$	Voltage difference between ASIP and ASIN (V_{ASIP} - V_{ASIN})	-0.3	40	V	1
$V_{ASIP-ASIN\_P}$	Pulse voltage between ASIP and ASIN (V_{ASIP} - V_{ASIN})	-0.3	50	V	2
V_{ASIP}	Pulse voltage between ASIP and 0V (V_{ASIP} – V_{0V})	-0.3	50	V	2, 3
V_{ASIN}	Voltage between ASIN and 0V (V_{ASIN} – V_{0V})	-6.0	6.0	V	3
V_{UIN}	Power supply input voltage	-0.3	40	V	
V_{UIN_P}	Pulse voltage at power supply input	-0.3	50	V	2
$V_{inputs1}$	Voltage at pins DI3 ... DI0, DO3 ... DO0, P3 ... P0, DSR, PST, LED1, LED2, FID, IRD, UOUT	-0.3	V_{UIN} + 0.3	V	
$V_{inputs2}$	Voltage at pins OSC1, OSC2, CAP, U5R	-0.3	7	V	
I_{in}	Input current into any pin except supply pins	-50	50	mA	4
H	Humidity non-condensing				5
V_{HBM1}	Electrostatic discharge – Human Body Model (HBM1)	3500		V	6
V_{HBM2}	Electrostatic discharge – Human Body Model (HBM2)	2000		V	7
V_{EDM}	Electrostatic discharge – Equipment Discharge Model (EDM)	400		V	8
θ_{STG}	Storage temperature	-55	125	°C	
P_{tot}	Total power dissipation		0.85	W	9
R_{thj}	Thermal resistance of SSOP 28 package	40	80	K/W	10

1 reverse polarity protection has to be performed externally

2 pulse with ≤ 50µs, repetition rate ≤ 0.5 Hz

3 $V_{ASIP-ASIN}$ and $V_{ASIP-ASIN\_P}$ must not be violated

4 Latch-up resistance, reference pin is 0V

5 Level 4 according to JEDEC-020A is guaranteed

6 HBM1: C = 100pF charged to V_{HBM1} with resistor R = 1.5kΩ in series, valid for ASIP-ASIN only.

7 HBM2: C = 100pF charged to V_{HBM2} with resistor R = 1.5kΩ in series, valid for all pins except ASIP-ASIN

8 EDM: C = 200pF charged to V_{EDM} with no resistor in series, valid for ASIP-ASIN only

9 at max. operating temperature, the allowed total power dissipation depends on additional thermal resistance from package to ambient and on the operation ambient temperature as shown in Figure 1.

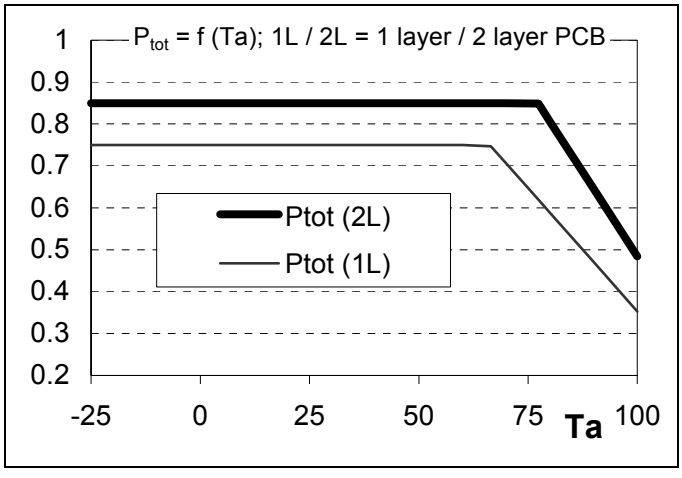

Figure 1: Ptot = f(θ_a)

10 Single layer board, P_{tot} = 0.5W; air velocity = 0m/s ⇒ max. value; air velocity = 2.5m/s ⇒ min. value

1.2 Operating Conditions

Table 2: Operating Conditions

Symbol	Parameter	Min	Max.	Unit	Note
V_{UIN}	Positive supply voltage for IC operation	16	33.1	V	1
V_{0V}, V_{GND}	Negative supply voltage	0	0	V	
V_{ASIP}	DC voltage at ASIP relating to V_{0V}	16	33.1	V	2
V_{ASIN}	DC voltage at ASIN relating to V_{0V}	-4	4	V	2
I_{UIN}	Operating current at V_{UIN} = 30V		6	mA	3
I_{CL1}	Max. output sink current at pins DO3...DO0, DSR		10	mA	
I_{CL2}	Max. output sink current at pins P0...P3, PST		10	mA	
θ_{amb}	Ambient temperature range, operating range	-25	85	°C	

[1] DC-Parameter: $V_{UINmin} = V_{UOUTmin} + V_{DROPmax}$

$V_{UINmax} = V_{UOUTmax} + V_{DROPmin}$

Below V_{UINmin} the power supply block may not be able to provide the specified output currents at UOUT and U5R.

[2] Outside of these limits the send current shape and send current amplitude cannot be guaranteed.

[3] f_c = 8.000 MHz, no load at any pin, transmitter turned off, digital state machine is in idle state

Table 3: Crystal Frequency

Symbol	Parameter	Nom.	Unit	Note
f_c	Crystal frequency	8.000/16.000	MHz	4

[4] The IC automatically detects whether the crystal frequency is 8.000MHz or 16.000MHz and controls the internal clock circuit accordingly. The frequency detection is locked as soon as one AS-i telegram was correctly received **at any input channel**. It can be reset by Power On Reset only.

Note: In Slave Mode the locking occurs if a Master Call was received. In Master-/ Repeater-/Monitor Mode a Master Call or a Slave Response that was received on any input channel, triggers the frequency locking.

The ASI4U supports an integrated clock watchdog. If no crystal or clock oscillation is recognized for 150µs the IC generates a RESET event until clock oscillation is available.

More detailed oscillator pin definitions can be found in chapter 3.10 on page 41.

1.3 Quality Standards

The quality of the IC will be ensured according to the ZMD quality standards. Functional device parameters are valid for device operating conditions specified in chapter 1.2. Production device tests are performed within the recommended ranges of V_{ASIP} - V_{ASIN}, V_{IN} - V_{0V}, θamb = + 25°C (+ 85°C and - 25°C on sample base only) unless otherwise stated.

1.4 Package Pin Assignment

Table 4: *ASI4U* Pin List

Package pin number	Name	Direction	Type	Description
1	ASIP	IN	Analog	AS-i Transmitter/Receiver input, to be connected to ASI+ lead of AS-i cable, via reverse polarity protection diode
2	ASIN	OUT	Analog	AS-i Transmitter/Receiver output, to be connected to ASI- lead of AS-i cable
3	0V		SUPPLY	IC Ground Common ground for all IC ports except ASIP/ASIN, To be connected to ASIN if no external coils are used
4	IRD	IN	Analog / CMOS (5V)	Addressing Channel input
5	FID	IN	Pull-up	Periphery Fault input
6	OSC2	OUT	Analog (5V)	Crystal oscillator
7	OSC1	IN	Analog / CMOS (5V)	Crystal oscillator / External clock input
8	DO3	OUT	Open Drain	Data port output D3
9	DO2	OUT	Open Drain	Data port output D2
10	DO1	OUT	Open Drain	Data port output D1
11	DO0	OUT	Open Drain	Data port output D0
12	GND		SUPPLY	Digital I/O ground, to be connected with 0V
13	P3	I/O	Pull-up/Open Drain	Parameter port P3
14	P2	I/O	Pull-up/Open Drain	Parameter port P2 / Receive Strobe output in Master Mode
15	P1	I/O	Pull-up/Open Drain	Parameter port P1 / Power Fail output in Master Mode
16	P0	I/O	Pull-up/Open Drain	Parameter port P0 / Data Clock output in Master Mode
17	DI0	IN	Pull-up	Data port input D0
18	DI1	IN	Pull-up	Data port input D1
19	DI2	IN	Pull-up	Data port input D2
20	DI3	IN	Pull-up	Data port input D3
21	PST	I/O	Pull-up/Open Drain	Parameter Strobe output (input function used for IC test purposes only)
22	DSR	I/O	Pull-up/Open Drain	Data Strobe output / Reset input

Package pin number	Name	Direction	Type	Description
23	LED2	OUT	Open Drain	LED output "Enhanced Diagnosis", to be activated by *LED2_Active* bit in the Firmware region of the E²PROM
24	LED1	I/O	Pull-up/Open Drain	LED output "AS-i-Diagnosis" / Addressing channel output (input function used for IC test purposes only)
25	CAP	I/O	Analog	Filter control (Electronic Inductor)
26	U5R	OUT	Analog	Regulated internal/external 5V supply
27	UOUT	OUT	Analog	Decoupled Actuator/Sensor supply
28	UIN		SUPPLY	Power supply input

All open drain outputs are NMOS based. Pull-up properties at input stages are achieved by current sources referring to U5R.

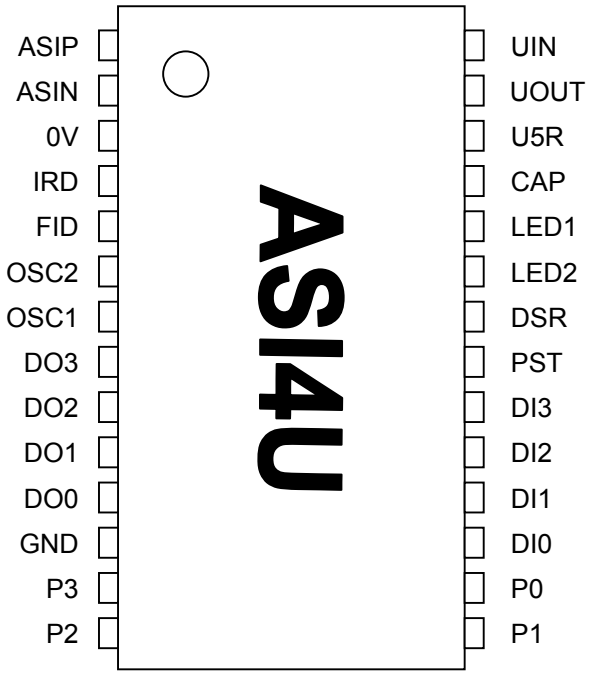

Figure 2: *ASI4U* Package Pin Assignment

2 Basic Functional Description

2.1 Functional Block Diagram

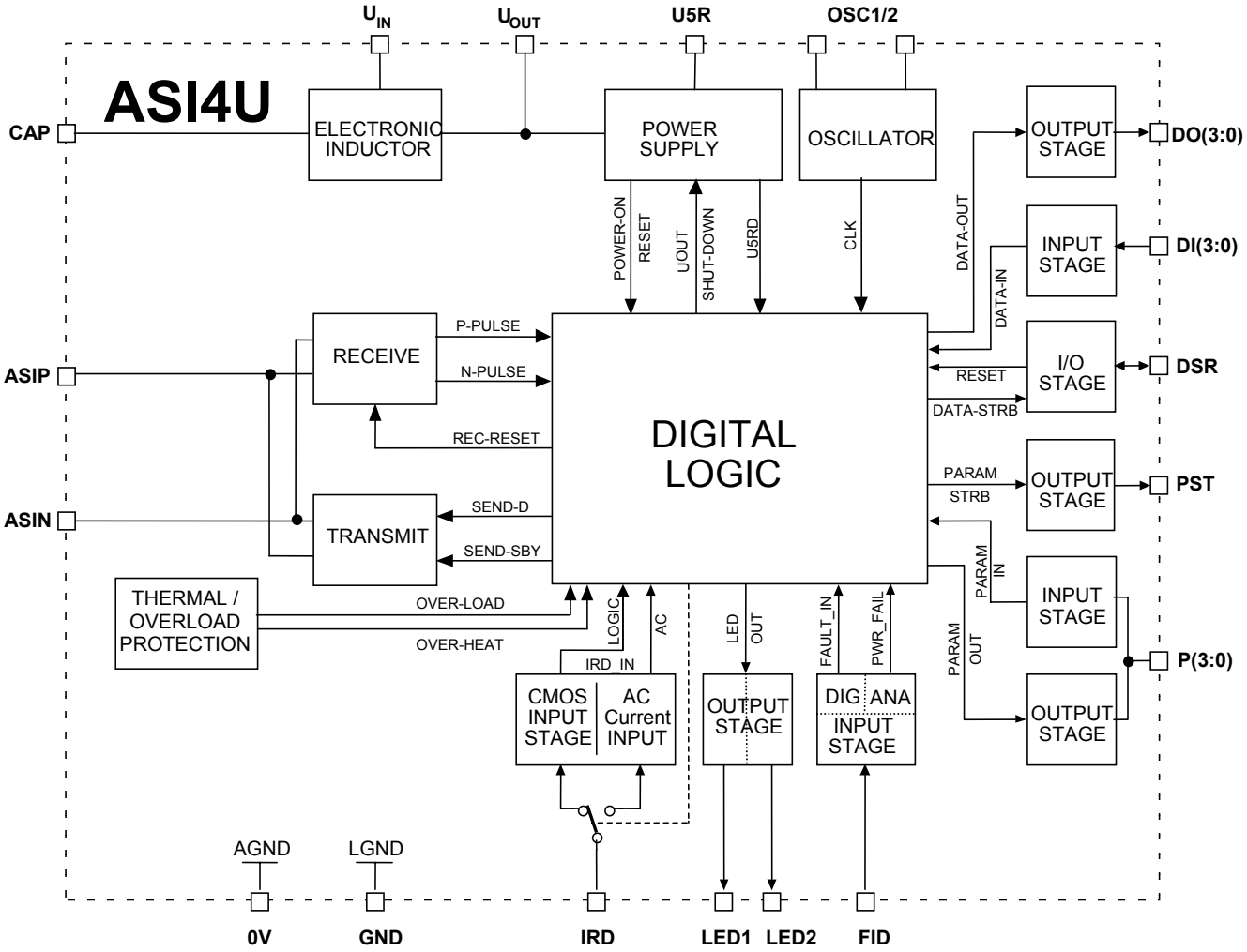

Figure 3: Functional Block Diagram

Following device functions are associated with the different blocks of the IC:

RECEIVE

The receive block converts the analog telegram waveform from the AS-i bus to a digital pulse coded signal that can be processed further by a digital UART circuit.

The RECEIVE block is directly connected to the AS-i line pins ASIP and ASIN. It converts the differential AS-i telegram to a single ended signal and removes the DC offset by high pass filtering. To adapt quickly on changing signal amplitudes in telegrams from different network users, the amplitude of the first telegram pulse is measured by a 3 bit flash ADC and the threshold of a positive and a negative comparator is set accordingly to about 50% of the measured level. The comparators generate the P-Pulse and N-Pulse signals.

TRANSMIT

The transmit block transforms a digital response signal to a correctly shaped send current signal which is applied to the AS-i bus. Due to the inductive network behavior of the network the changing send current induces voltage pulses on the network line that overlay the DC operating voltage. The voltage pulses shall have sin²-wave shapes. Hence, the send current shape must follow the integral of the sin²-wave function.

DIGITAL LOGIC

The digital logic block contains UART, Main State Machine, E²PROM memory and other control logic. E²PROM write access and other I/O operations of the Main State Machine are supported in Slave Mode only (see description of general IC operational modes below). In Master Mode the IC is basically equivalent to a physical layer transceiver.

If Slave Mode is activated, the UART demodulates the received telegrams, verifies telegram syntax and timing and controls a register interface to the Main State Machine. After reception of a correct telegram, the UART generates appropriate Receive Strobe signals, that tell the Main State Machine to start further processing. The Main State Machine decodes the telegram information and starts respective I/O processes or E²PROM access. A second register interface is used to send data back to the UART for construction of a telegram response. The UART modulates the response data into a Manchester-II-coded bit stream that is used to control the TRANSMIT unit.

ELECTRONIC INDUCTOR

The electronic inductor is basically a gyrator circuit. It provides an inductive behavior between the IC pins UIN and UOUT while the inductance is controlled by the capacitor on pin CAP. The inductor shall decouple the power regulator of the IC as well as the external load circuit from the AS-i bus and hence prevent cross talk or switching noise from disturbing the telegram communication on the bus.

The AS-i Complete Specification describes the input impedance behavior of a slave module by an equivalent circuit that consists of R, L and C in parallel. For example, a slave module in Extended Address Mode shall have R > 13.5 kOhm, L > 13.5 mH and C < 50pF. The electronic inductor of the ASI4U delivers values that are well within the required ranges for output currents up to 55mA. More detailed parameters can be found in chapter 3.17.2.

The electronic inductor requires an external capacitor of 10µF at pin UOUT for stability.

POWER SUPPLY

The power supply block consists of a bandgap referenced 5V-regulator as well as other reverence voltage and bias current generators for internal use. The 5V regulator requires an external capacitor at pin U5R of at least 1µF for stability. It can source up to 4mA for external use, however the power dissipation and the resulting device heating become a major concern, if too much current is drawn from the regulator.

OSCILLATOR

The oscillator supports direct connection of 8.000 MHz or 16.000 MHz crystals with a dedicated load capacity of 12pF and parasitic pin capacities of up to 8pF. The IC automatically detects the oscillation frequency of the connected crystal and controls the internal clock generator circuit accordingly.

After power-on reset the IC is set to 16.000 MHz operation by default. After about 200µs it will either switch to 8.000 MHz operation or remain in the 16.000 MHz mode. The frequency detection is active until the first AS-i telegram was successfully received in order to make sure the IC found the correct clock frequency setting. The detection result is locked thereafter to increase resistance against burst or other interferences.

The oscillator unit also contains a clock watch dog circuit that can generate an unconditioned IC reset if there was no clock oscillation for more than about 20µs. This is to prevent the IC from unpredicted behavior if no clock signal is available anymore.

THERMAL / OVERLOAD PROTECTION

The IC is self protected against thermal overheating and short circuiting of pin UOUT towards IC ground.

If the silicon die temperature rises above around 140°C for more than 2 seconds, the IC detects thermal overheating, switches off the electronic inductor, performs an IC reset and sets all analog blocks to power down mode. The 5V-regulator is of course also turned off in this state, however, there will still remain a voltage of about 3 … 3.5V available at U5R that is derived from the internal start circuitry. The overheat protection state can only be left by power-cycling the AS-i voltage.

Shortcutting pin UOUT towards IC ground leads to the same IC behavior as thermal overheating.

IRD CMOS / AC CURRENT INPUT

The IRD pin is input for the additional addressing channel in Slave Mode (see description of General IC Operational Modes below) or direct AS-i transmitter input in Master Mode. In Slave Mode it can be operated either in CMOS Mode or AC-current input mode. The later is provided for direct connection of a photo diode. More detailed information can be found in

	chapter *3.3 Addressing Channel Input IRD*.
FID DIGITAL / ANALOG STAGE	Pin FID can be set to digital CMOS mode or analog voltage input mode. In Slave Mode it is set to CMOS operation, in Master Mode it works in analog mode and acts as input for the power fail comparator.
INPUT STAGE	All digital inputs, except of the oscillator pins, have high voltage capabilities and partly Schmitt-Trigger and Pull-Up features. For more details see chapter *3.4 Digital Inputs - DC Characteristics*.
OUTPUT STAGE	All digital output stages, except of the oscillator pins, have high voltage capabilities and are implemented as NMOS open drain buffers. Each pin can sink up to 10mA of current.

2.2 General Operational Modes

The ASI4U provides two main and two additional sub operational modes. Main operation modes divide in Slave Mode and Master Mode. Sub operation modes divide in Repeater Mode and Monitor Mode. The later were derived from Master Mode in providing different output signals at the Parameter Port.

A definition of which operational mode becomes active is made by programming the flags *Master_Mode* and *Repeater_Mode* in the *Firmware Area* of the E²PROM (see also Table 7 on page 18). The E²PROM is read out at every initialization of the IC. Online mode switching is not provided. The following configurations apply:

Table 5: Assignment of operational modes

Selected Operational Mode	Master Mode Flag	Repeater Mode Flag
Slave Mode	0	0
Master Mode	1	0
Repeater Mode	1	1
Monitor Mode	0	1

In Slave Mode the ASI4U operates as fully featured AS-i Slave IC according to AS-i Complete Specification v3.0.

In Master Mode the ASI4U translates a digital output signal from the master control logic (etc. PLC, µP, …) to a correctly shaped, analog AS-i pulse sequence and vice versa. Every AS-i telegram received is checked for consistency with the AS-i communication protocol specifications and if no errors were found, an appropriate receive strobe signal is generated.

Master Mode and Monitor Mode differ in the kind of signaled telegrams. In Master Mode a single Receive Strobe signal is provided validating every correctly received Slave Response while in Monitor Mode two different Receive Strobe signals are available displaying every correctly received Master and Slave telegram separately. The Monitor Mode is intended for use in intelligent slaves and bus monitors that provide own telegram decoding mechanisms but do not check for correct telegram timing or syntax.

The Repeater Mode is specifically provided for AS-i bus repeater applications.

2.3 Slave Mode

The Slave Mode is probably the most complex operational mode of the IC. The ASI4U does not only support all mandatory AS-i Slave functions but also a variety of additional features that shall make AS-i Slave module design very easy and flexible.

2.3.1 AS-i communication channel

In slave mode the ASI4U can work on two different communication channels, the AS-i channel and the IRD channel. The AS-i channel is directly connected to AS-i Bus via the pins ASIP and ASIN. A receiver and a transmitter unit are connected in parallel to the pins that allow fully bi-directional communication through ASIP and ASIN.

The ASI4U is the first IC that supports floating operation of the AS-i receiver and transmitter (within certain limits) in relation to IC ground. Thus far, the ASIN pin always had to be on the same potential like IC ground, preventing full symmetrical input circuits with external coils. The following figures illustrate the new functionality. If one compares the relation Z1 / Z2, which is a measure for symmetry of the AS-i module input towards machine ground, it becomes obvious that the new circuit is more symmetrical since Z1 and Z2 are more equal than in the conventional solution. Please note, that this is not a complete application circuit.

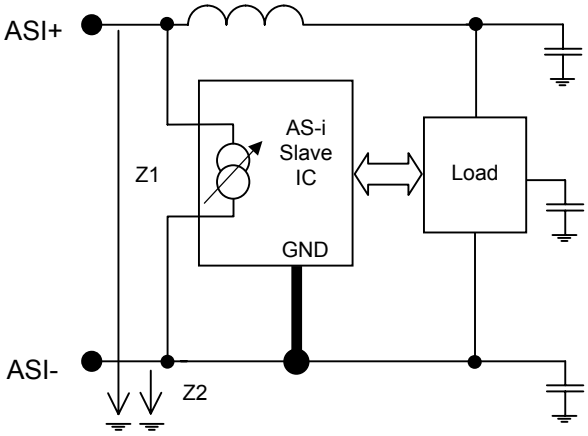

Figure 5: Conventional application of AS-i IC with one external coil

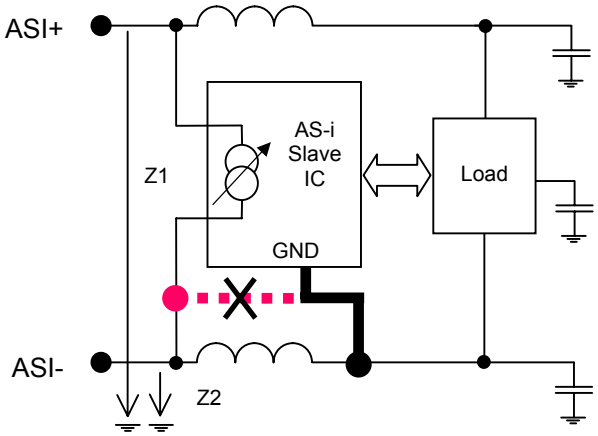

Figure 4: Newly supported application of AS-i IC with two external coils

2.3.2 IRD communication channel

Besides the AS-i communication channel the ASI4U can also operate on a second input channel, the so called IRD Input Channel or Addressing Channel. In this mode the IRD pin is input for an AS-i signal in Manchester-II-coded format. The signal can either be an AC-current signal generated by a photo diode or a 5V-CMOS signal. The IC automatically detects the type of the signal and switches the input path accordingly.

Output pin in IRD communication mode is LED1. It transmits the slave response as inverted Manchester-II-coded AS-i signal. The red LED, which is normally connected to LED1, can form the response transmitter in an optical communication system or LED1 can be directly connected to some external circuitry.

Activation of the IRD communication channel is achieved by a so called magic sequence, that is sent in advance of the desired communication. The construction of a magic sequence is described in detail in chapter *3.3 Addressing Channel Input IRD* on page 22. The IRD communication mode is basically left by IC reset, except in one special case that is also described in that chapter.

2.3.3 Parameter Port Pins

The ASI4U features a 4-bit wide parameter port and a related parameter strobe signal pin PST. There is a defined phase relation between a parameter output event, the parameter input sampling and the activation of the PST signal. Thus it can be used to trigger external logic or a micro controller to process the received parameter data or to provide new input data for the AS-i slave response.

AS-i Complete Specification V3.0 newly defines a bidirectional mode for parameter data. The ASI4U supports this feature, that can be activated by special E²PROM setting.

See chapter *3.6 Parameter Port and PST* on page 26 for further details.

2.3.4 Data Port Pins

An important feature of the ASI4U is the 8-bit wide data port that consists of a 4-bit wide input section and a 4-bit wide output section. The input and output sections work independently from each other allowing a maximum of 8 devices (4 input and 4 output devices) to be connected to the ASI4U. For special applications (compatibility), the so called Multiplex Mode can be activated that limits the output activation to a certain time frame. Thus, a 4-bit wide bi-directional data I/O Port can be realized by external connection of the corresponding data input and output pins.

The data port is accompanied by the data strobe signal DSR. There is a defined phase relation between a data output event, the input data sampling and the activation of the DSR signal. Thus, it can be used to trigger external logic or a micro controller to process the received data or to provide new input data for the AS-i slave response. See chapter *3.7 Data Port and DSR* on page 29 for further details.

2.3.5 Data Input Inversion

By default the logic signal (HIGH / LOW) that is present at the data input pins during the input sampling phase is transferred without modification to the send register, which is interfaced by the UART. By that, the signal becomes directly part of the slave response.

Some applications work with inverted logic levels. To avoid additional external inverters, the input signal can be inverted by the ASI4U before transferring it to the send register. The inversion of the input signals can either be done bit selective or jointly for all data input pins. See chapter *3.7.2 Input Data Pre-Processing* on page 30.

2.3.6 Data Input Filtering

To prevent input signal bouncing from being transferred to the AS-i Master, the data input signals can be digitally filtered. Filter times can be configured in 7 steps from 128µs up to 8.192ms. Additionally there is a so called AS-i Cycle Mode available. If activated, the filter time is determined by the actual AS-i cycle time. For more detailed information refer to chapter *3.7.2 Input Data Pre-Processing* on page 30.

The filter function can be enabled bit selective. Activation of the filters is done jointly either by E²PROM configuration or by the logic state of parameter port pin P2. See chapter *3.7.2 Input Data Pre-Processing* on page 30.

2.3.7 Fixed Data Output Driving

The fixed data output driving feature is thought to ease board level design for similar products that do not require the full data output port width. The user can select one or more bits from the data output port to be driven by a distinct logic level instead by the data that was sent by the master. The distinct output data is stored in the E²PROM and can be set during final module configuration. Thus it is possible to signal the actual IC profile to some external circuitry and to allow reuse of certain board designs for different product applications.

See chapter *3.7.3 Fixed Output Data Driving* on page 32 for further details.

2.3.8 Synchronous Data I/O Mode

AS-i Complete Specification V3.0 newly defines a synchronous data I/O feature, that allows a number of slaves in the network to switch their outputs at the same time and to have their inputs sampled jointly. This feature is especially useful if more than 4-bit wide data is to be provided synchronously to an application.

The synchronization point was defined to the data exchange event of the slave with the lowest address in the network. This definition relies on the cyclical slave polling with increasing slave addresses per cycle that is one of the basic communication principles of AS-i. The IC always monitors the data communication and detects the change from a higher to a lower slave address. If such a change was recognized, the IC assumes that the slave with the lower address has the lowest address in the network.

There are some special procedures that become active during the start of synchronous I/O mode operation and if more than three consecutive telegrams were sent to the same slave address. This is described in more detail in chapter *3.7.4 Synchronous Data I/O Mode* on page 32.

2.3.9 4 Input / 4 Output processing in Extended Address Mode

A new feature of AS-i Complete Specification v3.0 is also support of 4-bit wide output data in Extended Address Mode. In Extended Address Mode it was, up to Complete Specification v2.11, only possible to send three data output bits from the master to the slave because telegram bit I3 is used to select between A- and B- slave type for extended slave addressing (up to 62 slaves per network). In normal address mode I3 carries output data for pin D3.

The new definition introduces a multiplexed data transfer, so that all 4-bits of the data output port can be used again. A first AS-i cycle transfers the data for a 2-bit output nibble only, while the second AS-i cycle transfers the data for the contrary 2-bit nibble. Nibble selection is done by the remaining third bit. To ensure continuous alternation of bit information I2 and thus continued data transfer to both nibbles, a special watchdog was implemented that observes the state of I2 bit. The watchdog can be activated or deactivated by E²RPOM setting. It provides a watchdog filter time of about 327ms.

The multiplexed transfer of course increases the refresh time per output by a factor of two, however, some applications can tolerate this increase for the benefit of less external circuitry and better slave address efficiency. The sampling cycle of the data inputs remains unchanged since the meaning of I3 bit was not changed in the slave response with the definition of the Extended Address Mode.

More detailed information is described in chapter *3.7.5 Support of 4I/4O processing in Extended Address Mode, Profile 7.A.x.E* on page 34.

2.3.10 AS-i Safety Mode

The enhanced data input features described above require additional registers in the data input path that store the input values for a certain time before they hand them over to the AS-i transmitter. This causes a time delay in the input path that could lead to a delayed "turn off" event, if the registers were activated by intention or by accident in AS-i Safety Applications.

To safely exclude an activation of the enhanced data I/O features in Safety Applications, the IC provides a special Safety Mode that is strongly recommended to be used for AS-i Safety communication purposes. See chapter *3.7.6 Safety Mode Operation* on page 34 for further details.

2.3.11 Enhanced LED Status Indication

ASI4U newly supports enhanced status indication by two LED outputs. A special mode for direct application of Dual-LEDs and the respective different signaling modes is also implemented. Compared to the A²SI, the former U5RD pin was reassigned as LED2 pin. Thus, compatibility to existing A²SI board layouts is still guaranteed. However, it will require to keep LED2 pin disabled (default state at delivery) in order to avoid short-circuiting of U5R to ground. More detailed information on the different signaling schemes and their activation can be found in chapter *3.9 LED outputs* on page 40.

2.3.12 Communication Monitor/Watchdog

Data and Parameter communication are continuously observed by a communication monitor. If neither Data_Exchange nor Write_Parameter calls were addressed to and received by the IC within a time frame of about 41ms, a so called *No Data/Parameter Exchange* status is detected and signaled at LED1.

If the respective flags are set in the E²PROM the communication monitor can also act as communication watchdog, that initiates a complete IC reset after expiring of the watchdog timer. The watchdog mode can also be activated and deactivated by a signal at parameter port pin P0. For more detailed information see chapter *3.14 Communication Monitor/Watchdog* on page 47.

2.3.13 Write protection of ID_Code_Extension_1

As defined in AS-i Complete Specification v3.0 the ASI4U also supports write protection for ID_Code_Extension_1. The feature allows the activation of new manufacturer protected slave profiles and is enabled by E²PROM setting. It is described in more detail in chapter *3.16 Write Protection of ID_Code_Extension_1* on page 47

2.3.14 Summary of Master Calls

Table 6 on page 15 and the diagram at the following page show the complete set of Master Calls that are decoded by the ASI4U in Slave Mode. The "Enter Program Mode" call is intended for programming of the IC by the slave manufacturer only. It becomes deactivated as soon as the *Program_Mode_Disable* flag is set in the Firmware Area of the E²PROM.

AS-i Complete Specification compliance note:

In order to achieve full compliance to the AS-i Complete Specification, the *Program_Mode_Disable* flag must be set by the manufacturer of AS-i slave modules during the final manufacturing and configuration process and before an AS-i slave device is delivered to field application users.

Table 6: ASI4U Master Calls and Related Slave Responses

		Master Request														Slave Response						
Instruction	**MNE**	**ST**	**CB**	**A4**	**A3**	**A2**	**A1**	**A0**	**I4**	**I3**	**I2**	**I1**	**I0**	**PB**	**EB**	**SB**	**I3**	**I2**	**I1**	**I0**	**PB**	**EB**
Data Exchange	DEXG	0	0	A4	A3	A2	A1	A0	0	D3 ~Sel	D2	D1	D0	PB	1	0	D3 E3	D2 E2	D1 E1	D0 E0	PB	1
Write Parameter	WPAR	0	0	A4	A3	A2	A1	A0	1	P3 ~Sel	P2	P1	P0	PB	1	0	P3 I3	P2 I2	P1 I1	P0 I0	PB	1
Address Assignment	ADRA	0	0	0	0	0	0	0	A4	A3	A2	A1	A0	PB	1	0	0	1	1	0	0	1
Write Extented ID Code_1	WID1	0	1	0	0	0	0	0	0	ID3	ID2	ID1	ID0	PB	1	0	0	0	0	0	0	1
Delete Address	DELA	0	1	A4	A3	A2	A1	A0	0	0 Sel	0	0	0	PB	1	0	0	0	0	0	0	1
Reset Slave	RES	0	1	A4	A3	A2	A1	A0	1	1 ~Sel	1	0	0	PB	1	0	0	1	1	0	0	1
Read IO Configuration	RDIO	0	1	A4	A3	A2	A1	A0	1	0 Sel	0	0	0	PB	1	0	IO3	IO2	IO1	IO0	PB	1
Read ID Code	RDID	0	1	A4	A3	A2	A1	A0	1	0 Sel	0	0	1	PB	1	0	ID3	ID2	ID1	ID0	PB	1
Read ID Code_1	RID1	0	1	A4	A3	A2	A1	A0	1	0 Sel	0	1	0	PB	1	0	ID3	ID2	ID1	ID0	PB	1
Read ID Code_2	RID2	0	1	A4	A3	A2	A1	A0	1	0 Sel	0	1	1	PB	1	0	ID3	ID2	ID1	ID0	PB	1
Read Status	RDST	0	1	A4	A3	A2	A1	A0	1	1 ~Sel	1	1	0	PB	1	0	S3	S2	S1	S0	PB	1
Broadcast (Reset)	BR01	0	1	1	1	1	1	1	1	0	1	0	1	1	1	--- no slave response ---						
Enter Program Mode	PRGM	0	1	0	0	0	0	0	1	1	1	0	1	1	1	--- no slave response ---						

Note: In Extended Address Mode the "Select Bit" defines whether the A-Slave or B-Slave is being addressed. Depending on the type of master call bit I3 carries the select bit information (Sel = A-Slave) or the inverted select bit information (~Sel = B-Slave).

B-Slave with Profile 0.A (green shaded) | ASI Master Request (black/green) | ASI Slave Response (blue) | No Slave Response (blue shaded)

ADR != 0	I2 I1 I0	000	001	010	011	100	101	110	111
CB I4 I3	I3=Sel	(Slave Address != 0) AND (Progam Mode not activated)							
000	Sel=0	Data_Exchange /Sel D2 D1 D0							
001	Sel=1	Data_Exchange D3 D2 D1 D0			D3 D2 D1 D0				
010	Sel=0	Write_Parameter /Sel P2 P1 P0							
011	Sel=1	Write_Parameter P3 P2 P1 P0			P3 P2 P1 P0				
100	Sel=0	Delete_Addr x0							
101	Sel=1	Delete_Addr x0							
110	Sel=0	Rd_IO_Cfg <I3:I0>	Read_ID <I3:I0>	Read_ID_1<I3:I0>	Read_ID_2 <I3:I0>	Reset_Slave 0x6	Broadcast	Rd_Status <S3:S0>	
111	Sel=1	Rd_IO_Cfg <I3:I0>	Read_ID <I3:I0>	Read_ID_1<I3:I0>	Read_ID_2 <I3:I0>	Reset_Slave 0x6		Rd_Status <S3:S0>	

ADR == 0	I2 I1 I0	000	001	010	011	100	101	110	111
CB I4 I3		(Slave Address == 0) AND (Progam Mode not activated)							
000									
001				Address_Assignment A4 A3 A2 A1 A0					
010					0x6				
011									
100				Write_Var_Ext_Code1 ID3 ID2 ID1 ID0					
101					0x0				
110		Rd_IO_Cfg <I3:I0>	Read_ID <I3:I0>	Read_ID_1<I3:I0>	Read_ID_2 <I3:I0>		Broadcast		
111						Reset_Slave 0x6	EnterPmode	Rd_Status <S3:S0>	

	I2 I1 I0	000	001	010	011	100	101	110	111
CB I4 I3		Progam Mode activated							
000									
001		Data_Exchange - - - -			I3 I2 I1 I0	(EEPROM READ ACCESS)			
010									
011		Write_Parameter I3 I2 I1 I0			I3 I2 I1 I0	(EEPROM WRITE ACCESS)			
100				Write_Var_ID_Code ID3 ID2 ID1 ID0					
101					0x0				
110		Rd_IO_Cfg <I3:I0>	Read_ID <I3:I0>	Read_ID_1<I3:I0>	Read_ID_2 <I3:I0>	Reset_Slave 0x6	Broadcast	Rd_Status <S3:S0>	reserved
111		Rd_IO_Cfg <I3:I0>	Read_ID <I3:I0>	Read_ID_1<I3:I0>	Read_ID_2 <I3:I0>	Reset_Slave 0x6	EnterPmode	Rd_Status <S3:S0>	reserved

2.4 Master Mode

Master Mode and the related Repeater- and Monitor-Modes differ completely in their functional properties from the Slave Mode. While the IC can autonomously perform different tasks in Slave Mode, it will only act as physical layer transceiver in Master-, Repeater- and Monitor-Mode. The basic property of these modes is a modulation / demodulation of AS-i signals to Manchester-II-code and vice versa. The following figure shows the different data path configurations.

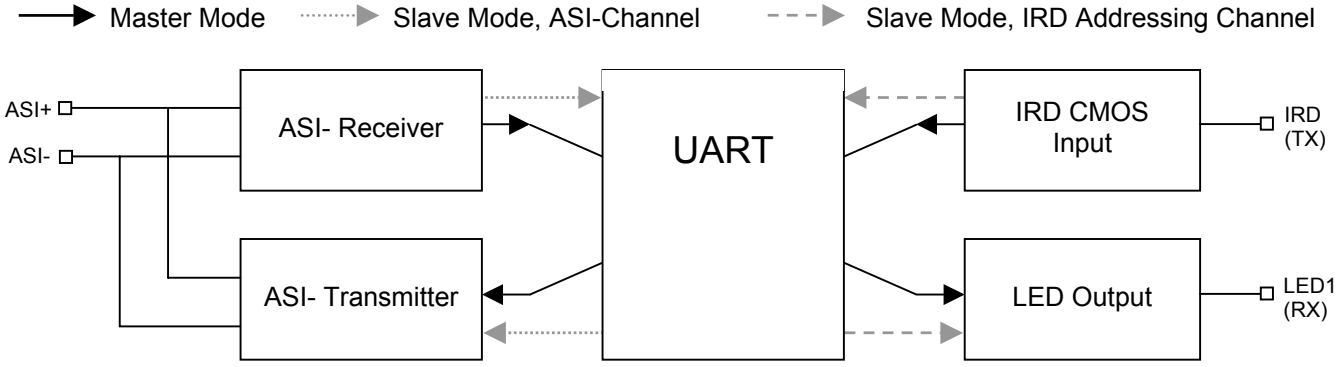

Figure 6: Data path in Master-, Repeater- and Monitor-Mode

Master-Mode, Repeater-Mode and Monitor-Mode differ from each other in the kind of signals that are available at the data I/O and parameter port pins of the IC. Following signal assignments are provided:

Pin	Master Mode	Repeater Mode	Monitor Mode
P0	Receive Clock	Hi-Z	Receive Clock
P1	Power Fail	Hi-Z	Power Fail
P2	Receive Strobe – Slave Telegram	Hi-Z	Receive Strobe – Slave Telegram
P3	Hi-Z	Hi-Z	Receive Strobe – Master Telegram
DI0	Inverting of IRD input signal. If both inputs are on different level, the IRD input signal is inverted before further processing, otherwise it is directly forwarded to the UART.		
DI1			
DI2	Inverting of LED output signal. If both inputs are on different level, the LED output signal is inverted after processing, otherwise it is directly forwarded to the LED1 output.		
DI3			
DO0	Hi-Z	Hi-Z	Pulse Code Error
DO1	Hi-Z	Hi-Z	No Information Error
DO2	Hi-Z	Hi-Z	Parity Bit Error
DO3	Hi-Z	Hi-Z	Manchester-II-Code Error at IRD Input

More detailed signal descriptions can be found in chapters *3.6 Parameter Port and PST*, *3.7 Data Port and DSR* as well as *3.12 UART*.

2.5 E²PROM

The ASI4U provides an on-chip E²PROM with typical write times of 12.5 ms and read times of 110ns. For security reasons the memory area is structured in two independent data blocks and a single bit *Security* flag.

The data blocks are named User Area and Firmware Area. The Firmware Area contains all manufacturing related configuration data (i.e. selection of operational modes, ID codes, …). It can be protected against undesired data modification by setting the *Program_Mode_Disable* flag to '1'.

The User Area contains only such data that is relevant for changes at the final application (i.e. field installation of slave module). The environment, where modifications of the user data may become necessary, can sometimes be rough and unpredictable. In order to ensure a write access cannot result in an undetected corruption of E²PROM data, additional security is provided when programming the User Area.

Any write access to the User Area (by calls *Address_Assignment* or *Write_ID_Code1*) is accompanied by two write steps to the *Security* flag, one before and one after the actual modification of user data.

The following procedure is executed when writing to the *User Area* of the E²PROM:

1. The *Security* flag is programmed to '1'.
2. The content of the *Security* flag is read back, verifying it was programmed to '1'.
3. The user data is modified.
4. A read back of the written data is performed.
5. If the read back has proven successful programming of the user data, the *Security* flag is programmed back to '0'.
6. The content of the *Security* flag is read back, verifying it was programmed to '0'.

In addition to a read out of the data areas, the *Security* flag of the E²PROM is also read and evaluated during IC initialization. In case the value of the *Security* flag equals '1' (i.e. due to an undesired interruption of a User Area write access), the entire User Area data is treated as corrupted and the Slave Address is set to 0x0 in the corresponding volatile shadow registers during initialization. Thus the programming of the User Area data can be repeated.

Table 7: E²PROM Content

ASI4U internal E²PROM Address [hex]	Bit Position	EEPROM Cell Content	EEPROM Register Content
0	0 … 3	*A0 … A3*	Slave address low nibble
1	0	*A4*	Slave address high nibble
2	0 … 2	*ID1_Bit0 … ID1_Bit2*	*ID_Code_Extension_1*
2	3	*ID1_Bit3*	*ID_Code_Extension_1*, A/B slave selection in extended address mode
3 … 7			Not implemented
8	0 … 3	*ID_Bit0 … ID_Bit3*	*ID_Code*
9	0 … 3	*ID2_Bit0 … ID2_Bit3*	*ID_Code_Extension_2*
A	0 … 3	*IO_Bit0 … IO_Bit3*	*IO_Code*
B	0	*Multiplex_Data*	Multiplexed bi-directional Data Port mode
	1	*Multiplex_Paramter*	Multiplexed bi-directional Parameter Port mode
	2	*P0_Watchdog_Activation*	Watchdog can be activated/deactivated by the logic value at parameter pin P0. Watchdog_Active must **not** be set.
	3	*Watchdog_Active*	Communication watchdog is continuously activated.

ASI4U internal E²PROM Address [hex]	Bit Position	EEPROM Cell Content	EEPROM Register Content
C	0	*Master_Mode*	If set, Firmware Area cannot be accessed.
	1	*Program_Mode_Disable*	If set, Firmware Area is protected against overriding.
	2	*Repeater_Mode*	If set, Firmware Area cannot be accessed.
	3	*Invert_Data_In*	All Data Port inputs are inverted.
D	0 … 3	*DI_Invert_Configuration*	Enables separate input data inverting for selected DI pins. *Invert_Data_In* must **not** be set.
E	0 … 3	*DI_Filter_Configuration*	Enables unitary anti-bouncing filters for selected DI pins
F	0 … 2	*DI_Filter_Time_Constant*	Defines a time constant for the input filter. For coding rules see chapter 3.7.2.
	3	*P1_Filter_Activation*	If flag is set, the logic value at the parameter pin P1 determines whether the filter function is active or inactive (see chapter 3.6.2.) If flag is not set, *DI_Filter_Configuration* activates the filter function.
10	0 … 3	*Data_Out_Configuration*	Defines whether the corresponding Data Port output pin is driven by the Data Output Register (sensitive to the *Data_Exchange* command) or the *Data_Out_Value* Register (E²PROM configured).
11	0 … 3	*Data_Out_Value*	Stores *static Data Port output* value if selected by *Data_Out_Configuration*
12	0	*Enhanced_Status_Indication*	If set, Enhanced Status Indication Mode according to AS-i Complete Specification is activated. **Activates LED2 output! For compatibility to A²SI board layouts this flag must not be set (='0').**
	1	*Dual_LED_Mode*	If set, LED1 and LED2 output signals are controlled to comply with Dual LED indication schemes of AS-i. Generated signals depend also on value of *Enhanced_Status_Indication* flag. Direct connection of a Dual LED is supported. **Activates LED2 output! For compatibility to A²SI board layouts this flag must not be set (= '0').**
	2	*FID_Invert*	The FID input value is inverted before further processing
	3	*Safety_Mode*	If set, the ASI4U Safety Mode is enabled and a special data input routing is activated.

ASI4U internal E²PROM Address [hex]	Bit Position	EEPROM Cell Content	EEPROM Register Content
13	0	*Synchronous_Data_IO*	Enables Synchronized Data I/O mode
	1	*P2_Sync_Data_IO_Activation*	If flag is set, the logic value at the parameter pin P2 determines whether the Synchonous Data IO Mode is active or inactive. If flag is not set, the Synchonous Data IO Mode is always active if it was enabled by the *Synchronous_Data_IO* flag.
	2	*Ext_Addr_4I/4O_Mode*	Enables 4 Input / 4 Output support in Extended Address Mode
	3	*ID_Code1_Protect*	If flag is set, *ID_Code_Extension_1* is write protected for user access. In Extended Address Mode, only Bits 2…0 are blocked. Bit 3 is used for A/B slave selection and must remain user accessible.
14	0 … 3	*ID1_Bit0 … ID1_Bit3*	*Protected_ID_Code_Extension_1* If *ID_Code1_Protect* flag is set, an *Read_ID_Code_1* request will be answered with the data stored in this register.
15	0 … 3	Trim Area, accessible by ZMD only	
16	0 … 3		
17	0 … 3		

☐ User Area ▒ Firmware Area

3 Detailed Functional Description

3.1 AS-i Receiver

The receiver detects (telegram) signals at the AS-i line, converts them to digital pulses and forwards them to the UART for further processing. The receiver is internally connected between the ASIP and ASIN pins. It supports floating (ground free) input signals within the voltage limits of ASIP and ASIN given in Table 2 at page 6.

Functional, the receiver removes the DC value of the input signal, band-pass filters the AC signal and extracts the digital output signals from the $\sin^2$-shaped input pulses by a set of comparators. The amplitude of the first pulse determines the threshold level for all following pulses. This amplitude is digitally filtered to guarantee stable conditions and to suppress burst spikes. This approach combines a fast adaptation to changing signal amplitudes with a high detection safety. The comparators are reset after every detection of a telegram pause at the AS-i line.

When the receiver is turned on, the transmitter is turned off to reduce the power consumption.

Table 8: Receiver Parameters

Symbol	Parameter	Min	Max	Unit	Note
V_{SIG}	AC signal peak-peak amplitude (between ASIP and ASIN)	3	8	V_{PP}	
V_{LSIGon}	Receiver comparator threshold level (refer to Figure 7)	45	55	%	Related to amplitude of 1st pulse

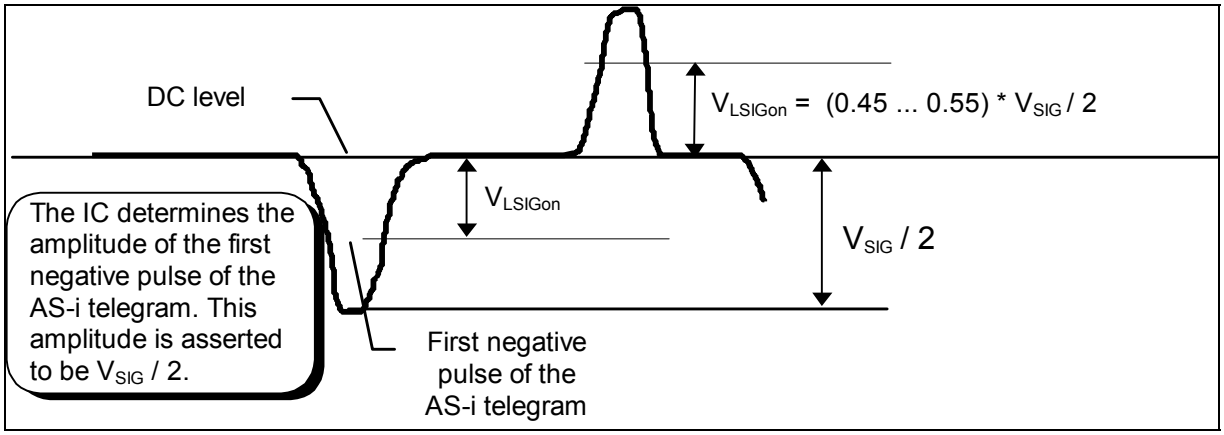

Figure 7: Receiver comparator threshold set-up in principle

3.2 AS-i Transmitter

The transmitter draws a modulated current between ASIP and ASIN to generate the communication signals. The shape of the current corresponds to the integral of a $\sin^2$-function. The transmitter comprises a current DAC and a high current driver. The driver requires a small bias current to flow. The bias current is ramped up slowly a certain time before the transmission starts so that any false voltage pulses on the AS-i line are avoided.

To support high symmetry extended power applications as shown in Figure 21 at page 52, the transmitter is designed to allow input voltages different from IC ground at the ASIN pin. The limits given in Table 2 at page 6 apply.

When the transmitter is turned on, the receiver is turned off to reduce the power consumption.

Table 9: Transmitter Current Amplitude

Symbol	Parameter	Min	Max	Unit	Note
I_{SIG}	Modulated transmitter peak current swing (between ASIP and ASIN)	55	68	mA_P	

3.3 Addressing Channel Input IRD

3.3.1 General Slave Mode Functionality

To ease the configuration process for slave modules at the field application, a secondary command input channel, the so-called Addressing Channel, IRD, is provided.

Once the channel is activated for communication, the IRD pin is receiving Manchester-II-coded (AS-i) master telegrams, while the LED1 pin is returning slave response telegrams in Manchester-II format.

Applying a so-called Magic Sequence at the IRD input activates the Addressing Channel. It doesn't matter whether the IC is communicating at the AS-i input channel or staying in idle mode. As long as the initialization process is finished and the IC is operating in Slave Mode, a correctly received Magic Sequence will reset the Data and Parameter Outputs, generate appropriate Data Strobe and Parameter Strobe signals, reset the *Data_Exchange_Disable* flag and turn the Addressing Channel active.

The Magic Sequence requires the reception of four consecutive correct AS-i telegrams in Manchester-II-Format within a timeframe of 8.192 ms (-6.25%). The telegrams will neither be answered nor otherwise internally processed. They are only checked for correct syntax (number of bits, correct start bit, end bit and parity) and timing (compliance to standard AS-i telegram timing).

To avoid a wrong activation of the Addressing Channel by undesired cross coupling of signals from the AS-i line to the IRD input, **two additional security features** are implemented.

1. The ASI4U resets the Magic Sequence telegram counter if more than 5 but less than 14 telegram bits were correctly received. Pulse signals that lead to detection of a communication error before the 6th telegram bit shall not reset the Magic Sequence counter in order to avoid a blocking of the IRD activation due to signal bouncing effects.
2. The ASI4U resets the Magic Sequence telegram counter if a telegram that was received at the IRD input correlates to the AS-i line input signal in terms of telegram reception time and content.

Note: The UART processes both input channels (AS-i line + IRD Addressing Channel) in parallel and generates *Receive_Strobe* signals after every correctly received Master telegram. A telegram correlation between both channels is found, if *Receive_Strobe* signals from both input channels arrive at a time frame of less or equal than 3µs and the telegram contents are equal too.

The Addressing Channel generally becomes **deactivated** by **IC reset.**

If the IC is locked to the Addressing Channel and AC Current Input Mode (see descriptions further below) is active, there are **four special IC functions** that were implemented to support existing handheld programming devices (from the company Pepperl+Fuchs):

1. The IC does not leave the Addressing Channel Mode after the reception of a *Reset_Slave* or *Broadcast_Reset* call if the *Data_Exchange_Disable* flag is cleared ('0'). This is always the case if the ASI4U had performed Data-/Parameter communication in advance of the reset. Thus the handheld had been operated in Data- or Parameter mode.
2. The IC does not leave the Addressing Channel during an IC reset that was caused by an expired Communication Watchdog.

   See chapter 3.14 for detailed descriptions of the Communication Monitor and Communication Watchdog.
3. Software controlled IC resets (resets through *Reset_Slave* or *Broadcast_Reset* calls) are performed slightly different than in normal slave IC operation.

   The IC still resets the Data and Parameter outputs immediately after reception of the calls and Data- and Parameter-Strobe Signals are generated. However, the IC initialization procedure is postponed for 2.048ms (-6.25%), keeping the IC blocked to any further telegram inputs at the Addressing Channel or the AS-i line input. This is to avoid an immediate reactivation of the Addressing Channel after IC initialization since the handheld programming device always sends five subsequent *Broadcast_Reset*. The ASI4U would otherwise process the first reset call from the handheld correctly but take the four remaining calls for a new Magic Sequence.
4. The UART is constantly set to Synchronous Receive Mode. This is because the signal sequence, that is generated by the handheld programming device, exhibits an additional signal transition in a time frame of 3 bit times after the end of the transmitted master call.

3.3.2 AC Current Input Mode

The IRD input allows direct connection of a Photo-Diode (referencing to 0V) and senses the generated photo current. A valid input signal has to have a certain current amplitude (range) and must not exceed a certain offset current value (Table 10 and Figure 8).

In contrast to A²SI versions, the IRD input of the ASI4U covers the entire input current range by a single amplifying stage with continues (logarithmical) gain adaptation. Thus, the cyclical gain switching is avoided and the IC can react more safely and without delay on different input signal amplitudes.

Table 10: IRD AC current input parameters

Symbol	Parameter	Min	Max	Unit	Note
I_{IRDO}	Input current offset		10	µA	
I_{IRDA}	Input current amplitude	25	100	µA	

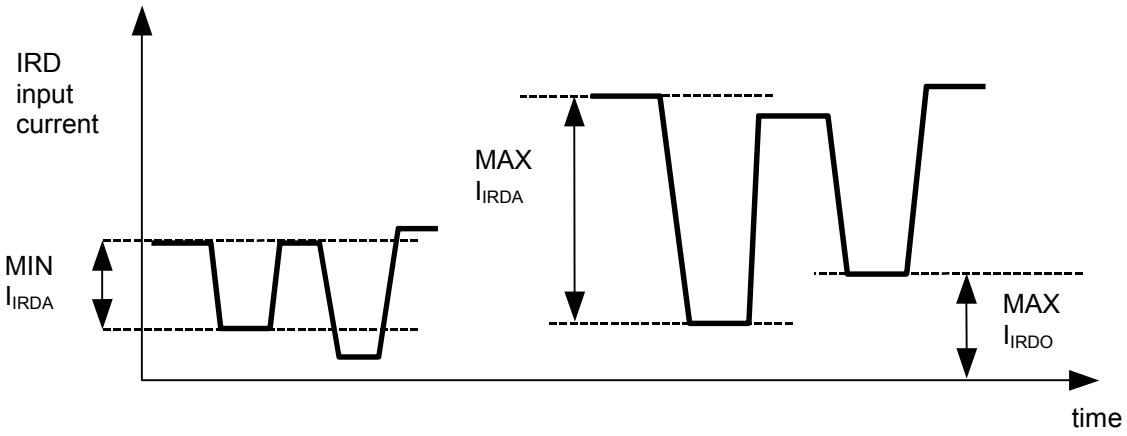

Figure 8: Addressing Channel Input (IRD), Photo-current Waveforms

Following photo-diode is suggested for optimal performance:

- TEMIC TEMD5000

3.3.3 CMOS Input Mode

In addition to the AC current input mode, the IRD input can also operate in CMOS input mode. Mode switching is only possible as long as the IC has not locked to the Addressing Channel by reception of a Magic Sequence already. On principle, that input mode that lead to the activation of the Addressing Channel will remain locked until the Addressing Channel is deactivated (by IC Reset).

The CMOS mode is entered if the IRD input voltage is **above 2.5V** (logic high) for more than 7.680 ms (-6.66%). It is left, if the IRD input voltage is **below 1.0V** (logic low) for more than 7.680 ms (-6.66%). The initial input mode after IC initialization is determined at the end of the initialization phase and depends on the value of the IRD input signal at that time.

Table 11: IRD current/voltage mode switching

Symbol	Parameter	Min	Max	Unit	Note
V_{IRD_VM}	Minimum IRD input voltage to activate CMOS mode of IRD	2.5		V	
V_{IRD_CM}	Maximum IRD input voltage to activate AC current mode of IRD		1.0	V	
$t_{IRD\_Mode\_Filter}$	Filter time constant for IRD input mode switching	7.68	8.192	ms	

The following input levels apply in CMOS mode:

Table 12: IRD CMOS Input Levels

Symbol	Parameter	Min	Max	Unit	Note
V_{IRD_IN}	Input voltage range	-0.3	V_{Uout}	V	
V_{IRD_IL}	Voltage range for input "low" level	0	1.0	V	
V_{IRD_IH}	Voltage range for input "high" level	2.5	V_{Uout}	V	
T_r /T_f	Rise/fall time		100	ns	[1]

[1] in Master Mode the rise/fall time of the IRD input signal should be as low as possible in order to avoid jitter on the AS-i line

3.3.4 Master-, Repeater- and Monitor-Mode

In Master-, Repeater-, and Monitor-Mode the IRD input is always configured in CMOS mode. The input levels specified in Table 12 apply.

The expected polarity of the Manchester-II-coded bit stream at the IRD pin depends on the values of the Pins DI0 and DI1.

Table 13: Polarity of Manchester-II-Signal at IRD in Master Mode

Input values at DI0 and DI1 are:	Description
Equal ("11", "00")	Manchester-II-Signal is low active (default logic output value at no communication is '1'). This mode is compatible to the A²SI IRD input
Unequal ("01", "10")	Manchester-II-Signal is high active (default logic output value at no communication is '0').

Note: The complemented definition was chosen to retain backward compatibility to A²SI based AS-i Master designs.

3.4 Digital Inputs - DC Characteristics

The following pins contain digital high voltage input stages:

- Input-only pins: **DI0 … DI3, FID**
- I/O pins: **P0 … P3, DSR, PST[1], LED2[1]**

Table 14: DC Characteristics of digital high voltage input pins

Symbol	Parameter	Min	Max	Unit	Note
V_{IL}	Voltage range for input "low" level	0	2.5	V	
V_{IH}	Voltage range for input "high" level	3.5	V_{UOUT}	V	
V_{HYST}	Hysteresis for switching level	0.25		V	
I_{IL}	Current range for input "low" level	-10	-3	µA	[2]
I_{IH}	Current range for input "high" level	-10	10	µA	$V_0 \geq V_{U5R}$
C_{DL}	Capacitance at pin DSR		10	pF	[3]

[1] PST and LED2 are inputs for test purposes only.

[2] The pull-up current is driven by a current source connected to U5R. It stays almost constant for input voltages ranging from 0 to 3.8V. The current source is disabled at the FID pin in Master- Repeater- and Monitor-Mode to provide a straight analog signal input for the Power Fail comparator.

[3] The internal pull-up current is sufficient to avoid accidental triggering of an IC reset if the DSR pin remains unconnected. For external loads at DSR a certain pull up resistor is required to ensure $V_{IH} \geq 3.5V$ in less than 35µs after the beginning of a DSR = Low pulse.

3.5 Digital Outputs - DC Characteristics

The following pins contain digital high voltage open drain output stages:

- Output-only pins: **DO0 … DO3, LED1**
- I/O pins: **P0 … P3, DSR, PST[1], LED2[1]**

Table 15: DC Characteristics of digital high voltage output pins

Symbol	Parameter	Min	Max.	Unit	Note
V_{OL1}	Voltage range for output "low" level	0	1	V	I_{OL1} = 10mA
V_{OL2}	Voltage range for output "low" level	0	0.4	V	I_{OL2} = 2mA
I_{OH}	Output leakage current	-10	10	µA	$V_{0H} \geq V_{U5R}$

[1] PST and LED2 are inputs for test purposes only.

3.6 Parameter Port and PST Pin

3.6.1 Slave Mode

The parameter port is configured for continuous bi-directional operation. Every pin contains an NMOS open drain output driver plus a high voltage high impedance digital input stage. Received parameter output data is stored at the Parameter Output Register and subsequently forwarded to the open drain output drivers. A certain time ($t_{PI\text{-}latch}$) after new output data has arrived at the port, the corresponding inputs are sampled.

The input value either results from a wired AND combination of the parameter output value and the signals driven to the port by external sources (*Multiplex_Parameter* ='0') or simply represents the externally driven input signals (*Multiplex_Parameter* ='1'). For further explanation see also Figure 9 and chapter 3.6.2.

The availability of new parameter output data is signaled by the *Parameter Strobe (PST)* signal.

Besides the basic I/O function, the first parameter output event after an IC reset has an additional meaning. It enables the data output at the Data Port (see chapters 3.7 and 3.11).

Any IC reset or the reception of a *Delete_Address* call turns the Parameter Output *Register* to 0xF and forces the parameter output drivers to high impedance state. Simultaneously a Parameter Strobe is generated, having the same t_{setup} timing and t_{PST} pulse width, as new output data would be driven.

Table 16: Timing Parameter Port

Symbol	Parameter	Min	Max	Unit	Note
t_{setupL}	Output data is valid LOW before PST-H/L	0.1	0.6	µs	[1]
t_{setupH}	Output driver is at high impedance state before PST-H/L	0.1	0.6	µs	[1]
t_{hold}	Output driver is at high impedance state after PST-H/L	0.1	0.6	µs	[1, 2]
t_{PST}	Pulse width of Parameter Strobe (PST)	5	6	µs	[3]
$t_{PI\text{-}latch}$	Acceptance of input data	11	13.5	µs	[4]

[1] The designed value is 0.5µs.

[2] t_{hold} is only valid, if the *Multiplex_Parameter* flag is set in the Firmware Area of the E²PROM.

[3] The timing of the resulting voltage signal also depends on the external pull up resistor.

[4] The parameter input data must be stable within the period defined by min. and max. values of $t_{PI\text{-}latch}$.

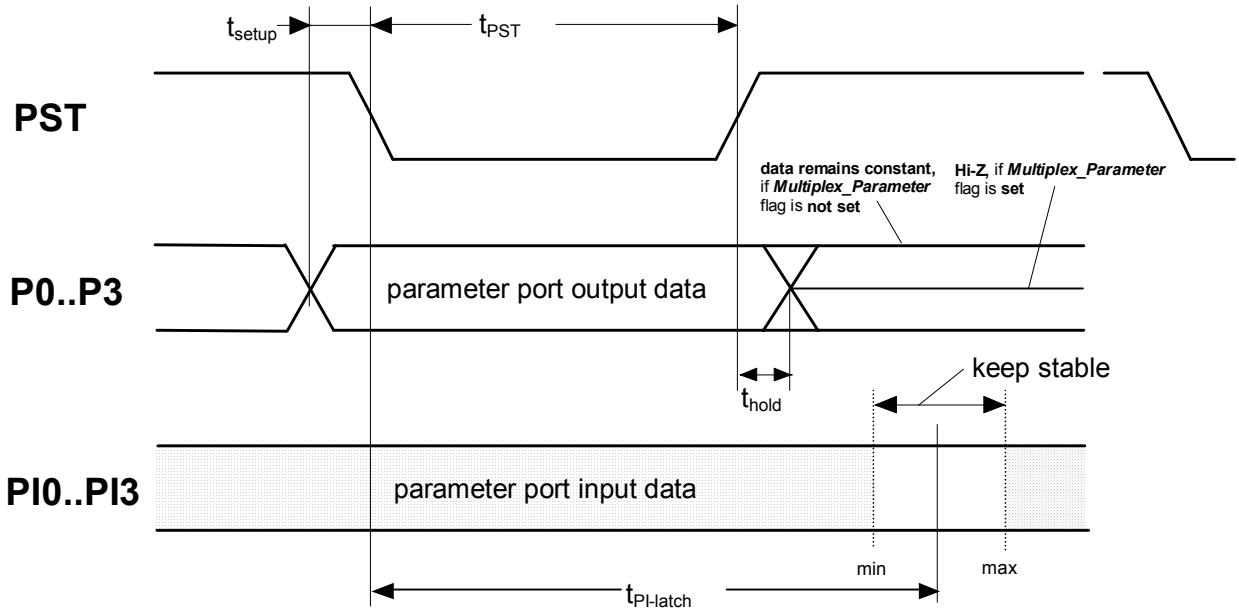

Figure 9: Timing Diagram Parameter Port P0 ... P3, PST

3.6.2 Parameter Multiplex Mode

AS-i Complete Specification v3.0 defines a so called Parameter Multiplex Mode. This new feature allows bi-directional data transfer through the parameter port. The bi-directionality is achieved by turning the Parameter Output Drivers off after the Parameter Strobe period and before the input sampling event. By turning off its output drivers during the Parameter Strobe pulse, an external microcontroller can read the data from the Parameter Port of the ASI4U, prepare new return data and place it to the port right after the Parameter Strobe signal.

The Parameter Multiplex Mode becomes activated by setting the corresponding *Multiplex_Parameter* flag (='1') in the E²PROM.

To keep full compatibility to A²SI based applications this flag should be kept zero ('0'). The A²SI did not allow real bi-directional parameter data transfer since it was not able to turn the output drivers off. The return value to a *Write_Parameter* call was always a wired AND combination of the output signal of the IC and the signal driven to the port by the external logic.

3.6.3 Special function of P0, P1 and P2

In case the *Watchdog_Active* flag is not set ('0') but the *P0_Watchdog_Activation* flag is set (= '1', Firmware Area of the E²PROM) the value of the *Parameter Port* signal P0 determines whether the communication watchdog is enabled or disabled. In compliance to Slave Profile 7D-5 the behavior is defined as follows:

Input Value at P0	State of Communication Watchdog
Low level ('0')	Disabled
High level ('1')	Enabled

If the *P1_Filter_Activation* flag is set in the E²PROM, the activation of the data input filters depends on the value of the *Parameter Port* signal P1. Following coding applies:

Input Value at P1	Data input filter function
Low level ('0')	Activated
High level ('1')	Deactivated

For further details refer to chapter *3.7 Data Port and DSR – Input Data Pre-Processing.*

If the *Synchronous_Data_I/O_Mode* flag is set in the E²PROM, the value of the parameter port P2 activates or deactivates the *Synchronous Data I/O Mode* of the ASI4U. Following coding applies:

Input Value at P2	Synchronous Data I/O Mode
Low level ('0')	Activated
High level ('1')	Deactivated

For further details refer to chapter *3.7 Data Port and DSR – Synchronous Data I/O Mode.*

The processed values of P0, P1 and P2 result from a wired-AND combination between the corresponding output value and the input value driven by an external signal source.

3.6.4 Master-, Repeater-, Monitor Mode

In Master-, Repeater- and Monitor Mode the Parameter Port is differently configured than in Slave Mode. The pins serve as output channels for additional support signals or become set to high impedance state. There is no input function associated with the Parameter Port pins.

Following support signals are provided at the Parameter Port in Master-, Repeater- and Monitor-Mode.

Table 17: Parameter Port output signals in Master-, Repeater-, Monitor-Mode

Pin	Master Mode	Repeater Mode	Monitor Mode
P0	*Receive Clock*	Hi-Z	*Receive Clock*
P1	*Power Fail*	Hi-Z	*Power Fail*
P2	*Receive Strobe – Slave Telegram*	Hi-Z	*Receive Strobe – Slave Telegram*
P3	Hi-Z	Hi-Z	*Receive Strobe – Master Telegram*

Receive Clock is provided to simplify external processing of Manchester-II-coded output data at LED1 pin. The availability of a new AS-i telegram bit at LED1 is signaled by a rising edge of receive clock so that the received data can simply be clocked into a shift register. The output signal is active high.

Power Fail signals a breakdown of the AS-i supply voltage. The output signal is active high. Further information regarding the *Power Fail* function refer to chapter *3.8 Fault Indication Input Pin* FID.

Receive Strobe – Slave Telegram is generated after every correctly received AS-i slave telegram. The output signal is active high.

Receive Strobe – Master Telegram is generated after every correctly received AS-i master telegram. The output signal is active high.

The generated pulse width is 1.0µs for both *Receive Strobe* signals at the output drivers (Hi-Z time). The resulting signal pulse width depends on the external pull-up resistor and the load circuit.

3.7 Data Port and DSR Pin

3.7.1 Slave Mode

The data port is divided in 4 output and 4 input pins. This makes it possible to control a maximum of 8 binary devices (4 input + 4 output devices) by a single AS-i Slave IC. Compatibility to multiplexed bi-directional operation, as it is defined in certain IO Configurations for AS-i Slaves, can be achieved by external connection of corresponding DI and DO pins and setting *Multiplex_Data* flag ='1' in the Firmware Area of the E²PROM.

Every output pin (DO0…DO3) contains an NMOS open drain output driver; every input pin (DI0…DI3) contains a high voltage high impedance input stage. Received output data is stored at the Data Output Register and subsequently forwarded to the DO-pins. A certain time ($t_{DI\text{-}latch}$) after new output data was written to the port, the DI-pins are sampled.

The availability of new output data is signaled by the Data Strobe (DSR) signal as shown in Figure 10. The DSR pin has an additional reset input function, that is described further in chapter *3.11 IC Reset.*

Table 18: Timing Data Port Outputs

Symbol	Parameter	Min	Max	Unit	Note
t_{setupL}	Output data is valid LOW before DSR-H/L	0.1	0.6	µs	1
t_{setupH}	Output driver is at high impedance state before DSR-H/L	0.1	0.6	µs	2
t_{hold}	Output driver is at high impedance state after DSR-H/L	0.1	0.6	µs	1, 2
t_{DSR}	Pulse width of Data Strobe (DSR)	5	6	µs	3
$t_{DI\text{-}latch}$	Acceptance of input data	11	13.5	µs	4

[1] The designed value is 0.5µs.

[2] Parameter is only valid if *Multiplex_Data* flag is set in the Firmware Area of the E²PROM.

[3] The timing of the resulting voltage signal also depends on the external pull up resistor.

[4] The input data must be stable within the period defined by min. and max. values of $t_{DI\text{-}latch}$.

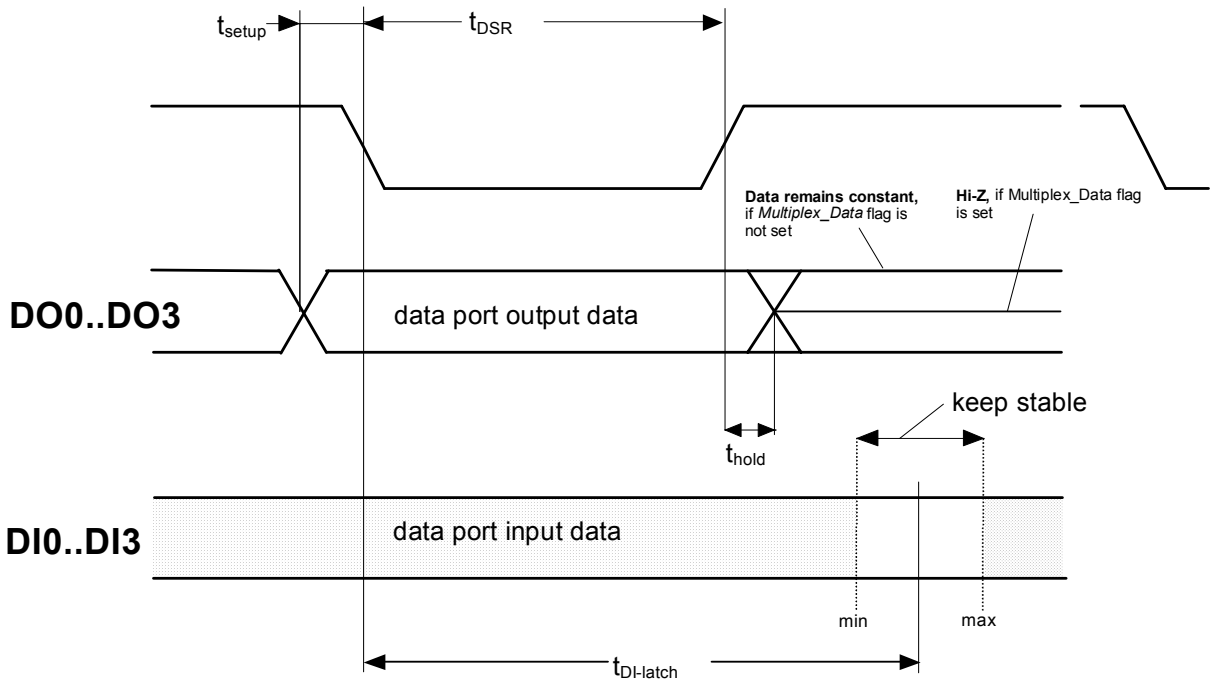

Figure 10: Timing diagram data port DO0 ... DO3, DI0 … DI3, DSR

Any IC reset or the reception of a *Delete_Address* call turns the Data Output Register to 0xF and forces the data output drivers to high impedance state. Simultaneously a *Data Strobe* is generated, having the same t_{setup} timing and t_{DSR} pulse width, as new output data would be driven.

All Data Port operations as well as the generation of a slave response to *Data_Exchange* (DEXG) requests depend on the value of *Data_Exchange_Disable* flag. It becomes set during IC reset or after a *Delete_Address* call prohibiting any data port activity after IC initialization or address assignment, as long as the external circuitry was not pre-conditioned by dedicated parameter output data. The *Data_Exchange_Disable* flag is cleared while processing a *Write_Parameter* (WPAR) request. Consequently the AS-i master has to send a WPAR call in advance of the first *Data_Exchange* (DEXG) request in order to enable Data Port operation at the slave.

3.7.2 Input Data Pre-Processing

Besides the standard input function the Data Port offers different data pre-processing features that can be activated by setting corresponding flags in the Firmware Area of the E²PROM. The data path is structured as follows:

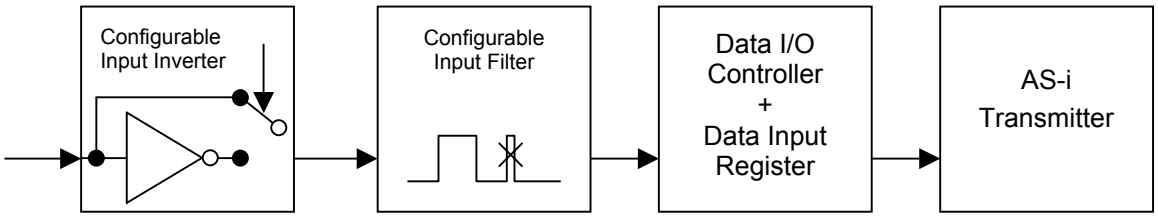

Figure 11: Input path at Data Port

- **Joint Input Inverting**

  The input values of all four data input channels are inverted when the *Invert_Data_In* flag is set. Any configurations made in the *DI_Invert_Configuration* register are ignored. The feature is kept for compatibility with A²SI product versions.

- **Selective Input Inverting**

  If the *Invert_Data_In* flag is not set, inverting of input data can be configured individually for every *Data Port* input channel by setting the corresponding flag in the *DI_Invert_Configuration* register. Hereby the index of the DI channel corresponds to the bit position within the register. Thus, the data at input channel **DI0** is inverted if **Bit 0** of the *DI_Invert_Configuration* register is set and consequently input channel **DI3** is inverted if **Bit 3** is set.

- **Selective Input Filtering**

  A digital anti-bouncing filter is provided at every *Data Input* channel to keep undesired signal bouncing at the DI pins away from the AS-i Master. If activated, a signal transition at the particular DI pin is passed to the Data Input Register only if the new value has remained constant for a certain time.

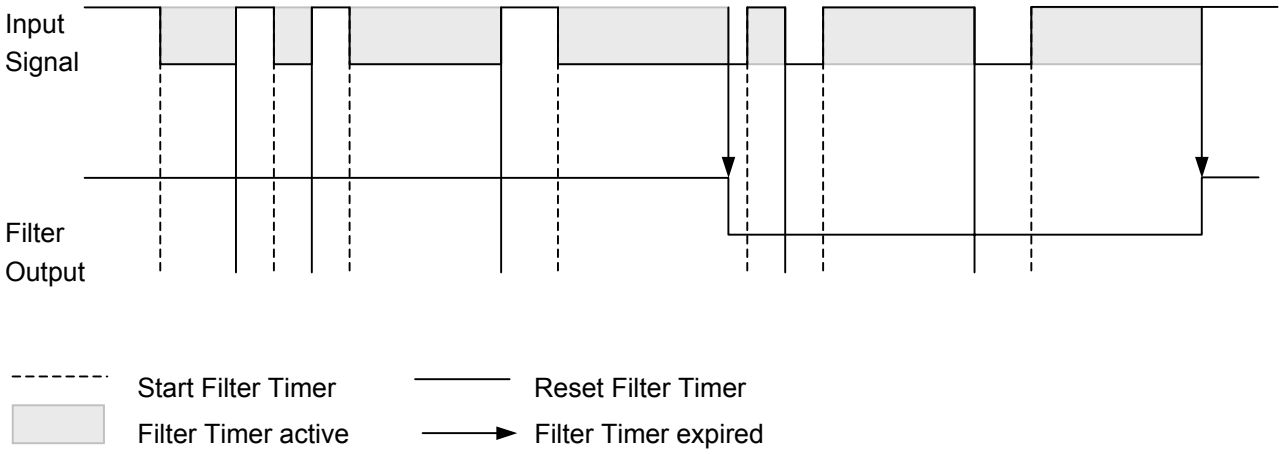

Figure 12: Principle of input filtering

The filter time can be adjusted jointly for all input channels in seven steps by programming the *DI_Filter_Time_Constant* register in the Firmware Area of the E²PROM. The following coding table applies:

Table 19: Data Input Filter Time Constants

	DI_Filter_Time_Constant, Tolerance = - 6.25%							
	0	1	2	3	4	5	6	7
Corresponding input filter time constant	128 µs	256 µs	512 µs	1024 µs	2048 µs	4096 µs	8192 µs	AS-i cycle

If *AS-i cycle* mode is selected, a new input value is returned to the master if equal input data was sampled for two consecutive *Data_Exchange* cycles. As long as the condition is not true, previous valid data is returned. To suppress undesired input data validation in case of immediately repeated *Data_Exchange* calls (i. e. AS-i Masters immediately repeat one *Data_Exchange* requests if no valid slave response was received on the first request) input data sampling is blocked for 256µs (-6.25%) after every sampling event in AS-i cycle mode.

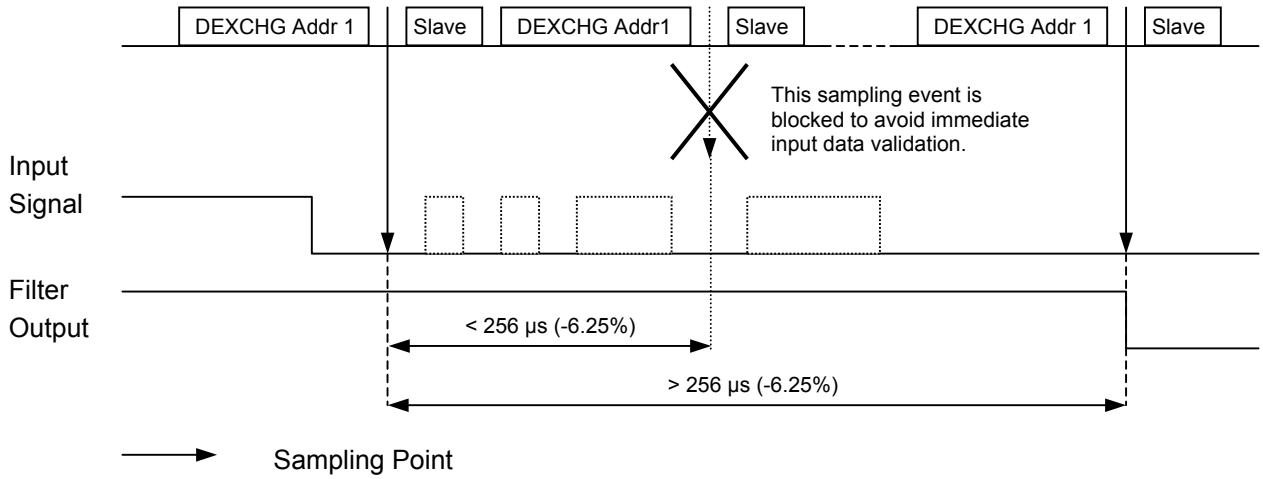

Figure 13: Principle of AS-i cycle input filtering (exemplary for Slave with Address 1)

The *DI_Filter_Configuration* register provides channel selective enabling of input filters; just as the *DI_Invert_Configuration* register allows individual inverting of the four Data Port input channels. Again, the index of the DI channel corresponds to the bit position within the register. Thus, data at input channel **DI0** is filtered if **Bit 0** of the *DI_Filter_Configuration* register is set and consequently input channel **DI3** is filtered if **Bit 3** is set.

In general the *Data Input Filters* become active, as the corresponding bit in the *DI_Filter_Configuration* Register is set.

- They are initialized with '0' and the filter timer is reset after the initialization phase of the IC. (The first is because an AS-i Master interprets data inputs at '0' to be inactive.)
- If the *P1_Filter_Activation* flag is set to '1', the filters will also start to run after the initialization phase, however the data to construct the slave response is either taken from the actual Data Input values or the filtered values, depending on the state of Parameter Port P1

Table 20: Input Filter Activation by Parameter Port Pin P1

P1_Filter_Activation Flag	Parameter P1	Data Input Filter Function
0	Don't care	ON, active filters depend on *DI_Filter_Configuration*
1	1	OFF
1	0	ON, active filters depend on *DI_Filter_Configuration*

If the IC is operated in Parameter Multiplex mode (see descriptions in chapter 3.6.1 and 3.6.2 on page 26 et sqq.) while the *P1_filter_activation* flag is set, the Parameter Multiplex mode remains disabled for parameter port pin P1. This is to avoid erroneous deactivation of the input filters if no external driver is connected.

Input data inverting and input data filtering are independent features that can be combined as required by the application. Programming the following E²PROM flags or registers activates them:

Table 21: E²PROM configuration for different Input Modes

E²PROM Flag or register name	Input Mode: Standard Input	Joint Input Inverting	Selective Input Inverting	Selective Input Filtering
Invert_Data_In	0	1	0	Input inverting is additionally possible
DI_Invert_Configuration	0x0	don't care	0x1 … 0xF	
DI_Filter_Configuration	0x0	Input filtering is additionally possible		0x1 … 0xF
DI_Filter_Time_Constant	Don't care			0x0 … 0x7

3.7.3 Fixed Output Data Driving

Besides the standard output function the Data Output Port provides an additional function to drive a fixed output value that is stored in the Firmware Area of the E²PROM. This feature is basically meant to support signaling of different Firmware Area setups to outside slave module circuitry. It presumes the application does not require all four Data Output pins.

The E²PROM *Data_Out_Configuration* register is used to determine whether the corresponding Data Port output signal is sensitive to *Data_Exchange* calls, or if the driven Data Output value is taken from the corresponding bit in the *Data_Out_Value* register, also located in the Firmware Area of the E²PROM.

The index of the DO signal corresponds to the bit position in the *Data_Out_Configuration* and *Data_Out_Value* registers. The fixed output driving capability is activated if the particular *Data_Out_Configuration* bit is set to '1'. The standard output mode is activated if *Data_Out_Configuration* is programmed to 0x0, which is the default state of the register.

3.7.4 Synchronous Data I/O Mode

As defined in the AS-i Complete Specification, a master successively polls the network rising the slave addresses from the lowest to the highest. Hence, data input and output operations normally take place at different times in different slaves. To support applications that require simultaneous Data I/O operations on a certain number of slaves in the network, a Synchronous Data I/O Mode is provided.

The feature is enabled if the *Synchronous_Data_IO* flag is set in the firmware area of the E²PROM (='1'). Activation of the feature additionally depends on the value of the *P2_Sync_Data_IO_Activation* flag. Following coding applies:

Table 22: Activation states of Synchronous Data IO Mode

Synchronous_Data_IO flag	*P2_Sync_Data_IO_Activation* flag	Input Value at P2	Synchronous Data I/O Mode
0	Don't care	Don't care	Deactivated
1	0	Don't care	Activated
1	1	Low level ('0')	Activated
1	1	High level ('1')	Deactivated

The Parameter Port signal **P2 is sampled at the rising edge of the Data Strobe** (L/H transition) signal to determine the Data I/O behavior at the next Data Output event.

If the IC is operated in Parameter Multiplex mode (see description in chapter 3.6.1 on page 26*)* while *Synchronous_Data_IO* flag **and** *P2_Sync_Data_IO_Activation* flag are set, the Parameter Multiplex mode remains disabled for parameter port pin P2. This is to avoid erroneous deactivation of the Synchronous Data IO mode in case no external driver is connected.

Once activated, input data sampling as well as output data driving events are moved to different times **synchronized** to the polling cycle of the AS-i network. Nevertheless, the communication principles between master and slave remain unchanged compared to regular operation. Following rules apply:

- Data I/O is triggered by the DEXG call to slave with the lowest slave address in the network. Based on the fact, that a master is calling slaves successively with rising slave addresses, the ASI4U considers the trigger condition true, if the slave address of a received DEXG call is less than the slave address of the previous (correctly received) DEXG call.

  Data I/O is only triggered, if the slave has (correctly) received data during the last cycle. If the slave did not receive data (i.e. due to a communication error) the Data Outputs are not changed and no Data Strobe is generated (arm+fire principle). The inputs however, are always sampled at the trigger event.
- If **the slave with the lowest address in the network** is operated in the Synchronous Data I/O Mode*,* it postpones the output event for the received data for a full AS-i cycle. This is to keep all output data of a particular cycle image together.

  Note: To make this feature useful, the master shall generate a data output cycle image once before the start of every AS-i cycle. The image is derived from the input data of the previous cycle(s) and other control events. If an AS-i cycle has started, the image shall not change anymore. In case A- and B-slaves are installed in parallel at one address, the master shall address all A-Slaves in one cycle and all B-Slaves in the other cycle.

  The input data, sampled at the slave with the lowest slave address in the network, is sent back to the master without any delay. Thus, the input data cycle image is fully captured at the end of an AS-i cycle, just as in networks without any Synchronous Data I/O Mode slaves. In other words, the input data sampling point has simply moved to the beginning of the AS-i cycle for all Synchronous Data I/O Mode slaves.
- The **first DEXG call** that is received by a particular slave after the activation of the Data Port (*Data_Exchange_Disable* flag was cleared by a WPAR call is processed like in regular operation. This is to capture decent input data for the first slave response and to activate the outputs as fast as possible.

  The Data I/O operation is repeated together with the I/O cycle of the other Synchronous Data I/O Mode slaves in the network at the common trigger event. By that, the particular slave has fully reached the Synchronous Data I/O Mode.
- If the ***P2_Sync_Data_IO_Activation*** **flag is set to '1'** at the slave with the lowest address in the network, one data output value is lost when the Synchronous Data I/O Mode is turned off (L/H transition at P2), while the value that is received in the cycle when the IC detects a signal change at P2 (H/L transition) is repeated. This particular behavior is caused by the fact that in *Synchronous Data I/O Mode* the data output at the slave with the lowest address is postponed for a full AS-i cycle (see description above).
- To avoid a general suppression of Data I/O in the special case that a slave in Synchronous Data I/O mode receives **DEXG calls only to its own address** (i.e. employment of a handheld programming device), the Synchronous Data I/O Mode is turned off, once the ASI4U receives three consecutive DEXG calls to its own slave address. The IC resumes to Synchronous Data I/O Mode operation after it observed a DEXG call to a different slave address than its own. The reactivation of the Synchronous Data I/O mode is handled likewise for the first DEXG call after activation of the Data Port (see description above).

The Data Strobe (DSR) signal is of course also generated in Synchronous Data I/O Mode. The timings of input sampling and output buffering correspond to the regular operation (refer to Figure 10 and Table 18).

3.7.5 Support of 4I/4O processing in Extended Address Mode, Profile 7.A.x.E

In Extended Address Mode the information bit I3 of the AS-i master telegram is used to distinguish between A- and B-slaves that operate in parallel at the same AS-i slave address. For more detailed information refer to AS-i Complete Specification.

Besides the benefit of an increased address range, the cycle time per slave is increased in Extended Address Mode from 5 ms to 10 ms and the useable output data is reduced from 4 to 3 bits. Because of the later, Extended Address Mode slaves can usually control a maximum of 3 data outputs only. The input data transmission is not effected since the slave response still carries 4 data information bits in Extended Address Mode.

Applications that require 4 bit wide output data in Extended Address Mode, but can tolerate further increased cycle times (i.e. push buttons and pilot lights), shall be directly supported by a new Slave Profile 7.A.x.E that is defined in the AS-i Complete Specification V3.0.

If the IC is operated in Extended Address Mode and the *Ext_Addr_4I/4O_Mode* flag is set (='1') in the E²PROM, it treats information bit I2 as selector for two 2-bit wide data output banks (*Bank_1, Bank_2*).

A master shall transmit data alternating to *Bank_1* and *Bank_2*, toggling the information bit I2 in the respective master calls. The ASI4U triggers a data output event (modification of the data output ports and generation of Data Strobe) only at a *Data_Exchange* call that contains I2='0' and if the ASI4U received a *Data_Exchange* call with I2='1' in the previous cycle. Thus, new output data is issued at the Data Port synchronously for both banks at a falling edge of I2. The I2 toggle detector starts on state I2='0' after reset.

Input data is captured and returned to the master at every cycle, independent of the value of information bit I2. In consequence the cycle time is different for input data and output data:

- **Data input values** become refreshed in the master image in **less than 10 ms**
- **Data output values** become refreshed at the slave in **less than 21 ms**

Following coding applies:

Table 23: Meaning of master call bits I0 … I3 in *Ext_Addr_4I/4O_Mode*

Bit in master call	Operation / Meaning
I0	If I2 = '1' then I0/I1 are directed to temporary data output registers DO0_tmp/DO1_tmp
I1	If I2 = '0' then I0/I1 are directed to the data output registers DO2/DO3 and DO0_tmp/DO1_tmp are directed to the data output registers DO0/DO1
I2	I2: /Sel-bit for transmission to *Bank_1* (DO0/DO1) / *Bank_2* (DO2/DO3)
I3	I3: /Sel-bit for A-Slave/B-Slave addressing

3.7.6 Safety Mode Operation

The enhanced data input features described above require additional registers in the data input path that store the input values for a certain time before they hand them over to the AS-i transmitter. This causes a time delay in the input path and would lead to a delayed "turn off" event in AS-i Safety Applications, which in turn results in an increase in safety reaction time of the application.

To safely exclude an activation of the enhanced data I/O features in Safety Applications, a special Safety Mode of the IC must always be selected once the ASI4U is used for safe AS-i communication purposes. The Safety Mode is activated by setting the *Safety_Mode* flag in the firmware area of the E²PROM.

The Safety Mode contains the following properties:

- **Additional Multiplexer**

  An additional 2:1-Multiplexer is added in front of the send multiplexer that is controlled by the *Safety_Mode* flag. For deactivated Safety Mode, the regular data path is active.

- **Exchange of data inputs**

  The internal data paths of D3 and D2 are exchanged in Safety Mode and have to be exchanged in the external code generator that controls the Data Inputs of the ASI4U as well. In case the Safety Mode became accidentally deactivated by an hardware fault, an exchange of the bits would be recognized after 4 cycles in a running application (see Figure 14).

- **Inverter at the data inputs**

  In Safety Mode it is still possible to use the Data Input Invert functionality (either joint input inverting or bit selective input inverting) of the IC. This allows to transform the default signal level of the external application (either High or Low) to the required default input level for AS-I Safety. For safety considerations there is no difference whether the inverter is integrated in the ASI4U IC or added externally. An error in the inverter or inverter activation will be recognized by a running application within the next cycle.

  The following feature descriptions relate to the logical signals after the (optional) data input inverters.

  Important Note: As described above, the pin assignment of DI2 and DI3 is exchanged in Safety Mode. However, the configuration register for selective input inverting is directly associated with the physical IC ports and is not changed. Thus, in Safety Mode Bit3 of the *DI_Invert_Configuration* register defines the inverting of the logical signal DI2 and Bit2 defines the inverting the signal DI3.

- **Modification of Code Sequence**

  The transmitted value for D0 is calculated according to the following equation:

  D0 = D0 XOR (D1 AND D2 AND D3)

  Thus, the ASI4U will generate '1110' from the input value '1111' and '1111' from the input value '1110'. To comply with the coding rules of the safe AS-i communication, which prohibit '1111' as a valid state in the data stream, the external code generator has to store '1111' instead of '1110'.

  In case the Safety Mode became accidentally deactivated by an hardware fault, the IC would not perform the D0 combination anymore. The Safety Monitor would notice this as an error by reception of '1111', see Figure 15.

- **Deactivation of the standard data path**

  Theoretically, the Safety Mode could become deactivated for a single bit only, if a (single) fault occurs at one of the multiplexers. This would lead to code sequences where three bits are routed in the Safety Path and the fourth bit is routed in the Standard Path. Therefore, an additional OR-Gate is added in the Standard Path, that ties the Standard Path to constant '1' once the Safety Mode is activated.

  A valid data transfer in Standard Mode or Safety Mode is only possible, if all four multiplexers are switched to the same direction. Any other state will be recognized by the Safety Monitor.

- **Activation of Data_Exchange_Disable**

  The *Data_Exchange_Disable* flag is set by the IC after Reset and will be cleared after the first Parameter call. As long as the flag is set, the IC does not respond to *Data_Exchange* calls. In case the Safety Mode is activated and the *Synchronous_Data_IO* flag or any of the *DI_Filter_Configuration* flags are set in the Firmware Area of the E²PROM, the *Data_Exchange_Disable* flag cannot be cleared. This prevents any data communication in that particular case. See Figure 16.

Following flow charts are valid in Safety Mode of the ASI4U:

Note: **>=1** represents a logical **OR**
=1 represents a logical **XOR**
& represents a logical **AND**

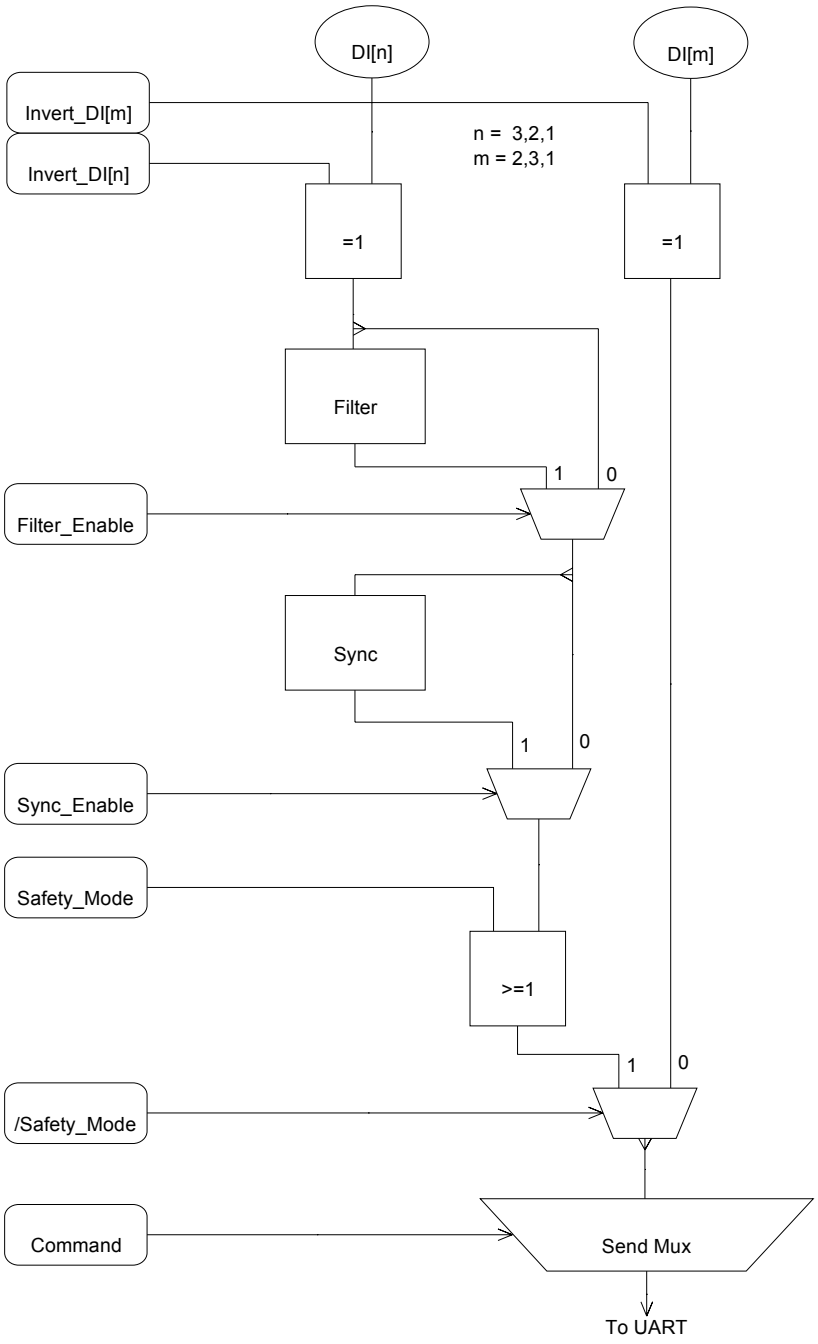

Figure 14: Flowchart - Input D3 (D2,D1) in Safety Mode

The IC contains only one single inverter that generates the inverted Safety Mode signal for all necessary purposes.

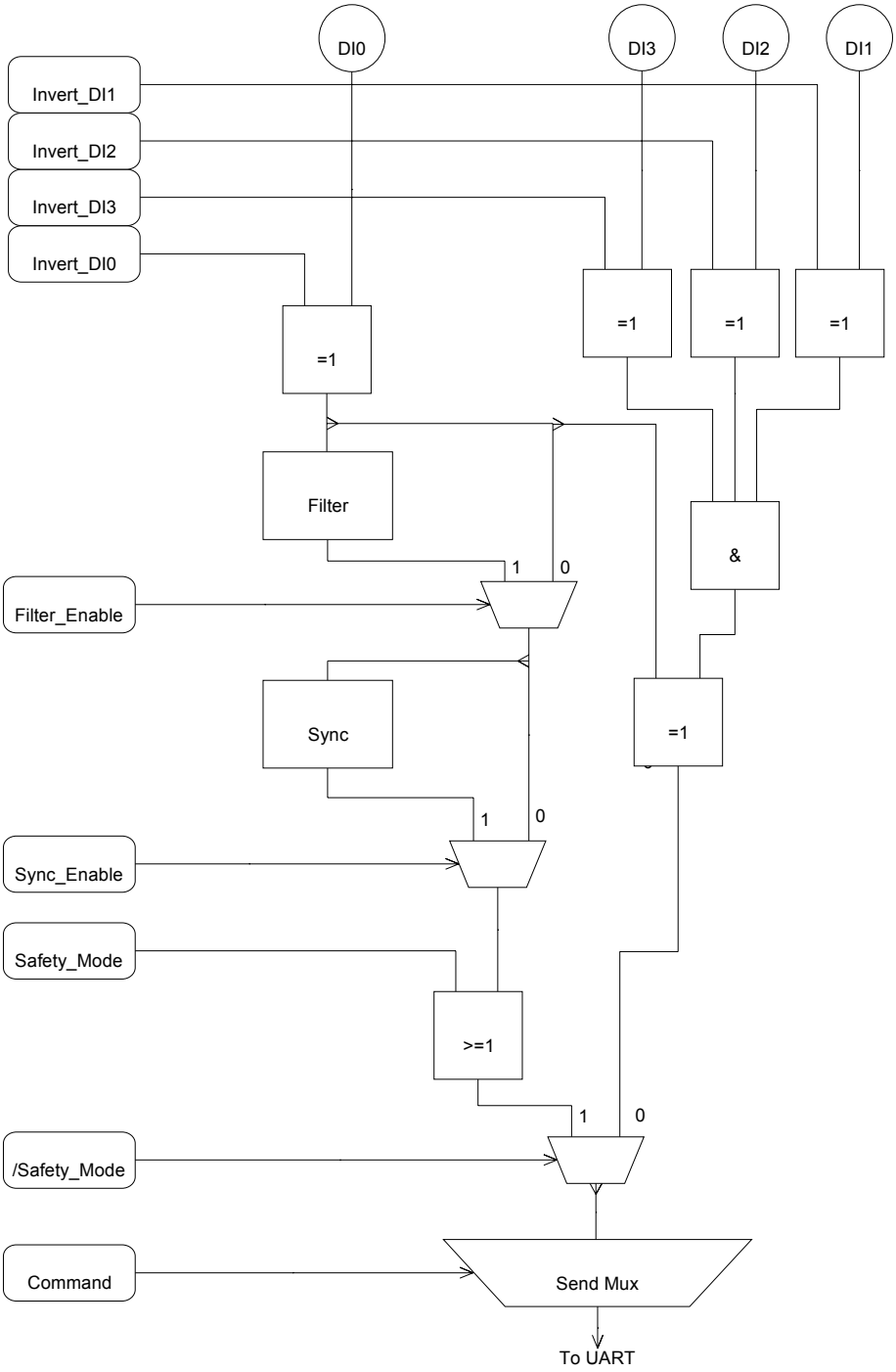

Figure 15: Flowchart - Input D0 in Safety Mode

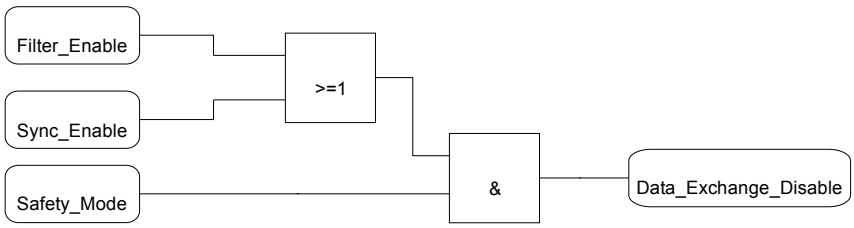

Figure 16: Flowchart - Data_Exchange_Disable

3.7.7 Master-, Repeater-, Monitor Mode

In Master-, Repeater- and Monitor Mode the data input and data output ports are differently configured than in Slave Mode. Following control signals are provided at the data input port in Master-, Repeater- and Monitor Mode:

Table 24: Control signal inputs in Master-, Repeater- and Monitor Mode

Data Input Port	Signal Name	Description
DI0	*invert_ird_a*	If the signals *invert_ird_a* and *invert_ird_b* are unequal, the IRD input signal is inverted before further processing. See Table 13.
DI1	*invert_ird_b*	
DI2	*invert_led1_a*	If the signals *invert_led1_a* and *invert_led1_b* are unequal, the LED1 output signal is inverted after processing. See Table 28.
DI3	*invert_led1_b*	

Note: The complemented definition was chosen to retain backward compatibility to A²SI based AS-i Master designs.

The Data Output Port is exclusively used in Monitor Mode to provide additional UART error signals. The signals are defined active low and will be set immediately after a telegram error was detected. They become reset at the beginning of the next telegram. Following signals are available:

Table 25: Error signal outputs in Monitor Mode

Data Port Output	UART Error Signal	Description	
DO0	*plscod_err*	Pulse Code Error	Indicates faulty AS-i pulses. This is a disjunction of alternation error, start bit error, end bit error
DO1	*no_info_err*	No Information Error Length Error	The output signal is a disjunction of *No_Information_Error* and *Length_Error* as defined in the Complete Spec 3.0. The Monitor Mode does not distinguish between synchronized and not synchronized UART Mode. There is always only one bit time supervised after the end of a telegram.
DO2	*parb_err*	Parity Bit Error	Received parity bit does not match the check sum calculated by the UART
DO3	*ird_man_err*	Man-II-Code Error at IRD input	Signal at IRD input violates MAN-II-Coding rules

3.7.8 Special function of DSR

Besides of its standard output function the *Data Strobe* Pin serves as external reset input for all operational modes of the IC. Pulling the DSR pin LOW for more than a minimum reset time generates an unconditioned reset of the IC, which is immediately followed by an re-initialization of the IC (E²PROM read out).

Further information on the IC reset behavior, especially in regard to the signal timing, can be found at chapter *3.11 IC Reset*.

3.8 Fault Indication Input Pin FID

3.8.1 Slave Mode

The fault indication input FID is provided for sensing a periphery fault-messaging signal in Slave Mode. It contains a high voltage high impedance input stage that influences the status bit S1 of an AS-i Slave directly. DC properties of the pin are specified at *Table 14: DC Characteristics of digital high voltage input pins*.

If the *FID_Invert* flag (Firmware Area of the E²PROM) is not set, a periphery fault is signaled by logic HIGH at the FID input. In this case S1 and FID are logically equivalent, which is the default state. In the opposite case, when *FID_Invert* = '1', the FID input value is inverted before any further processing. The *FID_Invert* feature was added to provide special support for certain fault conditions.

Signal transitions at the FID pin become visible in S1 with a slight delay, because a clock synchronizing circuit is in between.

3.8.2 Master- and Monitor Mode

In Master- and Monitor Mode the FID input provides a voltage sense comparator for power fail detection. Its threshold voltage is set to 2.00 V +/-3%.

A power fail event is recognized and displayed at the Parameter Pin P1 if the input voltage falls below the reference voltage for more than 0.7...0.9 ms. No power fail signal is generated while the IC is performing its initialization procedure.

Table 26: Power Fail Detection at FID (Master Mode and Monitor Mode)

Symbol	Parameter	Min	Max	Unit	Note
V_{FID-PF}	FID reference voltage to detect power fail	1.94.	2.06	V	[1]
R_{IN-FID}	Input resistance of FID input	2 Meg		Ohms	
t_{Loff}	Power supply break down time to generate a Power Fail Signal	0.7	0.9	ms	

[1] for the measurement for the AS-I-voltage an external voltage divider is necessary, see Application Notes.

3.9 LED outputs

3.9.1 Slave Mode

The ASI4U provides two LED pins for enhanced status indication. LED1 and LED2 both contain NMOS open drain output drivers. In addition, LED2 contains a high voltage high impedance input stage for purposes of the IC production test.

For compatibility to A²SI board layouts, where pin number 23 (former U5RD) had to be connected to U5R, the **LED2** function is turned **OFF by default**, keeping LED2 always at high impedance state. This is to protect LED2 against shorting the 5V supply (U5R) to ground. LED2 will be activated if the *Enhanced_Status_Indication* flag **and/or** the *Dual_LED_Mode* flag are set in the E²PROM.

In order to comply with the signaling schemes defined in the AS-i Complete Specification a **red LED** shall be connected to **LED1** and a **green LED** shall be connected to **LED2.** Direct operation of a **Dual LED** is also supported but requires the *Dual_LED_Mode* flag to be set. This is because LED1 and LED2 need to be controlled differently for AS-i compliant Dual LED signaling.

Following status indication is supported

Table 27: LED status indication

Symptom	Standard Status Indication		Extended Status Indication		Note
	Normal	Dual LED	Normal	Dual LED	
Power Off	○ ○	○	○ ○	○	No power supply available
Normal operation	green ○	green	green ○	green	Data communication is established
No data exchange	green red	red	green red	red	The *Data_Exchange_Disable* flag is still set, prohibiting Data Port communication. IC is waiting for a *Write_Parameter* request. The Communication Monitor has detected No Data Exchange status or the IC was reset by Watchdog IC Reset.
No data exchange (Address = 0)			green red	yellow red	Slave is waiting for address assignment. Data Port communication is not possible.
Periphery Fault	green red	red/ green alternating	green red alternating	red/ green alternating	Periphery Fault signal generated at FID input.
Serious Periphery Fault with Reset			green red	red	Data Strobe driven LOW for more than 44µs.

The flashing frequency of any flashing status indication is around **2 Hz**.

As mentioned above, Pin LED2 is deactivated in Normal - Standard Status Indication Mode (*Extended_Status_Indication* = '0' and *Dual_LED_Mode* = '0') for downward compatibility. In this case, the green LED shall be connected directly to pin UOUT or different sensor supply.

3.9.2 Communication via Addressing Channel

As soon as the *Addressing Channel* becomes activated for telegram communication (see chapter *3.3 Addressing Channel Input IRD* on page 22), LED1 is operated as Addressing Channel output port. This output mode takes precedence over any status indication at LED1. If the *Dual_LED_Mode* flag is set, LED2 is switched inactive (high impedance) while the *Addressing Channel* is active. This is to avoid interference to the data communication by mixed optical signals.

3.9.3 Master-, Repeater-, Monitor Mode

In Master-, Repeater- and Monitor Mode LED1 provides the Manchester-II-coded, re-synchronized equivalent of the telegram signal received at the AS-i input channel. The polarity of the Manchester-II-coded bit stream depends on the values of the Pins DI2 and DI3.

Table 28: Polarity of Manchester-II-Signal at LED1

Input values at DI2 and DI3 are:	Description
Equal ("11", "00")	Manchester-II-Signal is high active (default logic output value at no communication is '0'). This mode is compatible to the A²SI LED output
Unequal ("01", "10")	Manchester-II-Signal is low active (default logic output value at no communication is '1').

Note: The complemented definition was chosen to retain backward compatibility to A²SI based AS-i Master designs.

Every received AS-i telegram is checked for consistency with the protocol specifications and timing jitters become removed as long as they stay within the specified limits. In case a telegram error is detected, the output signal becomes disturbed in such a way that following logic can also recognize the MAN output signal being erroneous.

LED2 is always logic HIGH (high impedance) in Master-, Repeater- and Monitor Mode to reduce internal power dissipation of the IC. In such applications, the green LED shall be connected to Pin UOUT or different supply levels.

3.10 Oscillator Pins OSC1, OSC2

Table 29: Oscillator pin parameters

Symbol	Parameter	Min	Typ.	Max	Unit	Note
V_{OSC_IN}	Input voltage range	-0.3		V_{U5R}	V	
C_{OSC}	External parasitic capacitor at oscillator pins OSC1, OSC2	0		8	pF	
C_{LOAD}	Dedicated load capacity		12		pF	
V_{IL}	Input "low" voltage	0		1.5	V	[1]
V_{IH}	Input "high" voltage	3.5		V_{U5R}	V	[1]

[1] for external clock applied to OSC1

3.11 IC Reset

Any IC reset turns the Data Output and Parameter Output Registers to 0xF and forces the corresponding output drivers to high impedance state. Except at Power On Reset, Data Strobe and Parameter Strobe signals are simultaneously generated to visualize possibly changed output data to external circuitry.

The *Data_Exchange_Disable* flag becomes set during IC reset, prohibiting any data port activity right after IC initialization and as long as the external circuitry was not pre-conditioned by decent parameter output data. Consequently the AS-i master has to send a *Write_Parameter* call in advance of the first *Data_Exchange* request to an initialized slave. Following IC initialization times apply:

Table 30: IC Initialization times

Symbol	Parameter	Min	Max	Unit	Note
t_{INIT}	Initialization time after Software Reset (generated by master calls *Reset_Slave* or *Broadcast_Reset*) or external reset via DSR		2	ms	[1]
t_{INIT2}	Initialization time after power on		30	ms	[2]
t_{INIT3}	Initialization time after power on with high capacitive load		1000	ms	[3]

[1] guaranteed by design

[2] 'power on' starts latest at V_{UIN} = 18V, external capacitor at pin UOUT less than or equal 10µF

[3] C_{UOUT} = 470µF, t_{INIT3} is guaranteed by design only

3.11.1 Power On Reset

In order to force the IC into a defined state after power up and to avoid uncontrolled switching of the digital logic if the 5V supply (U5R) breaks down below a certain minimum level, a Power On Reset is executed under the following conditions:

Table 31: Power On Reset Threshold Voltages

Symbol	Parameter	Min	Max	Unit	Note
V_{POR1F}	V_{U5R} voltage to trigger internal reset procedure, falling voltage	1.2	1.7	V	[1]
V_{POR1R}	V_{U5R} voltage to trigger INIT procedure, rising voltage	3.5	4.3	V	[1]
t_{Low}	Power-on reset pulse width	4	6	µs	

[1] guaranteed by design

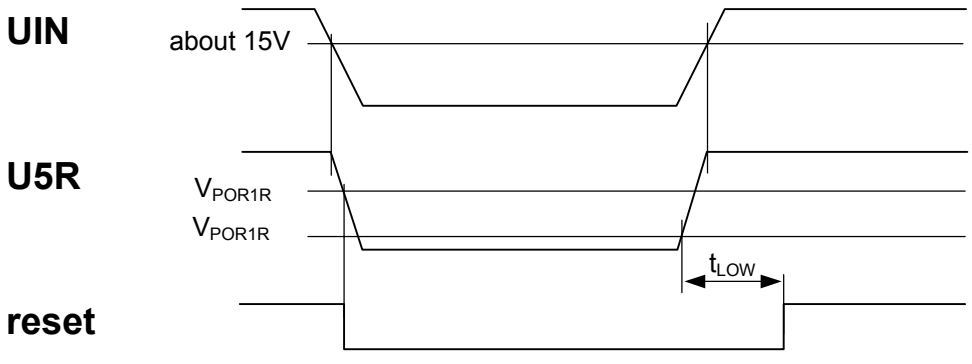

Figure 17: Power-On Behavior (all modes)

Note: The power-on reset circuit has a threshold voltage reference. This reference matches the process tolerance of the logic levels and must not be very accurate. All values depend slightly on the raise and fall time of the supply voltage.

3.11.2 Logic controlled Reset

The IC also becomes reset after reception of *Reset_Slave* or *Broadcast_Reset* commands, expiration of the (enabled) Communication Watchdog or entering of a forbidden state machine state (i.e. due to heavy EMI).

Note: In case the Addressing Channel is activated and the AC Current Input Mode is selected, *Reset_Slave* and *Broadcast_Reset* calls are processed differently than in normal operation! See corresponding explanations in chapter *3.3 Addressing Channel Input IRD* on page 22.

3.11.3 External Reset

The IC can be reset externally by pulling the DSR pin LOW for more than a minimum reset time. The external reset input function is provided in every operational mode of the IC – Slave Mode, Master Mode, Repeater Mode and Monitor Mode. The following signal timings apply:

Table 32: Timing of external reset

Symbol	Parameter	Min	Max	Unit	Note
$t_{noRESET}$	DSR LOW time for no reset initiation		35	µs	
t_{RESET}	Reset execution time, DSR H/L transition to Hi-Z output drives at DO0...DO3, P0…P3		44	µs	
t_{INIT}	State Machine initialization time after reset (E²PROM read out)		2	ms	

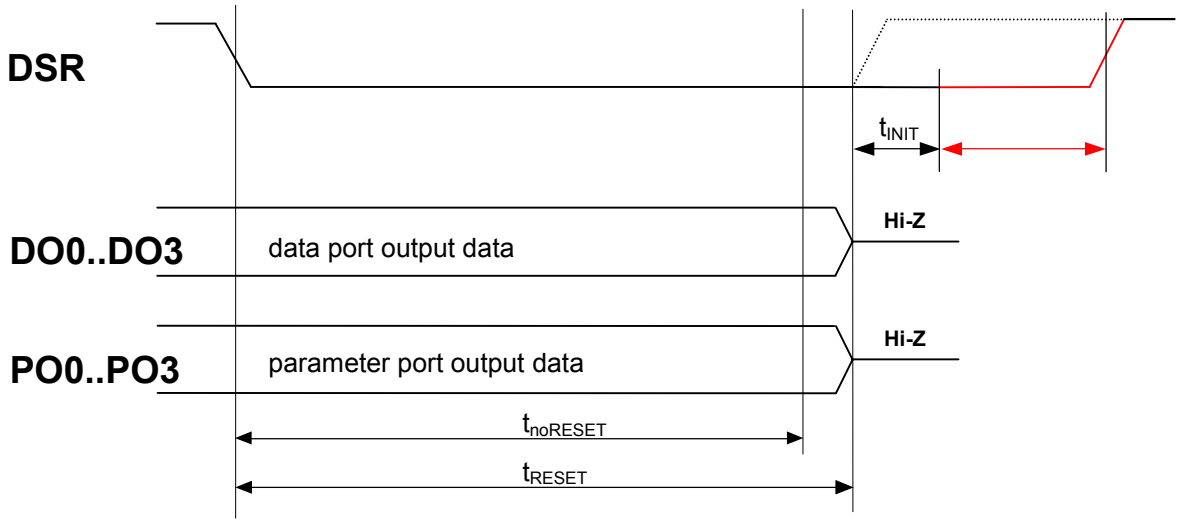

Figure 18: **Timing diagram external Reset via DSR**

In contrast to the A²SI, the external reset is generated "edge sensitive" to the expiration of the t_{RESET} timer. The initialization procedure is starting immediately after the event, independent of the state of DSR. A Serious Peripheral Fault is recognized in *Slave Mode* if DSR still remains LOW after t_{RESET} + t_{INIT}. The corresponding error state display is described in chapter *3.9 LED outputs* on page 40.

3.12 UART

The *UART* performs a syntactical and timing wise analysis of the received telegrams at both telegram input channels (AS-i input, Addressing Channel input), converts the pulse coded AS-i input signal into a Manchester-II-coded bit stream and provides the Receive Register with decoded telegram bits.

The UART also realizes the Manchester-II-coding of a slave answer (Slave Mode only) and controls the telegram data paths at the different operational modes of the IC (Slave Mode, Master Mode, Repeater Mode, Monitor Mode).

In Slave Mode data communication takes place on the AS-i input and AS-i output ports (AS-i receiver + AS-i transmitter) by default. The Addressing channel (IRD input + LED1 output) can be activated by a Magic Sequence sent to the IRD input (see chapter *3.3 Addressing Channel Input IRD*). If the Addressing Channel is activated, the AS-i channel is turned inactive. Re-activation of the AS-i channel requires a reset of the IC.

In Master-, Repeater- and Monitor Mode the output signal of the manchester coder (AS-i pulse to MAN signal conversion) is resynchronized and forwarded to pin LED1. Any pulse timing jitters of the received AS-i signal become removed, as long as they stay within the specified maximum limits. If the received AS-i telegram does not pass one of the different error checks (see detailed description below), the LED1 output is distorted in such a way that it will not form any AS-i telegram signal anymore.

In Master-, Repeater- and Monitor Mode the ASI4U provides a simple interface function between AS-i channel and Addressing Channel. The channel receiving an input signal first while the UART is in idle state (no active communication) is activated and locked until a communication pause is detected on that channel.

3.12.1 AS- i input channel

The comparator stages at the AS-i-line receiver generate two pulse-coded output signals (*p_pulse*, *n_pulse*) disjoining the positive and negative telegram pulses for further processing. To reduce UART sensitivity on erroneous spike pulses, pulse filters suppress any *p_pulse*, *n_pulse* activity of less than 750 ns width.

After filtering, the *p_pulse* and *n_pulse* signals are checked in accordance with the AS-i Complete Specification for following telegram transmission errors:

Start_bit_error — The initial pulse following a pause must have negative polarity. Violation of this rule is detected as *Start_bit_error*. The first pulse is the reference for bit decoding. The first bit detected shall be of the value 0.

Alternating_error — Two consecutive pulses must have different polarity. Violation of this rule is detected as *Alternating_error*.

Note: A negative pulse shall be followed by a positive pulse and vice versa.

Timing_error — Within any master request or slave response, the digital pulses that are generated by the receiver are checked to start in periods of $(n * 3\mu s)^{+1.500\mu s}_{-0.875\mu s}$ after the start of the initial negative pulse, where n = 1 ... 26 for a master request and n = 1 ... 12 for a slave response. Violation of this rule is detected as *Timing_error.*

Note: There is a certain pulse timing jitter associated with the receiver output signals (compared to the analog signal waveform) due to sampling and offset effects at the comparator stages.

In order to take the jitter effects into account, the timing tolerance specifications differ slightly from the definitions of the AS-i Complete Specification.

No_information_error — Derived from the Manchester-II-Coding rule, either a positive or negative pulse shall be detected in periods of $(n * 6\mu s)^{+1.500\mu s}_{-0.875\mu s}$ after the start of the initial negative pulse, where n = 1 ... 13 for a master request and n = 1 ... 6 for a slave response. Violation of this rule is detected as *No_information_error*.

Note: The timing specification relates to the receiver comparator output signals. There is a certain pulse timing jitter in the digital output signals (compared to the analog signal waveform) due to sampling and offset effects at the comparator stages.

In order to take the jitter effects into account, the timing tolerance specifications differ slightly from the definitions of the AS-i Complete Specification.

Parity_error	The sum of all information bits in master requests or slave responses (excluding start and end bits, including parity bit) must be even. Violation of this rule is detected as *Parity_error.*
End_bit_error	The pulse to be detected $(n * 6\mu s)^{+1.500\mu s}_{-0.875\mu s}$ after the start pulse shall be of positive polarity, where n = 13 (78 µs) for a master request and n = 6 (36 µs) for a slave response. Violation of this rule shall be detected as an *End_bit_error.* Note: This stop pulse shall finish a master request or slave response.
Length_error	Telegram length supervision is processed as follows. If during the first bit time after the end pulse of a master request (equivalent to the 15th Bit time) for synchronized slaves (during the first three bit times for not synchronized slaves, equivalent to the Bit times 15 to 17) or during the first bit time after the end pulse of a slave response (equivalent to the 8th Bit time) a signal different from a pause is detected, a *Length_error* is detected.

If at least one of these errors occurs, the received telegram is treated invalid. In this case, the UART will not generate a Receive Strobe signal, move to asynchronous state and wait for a pause at the AS-i line input. After a pause was detected, the UART is ready to receive the next telegram.

Receive Strobe signals are generally used to validate the correctness of the received data. In Master- and Monitor Mode the signals are visible at the *Parameter Ports* for further processing by external circuitry. Corresponding Parameter Port configurations can be found at Table 17 on page 28.

In Slave Mode, a *Master Receive Strobe* starts the internal processing of a master request. If the UART was in asynchronous state before the signal was generated, it changes to synchronous state thereafter. In case the received slave address matches the stored address of the IC, the transmitter is turned on by the Receive Strobe pulse, letting the output driver settle smoothly at the operation point.

3.12.2 Addressing Channel

The signal logic of the Addressing Channel follows the definition of a Manchester-II-coded AS-i signal. The default state (inactive) is defined by a logic high value. Depending on the input mode of the IRD pin (voltage/current) a logic HIGH is either represented by a voltage signal > 3.5V or an input current of I_{IRD_Offset} + $I_{IRD\_Amplitude}$.

A valid communication is started on a falling edge of the input signal (middle of Start Bit) and ended on a rising signal edge (middle of End Bit) and followed by the detection of a telegram pause. The information is represented by falling (='0') or rising ('1') signal transitions in the middle of every bit time (see Figure 19)

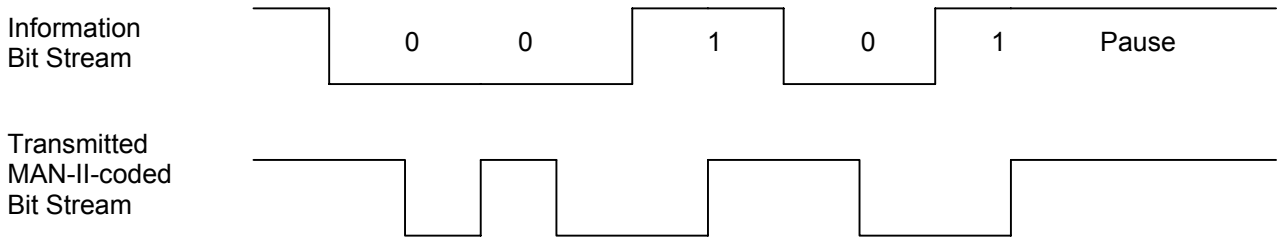

Figure 19: Manchester-II-Modulation principle

Equivalent to the AS-i input channel, the signals received at the Addressing Channel input (IRD pin) are checked for telegram transmission errors. The checking, however, is only performed in Slave Mode. In Master-, Repeater- and Monitor Mode, the IRD signal is checked only for logical correctness. It is directly forwarded to the AS-i line transmitter avoiding any additional logic delays.

Note: Because the telegram checking is disabled on the Addressing Channel in Master-, Repeater- and Monitor Mode, corresponding Receive Strobe signals are neither displayed at the Parameter Ports nor generated for internal purposes.

The master control logic must care to deliver correctly timed MAN-signals, ensuring that the resulting AS-i telegrams fulfill the specified timing limits.

Following telegram transmission errors are detected in Slave Mode:

Start_bit_error — The initial signal transition (after a pause) must be of falling edge. Violation of this rule is detected as *Start_bit_error*.

No_information_error — Within a received telegram, signal transitions (of rising or falling edge) must occur in periods of $(n * 6\mu s)^{+2.000\mu s}_{-1.000\mu s}$ after the initial falling slope, where n = 1 ... 13. Violation of this rule is detected as *No_information_error*.

Note: The Addressing Channel input (IRD) only accepts master requests in Slave Mode.

Parity_error — The sum of all information bits in master requests (excluding start and end bits, including parity bit) must be even. Violation of this rule is detected as *Parity_error*.

End_bit_error — The signal transition to be detected 13 * 6 µs (78 µs) after the initial falling start transition, shall be of rising slope. Violation of this rule is detected as an *End_bit_error*.

Note: This stop transition shall finish the master request.

Length_error — If during the first bit time after the end bit of a master request (equivalent to the 15th Bit time) for synchronized slaves (during the first three bit times for not synchronized slaves, equivalent to the Bit times 15 to 17) a signal different from a pause is detected, a *Length_error* is detected.

3.13 Main State Machine

The State Machine controls the overall behavior of the IC. Depending on the configuration data stored in the E²PROM, the State Machine activates one of the different IC operational modes and controls the digital I/O ports accordingly. In Slave Mode it processes the received master telegrams and computes the contents of the slave answer, if required. Table 6 on page 15 lists all master calls that are decoded by the ASI4U in Slave Mode.

To prevent the critical situation in which the IC gets locked in a not allowed state (i.e. by imission of strong electromagnetic radiation) and thereby could jeopardize the entire system, all prohibited states of the state machine will lead to an unconditioned logic reset which is comparable to the AS-i call "Reset Slave (RES)".

3.14 Communication Monitor/Watchdog

The IC contains an independent Communication Monitor that observes the processing of *Data_Exchange* and *Write_Parameter* requests. If no such requests have been processed for more than 40.960ms (+5%) the Communication Monitor recognizes a No Data/Parameter Exchange status and turns the red status LED (LED1) on. Any following *Data_Exchange* or *Write_Parameter* request will let the Communication Monitor start over and turn the red status LED off.

The Communication Monitor is only activated at slave addresses unequal to zero (0) and while the IC is processing the first *Write_Parameter* request after initialization. It becomes deactivated at any IC Reset or after the reception of a *Delete_Address* Request.

If the *Watchdog_Active* flag (E²PROM Firmware Area) is set or the *P0_Watchdog_Activation* flag is set and Parameter Port P0 is logic high, the Communication Monitor is switched to the so-called Watchdog Mode.

If the Communication Monitor detects a No Data/Parameter Exchange status in active Watchdog Mode, it immediately invokes an unconditioned IC Reset, switching all Data and Parameter Outputs inactive, generating corresponding Data and Parameter Strobe signals, setting the *Data_Exchange_Disable* flag and starting the IC initialization procedure.

In order to resume to normal Data Port communication after *a* Watchdog IC Reset, the master has to send a *Write_Parameter* request again before Data Port communication can be reestablished. This ensures new parameter setup of possibly connected external circuitry.

3.15 Toggle watchdog for 4I/4O processing in Extended Address Mode

As described in chapter 3.7.5 on page 34 a special 4I/4O data processing is supported in Extended Address Mode. The transmission of a 4 bit wide output word is achieved by alternation of a high and a low nibble in consecutive transactions. To ensure that both output nibbles become refreshed continuously by the Master, the alternation of the I2 bit in the *Data_Exchange* call can be supervised by an I2 toggle watchdog in the IC.

The Toggle Watchdog is enabled at slave addresses unequal to zero (0) and while the IC is processing the first data output event after initialization. It becomes disabled at any IC Reset or after the reception of a *Delete_Address* request.

The Toggle Watchdog function becomes activated only if the IC is operated in 4I/4O Mode (ID_code = 0xA, Ext_Addr_4I/4O_Mode = '1') and if either the *Watchdog_Active* flag is set in the E²PROM or the *P0_Watchdog_Activation* flag (also E²PROM) is set and Parameter Port P0 is logic HIGH.

If there is no alternation of bit I2 for **327ms (+16ms)** at any time after the enable event, an activated Toggle Watchdog invokes an unconditioned IC Reset, switching all Data and Parameter Outputs inactive, generating corresponding Data and Parameter Strobe signals, setting the *Data_Exchange_Disable* flag and starting the IC initialization procedure. Thus, the reaction of the IC is the same as for an expired Communication Watchdog.

3.16 Write Protection of ID_Code_Extension_1

The *ID_Code_Extension_1* register can either be manufacturer configurable or user configurable.

- If the flag *ID_Code1_Protect* is set ('1') in the firmware area of the E²PROM, *ID_Code_Extension1* is manufacturer configurable.

  In this case the slave response to a *Read_ID_Code_1* request is constructed out of the data stored in the *Protected_ID_Code_Extension1* register in Firmware Area of the E²PROM.

  It doesn't matter which data is stored in the *ID_Code_Extension1* register in the User Area. The IC will always respond with the protected manufacturer programmed value.

There is one exception to this principle. If the IC is operated in Extended Address Mode, Bit3 of the returned slave response is taken from the *ID_Code_Extension1* register in the *User Area*. This is because Bit 3 functions as A/B Slave selector bit in this case and must remain user configurable.

To ensure consistency of *ID_Code_Extension1* stored in the data image of Master as well as in the E²PROM of the slave, the ASI4U will not process a *Write_ID_Code1* request if the data sent does not match the data that is stored in protected part of the *ID_Code_Extension1* register. It will neither access the E²PROM nor send a slave response in this case.

Note: As defined in the AS-i Complete Specification a modification of the A/B Slave selector bit must be performed bit selective. That means the AS-i Master must read the *ID_Code_Extension1* first, modify Bit3 and send the new 4 bit word that consists of the modified Bit3 and the unmodified Bits 2 … 0 back to the slave.

- If the *ID_Code1_Protect* flag is not set ('0'), *ID_Code_Extension1* is completely user configurable. The data to construct the slave response to a *Read_ID_Code_1* request is completely taken from the *ID_Code_Extension1* register in the user area.

  In this configuration a *Write_ID_Code1* request will always be answered and initiate an E²PROM write access procedure.

3.17 Power Supply

The power supply block provides a sensor supply, which is inductively decoupled from the AS-i bus voltage, at pin UOUT. The decoupling is realized by an electronic inductor circuit, which basically consists of a current source and a controlling low pass. The time constant of the low pass, that has influence to the resulting input impedance at pin UIN, can be adjusted by an external capacitor at pin CAP.

The electronic inductor can be turned off if pin CAP is connected to 0V. This shuts down the current source between UIN and UOUT requiring an external connection between UIN and UOUT for proper IC operation. The possibility to turn off the electronic inductor is helpful to realize high symmetrical extended power applications (i.e. AS-i connected actuators with large load currents).

Overloading the electronic inductor for more than 2 seconds by drawing too much current shuts down the entire IC in order to avoid a deviation of the input impedance, which would have negative influence to the communication of the remaining AS-i network clients. The fail-safe shutdown mode can only be left by power cycling the AS-i supply voltage.

A second function of the power supply block is to generate a regulated 5V supply for operation of the internal logic and some analog circuitry. The voltage is provided at pin U5R an can be used to supply external circuitry as well, as long as the current requirements stay within in the specified limits. See Table 33 below. Because the 5V supply is generated out of the decoupled sensor supply at UOUT, the current drawn at U5R has to be subtracted from the total available load current at UOUT.

The power supply dissipates the major amount of power:

$$Ptot = V_{Drop} * I_{UOUT} + (V_{UOUT}-5V) * I_{5V}$$

In total, the power dissipation shall not exceed the specified values of chapter 1.1.

To cope with fast internal and external load changes (spikes) external capacitors at UOUT and U5R are required. The 0V pin defines the ground reference voltage for both UOUT and U5R.

3.17.1 Voltage Output Pins UOUT and U5R

Table 33: Properties of voltage output pins UOUT and U5R

Symbol	Parameter	Min	Max	Unit	Note
V_{UIN}	Positive supply voltage for IC operation	16	33.1	V	[1]
V_{DROP}	Voltage drop from pin UIN to pin UOUT	5.5 [2]	6.7 [2]	V	V_{UIN} > 22V
V_{UOUT}	UOUT output supply voltage	V_{UIN}- $V_{DROPmax}$	V_{UIN}- $V_{DROPmin}$	V	$I_{UOUTmax}$
V_{UOUTp}	UOUT output voltage pulse deviation		1.5	V	[2]
t_{UOUTp}	UOUT output voltage pulse deviation width		2	ms	[2]
V_{U5R}	5V supply voltage	4.5	5.5	V	
I_{UOUT}	UOUT output supply current	0	55 [2]	mA	I_{U5R} = 0 [2]
I_{5V}	U5R output supply current	0	4	mA	
I_o	Total output current I_{UOUT} + I_{5V}		55	mA	
I_{UOUTS}	Short circuit output current	50		mA	
C_{BUOUT}	Blocking capacitance at UOUT	10	470	µF	
C_{B5V}	Blocking capacitance at U5R	1		µF	

[1] Parameter copied from *Table 2: Operating Conditions*

[2] C_{UOUT} = 10µF, output current switches from 0 to $I_{UOUTmax}$ and vice versa

3.17.2 Input Impedance (AS-i bus load)

The following parameters are determined with short cut between the pins ASIP and UIN and the pins ASIN and 0V, respectively.

Table 34: AS-i Bus Load Properties

Symbol	Parameter	Min	Max	Unit	Note
R_{IN1}	Equivalent resistor of the IC	13,5		kΩ	1,2
L_{IN1}	Equivalent inductor of the IC	13,5		mH	1,2
C_{IN1}	Equivalent capacitor of the IC		30	pF	1,2
R_{IN2}	Equivalent resistor of the IC	13,5		kΩ	1,2
L_{IN2}	Equivalent inductor of the IC	12	13,5	mH	1,2
C_{IN2}	Equivalent capacitor of the IC		15 + (L-12mH)*10pF/mH	pF	1,2
C_{Zener}	Parasitic capacitance of the external over-voltage protection diode (Zener diode)		20	pF	1

[1] The equivalent circuit of a slave, which is calculated from the impedance of the IC and the paralleled external over-voltage protection diode (Zener diode), has to satisfy the requirements of the AS-i Complete Specification for Extended Address Mode slaves.

[2] Subtracting the maximum parasitic capacitance of the external over voltage protection diode (20pF) either the triple R_{IN1}, L_{IN1} and C_{IN1} or the triple R_{IN2}, L_{IN2} and C_{IN2} has to be reached by the IC to fulfill the AS-i Complete Specification.

Table 35: CAP pin parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CAP_IN}	Input voltage range	-0.3		V_{U5R}	V	
C_{CAP}	External decoupling capacitor		47		nF	

Note: In some application a serial to C_{CAP} connected resistor may enhance the impedance behavior of the internal electronic inductor. Depending of the application this resistor has to be dimensioned between 10 … 100Ω .

The decoupling capacitor defines an internal low-pass filter time constant; lower values decrease the impedance but improve the turn-on time. Higher values do not improve the impedance but do increase the turn-on time.

The turn-on time also depends on the load capacitor at UOUT. After connecting the slave to the power the capacitor is charged with the maximum current I_{UOUT}. The impedance will increase when the voltage allows the analog circuitry to fully operate.

3.18 Thermal and Overload Protection

The IC continuously observes its silicon die temperature. If the temperature rises above around 140°C for more than 2 seconds the IC will be put into shutdown and stay there until the next power-on reset occurs.

The circuit also becomes shut down if U_{OUT} is overloaded (e.g. shorted to GND) for more than 2 seconds.

Table 36: Shutdown Temperature

Symbol	Parameter	Min	Max	Unit	Note
T_{Shut}	Chip temperature for over temperature shut down	125	160	°C	

4 Application Circuits

The following figures show typical application cases of the ASI4U. Please note that these schematics show only principle circuit drafts. For more detailed application information see the separate **ASI4U Application Notes** document.

Figure 20 outlines a standard slave application circuit compliant to the first AS-i IC.

Figure 21 shows an extended power application circuit with externally decoupled sensor supply.

A Master Mode application is shown in Figure 22.

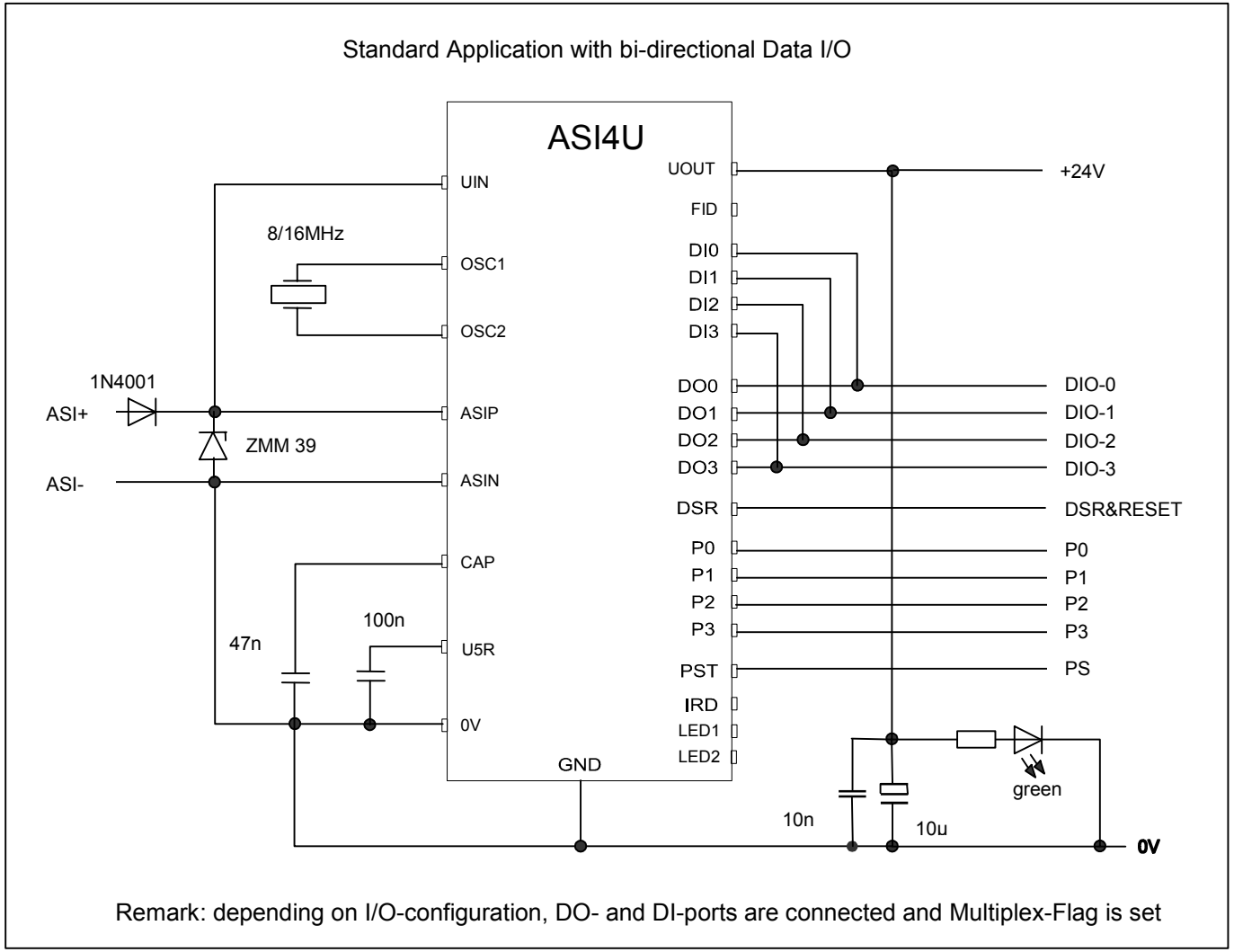

Figure 20: Standard Application circuit with bi-directional Data I/O

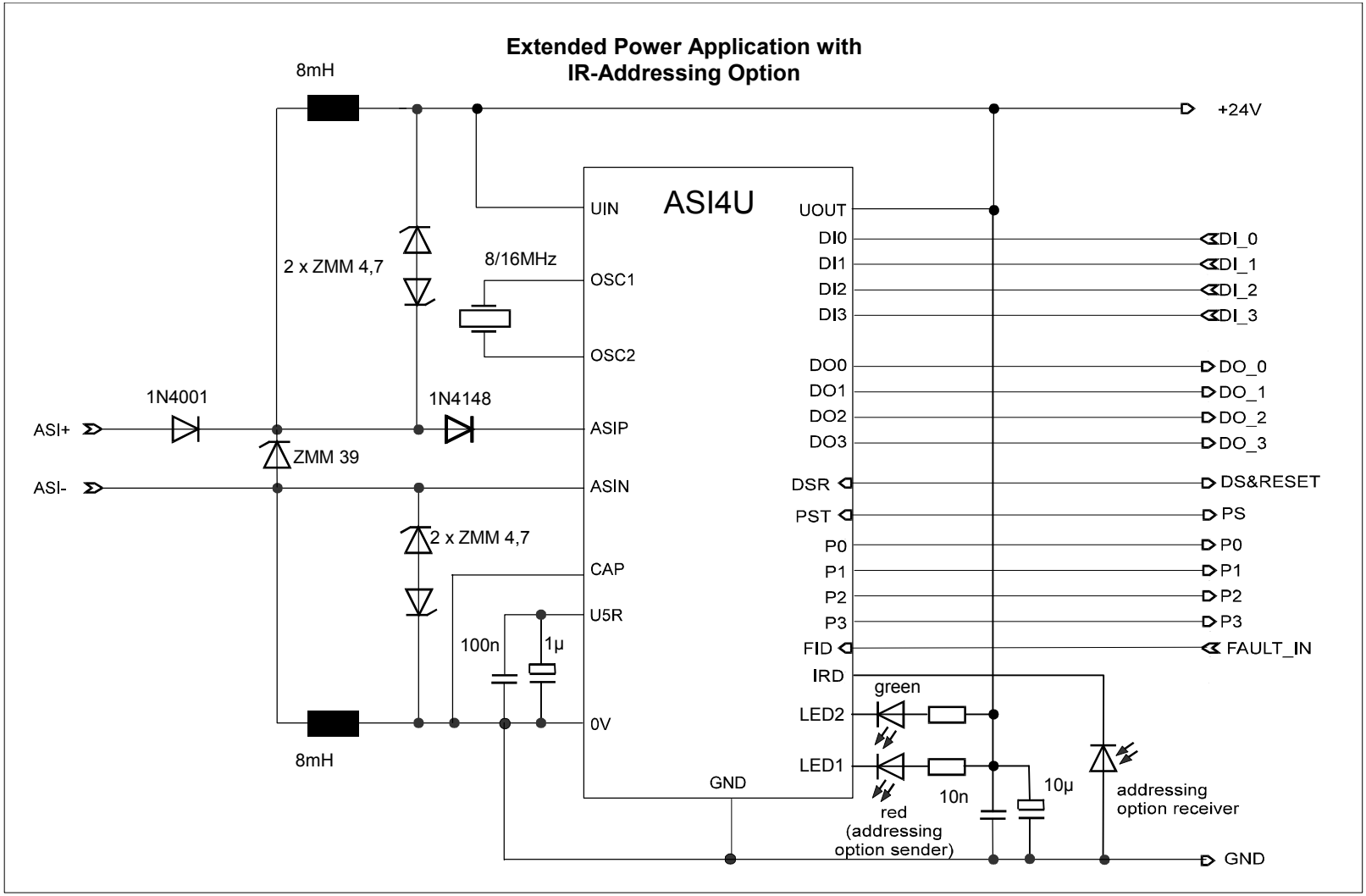

Figure 21: Extended power application circuit

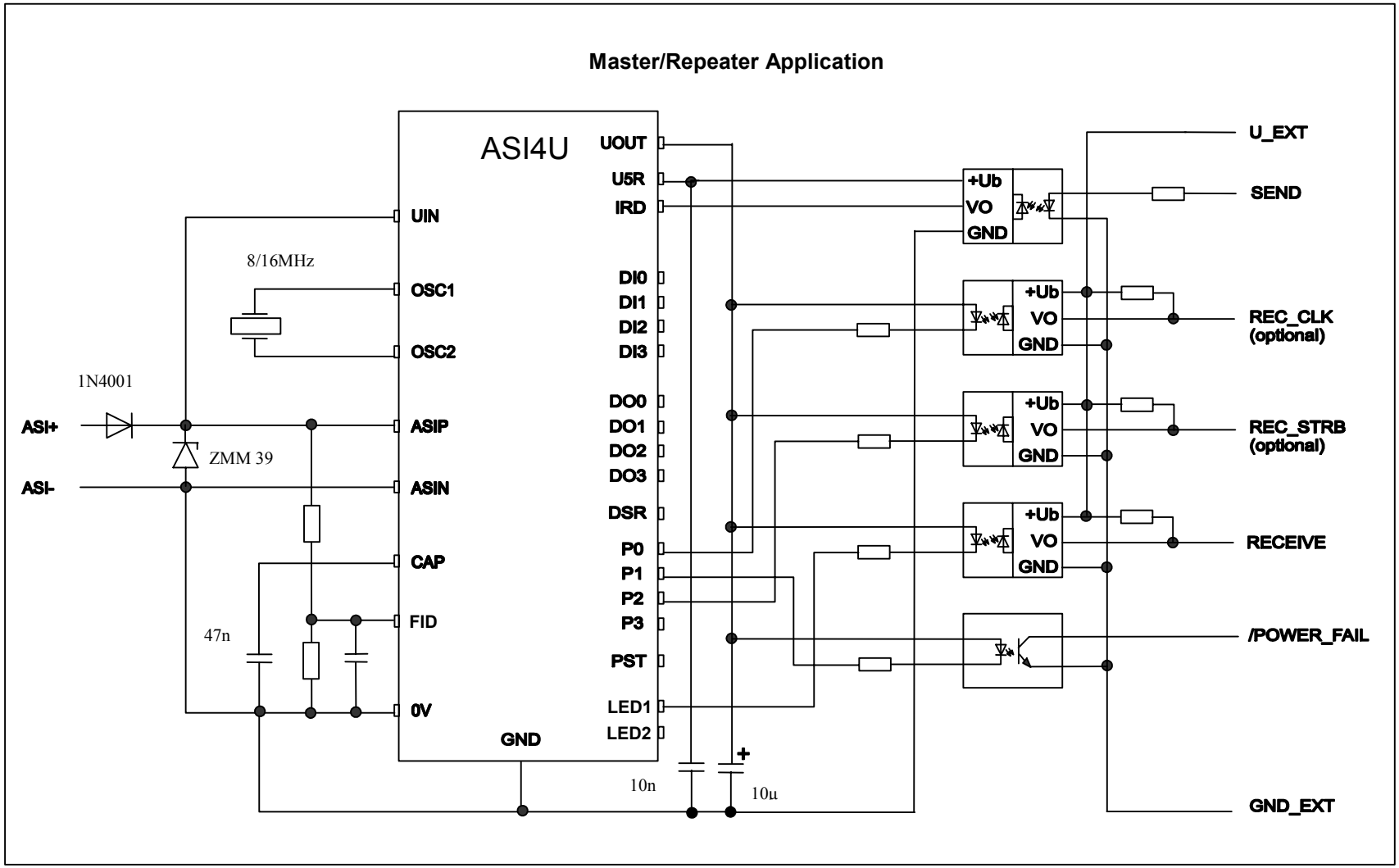

Figure 22: ASI4U Master Mode Application

5 Package Outline

The IC is packaged in a 28 pin SSOP-package (Figure 23) that has the dimensions as shown in Figure 24 and Table 37.

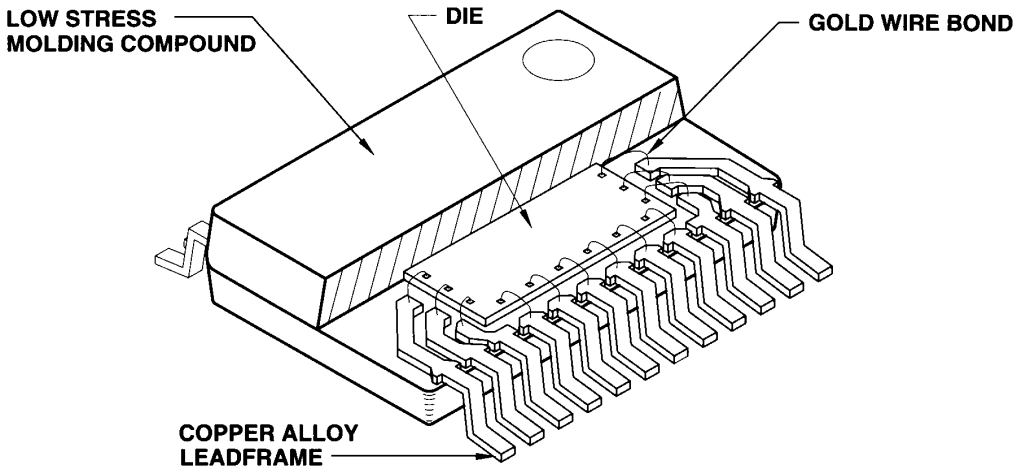

Figure 23: SSOP Package

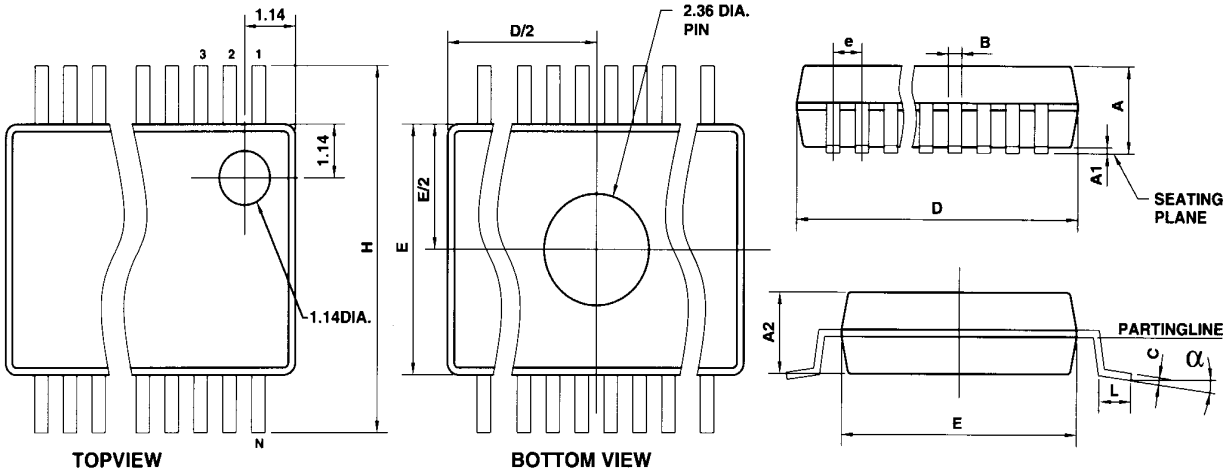

Figure 24: Package Outline Dimensions

Table 37: Package Dimensions (mm)

Symbol	A	A1	A2	B	C	D	E	e	H	L	α
Nominal	1.86	0.13	1.73	0.30	0.15	10.20	5.30	0.65 BSC	7.80	0.75	4°
Maximum	1.99	0.21	1.78	0.38	0.20	10.33	5.38		7.90	0.95	8°
Minimum	1.73	0.05	1.68	0.25	0.13	10.07	5.20		7.65	0.55	0°

6 Package Marking

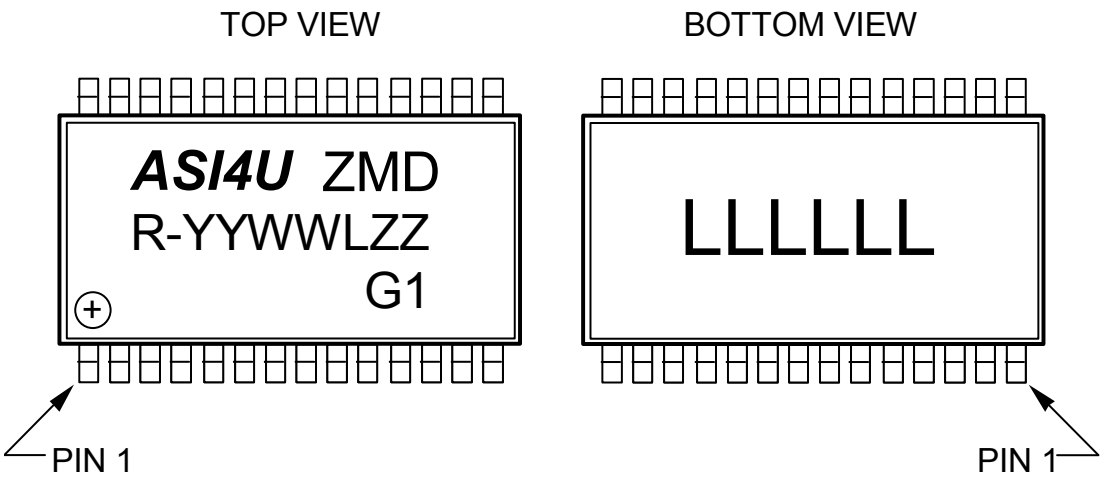

Figure 25: Package Marking

Top Marking:	ASI4U	Product name
	ZMD	Manufacturer
	R-	Revision code
	YYWW	Date code (year and week)
	L	Assembly location
	ZZ	Traceability code
	G1	"green" RoHS-compliant package
Bottom Marking:	LLLLLL	ZMD Lot Number

For ICs pre-programmed to Master Mode the string "-M" follows the product name.
For ICs capable for an operation temperature up to 105°C the string "-E" follows the product name.

7 Ordering Information

Ordering Code	Package	RoHS Conform	Op. Temp. Range	Delivery Form	Version	Device Marking***	Min. Order Quantity (MOQ)	Remarks
ASI4UC-ST	SSOP28/5,3mm	N	-25° .. +85°C	Tube	Standard	ASI4U ZMD	705	(47 parts/tube)
ASI4UC-SR	SSOP28/5,3mm	N	-25° .. +85°C	Tape&Reel	Standard	C-YYWWLZZ	1500	
ASI4UC-G1-ST	SSOP28/5,3mm	Y	-25° .. +85°C	Tube	Standard	ASI4U ZMD	705	(47 parts/tube)
ASI4UC-G1-SR	SSOP28/5,3mm	Y	-25° .. +85°C	Tape&Reel	Standard	C-YYWWLZZ	1500	
ASI4UC-G1-SR-7	SSOP28/5,3mm	Y	-25° .. +85°C	Tape&Reel	Standard	G1	500	7 inch reel
ASI4UC-G1-MT**	SSOP28/5,3mm	Y	-25° .. +85°C	Tube	Master	ASI4U-M ZMD	705	(47 parts/tube)
ASI4UC-G1-MR**	SSOP28/5,3mm	Y	-25° .. +85°C	Tape&Reel	Master	C-YYWWLZZ	1500	
						G1		
ASI4UC-E-G1-ST**	SOP28/300mil	Y	-25° .. +105°C	Tube	Standard	ASI4U-E ZMD	540	(27 parts/tube)
ASI4UC-E-G1-SR**	SOP28/300mil	Y	-25° .. +105°C	Tape&Reel	Standard	C-YYWWLZZ	1000	
						G1		
ASI4U Samples	SSOP28/5,3mm	Y/N*	-25° .. +85°C	sample box or tube	Standard	ASI4U ZMD C-YYWWLZZ [G1]*		

* Dependent on current inventory samples may be delivered RoHS conform (marked with "G1") or not.
** Not available yet. Planed to be available Q3/2006.
*** YYWW: Year / Workweek (Datecode); ZZ: Traceability Code (AA, AB, ...).

8 Related Documents

- ASI4U Product Flyer
- ASI4U Safety Advice
- ZMD AS-i IC Ordering Guide

9 Related Products

- A2SI Universal AS-Interface IC
- A2SI-Lite Low-cost AS-Interface IC
- SAP5 Universal AS-Interface IC

10 Contact Information

10.1 ZMD Sales

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10.4 AS-International Association

Documentation and promotional materials as well as detailed technical specifications regarding the AS-Interface Bus Standard are available from:

AS-International Association:	Contact - Rolf Becker Zum Taubengarten 52 D-63571 Gelnhausen PO Box 1103 Zip (63551) Phone: +49 6051 47 32 12 Fax: +49 6051 4732 82 E-mail: info@as-interface.net Internet: www.as-interface.net

Refer to www.as-interface.net for contact information on local AS-Interface associations which provide special support within Europe, in the US and in Japan.

For the current revision of this document and for additional product information please look at www.zmd.biz.