Features

- Lead free versions available
- RoHS compliant (lead free version)*
- New Product Development
- Integrated Passive Device
- RF Low Pass Filter Performance
- ESD Protection to IEC61000-4-2 Spec.

BOURNS®

2FAD-C20R Series - Integrated Passive & Active Device using CSP

General Information

The 2FAD-C20R devices, manufactured using Thin Film On Silicon technology provide ESD protection and EMI filtering for the data port of portable electronic devices such as cell phones, modems and PDAs. The device incorporates six low pass filter channels. Each channel has a series 100 ohm resistor assuring a minimum of -30 dB attenuation from 800 MHz to 3 GHz. The device is suitable for EMI filtering of GSM, CDMA, W-CDMA, WLAN and Bluetooth frequencies.

Each external port of the six channels includes a back-to-back 6.5 Volt Zener diode for ESD protection. Two additional standalone 6.5 Volt Zener diodes are available for ESD protection on power lines or USB data ports. The ESD protection provided by the component enables an eight line data port to withstand a minimum ±8 KV Contact / ±15 KV Air Discharge when tested according to the ESD method specified in IEC 61000-4-2. The device measures 2.04 mm x 2.64 mm and is available in a 20 pin (4 x 5 array) CSP package intended to be mounted directly onto an FR4 printed circuit board. The CSP device meets typical thermal cycle and bend test specifications without the use of an underfill material.

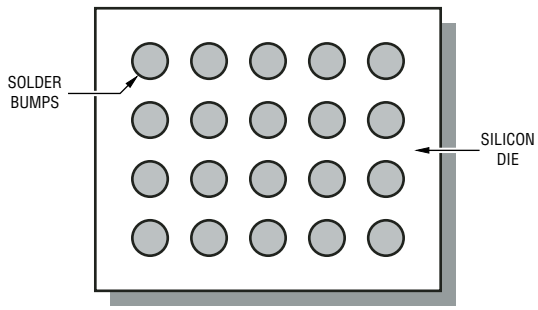


Figure 1 – CSP Format

Electrical & Thermal Characteristics

Electrical Characteristics (T_A = 25 °C unless otherwise noted)	**Symbol**	**Minimum**	**Nominal**	**Maximum**	**Unit**
Zener Diode Breakdown Voltage @ 1 mA	V_{BR}	6	7.2	8	V
Leakage Current @ 3 V	I_R			1	uA
ESD Performance (Note 1 & 2) Withstand: Contact Discharge		±8			kV
Withstand: Air Discharge		±15			kV
Let Through: Contact Discharge				±150	V
Let Through: Air Discharge				±150	V
Channel Specification Resistance	R	90	100	110	Ω
Capacitance @ 1 V & 1 MHz	C		50	55	pF
Filter Attenuation: 800 MHz – 3000 MHz		-30	-40		dB
Thermal Characteristics (T_A = 25 °C unless otherwise noted)					
Operating Temperature	T_J	-40	25	+85	°C
Storage Temperature	T_{stg}	-60	25	+125	°C
Total Power Dissipation @ 70 °C	P_D			100	mW

Note: 1. *The IEC 61000-4-2 test method will be adapted for component level testing. The device will provide the specified ESD protection performance on the "EXT1 – EXT8" pins only.*
2. *"Let Through" is a measure of the component of an incident ESD transient that the protection device allows through to the downstream circuitry.*

*RoHS Directive 2002/95/EC Jan 27 2003 including Annex

Mechanical Characteristics

This is a Silicon-based device and is packaged using chip scale packaging technology. Solder bumps, formed on the Silicon die, provide the interconnect medium from die to PCB. The bumps are arranged on the die in a regular grid formation. The grid pitch is 0.5 mm and the dimensions for the CSP packaged device are shown in Fig. 2 below.

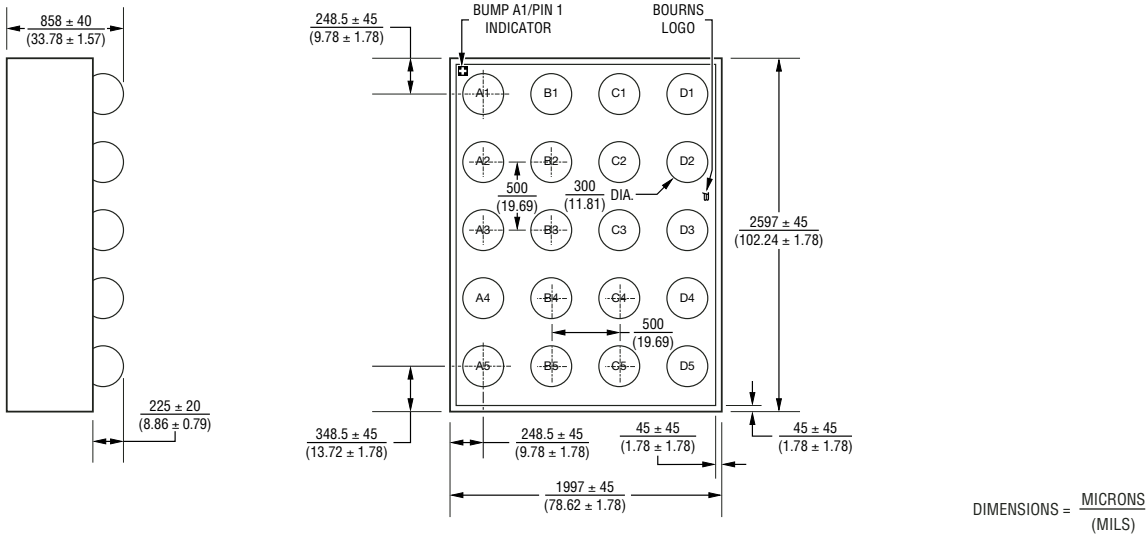


Fig. 2 – Device Mechanical Drawing

Reliability

Reliability data exists and continues to be gathered on an ongoing basis for Bourns Integrated Passive and Active Devices using CSP packaging.

"Package level" testing of the integrity of the solder joint is carried out on an independent Daisy-Chain test device. A 25-Pin Daisy Chain component is available from Bourns for this purpose. (Part No: 2TAD-C25R) This is a 5 x 5 array, featuring 0.5 mm pitch solder bumps. The Distance to Neutral Point (DNP) on that component is larger than that of the 2FAD-C20R and is thus deemed a worse case for Thermal Cycle testing.

"Silicon level" reliability performance will be assured by similarity to other integrated passive CSP devices from Bourns.

Individual Channel Schematic

This section contains the schematic (See Fig. 3 below) for the single channel in the integrated passive device. Note that the electrical parameters of primary interest are (a) DC Resistance (b) ESD performance and (c) low pass filter attenuation. In terms of DC parameters it should be noted that all resistor values have a tolerance of ±10 %. This schematic consists of a series 100 ohm resistance and two Back to Back Zener 6.5 Volt diodes for ESD protection.

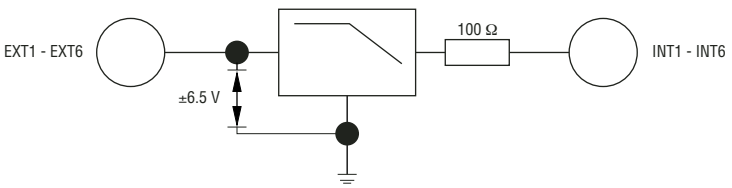


Fig. 3 - Channel Schematic

Key Design Parameters

Source Impedance: 50 Ω

Load Impedance: 50 Ω

DC Channel Resistance: 100 Ω ±10 %

Channel Capacitance: 55 pF Max @ 1 V & 1 MHz

V_{BR}: 6 V Min, 8 V Max @ I_{BR} = 1 mA.

I_R: 1 uA Max @ V_R = 3 V

Filter Attenuation: -30 dB Minimum
@ 800 MHz - 3000 MHz

Block Diagram

Figure 4 contains a block diagram of the CSP device. This diagram includes the pin names and basic electrical connections associated with each channel.

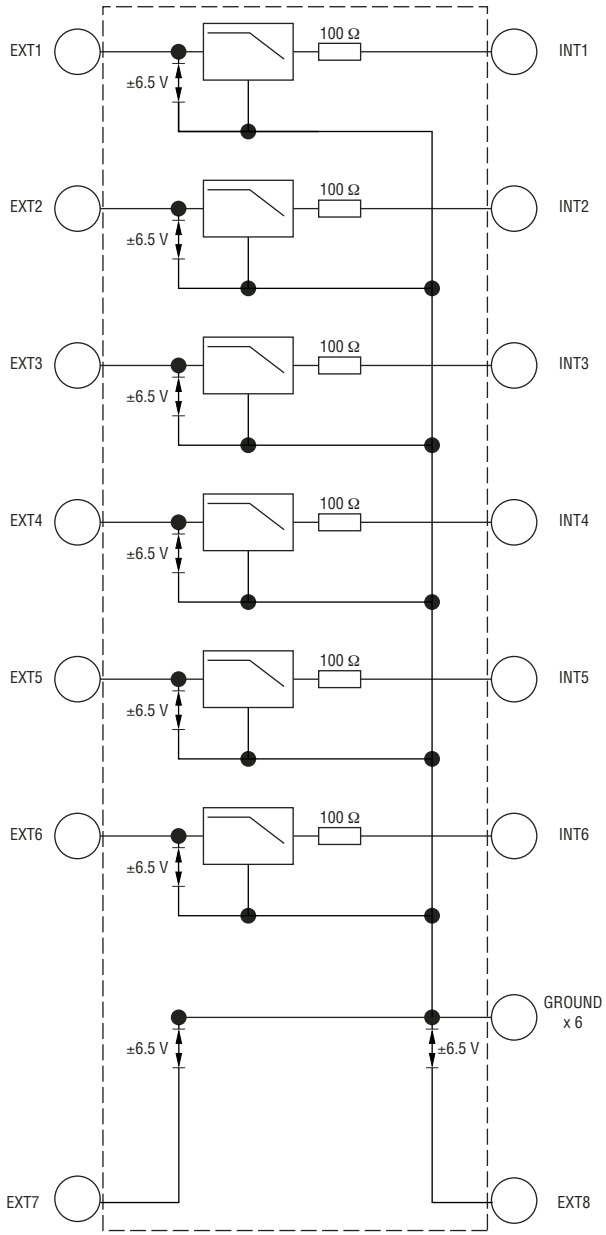


Fig. 4 – Device Block Diagram

Marking

The device will be laser marked on the backside according to the following Fig. 5 scheme below. Position A1, on the Bump Grid is located at the top left of the die when the die is orientated so that the mark is read in the normal fashion.

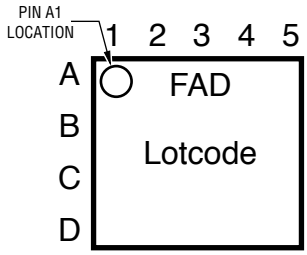
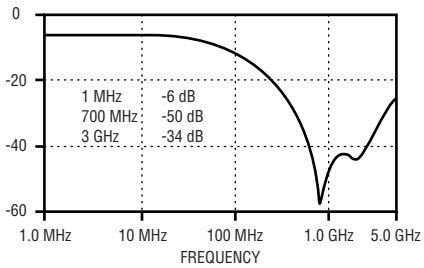


Fig. 5 – Backside Laser Mark

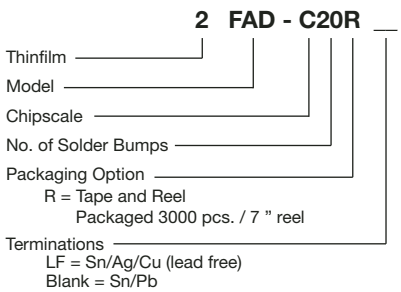
PCB Design and SMT Processing

Please consult Bourns' *Thin Film on Silicon using CSP* Users Guide Application Note for notes on PCB design and SMT processing.

2FAD-C20R Frequency Response



How to Order



Device Pin Out

The Pin-Out for the device is shown in Fig. 6. Note also that the device is shown with bumps facing up.

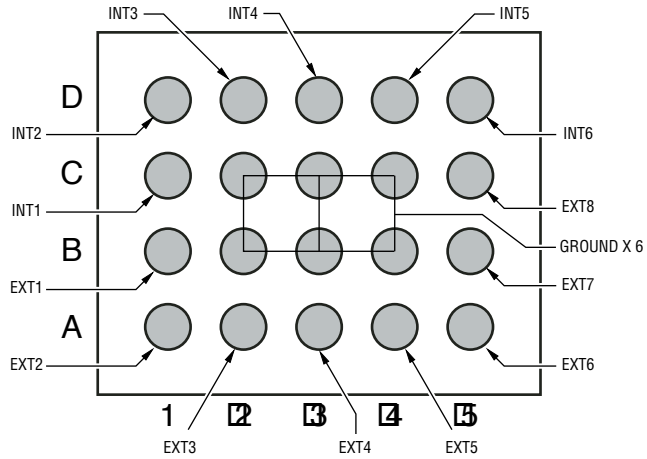


Fig. 6 (a) - Device Pin Out "Bumps Up" View

Function	Pin Out	Function	Pin Out
EXT2	A1	INT1	C1
EXT3	A2	Ground	C2
EXT4	A3	Ground	C3
EXT5	A4	Ground	C4
EXT6	A5	EXT8	C5
EXT1	B1	INT2	D1
Ground	B2	INT3	D2
Ground	B3	INT4	D3
Ground	B4	INT5	D4
EXT7	B5	INT6	D5

Fig. 6 (b) - Pin Listings

Packaging

The product will be dispensed in an 8 mm x 4 mm Tape and Reel format - see Fig. 7 diagram below. The Tape and Reel package will conform to customer specification.

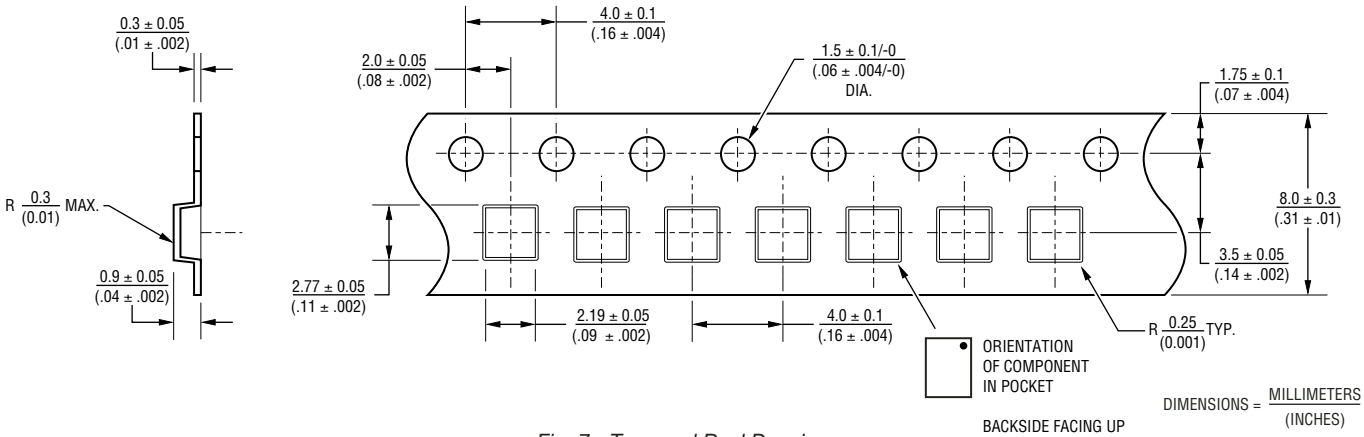


Fig. 7 - Tape and Reel Drawing

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