512Kx64 5V FLASH MODULE *PRELIMINARY**

FEATURES

- Access Times of 70, 90, 120, 150ns
- Packaging
  - 116 lead, 40mm square, Hermetic CQFP (Package 504)
- 100,000 Erase/Program Cycles Minimum
- Sector Architecture
  - 8 equal size sectors of 64KBytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- Organized as 512Kx64, user configurable as 1Mx32, 2Mx16, or 4Mx8.
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Programming. 5V ± 10% Supply.
- Low Power CMOS, 6.5mA Standby
- Embedded Erase and Program Algorithms
- TTL Compatible Inputs and CMOS Outputs
- Built-in Decoupling Caps for Low Noise Operation
- Page Program Operation and Internal Program Control Time
- Weight

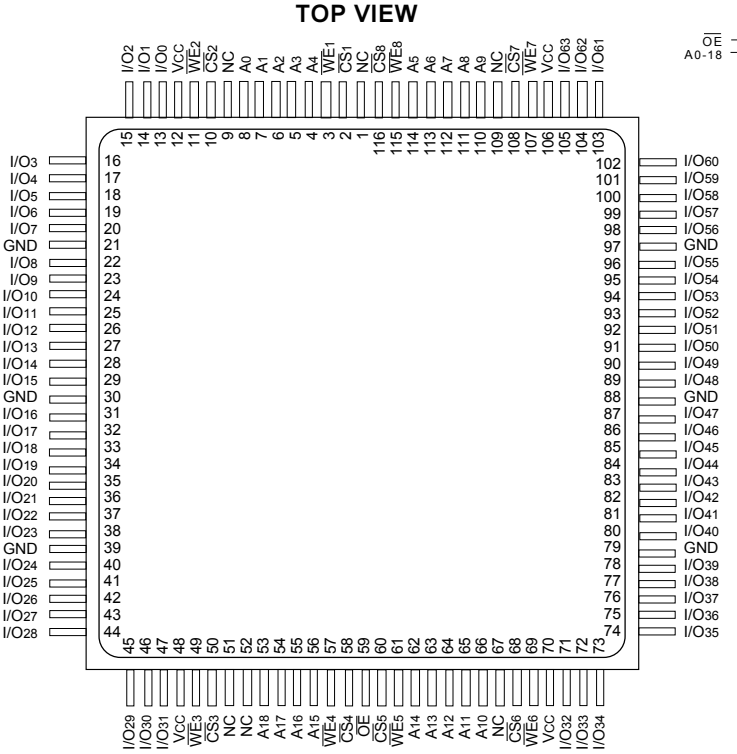
  WF512K64-XG4WX5 - 20 grams typical

* *This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

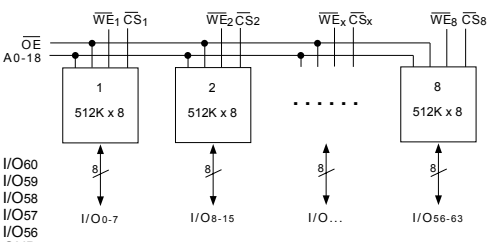
Note: Programming information available upon request.

FIG. 1 PIN CONFIGURATION FOR WF512K64-XG4WX5

TOP VIEW



BLOCK DIAGRAM



PIN DESCRIPTION

I/O0-63	Data Inputs/Outputs
A0-18	Address Inputs
$\overline{WE}_{1-8}$	Write Enables
$\overline{CS}_{1-8}$	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Operating Temperature	-55 to +125	°C
Supply Voltage Range (V_{CC})	-2.0 to +7.0	V
Signal voltage range (any pin except A_9) (2)	-2.0 to +7.0	V
Storage Temperature Range	-65 to +150	°C
Lead Temperature (soldering, 10 seconds)	+300	°C
Data Retention (Mil Temp)	20 years	
Endurance (write/erase cycles) (Mil Temp)	100,000 cycles min.	
A_9 Voltage for sector protect (V_{ID}) (3)	-2.0 to +14.0	V

NOTES:

1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may overshoot V_{SS} to -2.0 V for periods of up to 20ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5V. During voltage transitions, outputs may overshoot to Vcc + 2.0 V for periods of up to 20ns.
3. Minimum DC input voltage on A_9 pin is -0.5V. During voltage transitions, A_9 may overshoot Vss to -2V for periods of up to 20ns. Maximum DC input voltage on A_9 is +13.5V which may overshoot to 14.0 V for periods up to 20ns.

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	100	pF
$\overline{WE}$ capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
$\overline{CS}$ capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	100	pF

This parameter is guaranteed by design but not tested.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C
Operating Temp. (Ind.)	T_A	-40	+85	°C
A_9 Voltage for Sector Protect	V_{ID}	11.5	12.5	V

DC CHARACTERISTICS - CMOS COMPATIBLE

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LOx32}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
V_{CC} Active Current for Read (1)	I_{CC1}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz		380	mA
V_{CC} Active Current for Program or Erase (2)	I_{CC2}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}		480	mA
V_{CC} Standby Current	I_{CC4}	V_{CC} = 5.5, CS = V_{IH}, f = 5MHz		13	mA
V_{CC} Static Current	I_{CC3}	V_{CC} = 5.5, CS = V_{IH}		1.2	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0 mA, V_{CC} = 4.5		0.45	V
Output High Voltage	V_{OH1}	I_{OH} = -2.5 mA, V_{CC} = 4.5	0.85 x V_{CC}		V
Low V_{CC} Lock-Out Voltage	V_{LKO}		3.2	4.2	V

NOTES:

1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{CS}$ CONTROLLED

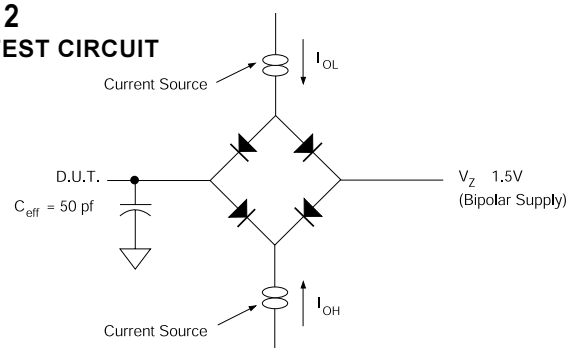
(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max			
Write Cycle Time	t_{AVAV}	t_{WC}	70		90		120		150		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		0		ns
Chip Select Pulse Width	t_{ELEH}	t_{CP}	45		45		50		50		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	45		45		50		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	45		45		50		50		ns
Chip Select Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300		300	µs
Chip and Sector Erase Time (2)	t_{WHWH2}			15		15		15		15	sec
Read Recovery Time	t_{GHEL}		0		0		0		0		ns
Chip Programming Time				11		11		11		11	sec
Chip Erase Time (3)				64		64		64		64	sec

NOTES:

1. Typical value for t_{WHWH1} is 7µs.
2. Typical value for t_{WHWH1} is 1sec.
3. Typical value for Chip Erase Time is 8sec.

FIG. 2
AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 ý.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
IOL & IOH are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{WE}$ CONTROLLED

(V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter	Symbol		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	70		90		120		150		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	45		45		50		50		ns
Address Setup Time	t_{AVWH}	t_{AS}	0		0		0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	45		45		50		50		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		0		ns
Address Hold Time	t_{WHAX}	t_{AH}	45		45		50		50		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	20		20		20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300		300	µs
Sector Erase Time (2)	t_{WHWH2}			15		15		15		15	sec
Read Recovery Time before Write	t_{GHWL}		0		0		0		0		ns
V_{CC} Set-up Time		t_{VCS}	50		50		50		50		µs
Chip Programming Time				11		11		11		11	sec
Output Enable Setup Time		t_{OES}	0		0		0		0		ns
Output Enable Hold Time (4)		t_{OEH}	10		10		10		10		ns
Chip Erase Time (3)				64		64		64		64	sec

NOTES:

1. Typical value for t_{WHWH1} is 7µs.
2. Typical value for t_{WHWH1} is 1sec.
3. Typical value for Chip Erase Time is 8sec.
4. For Toggle and Data Polling.

AC CHARACTERISTICS – READ ONLY OPERATIONS

(V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter	Symbol		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	70		90		120		150		ns
Address Access Time	t_{AVQV}	t_{ACC}		70		90		120		150	ns
Chip Select Access Time	t_{ELQV}	t_{CE}		70		90		120		150	ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		35		35		50		55	ns
Chip Select to Output High Z (1)	t_{EHQZ}	t_{DF}		20		20		30		35	ns
Output Enable High to Output High Z (1)	t_{GHQZ}	t_{DF}		20		20		30		35	ns
Output Hold from Address, $\overline{CS}$ or $\overline{OE}$ Change, whichever is First	t_{AXQX}	t_{OH}	0		0		0		0		ns

1. Guaranteed by design, but not tested

FIG. 3
AC WAVEFORMS FOR READ OPERATIONS

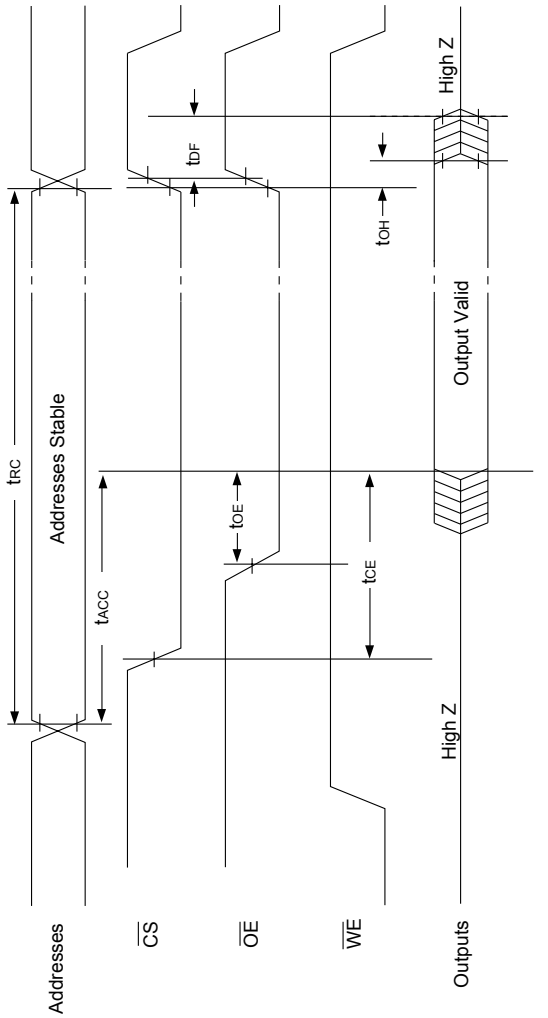
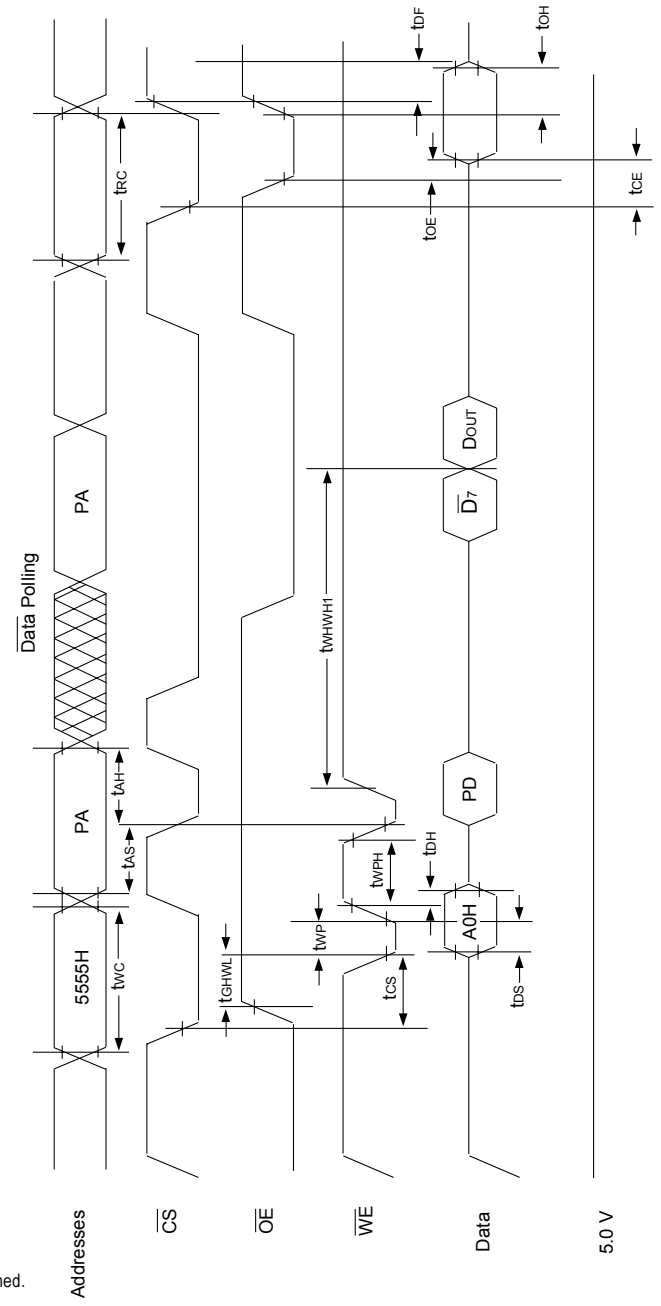
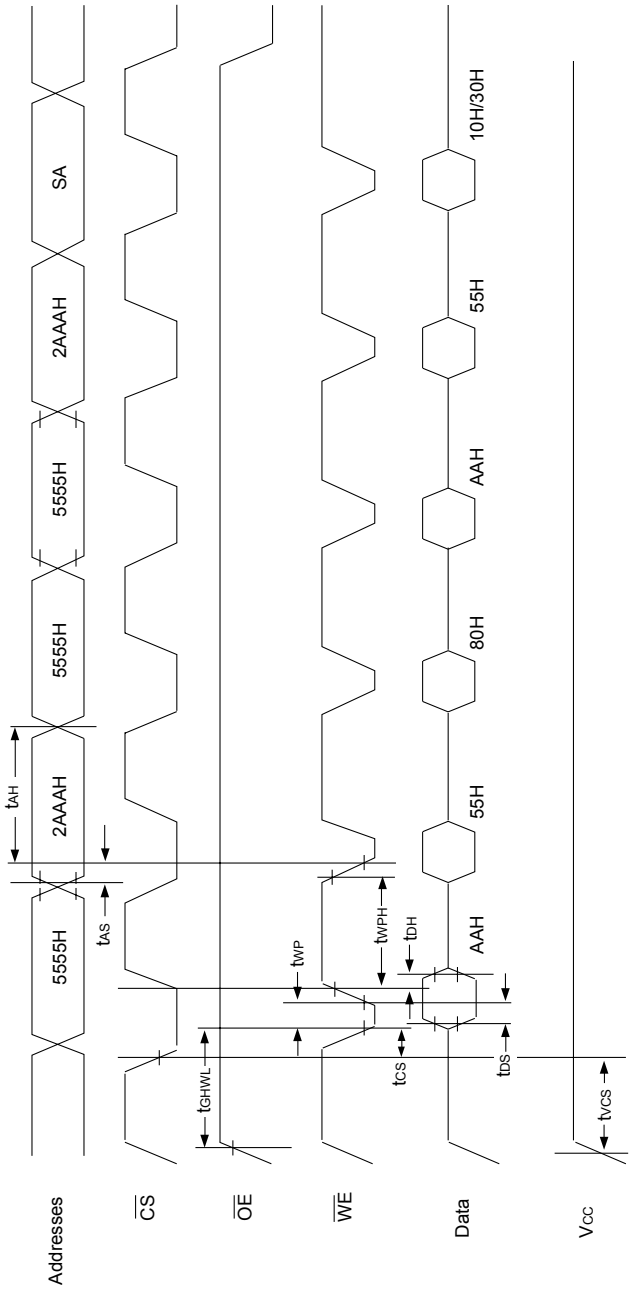


FIG. 4
WRITE/ERASE/PROGRAM OPERATION, $\overline{WE}$ CONTROLLED



NOTES:
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. $\overline{D7}$ is the output of the complement of the data written to each chip.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

FIG. 5
AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS



NOTE:

1. SA is the sector address for Sector Erase.

FIG. 6
AC WAVEFORMS FOR $\overline{\text{DATA}}$ POLLING DURING EMBEDDED ALGORITHM OPERATIONS

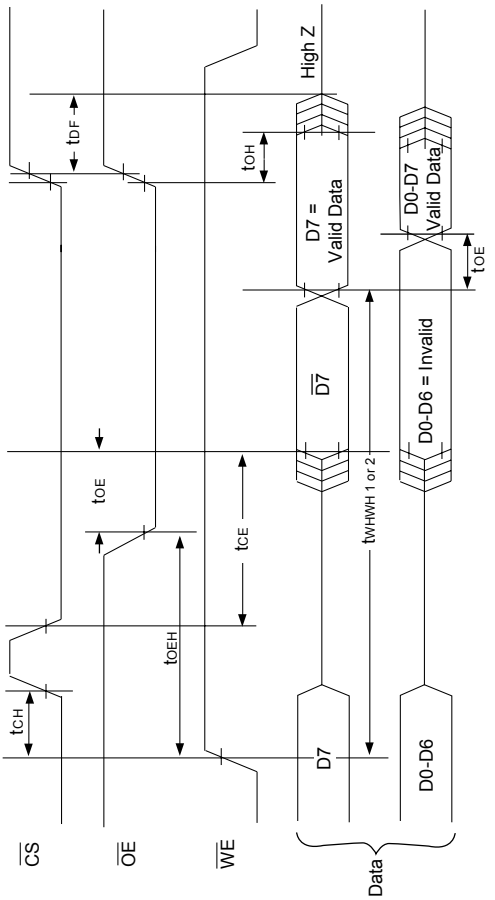
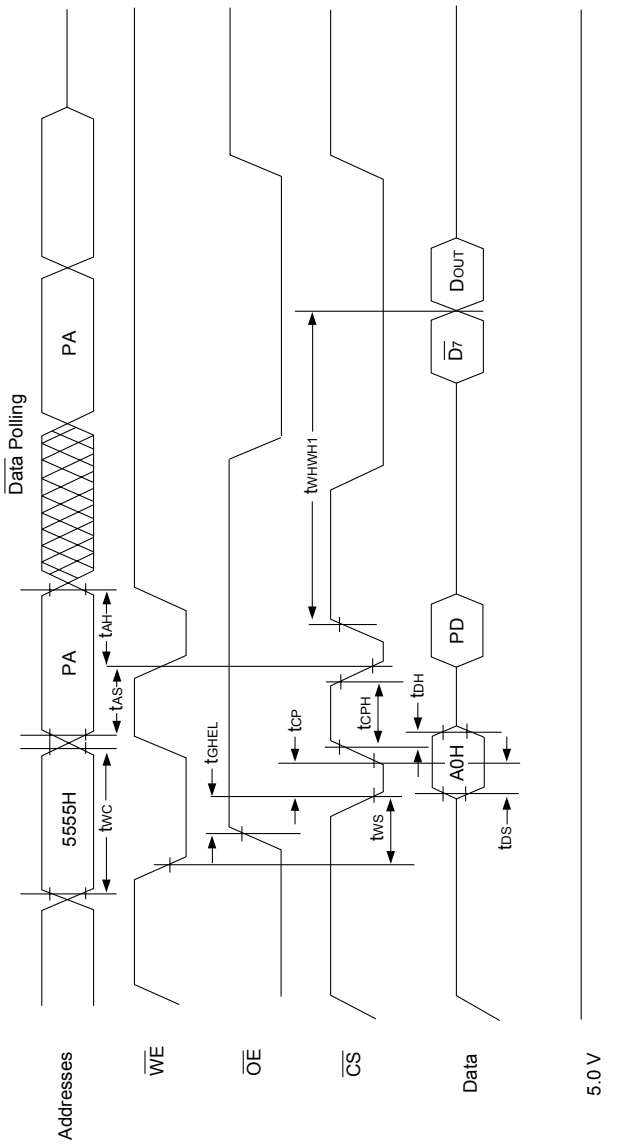


FIG. 7
ALTERNATE $\overline{CS}$ CONTROLLED PROGRAMMING OPERATION TIMINGS



Notes:
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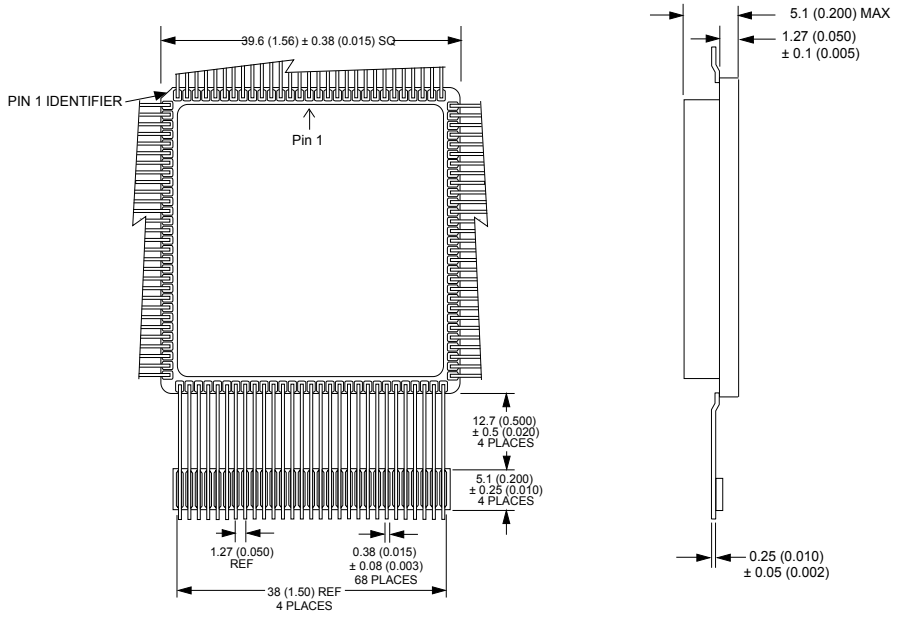
5. Figure indicates the last two bus cycles of a four bus cycle sequence.

PACKAGE 504: 116 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G4W)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W F 512K64 - XXX G4W X 5

VPP PROGRAMMING VOLTAGE
5 = 5V

DEVICE GRADE:

M = Military Screened	-55°C to +125°C
I = Industrial	-40°C to +85°C
C = Commercial	0°C to + 70°C

PACKAGE TYPE:
G4W = 116 Lead 40mm Ceramic Quad Flat Pack, CQFP (Package 504)

ACCESS TIME (ns)

ORGANIZATION, 512K x 64
User configurable as 1M x 32, 2M x 16 or 4M x 8

Flash

WHITE ELECTRONIC DESIGNS CORP.