1GB – 2x64Mx64, SDRAM UNBUFFERED

FEATURES

- PC100 and PC133 compatible
- Burst Mode Operation
- Auto and Self Refresh capability
- LVTTL compatible inputs and outputs
- Serial Presence Detect with EEPROM
- Fully synchronous: All signals are registered on the positive edge of the system clock
- Programmable Burst Lengths: 1, 2, 4, 8 or Full Page
- 3.3V ± 0.3V Power Supply
- 168 Pin DIMM
  - PCB: 29.41mm (1.158")

DESCRIPTION

The WV3DG64127V is a 2x64Mx64 synchronous DRAM module which consists of sixteen stacked 64Mx8 bit with 4 banks SDRAM components in TSOP II package and one 2K EEPROM which are mounted on a 168 Pin DIMM multilayer FR4 Substrate.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

NOTE: Consult factory for availability of:
- Lead-free products
- Vendor source control option
- Industrial temperature option

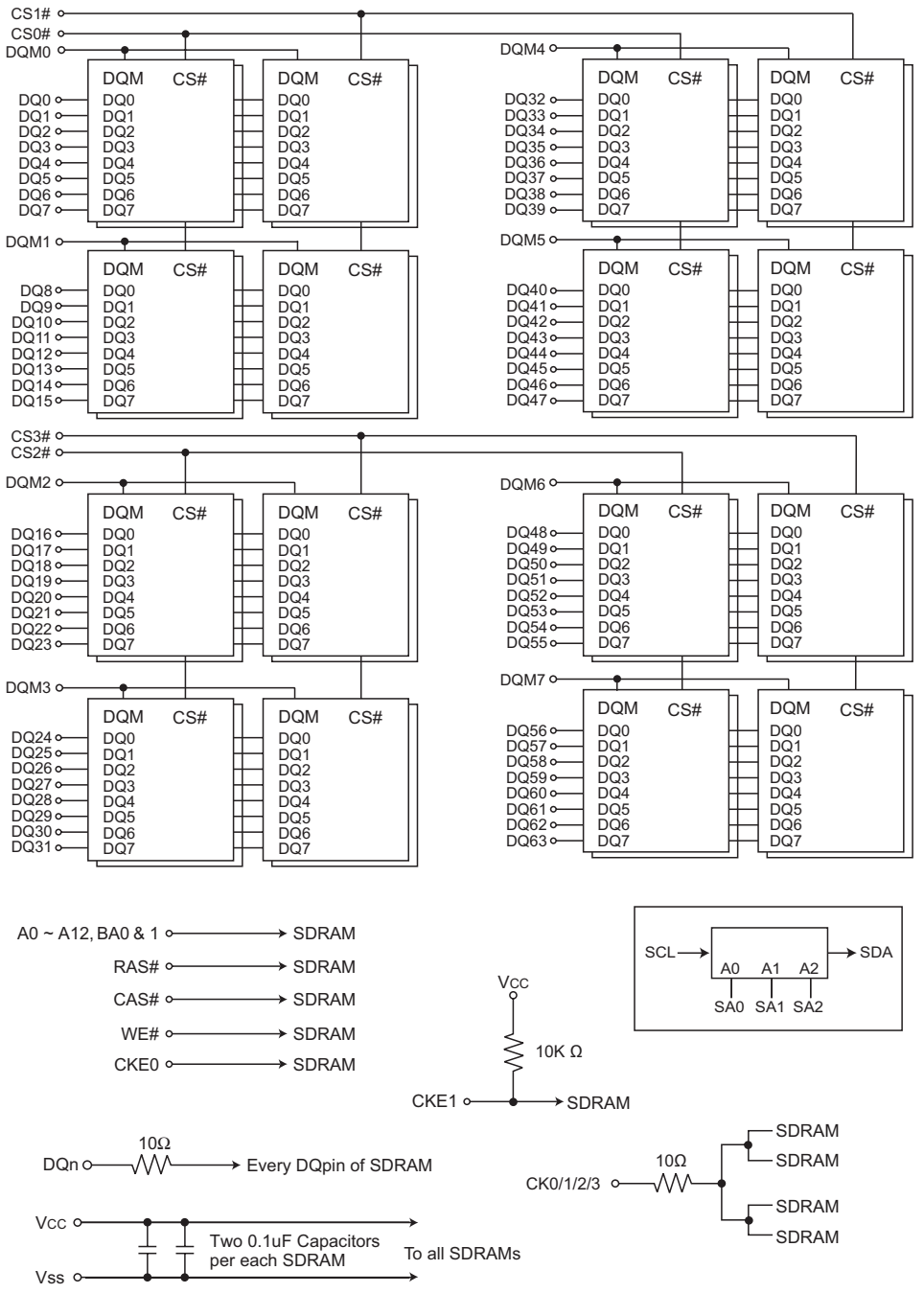
PIN CONFIGURATIONS (FRONT SIDE/BACK SIDE)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	V_{SS}	29	DQM1	57	DQ18	85	V_{SS}	113	DQM5	141	DQ50
2	DQ0	30	CS0#	58	DQ19	86	DQ32	114	CS1#	142	DQ51
3	DQ1	31	DNU	59	V_{CC}	87	DQ33	115	RAS#	143	V_{CC}
4	DQ2	32	V_{SS}	60	DQ20	88	DQ34	116	V_{SS}	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	V_{CC}	34	A2	62	NC	90	V_{CC}	118	A3	146	NC
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	DNU
8	DQ5	36	A6	64	V_{SS}	92	DQ37	120	A7	148	V_{SS}
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	V_{SS}	40	V_{CC}	68	V_{SS}	96	V_{SS}	124	V_{CC}	152	V_{SS}
13	DQ9	41	V_{CC}	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	V_{SS}	71	DQ26	99	DQ43	127	V_{SS}	155	DQ58
16	DQ12	44	DNU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2#	73	V_{CC}	101	DQ45	129	CS3#	157	V_{CC}
18	V_{CC}	46	DQM2	74	DQ28	102	V_{CC}	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DNU	76	DQ30	104	DQ47	132	NC	160	DQ62
21	CBO	49	V_{CC}	77	DQ31	105	CB4	133	V_{CC}	161	DQ63
22	CB1	50	NC	78	V_{SS}	106	CB5	134	NC	162	V_{SS}
23	V_{SS}	51	NC	79	CLK2	107	V_{SS}	135	NC	163	CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	SA0
26	V_{CC}	54	V_{SS}	82	SDA	110	V_{CC}	138	V_{SS}	166	SA1
27	WE#	55	DQ16	83	SCL	111	CAS#	139	DQ48	167	SA2
28	DQM0	56	DQ17	84	V_{CC}	112	DQM4	140	DQ49	168	V_{CC}

PIN NAMES

A0 – A12	Address input (Multiplexed)
BA0-1	Select Bank
DQ0-63	Data Input/Output
CLK0-CLK3	Clock input
CKE0, CKE1	Clock Enable input
CS0# - CS3#	Chip select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DQM0-7	DQM
V_{CC}	Power Supply
V_{SS}	Ground
SDA	Serial data I/O
SCL	Serial clock
DNU	Do not use
NC	No Connect

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}, V_{CCQ}	-1.0 ~ 4.6	V
Storage Temperature	TSTG	-55 ~ +150	°C
Power Dissipation	PD	32	W
Short Circuit Current	IOS	50	mA

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

Voltage Referenced to: V_{SS} = 0V, 0°C ≤ T_A ≤ +70°C

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	3.0	3.3	3.6	V	
Input High Voltage	V_{IH}	2.0	3.0	V_{CCQ}+0.3	V	1
Input Low Voltage	V_{IL}	-0.3	—	0.8	V	2
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = -2mA
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = -2mA
Input Leakage Current	I_{LI}	-10	—	10	µA	3

Note:
1. V_{IH} (max)= 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min)= -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{CC}
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE

T_A = 25°C, f = 1MHz, V_{CC} = 3.3V, V_{REF}=1.4V ± 200mV

Parameter	Symbol	Max	Unit
Input Capacitance (A0-A12)	C_{IN1}	150	pF
Input Capacitance (RAS#,CAS#,WE#)	C_{IN2}	150	pF
Input Capacitance (CKE0-CKE1)	C_{IN3}	80	pF
Input Capacitance (CK0-CK3)	C_{IN4}	45	pF
Input Capacitance (CS0#-CS3#)	C_{IN5}	45	pF
Input Capacitance (DQM0-DQM7)	C_{IN6}	30	pF
Input Capacitance (BA0-BA1)	C_{IN7}	150	pF
Data input/output capacitance (DQ0-DQ63)	C_{OUT}	30	pF

I_{DD} SPECIFICATIONS AND CONDITIONS

V_{CC}, V_{CCQ} = +3.3V ±0.3V; SDRAM component values only

Parameter	Symbol	Test Condition		Version			Unit	Note
				7	75	10		
Operating current (One bank active)	I_{CC1}	Burst length = 1, $t_{RC} \geq t_{RC}$(min), IO = 0 mA		2080	1920	1920	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		64			mA	
	I_{CC2PS}	CKE & CLK ≥ V_{IL}(max), t_{CC} = ∞		64				
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), CS# ≥ VIH(min), t_{CC} = 10ns Input signals are changed one time during 20ns		640			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		320				
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		200			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		200				
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), CS# ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		960			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		800			mA	
Operating current (Burst mode)	I_{CC4}	IO = 0 mA Page burst 4banks Activated. t_{CCD} = 2CLKs		2240	2240	2080	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		4000	3680	3520	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	C	96			mA	

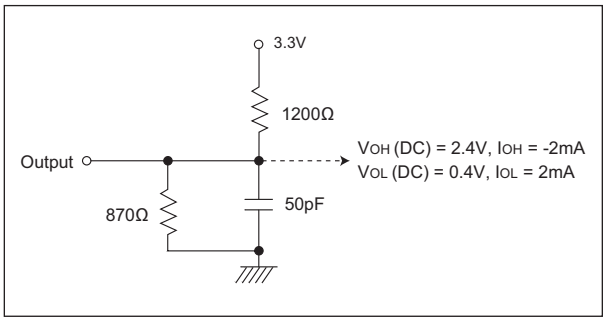
Notes:
1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noted, input swing is CMOS (V_{IH}/V_{IL} = V_{CCQ}/V_{JSQ})

AC OPERATING TEST CONDITIONS

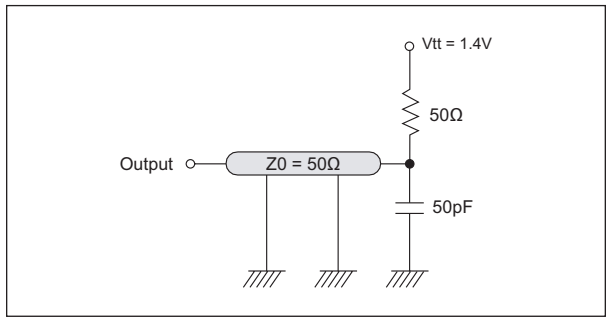
V_{CC}, V_{CCQ} = +3.3v ±0.3V, 0°C - 70°C

Parameter	Value	Unit
AC input levels (V_{IH}/V_{IL})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	t_R/t_F = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	

DC OUTPUT LOAD CIRCUIT



AC OUTPUT LOAD CIRCUIT



OPERATING AC PARAMETER

V_{CC}, V_{CCQ} = +3.3v ±0.3V, 0°C - 70°C)

Parameter		Symbol	Version			Unit	Note
			7	75	10		
Row active to row active delay		$t_{RRD(min)}$	15	15	20	ns	1
RAS# to CAS# delay		$t_{RCD(min)}$	15	20	20	ns	1
Row precharge time		$t_{RP(min)}$	15	20	20	ns	1
Row active time		$t_{RAS(min)}$	45	45	50	ns	1
		$t_{RAS(max)}$	100			us	
Row cycle time		$t_{RC(min)}$	60	65	70	ns	1
Last data in to row precharge		$t_{RDL(min)}$	2			CLK	2
Last data in to Active delay		$t_{DAL(min)}$	2 CLK + tRP			—	
Last data in to new col. address delay		$t_{CDL(min)}$	1			CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1			CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Notes:

1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

OPERATING AC PARAMETERS

V_{CC}, V_{CCQ} = +3.3v ±0.3V, 0°C - 70°C

Parameter		Symbol	7		75		10		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	t_{CC}	7.5	1000	7.5	1000	10	1000	ns	1
	CAS latency=2		7.5		10		10			
CLK to valid output delay	CAS latency=3	t_{SAC}		5.4		5.4		6	ns	1, 2
	CAS latency=2			5.4		6		6		
Output data hold time	CAS latency=3	t_{OH}	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		t_{CH}	2.5		2.5		3		ns	3
CLK low pulse width		t_{CL}	2.5		2.5		3		ns	3
Input setup time		t_{SS}	1.5		1.5		2		ns	3
Input hold time		t_{SH}	0.8		0.8		1		ns	3
CLK to output in Low-Z		t_{SLZ}	1		1		1		ns	2
CLK to outpu in Hi-Z	CAS latency=3	t_{SHZ}		5.4		5.4		6	ns	
	CAS latency=2			5.4		6		6		

Notes :

1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

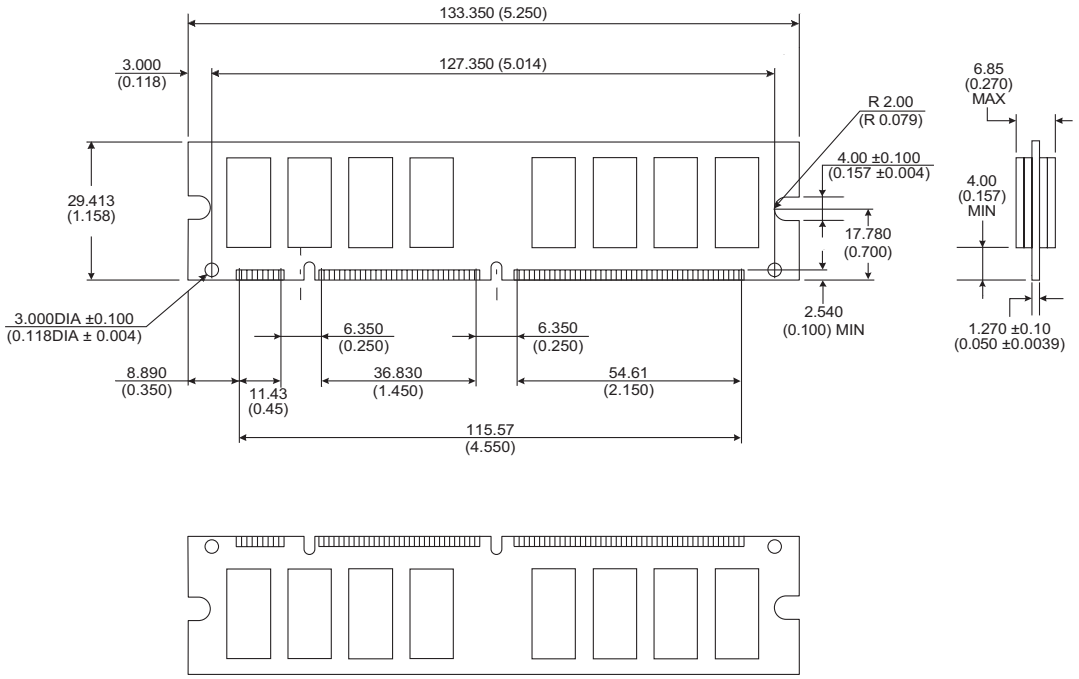
ORDERING INFORMATION

Part Number	Speed	CAS Latency	Height*
WV3DG64127V10D2	100MHz	CL=2	29.41 (1.158")
WV3DG64127V7D2	133MHz	CL=2	29.41 (1.158")
WV3DG64127V75D2	133MHz	CL=3	29.41 (1.158")

NOTES:

- Consult Factory for availability of Lead-Free products. (F = Lead-Free, G = RoHS Compliant)
- Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS



***ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)**

Document Title

1GB - 2x64Mx64, SDRAM UNBUFFERED

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	4-05	Advanced