

**TECHNICAL DATA**  
Datasheet 4171, Rev. -

**Three-Phase MOSFET BRIDGE, With Gate Driver and Optical Isolation**

**DESCRIPTION:** A 200 VOLT, 70 AMP, THREE PHASE MOSFET BRIDGE

**ELECTRICAL CHARACTERISTICS PER MOSFET DEVICE**

(T<sub>j</sub>=25°C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
<b>MOSFET SPECIFICATIONS</b>					
Drain-to-Source Breakdown Voltage I <sub>D</sub> = 500 μA, V <sub>GS</sub> = 0V	BV <sub>DSS</sub>	200	-	-	V
Continuous Drain Current T <sub>C</sub> = 25 °C T <sub>C</sub> = 90 °C	I <sub>D</sub>	-	-	70 60	A
Pulsed Drain Current, Pulse Width limited by T <sub>jmax</sub>	I <sub>DM</sub>	-	-	300	A
Gate to Source Voltage	V <sub>GS</sub>	-	-	+/-20	V
Gate- Source Leakage Current , V <sub>GE</sub> = +/-20V	I <sub>GSS</sub>	-	-	+/- 200	nA
Zero Gate Voltage Drain Current V <sub>DS</sub> = 200 V, V <sub>GS</sub> =0V T <sub>i</sub> =25°C V <sub>DS</sub> = 160 V, V <sub>GS</sub> =0V T <sub>i</sub> =125°C	I <sub>CSS</sub>	-	-	1 3	mA mA
Static Drain-to-Source On Resistance, °C I <sub>D</sub> = 50A, V <sub>GS</sub> = 15V,	R <sub>DSon</sub>	-	0.023 0.050	0.025 -	V
Maximum Thermal Resistance	R <sub>θJC</sub>	-	-	0.35	°C/W
Maximum operating Junction Temperature	T <sub>jmax</sub>	-40	-	150	°C
Maximum Storage Junction Temperature	T <sub>jmax</sub>	-55	-	150	°C

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Over-Temperature Shutdown					
Over-Temperature Shutdown	Tsd	90	100	115	°C
Over-Temperature Output	Tso		10		10mV/°C
Over-Temperature Shutdown Hysteresis			20		°C

DIODES CHARACTERISTICS					
Continuous Source Current, $T_C = 90\text{ }^\circ\text{C}$	$I_S$	-	-	60	A
Diode Forward Voltage, $I_S = 50\text{A}, T_j = 25\text{ }^\circ\text{C}$	$V_{SD}$	-		1.5	V
Diode Reverse Recovery Time ( $I_S=50\text{A}, V_{DD}=100\text{V}, di/dt=100\text{ A}/\mu\text{s}$ )	$t_{rr}$	-	220	-	nsec
Gate Driver					
Supply Voltage	VCC	10	15	20	V
Input On Current	HIN, LIN	2		5.0	mA
Opto-Isolator Logic High Input Threshold	$I_{th}$	-	1.6	-	mA
Input Reverse Breakdown Voltage	$BV_{in}$	5.0	-	-	V
Input Forward Voltage @ $I_{in} = 5\text{mA}$	$V_F$	-	1.5	1.7	V
Under Voltage Lockout	VCCUV	11.5	-	12.5	V
ITRIP Reference Voltage <sup>(1)</sup>	Itrip-ref	2.5	2.6	2.7	V
Input-to-Output Turn On Delay	$t_{ond}$	-	TBD	-	nsec
Output Turn On Rise Time	$t_r$	-	TBD	-	
Input-to-Output Turn Off Delay	$t_{offd}$	-	TBD	-	
Output Turn Off Fall Time	$t_f$	-	TBD	-	
@ VCC=100V, ID=50A, $T_C = 25$					
Input-Output Isolation Voltage	-	1500	-	-	V

(1) ITRIP Cycle-by cycle current limit is internally set to 70A peak. The set point can be lowered by connecting a resistor between Itrip-ref and Gnd. The set point can be increased by connecting a resistor between Itrip-ref and +5V ref

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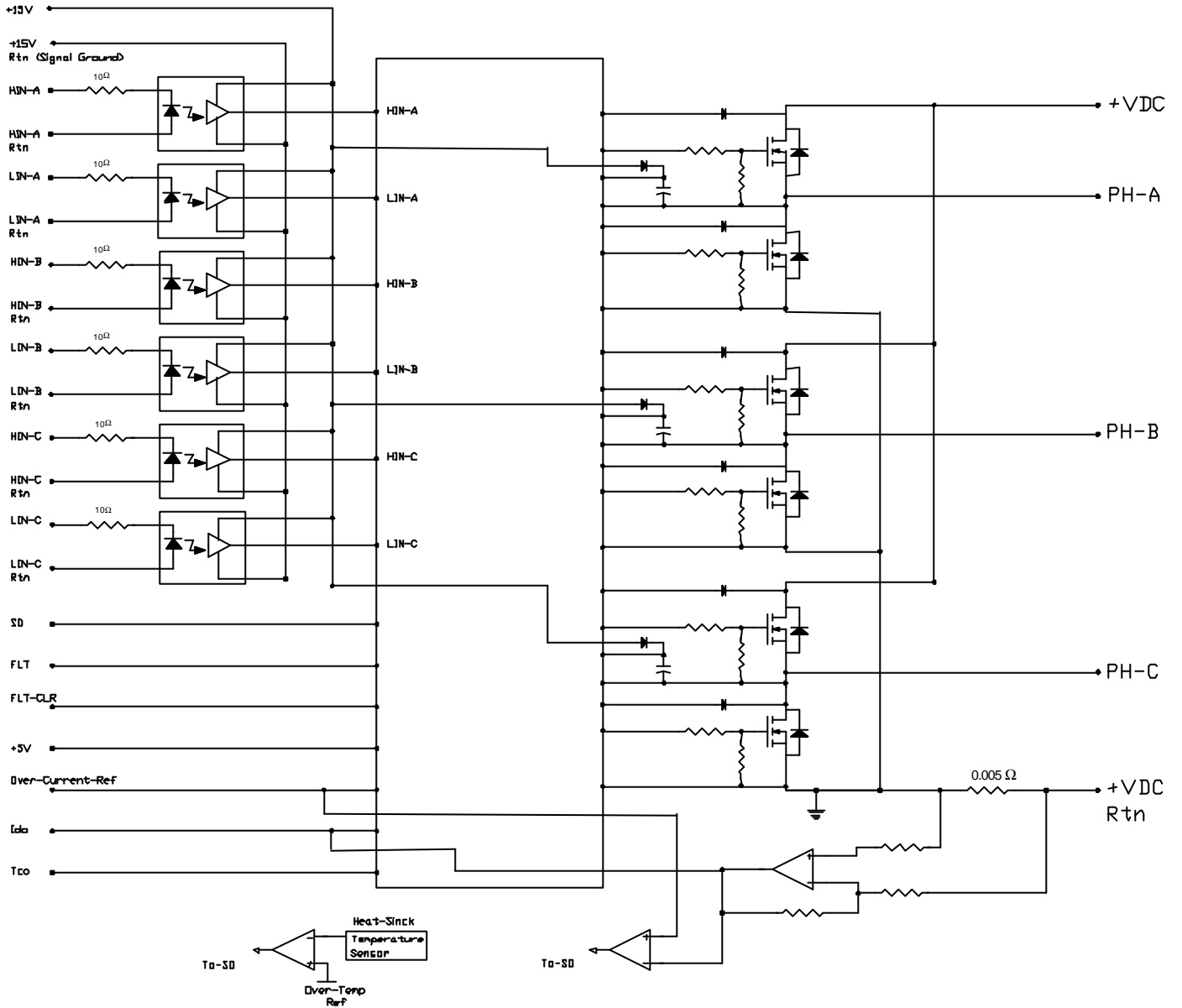
**Pin Description**

Pin Number	Function	Pin Number	Function
1	Isolated Input for High-side MOSFET of Phase A	18	NC
2	Return for Input at 1	19	+15V Input
3	NC	20	+15V Rtn (Signal Ground) <sup>(3)</sup>
4	Isolated Input for Low-side MOSFET of Phase A	21	SD <sup>(3)</sup>
5	Return for Input at 4	22	Fault Output <sup>(3)</sup>
6	NC	23	Fault Clear Input <sup>(3)</sup>
7	Isolated Input for High-side MOSFET of Phase B	24	+5V Output
8	Return for Input at 7	25	Over-Current Trip Set Point <sup>(3)</sup>
9	NC	26	DC Bus Current Output with Total Gain of 0.06 V/A
10	Isolated Input for Low-side MOSFET of Phase B	27	Case Temperature Output with Gain of 0.010 V/°C
11	Return for Input at 10	28 & 29	Phase A Output
12	Isolated Input for High-side MOSFET of Phase C	30 & 31	Phase B Output
13	Return for Input at 12	32 & 33	Phase C Output
14	Isolated Input for Low-side MOSFET of Phase C	34 & 35	DC Bus "+VDC Return"
15	Return for Input at 14	36 & 37	DC Bus "+VDC" Input
16	NC	Case	Isolated From All Terminals
17	NC		

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**Schematic Diagram:**

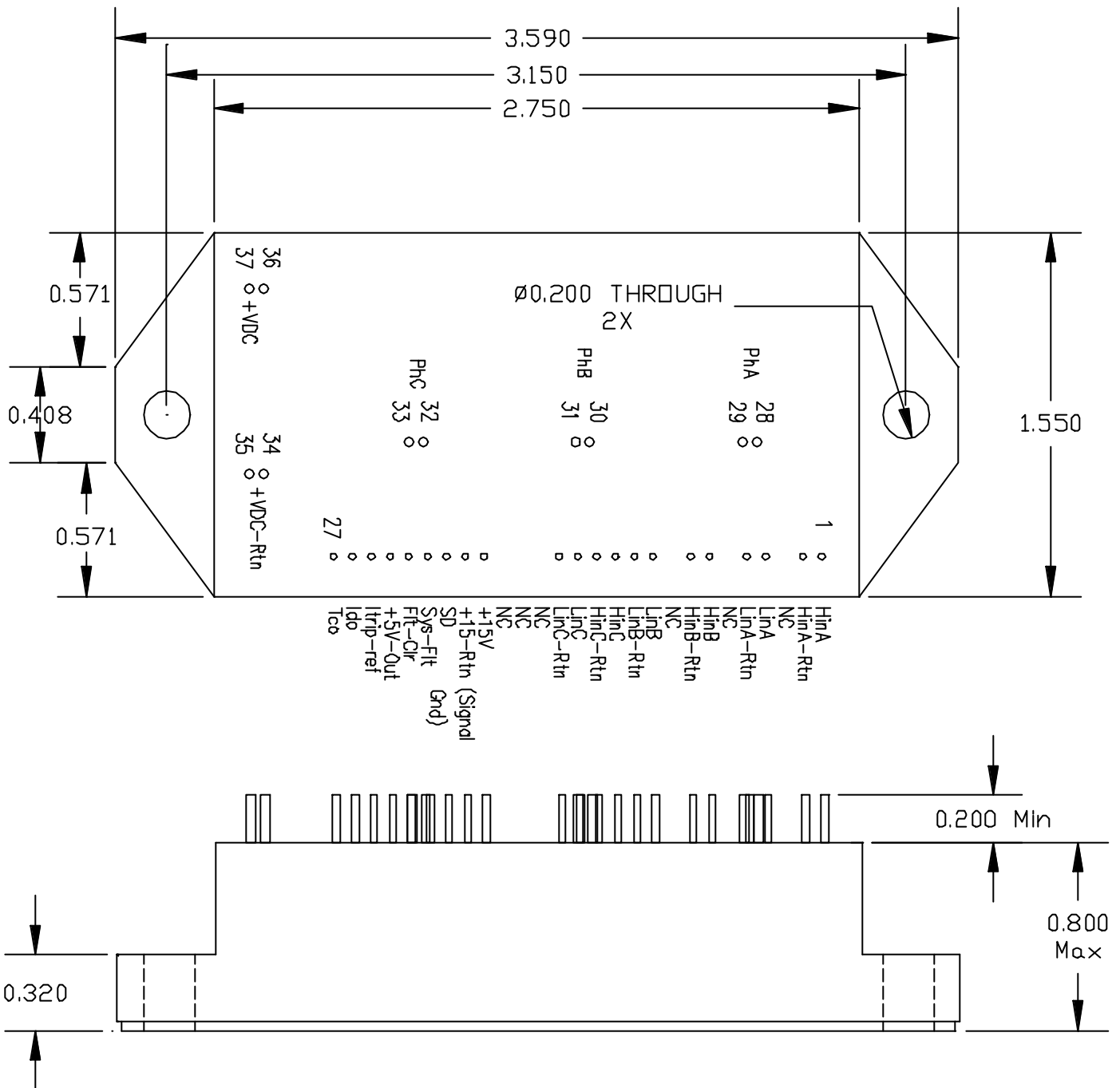


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**Package Drawing Top View**  
 (All dimensions are in inches, tolerance is +/- 0.010")



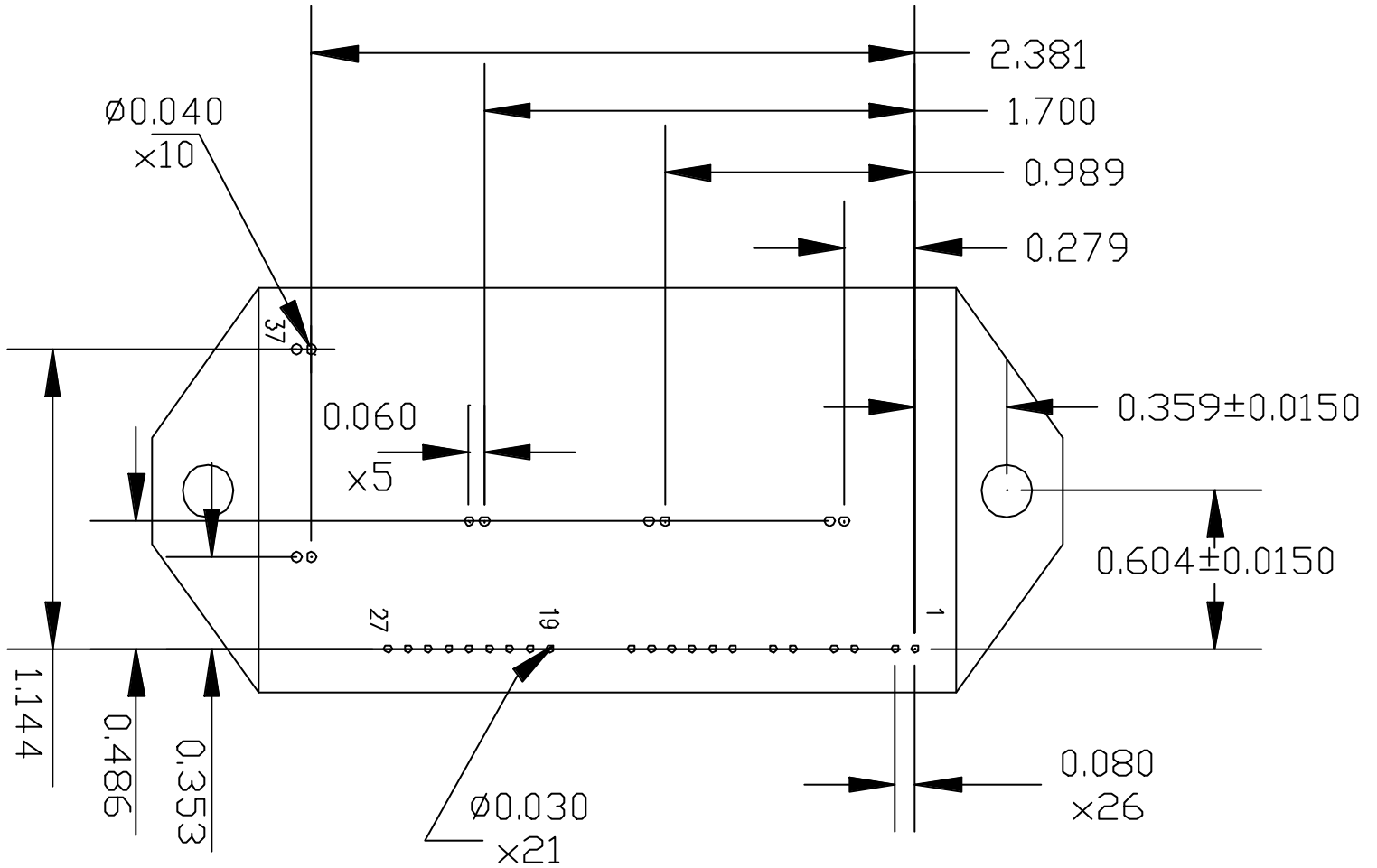
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**Package Pin Locations**

(All dimensions are in inches; tolerance is +/- 0.005" except otherwise specified)



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**Application Notes:****a- Shutdown Feature:**

- 1- Pin 21, SD is a dual function input/output, active low input. It is internally pulled high. As a low input, it shuts down all MOSFETs regardless of the Hin and Lin signals.
- 2- SD is also internally activated by the over-temperature shutdown, over-current limit, under-voltage shutdown, and desaturation protection.
- 3- Over-temperature shutdown, and over-current limit are not latching features.
- 4- Under-voltage shutdown is automatically reset once the VCC rises above the 12.1V threshold limit.
- 5- Desaturation shutdown is a latching feature and internally reset.
- 6- When any of the internal protection features are activated, SD is pulled down.
- 7- SD can be used to shutdown all MOSFETs by an external command. An open collector switch shall be used to pull down SD externally.
- 8- Also, SD can be used as a fault condition output. Low output at SD indicates a fault situation.

**b- Fault Output Feature:**

- 1- Pin 22, Flt is a dual function pin. It is internally pulled high. If pulled down, it will freeze the status of all the six MOSFETs regardless of the Hin and Lin signals
- 2- Pin 22 as an output reports desaturation protection activation. When desaturation protection is activated a low output for about 9  $\mu$ sec is reported.
- 3- If any other protection feature is activated, it will not be reported by Pin 22.

**c- Fault Clear Output:**

- 1- Pin 23, Flt-Clr is a fault clear input. It can be used to reset a latching fault condition, due to desaturation protection.
- 2- Pin 23 is internally pulled down. A latching fault due to desaturation can be cleared by pulling high this input.
- 3- An internal fault clear is activated after 100  $\mu$ sec delay. If desired to clear the fault earlier, this input can be used.

**d- Signal Ground:**

Pin 20, Signal Gnd is the signal ground for all signals at Pins 19 through 27. This ground is internally connected to the +VDC Rtn. **No external connection shall be established between Signal Gnd and +VDC Rtn.**

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