SONY CXA1389AQ

Cable Driver for Digital Transfer

Description

The CXA1389AQ arranges the driver part into a single chip to easily compose a digital data transfer system.

Features

- 1 differential input 3 differential outputs
- Sufficient drive capacity
- Stability due to minimal waveform distortion

Structure

Bipolar silicon monolithic IC.

Applications

Data transfer between digital signal processing equipment.

Absolute Maximum Ratings

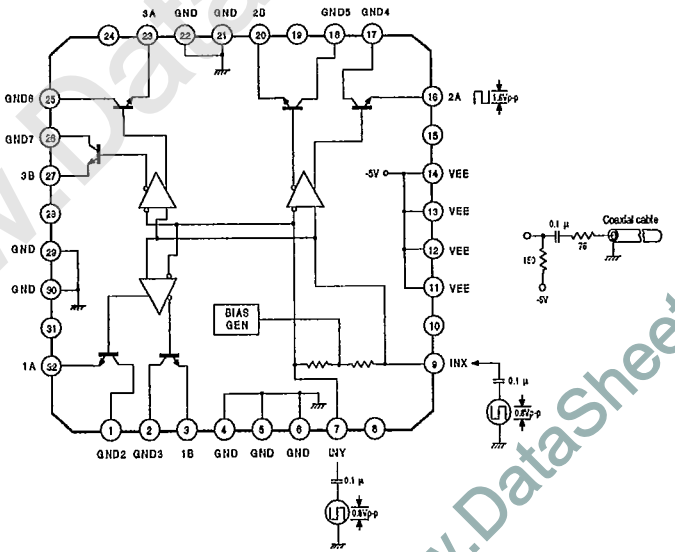
• Supply voltage	Vcc	7.0	V
• Storage temperature	Tstg	-65 to +150	°C
• Allowable power	PD	500	mW

Operating Conditions

• Supply voltage	Vcc	4.8 to 5.2	V
• Operating temperature	Topr	-20 to +75	°C

Block Diagram

When the below input is applied between INX and INY, in-phase 1.6Vp-p is output at 1A, 2A and 3A.
In reversed phase, 1.6Vp-p is output at 18, 28 and 38. * Various output pins are connected as indicated below.



Electrical Characteristics

(Ta = 25 °C)

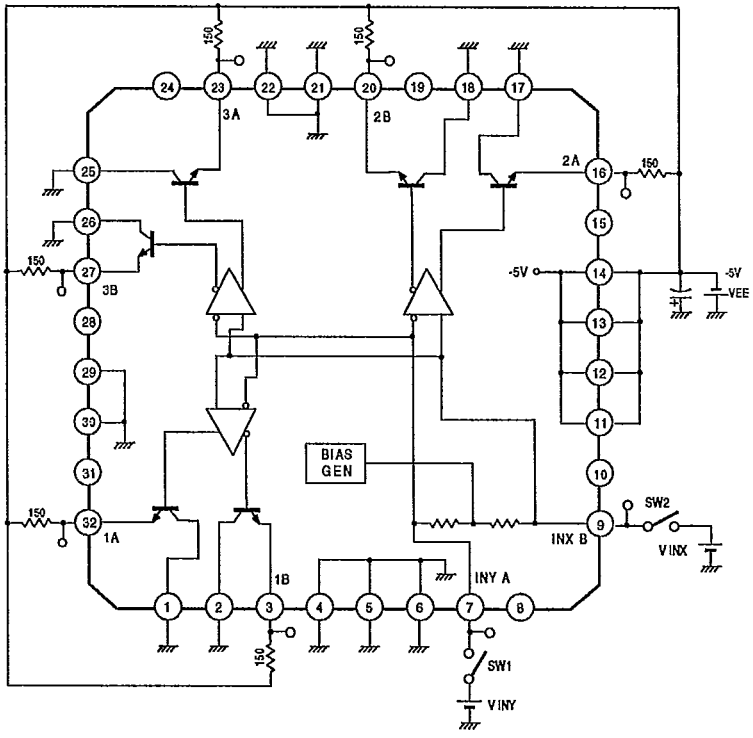
Test Pin	Item	Symbol	Bias Conditions		SW ON	Test Point	Min.	Typ.	Max.	Unit	Test
			V INY	V INX							
1	Pin voltage INY	V1	---	---	---	7 pin	-2.9	-2.7	-2.5	V	Test of pin voltage
2	Pin voltage INX	V2	---	---	---	9 pin	-2.9	-2.7	-2.5	V	
3	Pin voltage 1A	A1-1	---	---	---	32 pin	-3.1	-2.7	-2.5	V	
4	Pin voltage 1B	B1-1	---	---	---	3 pin	-3.1	-2.7	-2.5	V	
5	Pin voltage 2A	A2-1	---	---	---	16 pin	-3.1	-2.7	-2.5	V	
6	Pin voltage 2B	B2-1	---	---	---	20 pin	-3.1	-2.7	-2.5	V	
7	Pin voltage 3A	A3-1	---	---	---	23 pin	-3.1	-2.7	-2.5	V	
8	Pin voltage 3B	B3-1	---	---	---	27 pin	-3.1	-2.7	-2.5	V	
9	Current power supply	IEE	---	---	---	VEE	-143		-77	mA	Current power supply at V_{EE}
10	DC applied 1A	A1-2	V1+0.2	V2-0.2	SW1 SW2	32 pin	0.31	0.39	0.47	V	Output DC voltage when +0.2V is applied to INY and -0.2V to INX. (A1-2)=Test value-(A1-1) (B1-2)=Test value-(B1-1) The differnce with the previous pin voltage is recorded. Same for A2-2, B2-2, A3-2, B3-2.
11	DC applied 1B	B1-2	↓	↓		3 pin	-0.47	-0.39	-0.31	V	
12	DC applied 2A	A2-2	↓	↓		16 pin	0.31	0.39	0.47	V	
13	DC applied 2B	B2-2	↓	↓		20 pin	-0.47	-0.39	-0.31	V	
14	DC applied 3A	A3-2	↓	↓		23 pin	0.31	0.39	0.47	V	
15	DC applied 3B	B3-2	↓	↓		27 pin	-0.47	-0.39	-0.31	V	
16	Amplitude 1A+1B	V1-1	Calculation				0.65	0.75	0.85	V	(V1-1 = (A1-2) - (B1-2) Amplitude calculated from T10 width T15 V2-1, V3-1.
17	Amplitude 1A+1B	V2-1	Calculation				0.65	0.75	0.85	V	
18	Amplitude 1A+1B	V3-1	Calculation				0.65	0.75	0.85	V	
19	Amplitude 1A+1B		Calculation				0.65	1.0	1.15	---	- (A1-2) / (B1-2)
20	Amplitude 1A+1B		Calculation				0.65	1.0	1.15	---	- (A1-2) / (B1-2)
21	Amplitude 1A+1B		Calculation				0.65	1.0	1.15	---	- (A1-2) / (B1-2)

Electrical Characteristics

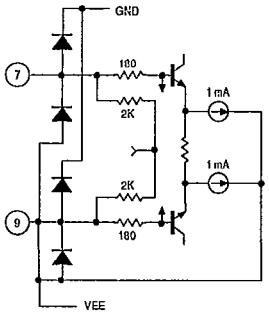
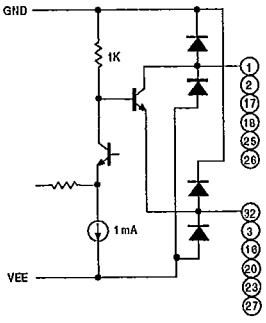
(Ta = 25 °C)

Test Pin	Item	Sym-bol	Bias conditions		SW ON	Test Point	Min.	Typ.	Max.	Unit	Test
			V INY	VINX							
22	DC applied 1A	A1-3	V1-0.4	V2+0.4	SW1 SW2	32 pin	-0.9	-0.75	-0.6	V	Output DC voltage is tested when -0.4V is applied to INY and +0.4V to INX. (A1-3)=Test value - (A1-1) (B1-3)=Test value - (B1-1) The difference with the previous pin voltage is recorded. Same for A2-2. B2-3, A3-3, B3-3.
23	DC applied 1B	B1-3	↓	↓		3 pin	0.6	0.75	0.9	V	
24	DC applied 2A	A2-3	↓	↓		16 pin	-0.9	-0.75	-0.6	V	
25	DC applied 2B	B2-3	↓	↓		20 pin	0.6	0.75	0.9	V	
26	DC applied 3A	A3-3	↓	↓		23 pin	-0.9	-0.75	-0.6	V	
27	DC applied 3B	B3-3	↓	↓		27 pin	0.6	0.75	0.9	V	
28	Amplitude 1A + 1B	V1-2	Calculation				1.3	1.5	1.7	V	(V1-2)=(A1-3)+(B1-3)
29	Amplitude 2A + 2B	V2-2	Calculation				1.3	1.5	1.7	V	Amplitude calculated from T22 with T27 as base. Same for V2-2, V3-2.
30	Amplitude 3A + 3B	V3-2	Calculation				1.3	1.5	1.7	V	
31	Amplitude ratio 1A / 1B		Calculation				0.85	1.0	1.15	---	- (A1-3) / (B1-3)
32	Amplitude ratio 2A / 2B		Calculation				0.85	1.0	1.15	---	- (A2-3) / (B2-3)
33	Amplitude ratio 3A / 3B		Calculation				0.85	1.0	1.15	---	- (A3-3) / (B3-3)
34	Linearity 1	V1-3	Calculation				1.7	1.9	2.1	---	- (V1-2) / (V1-1)
35	Linearity 2	V2-3	Calculation				1.7	1.9	2.1	---	- (V2-2) / (V1-1)
36	Linearity 3	V3-3	Calculation				1.7	1.9	2.1	---	- (V3-2) / (V1-1)

Electrical Characteristics Test Circuit



Pin Description

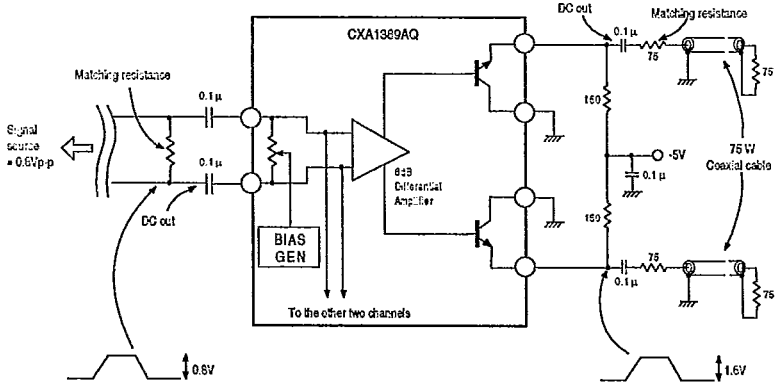
Pin No.	Symbol	Standard DC Voltage	Equivalent Circuit	Description
7 9	INY INX	-2.7V		Input pin of the differential amplifier. Input executed after DC portion is cut off.
1 2 17 18 25 26	GND2 GND3 GND4 GND5 GND6 GND7	----		Collector of the emitter follower output Tr. Connect to GND.
32 3 16 20 23 27	1A 1B 2A 2B 3A 3B	-2.7V		Emitter of emitter follower output Tr. To use, connect pull-down resistor. (Even when only 1 side is used pull-down is executed in pairs.) Pairs 32 16 23 3 20 27

Description of Operation

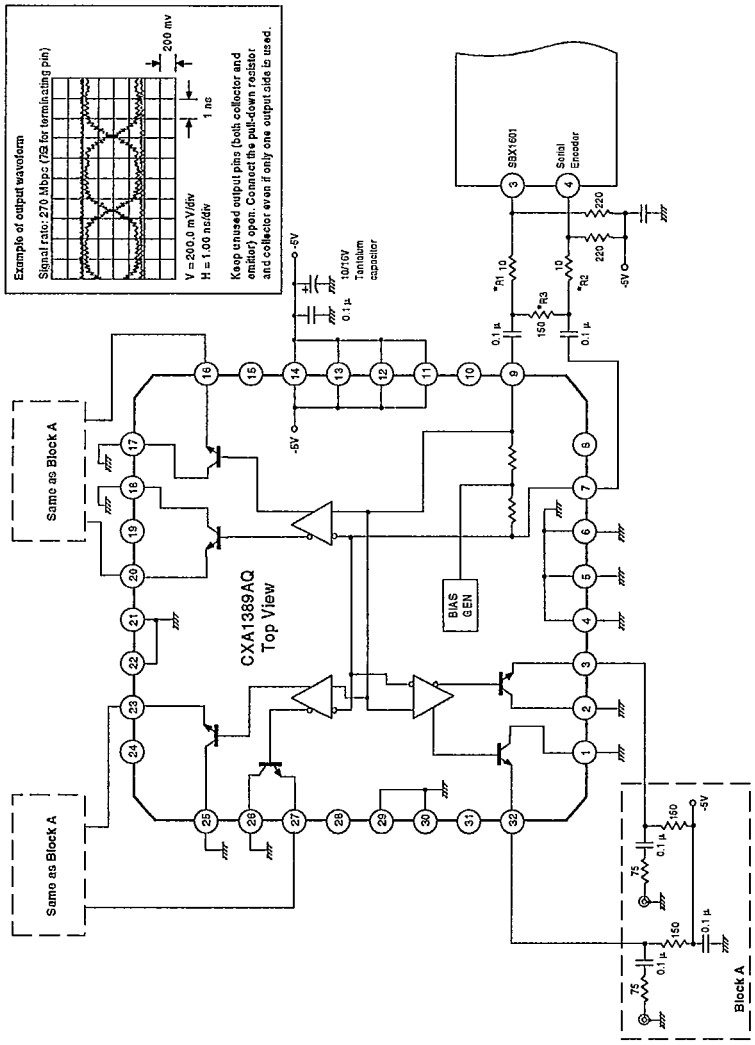
The CXA1389AQ consists of 3 pairs of differential amplifiers (3 pairs of differential outputs) and a bias generating circuit that amplify and output to about 6dB one pair of differential input pins and that input.
The input pin is internally biased and the signal DC portion is cut off with capacitor before application.

Adjustment of the PCB pattern design and the machinery resistance value is executed to obtain a goof eye pattern at the input pin. This, because the wave form distortion of the input pin directly becomes the distortion of the output wave form.

Signals amplified to about 6dB are output at the emitter follower. Between the output pin and the co-axial, a 68 to 75 resistance and a capacitor to cut off the DC portion, are connected to match 75 co-axial cable. In this case a signal almost similar in level to the input is transferred to the co-axial cable.



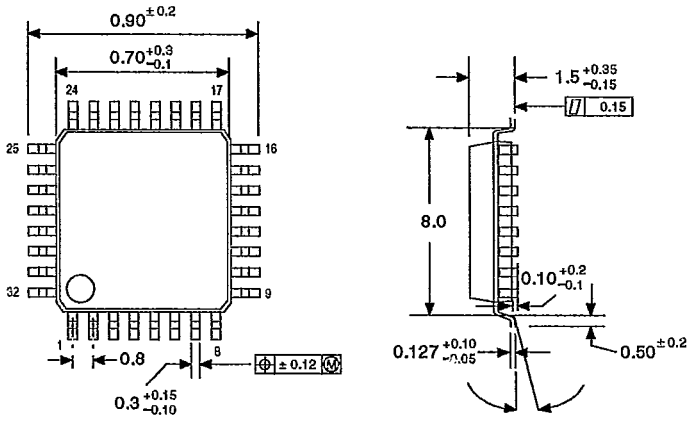
Application Circuit



- The marked * resistance is alterd through the PCB pattern. Adjustment is performed to obtain a good eye pattern at Pins 7 abd 9.
- Keep the GND pin pattern as short as possible and provide sufficient GND. A weak GND will cause unstable operation.
- Since power consumption is large, conceive a pattern taking due consideration of the radiation from the PCB.

Package Outline

Unit:mm



SONY NAME	QFP-32P-L01
EIAJ NAME	*QFP032-P-0707-A
JDEC CODE	