

# 16-bit Proprietary Microcontroller

CMOS

## F<sup>2</sup>MC-16LX MB90378 Series

# MB90F378/V378

### ■ DESCRIPTION

The MB90378 series is a line of general-purpose, 16-bit microcontrollers designed for those applications which require high-speed real-time processing. The instruction set is designed to be optimized for controller applications which inheriting the AT architecture of F<sup>2</sup>MC-16LX family and allow a wide range of control tasks to be processed efficiently at high speed.

A built-in LPC interface, serial IRQ and PS/2 interface simplifies communication with host CPU and PS/2 devices in computer system. Moreover, SMBus compliant I<sup>2</sup>C\*<sup>2</sup> and A/D converter implements the smart battery control. With these features, the MB90378 series matches itself as keyboard controller with smart battery control.

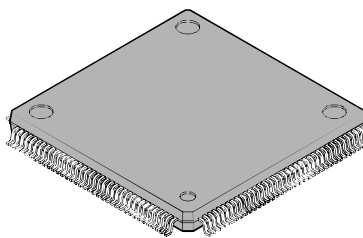
While inheriting the AT architecture of the F<sup>2</sup>MC\*<sup>1</sup> family, the instruction set for the F<sup>2</sup>MC-16LX CPU core of the MB90378 series incorporates additional instructions for high-level languages, supports extended addressing modes, and contains enhanced multiplication and division instructions as well as a substantial collection of improved bit manipulation instructions. In addition, the MB90378 series has an on-chip 32-bit accumulator which enables processing of long-word data.

\*1 : F<sup>2</sup>MC stands for FUJITSU Flexible Microcontroller, a registered trademark of FUJITSU LIMITED.

\*2 : Purchase of Fujitsu I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Rights to use, these components in an I<sup>2</sup>C system provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips.

### ■ PACKAGE

144-pin plastic LQFP



(FPT-144P-M12)

# MB90378 Series

## ■ FEATURES

### ● Clock

- Embedded PLL clock multiplication circuit
- Operating clock (PLL clock) can selected from divided-by-2 of oscillation or one to four times the oscillation (at oscillation of 4 MHz to 20 MHz)
- Minimum instruction execution time of 50 ns (at oscillation of 5 MHz, four times the PLL clock, operation at  $V_{CC}$  of 3.3 V)

### ● CPU addressing space of 16 Mbytes

Internal 24-bit addressing

### ● Instruction set optimized for controller applications

- Rich data types (bit, byte, word, long word)
- Rich addressing mode (23 types)
- High code efficiency
- Enhanced precision calculation realized by the 32-bit accumulator

### ● Instruction set designed for high level language (C) and multi-task operations

- Adoption of system stack pointer
- Enhanced pointer indirect instructions
- Barrel shift instructions

### ● Program patch function (2 address pointer)

### ● Improved execution speed

4-byte instruction queue

### ● Powerful interrupt function

- Priority level programmable : 8 levels
- 32 factors of stronger interrupt function

### ● Automatic data transmission function independent of CPU operation

- Extended intelligent I/O service function (EI<sup>2</sup>OS)
- Maximum 16 channels

### ● Low-power consumption (standby) mode

- Sleep mode (mode in which CPU operating clock is stopped)
- Timebase timer mode (mode in which operations other than timebase timer and watch timer are stopped)
- Stop mode (mode in which all oscillations are stopped)
- CPU intermittent operation mode
- Watch mode

### ● Dual operation flash

Upper and lower banks of flash memory can be used to execute erase/program and read operation concurrently (MB90F378)

### ● Package

LQFP-144 (FPT-144P-M12 : 0.4 mm pitch)

### ● Process

CMOS technology

# MB90378 Series

## ■ PRODUCT LINEUP

Part number	MB90F378	MB90V378
Classification	Flash type ROM	—
ROM size	128 Kbytes (112 Kbytes + 16 Kbytes) Dual operation	—
RAM size	6 Kbytes	15.6 Kbytes
CPU function	Number of instruction : 351 Minimum execution time : 50 ns/5 MHz (PLL x 4) Addressing mode : 23 Data bit length : 1, 8, 16 bits Maximum memory space : 16 Mbytes	
I/O port	I/O port (Nch) : 25 I/O port (CMOS) : 68 I/O port (CMOS with pull-up control) : 32 Total : 125	
16-bit reload timer	Reload timer : 6 channels Reload mode, single-shot mode or event count mode selectable	
8/16-bit PPG timer	PPG timer : 2 channels (8-bit mode, 4 channels)	
16-bit PPG timer	PPG timer : 3 channels PWM mode or single-shot mode selectable	
Bit decoder	Bit decoder : 1 channel	
Parity generator	Parity generator : 1 channel Selectable odd/even parity	
PS/2 interface	PS/2 interface : 3 channels 4 selectable sampling clocks	
LPC interface	LPC bus interface : 1 channel Universal peripheral Interface : 4 channels GA20 output control : for UPI ch 0 only Data buffer array : 80 bytes	
Serial IRQ controller	Serial IRQ request : 6 channels LPC clock monitor/control	
UART	With full-duplex double buffer (variable data length) Clock asynchronous or clock synchronized transmission (with start and stop bits) can be selectively used	
I <sup>2</sup> C	I <sup>2</sup> C (SMBus compliant) : 1 channel Support I <sup>2</sup> C bus of PHILIPS and the SMBus proposed by Intel I <sup>2</sup> C bus Selectable packet error check Timeout detection function	
Multi-address I <sup>2</sup> C	Multi-address I <sup>2</sup> C (SMBus compliant) : 1 channel Support I <sup>2</sup> C bus of PHILIPS and the SMBus proposed by Intel I <sup>2</sup> C bus Selectable packet error check Timeout detection function 6 addresses support ALERT function	

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# MB90378 Series

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Parameter	MB90F378	MB90V378
Bridge circuit	Three bus connection routes can be switched by I <sup>2</sup> C/multi-address I <sup>2</sup> C	
DTP/external interrupt	8 independent channels Selectable causes : Rise/fall edge, fall edge, "L" level or "H" level	
Extended external interrupt	8 multiplex channels × 2 set Selectable causes : Rise/fall edge, fall edge, rise edge or "L" level	
Key-on wake-up interrupt	8 independent channels Causes : "L" level	
8/10-bit A/D converter	8/10-bit resolution : 12 channels Conversion time : Less than 4.2 μs (20 MHz internal clock)	
8-bit D/A converter	8-bit resolution : 2 channels	
LCD controller/driver	Up to 9 SEG × 4 COM Selectable LCD output or CMOS I/O port	
Low-power consumption	Stop mode/Sleep mode/CPU intermittent operation mode/Watch mode	
Process	CMOS	
Package	LQFP-144 (FPT-144P-M12 : 0.4 mm pitch)	PGA299
Operating voltage	2.7 V to 3.6 V at 20 MHz*	

\* : Varies with conditions such as the operating frequency (see "■ ELECTRICAL CHARACTERISTICS"). Assurance for the MB90V378 is given only for operation with a tool at power supply voltage of 2.7 V to 3.6 V, an operating temperature of 0 °C to +25 °C, and an operating frequency of 1 MHz to 20 MHz.

## ■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB90F378	MB90V378
FPT-144P-M12	○	X
PGA299	X	○

○ : Available

X : Not available

Note : For more information about each package, see "■ PACKAGE DIMENSIONS".

## ■ DIFFERENCES AMONG PRODUCTS

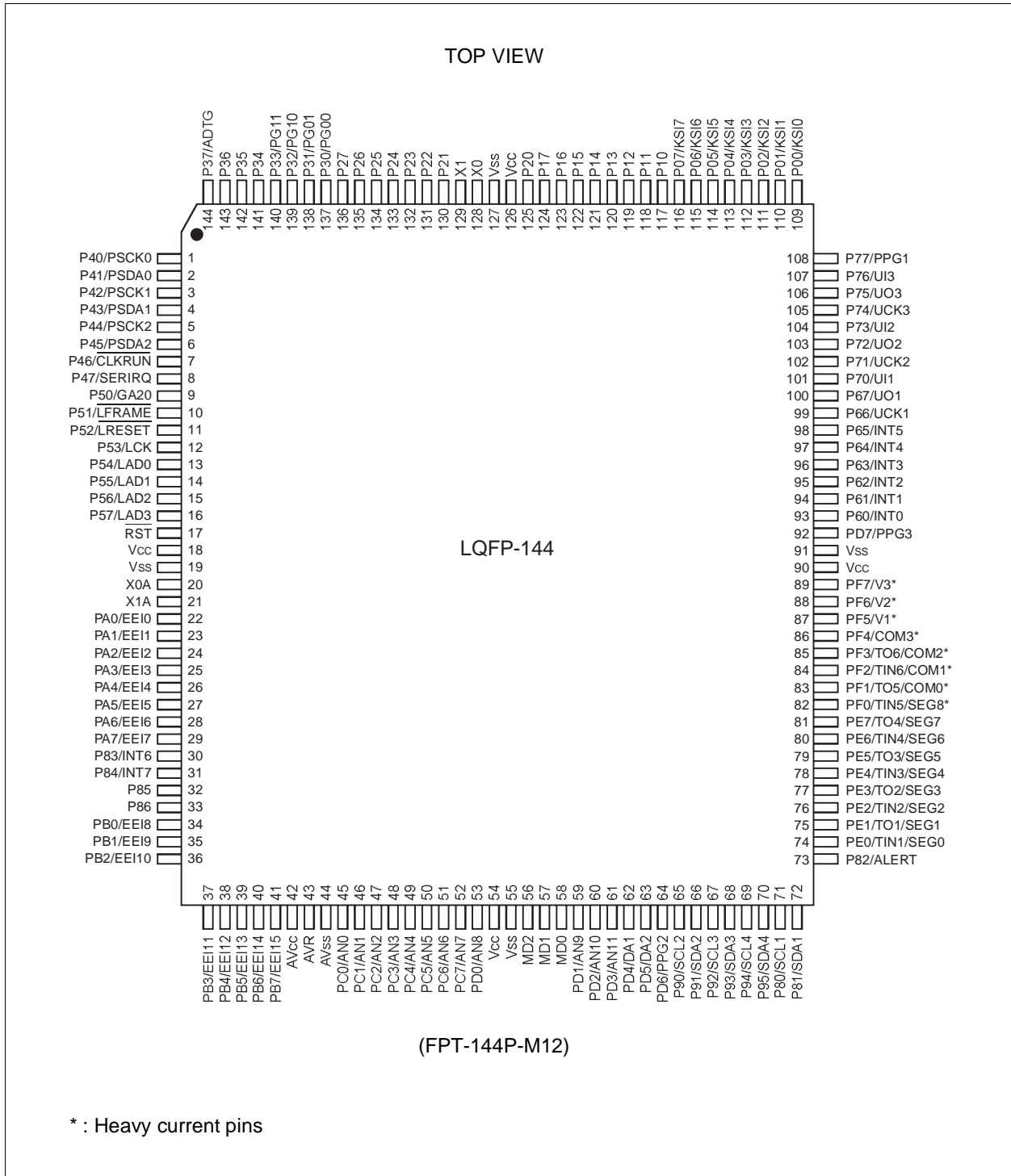
### Memory size

In evaluation with an evaluation product, note the difference between the evaluation product and the product actually used. The following items must be taken into consideration.

- The MB90V378 does not have an internal ROM, however, operations equivalent to chips with an internal ROM can be evaluated by using a dedicated development tool, enabling selection of ROM size by settings of the development tool.
- In the MB90V378, images from FF4000<sub>H</sub> to FFFFFFF<sub>H</sub> are mapped to bank 00, and FF0000<sub>H</sub> to FF3FFF<sub>H</sub> are mapped to bank FF only. (This setting can be changed by the development tool configuration.)
- In the MB90F378, images from FF4000<sub>H</sub> to FFFFFFF<sub>H</sub> are mapped to bank 00, and FF0000<sub>H</sub> to FF3FFF<sub>H</sub> are mapped to bank FF only.

# MB90378 Series

## PIN ASSIGNMENT



# MB90378 Series

## ■ PIN DESCRIPTION

Pin no. LQFP-144	Pin name	I/O circuit	Pin status during reset	Function
128,129	X0,X1	A	Oscillating	Main oscillation I/O pins.
20,21	X0A,X1A	A	Oscillating	Sub-clock oscillation I/O pins.
17	$\overline{RST}$	B	Reset input	External reset input pin.
58, 57, 56	MD0 to MD2	C	Mode input	Input pin for operation mode specification. Connect this pin directly to Vcc or Vss.
109 to 116	P00 to P07	D	Port input	General-purpose I/O ports.
	KSI0 to KSI7			Can be used as key-on wake-up interrupt input ch 0 to 7. Input is enabled when 1 is set in EICR : EN0 to 7 in standby mode.
117 to 124	P10 to P17	E		General-purpose I/O ports.
125, 130 to 136	P20 to P27	E		General-purpose I/O ports.
137, 138	P30, P31	E		General-purpose I/O ports.
	PG00, PG01			8/16-bit PPG timer output pins. 8-bit x 2 channels mode use : Event output from PG00/PG01 16-bit x 1channel mode use : Event output from PG00
139, 140	P32, P33	E		General-purpose I/O ports.
	PG10, PG11			8/16-bit PPG timer output pins. 8-bit x 2 channels mode use : Event output from PG10/PG11. 16-bit x 1channel mode use : Event output from PG10.
141 to 143	P34 to P36	E		General-purpose I/O ports.
144	P37	E		General-purpose I/O port.
	ADTG			External trigger input pin (ADTG) for the A/D converter.
1	P40	F		General-purpose Nch open-drain I/O port.
	PSCK0			Serial clock I/O pin for PS/2 interface ch 0. This function is selected when PS/2 interface ch 0 is enabled.
2	P41	F		General-purpose Nch open-drain I/O port.
	PSDA0			Serial data I/O pin for PS/2 interface ch 0. This function is selected when PS/2 interface ch 0 is enabled.
3	P42	F		General-purpose Nch open-drain I/O port.
	PSCK1			Serial clock I/O pin for PS/2 interface ch 1. This function is selected when PS/2 interface ch 1 is enabled.
4	P43	F		General-purpose Nch open-drain I/O port.
	PSDA1			Serial data I/O pin for PS/2 interface ch 1. This function is selected when PS/2 interface ch 1 is enabled.

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# MB90378 Series

Pin no.	Pin name	I/O circuit	Pin status during reset	Function
LQFP-144				
5	P44	F	Port input	General-purpose Nch open-drain I/O port.
	PSCK2			Serial clock I/O pin for PS/2 interface ch 2. This function is selected when PS/2 interface ch 2 is enabled.
6	P45	F		General-purpose Nch open-drain I/O port.
	PSDA2			Serial data I/O pin for PS/2 interface ch 2. This function is selected when PS/2 interface ch 2 is enabled.
7	P46	G		General-purpose Nch open-drain I/O port.
	$\overline{\text{CLKRUN}}$			LPC clock status / restart request I/O pin for serial IRQ controller. This function is selected when serial IRQ and LPC clock restart request is enabled.
8	P47	H		General-purpose I/O port.
	SERIRQ			Serial IRQ data I/O pin for serial IRQ controller. This function is selected when serial IRQ is enabled.
9	P50	J		General-purpose Nch open-drain I/O port.
	GA20			GA20 output for LPC interface. This function is selected when GA20 function is enabled.
10	P51	H		General-purpose I/O port.
	$\overline{\text{LFRAME}}$			LFRAME input for LPC interface. This function is selected when LPC interface is enabled.
11	P52	H		General-purpose I/O port.
	$\overline{\text{LRESET}}$			Reset input for LPC interface. This function is selected when LPC interface is enabled.
12	P53	H		General-purpose I/O port.
	LCK			Clock input for LPC interface. This function is selected when LPC interface is enabled.
13 to 16	P54 to P57	H		General-purpose I/O ports.
	LAD0 to LAD3			Address/Data I/O for LPC interface. This function is selected when LPC interface is enabled.
93 to 98	P60 to P65	I		General-purpose I/O ports.
	INT0 to INT5			Can be used as DTP/external interrupt request input ch 0 to 5. Input is enabled when 1 is set in ENIR: EN0 to 5 in standby mode.
99	P66	I	General-purpose I/O port.	
	UCK1		Serial clock I/O pin for UART ch 1. This function is enabled when UART ch 1 enables clock output.	

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# MB90378 Series

Pin no.	Pin name	I/O circuit	Pin status during reset	Function
LQFP-144				
100	P67	I	Port input	General-purpose I/O port.
	UO1			Serial data output pin for UART ch 1. This function is enabled when UART ch 1 enables data output.
101	P70	I		General-purpose I/O port.
	UI1			Serial data input pin for UART ch 1. While UART ch 1 is operating for input, the input of this pin is used as required and must not be used for any other input.
102	P71	I		General-purpose I/O port.
	UCK2			Serial clock I/O pin for UART ch 2. This function is enabled when UART ch 2 enables clock output.
103	P72	I		General-purpose I/O port.
	UO2			Serial data output pin for UART ch 2. This function is enabled when UART ch 2 enables data output.
104	P73	I		General-purpose I/O port.
	UI2			Serial data input pin for UART ch 2. While UART ch 2 is operating for input, the input of this pin is used as required and must not be used for any other input.
105	P74	I		General-purpose I/O port.
	UCK3			Serial clock I/O pin for UART ch 3. This function is enabled when UART ch 3 enables clock output.
106	P75	I		General-purpose I/O port.
	UO3			Serial data output pin for UART ch 3. This function is enabled when UART ch 3 enables data output.
107	P76	I		General-purpose I/O port.
	UI3			Serial data input pin for UART ch 3. While UART ch 3 is operating for input, the input of this pin is used as required and must not be used for any other input.
108	P77	I		General-purpose I/O port.
	PPG1			Output pin for PPG ch 1. This function is enabled when PPG ch 1 output is enabled.
71	P80	T		General-purpose Nch open-drain I/O port.
	SCL1			Serial clock I/O pin for multi-address I <sup>2</sup> C.
72	P81	T	General-purpose Nch open-drain I/O port.	
	SDA1		Serial data I/O pin for multi-address I <sup>2</sup> C.	

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# MB90378 Series

Pin no. LQFP-144	Pin name	I/O circuit	Pin status during reset	Function
73	P82	J	Port input	General-purpose Nch open-drain I/O port.
	ALERT			ALERT output pin for multi-address I <sup>2</sup> C.
30, 31	P83, P84	I		General-purpose I/O ports.
	INT6, INT7			Can be used as DTP/external interrupt request input ch6, 7. Input is enabled when 1 is set in ENIR: EN6, 7 in standby mode.
32	P85	I		General-purpose I/O port.
33	P86	I		General-purpose I/O port.
65	P90	T		General-purpose Nch open-drain I/O port.
	SCL2			Serial clock I/O pin for bridge circuit.
66	P91	T		General-purpose Nch open-drain I/O port.
	SDA2			Serial data I/O pin for bridge circuit.
67	P92	T		General-purpose Nch open-drain I/O port.
	SCL3			Serial clock I/O pin for bridge circuit.
68	P93	T		General-purpose Nch open-drain I/O port.
	SDA3			Serial data I/O pin for bridge circuit.
69	P94	T		General-purpose Nch open-drain I/O port.
	SCL4			Serial clock I/O pin for bridge circuit.
70	P95	T		General-purpose Nch open-drain I/O port.
	SDA4			Serial data I/O pin for bridge circuit.
22 to 29	PA0 to PA7	I		General-purpose I/O ports.
	EEI0 to EEI7			External IRQ input pin for Extend External Interrupt request ch0 to 7. When IRQ detect, prepare to the CPU Interrupt. (Multiplex)
34 to 41	PB0 to PB7	I	General-purpose I/O ports.	
	EEI8 to EEI15		External IRQ input pin for Extend External Interrupt request ch8 to 15. When IRQ detect, prepare to the CPU Interrupt. (Multiplex)	
45 to 52	PC0 to PC7	M	A/D input	General-purpose I/O ports.
	AN0 to AN7			A/D converter analog input pin 0 to 7. This function is enabled when the analog input specification is enabled (ADER1).
53, 59 to 61	PD0 to PD3	M	General-purpose I/O ports.	
	AN8 to AN11		A/D converter analog input pin 8 to 11. This function is enabled when the analog input specification is enabled (ADER2).	

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# MB90378 Series

Pin no.	Pin name	I/O circuit	Pin status during reset	Function
LQFP-144				
62, 63	PD4, PD5	N	Port input	General-purpose I/O ports.
	DA1, DA2			D/A converter analog output 1, 2. This function is selected when D/A converted is enabled.
64, 92	PD6, PD7	H		General-purpose I/O ports.
	PPG2, PPG3			Output pin for PPG ch 2, 3. This function is selected when PPG ch 2, 3 output is enabled.
74	PE0	O		General-purpose I/O port.
	SEG0			Segment output pin for LCD controller/driver. This function is selected when LCD segment output is enabled.
	TIN1			External clock input pin for reload timer 1.
75	PE1	O		General-purpose I/O port.
	SEG1			Segment output pin for LCD controller/driver. This function is selected when LCD segment output is enabled.
	TO1			Event output pin for reload timer 1.
76	PE2	O		General-purpose I/O port.
	SEG2			Segment output pin for LCD controller/driver. This function is selected when LCD segment output is enabled.
	TIN2			External clock input pin for reload timer 2.
77	PE3	O		General-purpose I/O port.
	SEG3			Segment output pin for LCD controller/driver. This function is selected when LCD segment output is enabled.
	TO2			Event output pin for reload timer 2.
78	PE4	O	General-purpose I/O port.	
	SEG4		Segment output pin for LCD controller/driver. This function is selected when LCD segment output is enabled.	
	TIN3		External clock input pin for reload timer 3.	
79	PE5	O	General-purpose I/O port.	
	SEG5		Segment output pin for LCD controller/driver. This function is selected when LCD segment output is enabled.	
	TO3		Event output pin for reload timer 3.	
80	PE6	O	General-purpose I/O port.	
	SEG6		Segment output pin for LCD controller/driver. This function is selected when LCD segment output is enabled.	
	TIN4		External clock input pin for reload timer 4.	

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# MB90378 Series

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Pin no.	Pin name	I/O circuit	Pin status during reset	Function
LQFP-144				
81	PE7	O	Port input	General-purpose I/O port.
	SEG7			Segment output pin for LCD controller/driver. This function is selected when LCD segment output is enabled.
	TO4			Event output pin for reload timer 4.
82	PF0	P		General-purpose Nch Open-drain I/O port.
	SEG8			Segment output pin for LCD controller/driver. This function is selected when LCD segment output is enabled.
	TIN5			External clock input pin for reload timer 5.
83	PF1	P		General-purpose Nch Open-drain I/O port.
	COM0			COM output pin for LCD controller/driver. This function is selected when LCD COM output is enabled.
	TO5			Event output pin for reload timer 5.
84	PF2	P		General-purpose Nch Open-drain I/O port.
	COM1			COM output pin for LCD controller/driver. This function is selected when LCD COM output is enabled.
	TIN6			External clock input pin for reload timer 6.
85	PF3	P	General-purpose Nch Open-drain I/O port.	
	COM2		COM output pin for LCD controller/driver. This function is selected when LCD COM output is enabled.	
	TO6		Event output pin for reload timer 6.	
86	PF4	P	General-purpose Nch Open-drain I/O port.	
	COM3		COM output pin for LCD controller/driver. This function is selected when LCD COM output is enabled.	
87 to 89	PF5 to PF7	Q	Power input	General-purpose Nch Open-drain I/O ports.
	V1 to V3			Power input pin for LCD controller/driver. This function is selected when external voltage divider is enabled.
42	AV <sub>cc</sub>	R	Power input	V <sub>cc</sub> power input pin for analog circuits.
43	AV <sub>R</sub>	S		V <sub>ref+</sub> input pin for the A/D converter. This voltage must not exceed V <sub>cc</sub> . V <sub>ref-</sub> is fixed to AV <sub>ss</sub> .
44	AV <sub>ss</sub>	R		V <sub>ss</sub> power input pin for analog circuits.
19,55,91,127	V <sub>ss</sub>	–	Source Power input	Power (0 V) input pin.
18,54,90,126	V <sub>cc</sub>	–		Power (3.3 V) input pin.

# MB90378 Series

## I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		Main/Sub clock (main/sub clock crystal oscillator) <ul style="list-style-type: none"> <li>• At an oscillation feedback resistor of approximately 1 M<math>\Omega</math></li> </ul>
B		<ul style="list-style-type: none"> <li>• CMOS hysteresis input</li> <li>• Pull-up resistor approximately 50 k<math>\Omega</math></li> </ul>
C		<ul style="list-style-type: none"> <li>• CMOS hysteresis input</li> </ul>
D		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS hysteresis input</li> <li>• Selectable pull-up resistor approximately 50 k<math>\Omega</math></li> <li>• I<sub>OL</sub> = 4 mA</li> </ul>
E		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• Selectable pull-up resistor approximately 50 k<math>\Omega</math></li> <li>• I<sub>OL</sub> = 4 mA</li> </ul>
F		<ul style="list-style-type: none"> <li>• Nch open-drain output</li> <li>• CMOS hysteresis input</li> <li>• I<sub>OL</sub> = 4 mA</li> <li>• 5 V tolerant</li> </ul>

(Continued)

# MB90378 Series

Type	Circuit	Remarks
G		<ul style="list-style-type: none"> <li>• Nch open-drain output</li> <li>• CMOS input</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> </ul>
H		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> </ul>
I		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS hysteresis input</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> </ul>
J		<ul style="list-style-type: none"> <li>• Nch open-drain output</li> <li>• CMOS input</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> <li>• 5 V tolerant</li> </ul>
M		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• A/D analog input</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> </ul>

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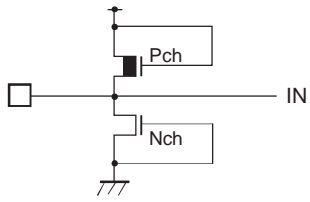
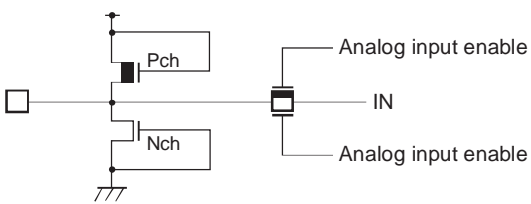
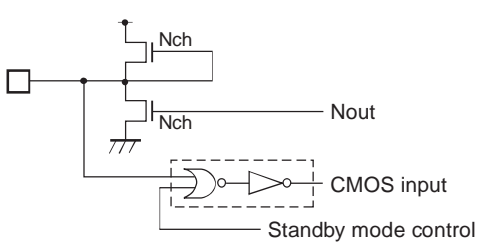
# MB90378 Series

Type	Circuit	Remarks
N		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• D/A analog output</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> </ul>
O		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS hysteresis input</li> <li>• Segment output</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> </ul>
P		<ul style="list-style-type: none"> <li>• Nch open-drain output</li> <li>• CMOS hysteresis input</li> <li>• Segment output</li> <li>• <math>I_{OL} = 12 \text{ mA}</math></li> </ul>
Q		<ul style="list-style-type: none"> <li>• Nch open-drain output</li> <li>• CMOS hysteresis input</li> <li>• LCD driving power supply</li> <li>• <math>I_{OL} = 12 \text{ mA}</math></li> </ul>

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# MB90378 Series

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Type	Circuit	Remarks
R		<ul style="list-style-type: none"> <li>• Power supply input protection circuit</li> </ul>
S		<ul style="list-style-type: none"> <li>• A/D converter reference voltage (AVR) input pin with protection circuit</li> </ul>
T		<ul style="list-style-type: none"> <li>• Nch open-drain output</li> <li>• CMOS input</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> <li>• 5 V tolerant</li> </ul>

# MB90378 Series

## ■ HANDLING DEVICES

### 1. Be sure that the maximum rated voltage is not exceeded (latch-up prevention).

A latch-up may occur on a CMOS IC if a voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  is applied to an input or output pin other than medium-to-high voltage pins. A latch-up may also occur if a voltage higher than the rating is applied between  $V_{CC}$  pin and  $V_{SS}$  pin. A latch-up causes a rapid increase in the power supply current, which can result in thermal damage to an element. Take utmost care that the maximum rated voltage is not exceeded.

When turning the power on or off to analog circuits, be sure that the analog supply voltages ( $AV_{CC}$ ,  $AVR$ ) and analog input voltage do not exceed the digital supply voltage ( $V_{CC}$ ).

### 2. Stabilize the supply voltages

Even within the operation guarantee range of the  $V_{CC}$  supply voltage, a malfunction can be caused if the supply voltage undergoes a rapid change. For voltage stabilization guidelines, the  $V_{CC}$  ripple fluctuations (P-P value) at commercial frequencies (50 Hz to 60 Hz) should be suppressed to "10%" or less of the reference  $V_{CC}$  value. During a momentary change such as when switching a supply voltage, voltage fluctuations should also be suppressed so that the "transient fluctuation rate" is 0.1 V/ms or less.

### 3. Power-on

To prevent a malfunction in the built-in voltage drop circuit, secure "50  $\mu$ s (between 0.2 V and 1.8 V)" or more for the voltage rise time during power-on.

### 4. Treatment of unused input pins

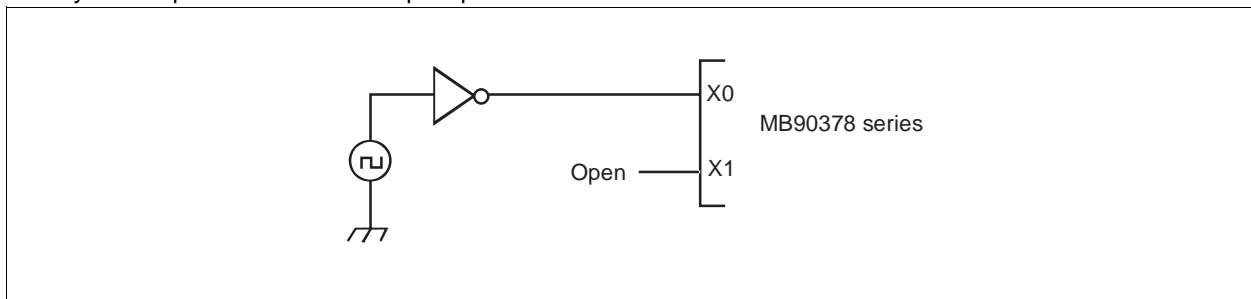
An unused input pin may cause a malfunction if it is left open. Every unused input pin should be pulled up or down.

### 5. Treatment of A/D converter, and D/A converter power pin

When the A/D converter, D/A converter and comparator is not used, connect the pins as follows:  $AV_{CC} = V_{CC}$ ,  $AV_{SS} = AVR = V_{SS}$ .

### 6. Notes on external clock

When an external clock is used, the oscillation stabilization wait time is required at power-on reset or at cancellation of sub-clock mode or stop mode. As shown in diagram below, when an external clock is used, connect only the X0 pin and leave the X1 pin open.





## 7. Power supply pins

When a device has two or more  $V_{CC}$  or  $V_{SS}$  pins, the pins that should have equal potential are connected within the device in order to prevent a latch-up or other malfunction. To reduce extraneous emission, to prevent a malfunction of the strobe signal due to an increase in the group level, and to maintain the local output current rating, connect all these power supply pins to an external power supply and ground them.

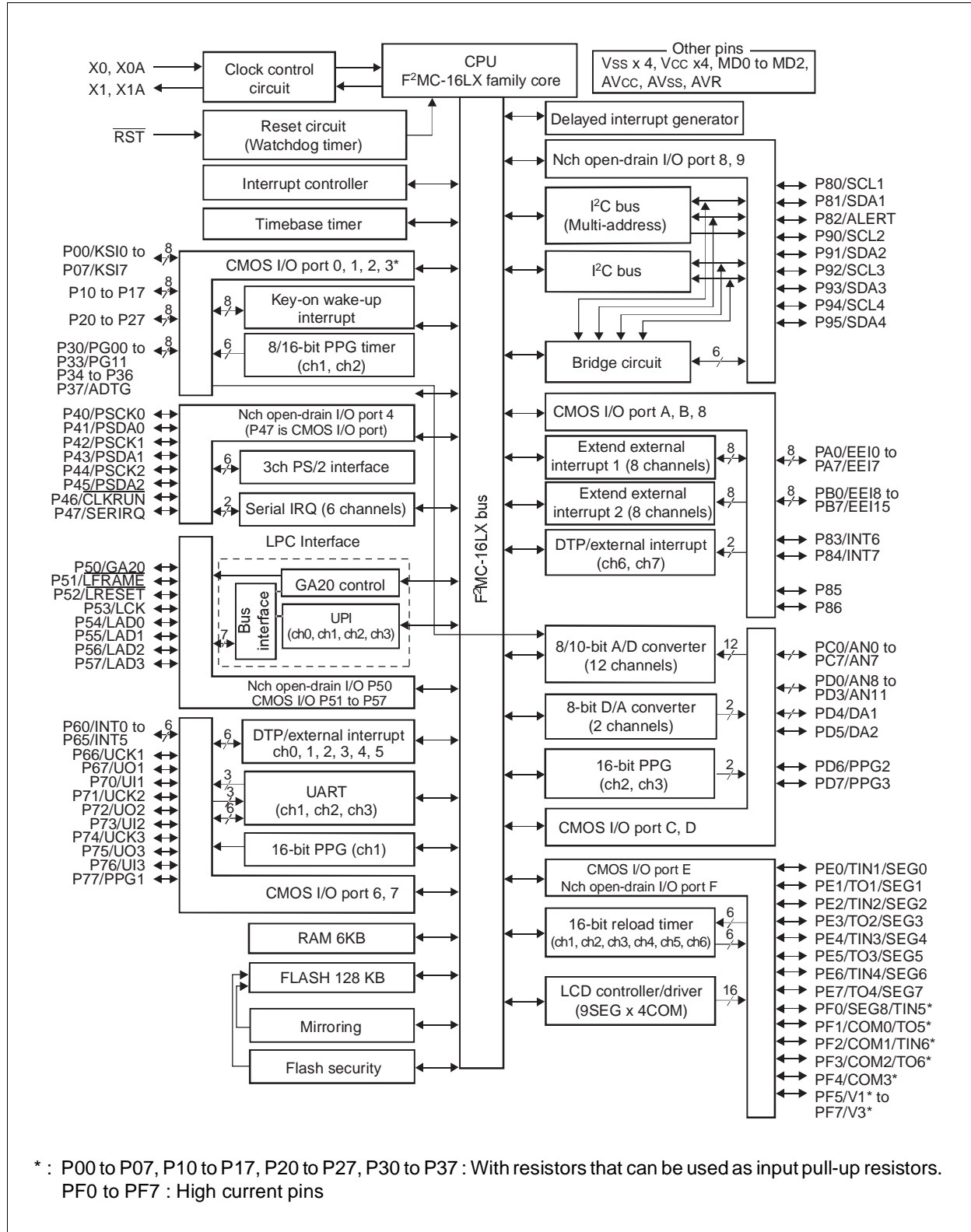
The current source should be connected to the  $V_{CC}$  and  $V_{SS}$  pins of the device with minimum impedance. It is recommended that a bypass capacitor of about 0.1  $\mu\text{F}$  be connected near the terminals between  $V_{CC}$  and  $V_{SS}$ .

## 8. Analog power-on sequence of A/D converter and D/A converter

The power to the A/D converter and D/A converter ( $AV_{CC}$ , AVR) and analog inputs (AN0 to AN11) must be turned on after the power to the digital circuits ( $V_{CC}$ ) is turned on. When turning off the power, turn off the power to the digital circuits ( $V_{CC}$ ) after turning off the power to the A/D converter, D/A converter and analog inputs. When the power is turned on or off, AVR should not exceed  $AV_{CC}$ . Also, when a pin that is used for A/D analog input is also used as an input port, the input voltage should not exceed  $AV_{CC}$ . (The power to the analog circuits and the power to the digital circuits can be simultaneously turned on or off.)

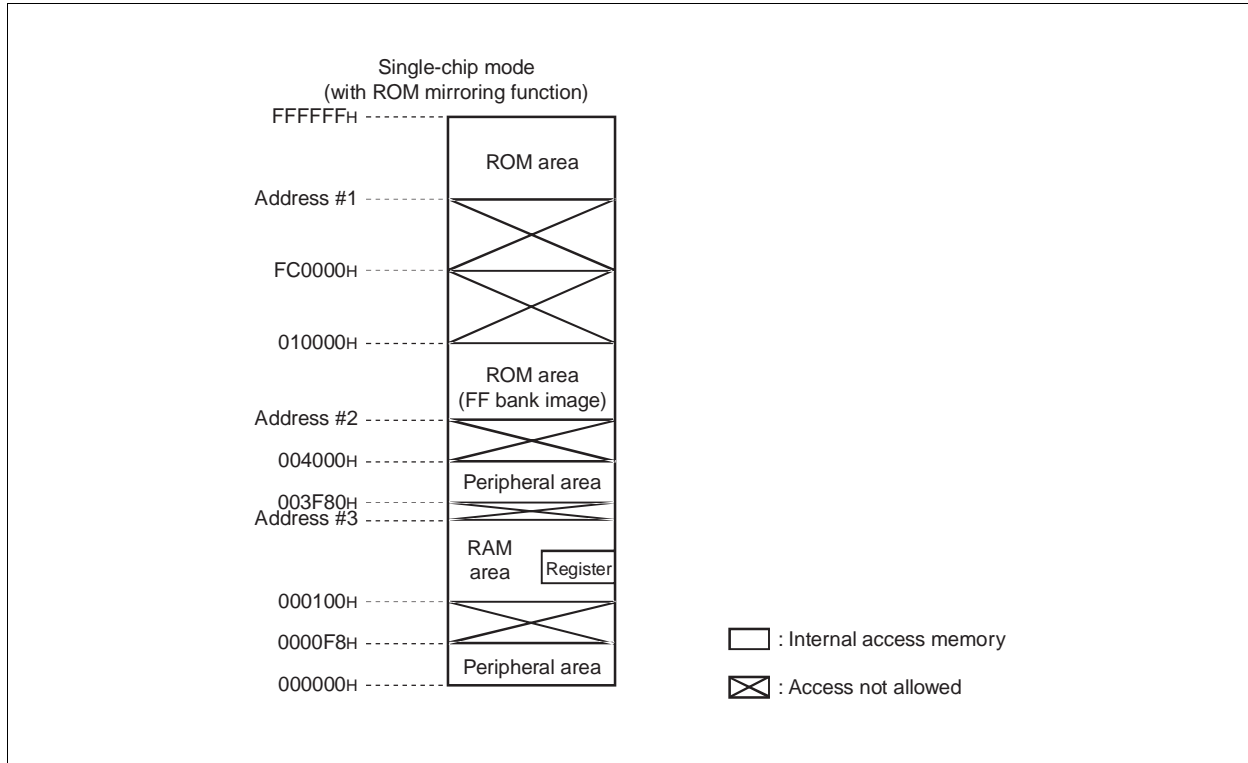
# MB90378 Series

## ■ BLOCK DIAGRAM



# MB90378 Series

## MEMORY MAP



Model	Address #1	Address #2	Address #3
MB90F378	FE0000H	004000H	001900H
MB90V378	FE0000H*	004000H*	003F80H

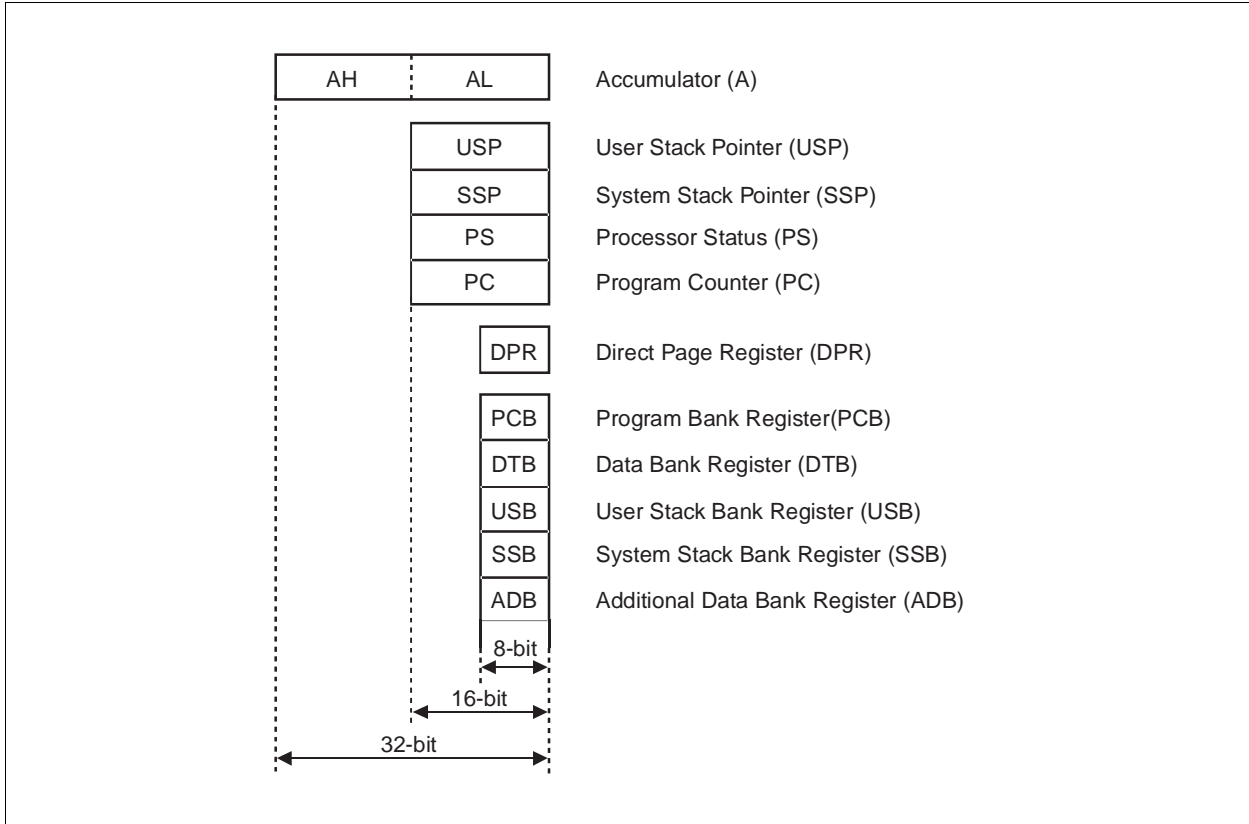
\* : The MB90V378 does not contain ROM. Assume that the development tool uses these area for its ROM decode areas.

- Notes :
- If single-chip mode (without ROM mirroring function) is selected, see Chapter 32, "ROM Mirroring Function Selection Module" of the MB90378 series H/W manual.
  - ROM data in the FF bank can be seen as an image in the higher 00 bank to validate the small model C compiler. Because addresses of the 16 low-order bits in the FF bank are the same, the table in ROM can be referenced without the "far" specification. For example, when 00C000H is accessed, the contents of ROM at FFC000H are actually accessed. The ROM area in the FF bank exceeds 48 Kbytes, and all areas cannot be seen as images in the 00 bank. Because ROM data from FF4000H to FFFFFFFH is seen as an image at 004000H to 00FFFFH, the ROM data table should be stored in the area from FF4000H to FFFFFFFH.

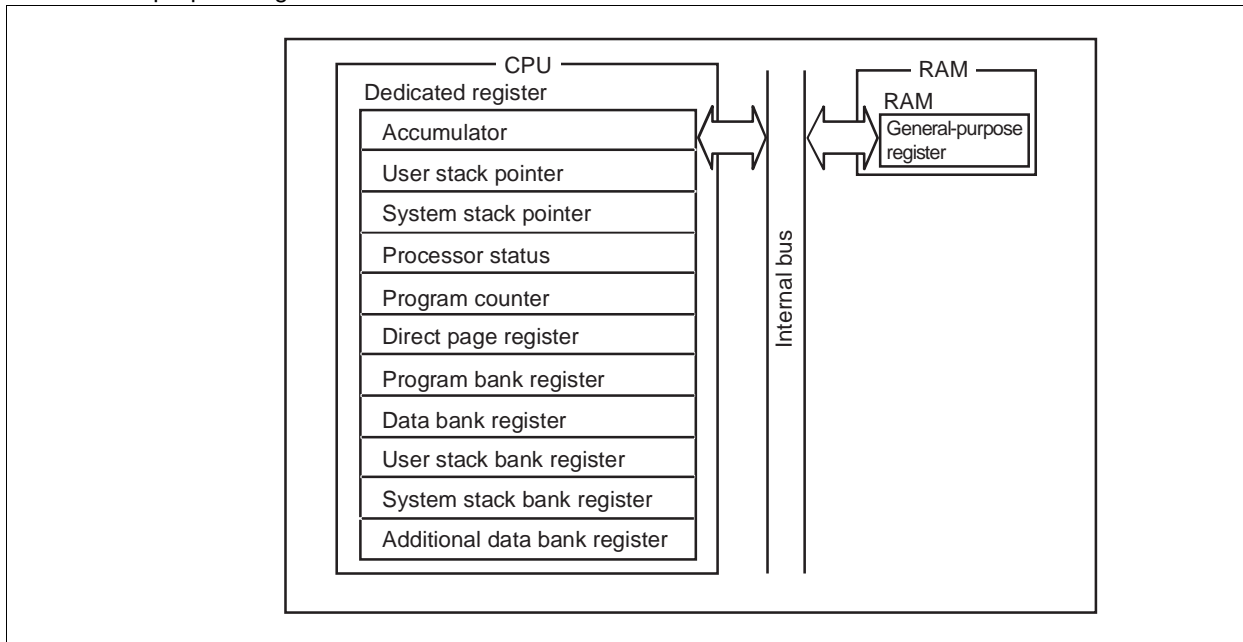
# MB90378 Series

## ■ F<sup>2</sup>MC-16LX CPU PROGRAMMING MODEL

- Dedicated registers

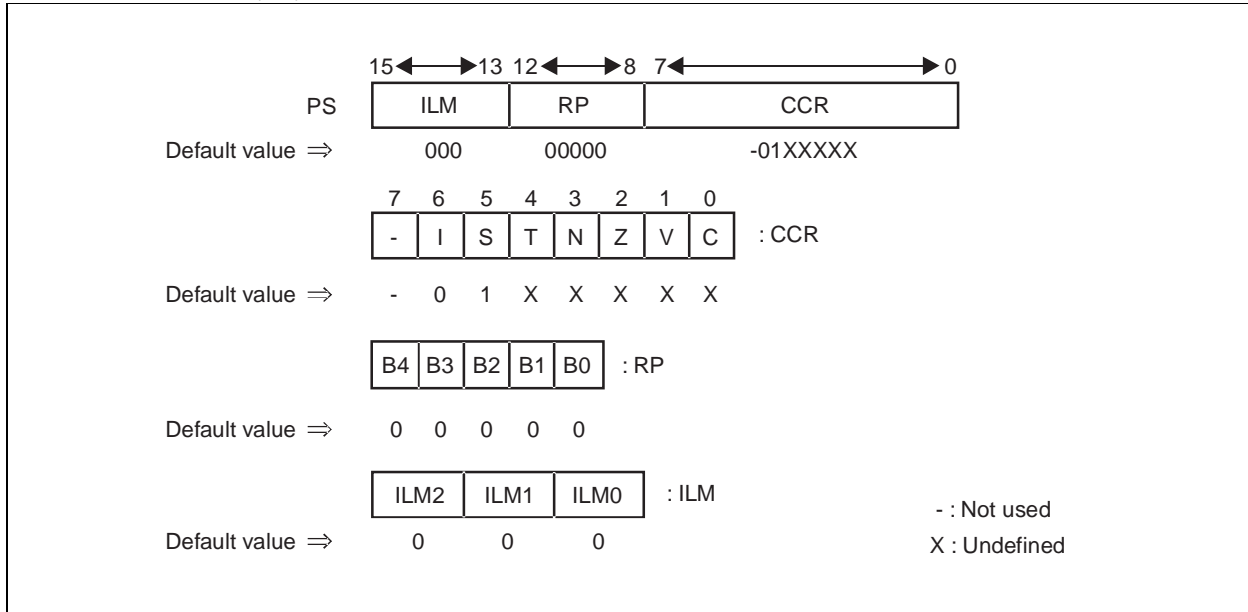


- General-purpose registers



# MB90378 Series

## • Processor status (PS)



# MB90378 Series

## ■ I/O MAP

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
000000 <sub>H</sub>	PDR0	Port 0 data register	R/W	R/W	Port 0	XXXXXXXX <sub>B</sub>
000001 <sub>H</sub>	PDR1	Port 1 data register	R/W	R/W	Port 1	XXXXXXXX <sub>B</sub>
000002 <sub>H</sub>	PDR2	Port 2 data register	R/W	R/W	Port 2	XXXXXXXX <sub>B</sub>
000003 <sub>H</sub>	PDR3	Port 3 data register	R/W	R/W	Port 3	XXXXXXXX <sub>B</sub>
000004 <sub>H</sub>	PDR4	Port 4 data register	R/W	R/W	Port 4	X1111111 <sub>B</sub>
000005 <sub>H</sub>	PDR5	Port 5 data register	R/W	R/W	Port 5	XXXXXXXX1 <sub>B</sub>
000006 <sub>H</sub>	PDR6	Port 6 data register	R/W	R/W	Port 6	XXXXXXXX <sub>B</sub>
000007 <sub>H</sub>	PDR7	Port 7 data register	R/W	R/W	Port 7	XXXXXXXX <sub>B</sub>
000008 <sub>H</sub>	PDR8	Port 8 data register	R/W	R/W	Port 8	-XXXX111 <sub>B</sub>
000009 <sub>H</sub>	PDR9	Port 9 data register	R/W	R/W	Port 9	--111111 <sub>B</sub>
00000A <sub>H</sub>	PDRA	Port A data register	R/W	R/W	Port A	XXXXXXXX <sub>B</sub>
00000B <sub>H</sub>	PDRB	Port B data register	R/W	R/W	Port B	XXXXXXXX <sub>B</sub>
00000C <sub>H</sub>	PDRC	Port C data register	R/W	R/W	Port C	XXXXXXXX <sub>B</sub>
00000D <sub>H</sub>	PDRD	Port D data register	R/W	R/W	Port D	XXXXXXXX <sub>B</sub>
00000E <sub>H</sub>	PDRE	Port E data register	R/W	R/W	Port E	XXXXXXXX <sub>B</sub>
00000F <sub>H</sub>	PDRF	Port F data register	R/W	R/W	Port F	11111111 <sub>B</sub>
000010 <sub>H</sub>	DDR0	Port 0 direction register	R/W	R/W	Port 0	00000000 <sub>B</sub>
000011 <sub>H</sub>	DDR1	Port 1 direction register	R/W	R/W	Port 1	00000000 <sub>B</sub>
000012 <sub>H</sub>	DDR2	Port 2 direction register	R/W	R/W	Port 2	00000000 <sub>B</sub>
000013 <sub>H</sub>	DDR3	Port 3 direction register	R/W	R/W	Port 3	00000000 <sub>B</sub>
000014 <sub>H</sub>	DDR4	Port 4 direction register	R/W	R/W	Port 4	0----- <sub>B</sub>
000015 <sub>H</sub>	DDR5	Port 5 direction register	R/W	R/W	Port 5	0000000- <sub>B</sub>
000016 <sub>H</sub>	DDR6	Port 6 direction register	R/W	R/W	Port 6	00000000 <sub>B</sub>
000017 <sub>H</sub>	DDR7	Port 7 direction register	R/W	R/W	Port 7	00000000 <sub>B</sub>
000018 <sub>H</sub>	PGDR	Parity generator data register	R/W	R/W	Parity generator	XXXXXXXX <sub>B</sub>
000019 <sub>H</sub>	PGCSR	Parity generator control status register	R/W	R/W		X-----0 <sub>B</sub>
00001A <sub>H</sub>	DDRA	Port A direction register	R/W	R/W	Port A	00000000 <sub>B</sub>
00001B <sub>H</sub>	DDRB	Port B direction register	R/W	R/W	Port B	00000000 <sub>B</sub>
00001C <sub>H</sub>	DDRC	Port C direction register	R/W	R/W	Port C	00000000 <sub>B</sub>
00001D <sub>H</sub>	DDRD	Port D direction register	R/W	R/W	Port D	00000000 <sub>B</sub>
00001E <sub>H</sub>	DDRE	Port E direction register	R/W	R/W	Port E	00000000 <sub>B</sub>
00001F <sub>H</sub>	DDR8	Port 8 direction register	R/W	R/W	Port 8	-0000--- <sub>B</sub>

(Continued)

# MB90378 Series

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
000020 <sub>H</sub>	SMR1	Serial mode register 1	R/W	R/W	UART1	00000-00 <sub>B</sub>
000021 <sub>H</sub>	SCR1	Serial control register 1	R/W	R/W		00000100 <sub>B</sub>
000022 <sub>H</sub>	SIDR1/ SODR1	Input data register 1/ Output data register 1	R/W	R/W		XXXXXXXX <sub>B</sub>
000023 <sub>H</sub>	SSR1	Serial status register 1	R/W	R/W		00001000 <sub>B</sub>
000024 <sub>H</sub>	M2CR1	Mode 2 control register 1	R/W	R/W		----1000 <sub>B</sub>
000025 <sub>H</sub>	CDCR1	Clock division control register 1	R/W	R/W	Communication prescaler 1	00--0000 <sub>B</sub>
000026 <sub>H</sub>	ENIR	Interrupt/DTP enable register	R/W	R/W	DTP/external interrupt	00000000 <sub>B</sub>
000027 <sub>H</sub>	EIRR	Interrupt/DTP cause register	R/W	R/W		XXXXXXXX <sub>B</sub>
000028 <sub>H</sub>	ELVR	Request level setting register	R/W	R/W		00000000 <sub>B</sub>
000029 <sub>H</sub>			R/W	R/W		00000000 <sub>B</sub>
00002A <sub>H</sub>	ADER1	Analog input enable register 1	R/W	R/W	Port C, A/D	11111111 <sub>B</sub>
00002B <sub>H</sub>	ADER2	Analog input enable register 2	R/W	R/W	Port D, A/D	----1111 <sub>B</sub>
00002C <sub>H</sub>	BRSR	Bridge circuit selection register	R/W	R/W	Bridge circuit	--000000 <sub>B</sub>
00002D <sub>H</sub>	ADC0	A/D control register	R/W	R/W	8/10-bit A/D converter	00000000 <sub>B</sub>
00002E <sub>H</sub>	ADCR0	A/D data register	R	R		XXXXXXXX <sub>B</sub>
00002F <sub>H</sub>	ADCR1		R/W	R/W		00000-XX <sub>B</sub>
000030 <sub>H</sub>	ADCS0	A/D control status register	R/W	R/W		00----- <sub>B</sub>
000031 <sub>H</sub>	ADCS1		R/W	R/W		00000000 <sub>B</sub>
000032 <sub>H</sub>	SICRL	Serial interrupt request register	R/W	R/W		Serial IRQ
000033 <sub>H</sub>	SICRH	Serial interrupt control register	R/W	R/W	00000000 <sub>B</sub>	
000034 <sub>H</sub>	SIFR1	Serial interrupt frame number register 1	R/W	R/W	--000000 <sub>B</sub>	
000035 <sub>H</sub>	SIFR2	Serial interrupt frame number register 2	R/W	R/W	--000000 <sub>B</sub>	
000036 <sub>H</sub>	SIFR3	Serial interrupt frame number register 3	R/W	R/W	--000000 <sub>B</sub>	
000037 <sub>H</sub>	SIFR4	Serial interrupt frame number register 4	R/W	R/W	--000000 <sub>B</sub>	
000038 <sub>H</sub>	PDCRL1	PPG1 down counter register	—	R	16-bit PPG timer (ch1)	11111111 <sub>B</sub>
000039 <sub>H</sub>	PDCRH1		—	R		11111111 <sub>B</sub>
00003A <sub>H</sub>	PCSRL1	PPG1 period setting register	—	W		XXXXXXXX <sub>B</sub>
00003B <sub>H</sub>	PCSRH1		—	W		XXXXXXXX <sub>B</sub>
00003C <sub>H</sub>	PDUTL1	PPG1 duty setting register	—	W		XXXXXXXX <sub>B</sub>
00003D <sub>H</sub>	PDUTH1		—	W		XXXXXXXX <sub>B</sub>
00003E <sub>H</sub>	PCNTL1	PPG1 control status register	R/W	R/W		--000000 <sub>B</sub>
00003F <sub>H</sub>	PCNTH1		R/W	R/W		00000000 <sub>B</sub>

(Continued)

# MB90378 Series

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
000040 <sub>H</sub>	PDCRL2	PPG2 down counter register	—	R	16-bit PPG timer (ch2)	11111111 <sub>B</sub>
000041 <sub>H</sub>	PDCRH2		—	R		11111111 <sub>B</sub>
000042 <sub>H</sub>	PCSRL2	PPG2 period setting register	—	W		XXXXXXXX <sub>B</sub>
000043 <sub>H</sub>	PCSRH2		—	W		XXXXXXXX <sub>B</sub>
000044 <sub>H</sub>	PDUTL2	PPG2 duty setting register	—	W		XXXXXXXX <sub>B</sub>
000045 <sub>H</sub>	PDUTH2		—	W		XXXXXXXX <sub>B</sub>
000046 <sub>H</sub>	PCNTL2	PPG2 control status register	R/W	R/W		--00000 <sub>B</sub>
000047 <sub>H</sub>	PCNTH2		R/W	R/W		00000000 <sub>B</sub>
000048 <sub>H</sub>	PDCRL3	PPG3 down counter register	—	R	16-bit PPG timer (ch3)	11111111 <sub>B</sub>
000049 <sub>H</sub>	PDCRH3		—	R		11111111 <sub>B</sub>
00004A <sub>H</sub>	PCSRL3	PPG3 period setting register	—	W		XXXXXXXX <sub>B</sub>
00004B <sub>H</sub>	PCSRH3		—	W		XXXXXXXX <sub>B</sub>
00004C <sub>H</sub>	PDUTL3	PPG3 duty setting register	—	W		XXXXXXXX <sub>B</sub>
00004D <sub>H</sub>	PDUTH3		—	W		XXXXXXXX <sub>B</sub>
00004E <sub>H</sub>	PCNTL3	PPG3 control status register	R/W	R/W		--00000 <sub>B</sub>
00004F <sub>H</sub>	PCNTH3		R/W	R/W		00000000 <sub>B</sub>
000050 <sub>H</sub>	PSCR0	PS/2 interface control register 0	R/W	R/W	3-channel PS/2 interface	0--00000 <sub>B</sub>
000051 <sub>H</sub>	PSSR0	PS/2 interface status register 0	R/W	R/W		00000000 <sub>B</sub>
000052 <sub>H</sub>	PSCR1	PS/2 interface control register 1	R/W	R/W		0--00000 <sub>B</sub>
000053 <sub>H</sub>	PSSR1	PS/2 interface status register 1	R/W	R/W		00000000 <sub>B</sub>
000054 <sub>H</sub>	PSCR2	PS/2 interface control register 2	R/W	R/W		0--00000 <sub>B</sub>
000055 <sub>H</sub>	PSSR2	PS/2 interface status register 2	R/W	R/W		00000000 <sub>B</sub>
000056 <sub>H</sub>	PSDR0	PS/2 interface data register 0	R/W	R/W		00000000 <sub>B</sub>
000057 <sub>H</sub>	PSDR1	PS/2 interface data register 1	R/W	R/W		00000000 <sub>B</sub>
000058 <sub>H</sub>	PSDR2	PS/2 interface data register 2	R/W	R/W		00000000 <sub>B</sub>
000059 <sub>H</sub>	PSMR	PS/2 interface mode register	R/W	R/W		----0000 <sub>B</sub>
00005A <sub>H</sub>	DAT0	D/A converter data register 0	R/W	R/W	8-bit D/A converter	XXXXXXXX <sub>B</sub>
00005B <sub>H</sub>	DAT1	D/A converter data register 1	R/W	R/W		XXXXXXXX <sub>B</sub>
00005C <sub>H</sub>	DACR0	D/A control register 0	R/W	R/W		-----0 <sub>B</sub>
00005D <sub>H</sub>	DACR1	D/A control register 1	R/W	R/W		-----0 <sub>B</sub>

(Continued)



# MB90378 Series

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
00005E <sub>H</sub>	UPAL1	UPI1 address register (lower)	R/W	R/W	LPC interface	XXXXXXXX <sub>B</sub>
00005F <sub>H</sub>	UPAH1	UPI1 address register (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
000060 <sub>H</sub>	UPAL2	UPI2 address register (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
000061 <sub>H</sub>	UPAH2	UPI2 address register (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
000062 <sub>H</sub>	UPAL3	UPI3 address register (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
000063 <sub>H</sub>	UPAH3	UPI3 address register (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
000064 <sub>H</sub>	UPCL	UPI control register (lower)	R/W	R/W		00000000 <sub>B</sub>
000065 <sub>H</sub>	UPCH	UPI control register (upper)	R/W	R/W		-000-000 <sub>B</sub>
000066 <sub>H</sub>	UPDI0/ UPDO0	UPI0 data input register/ data output register	R/W	R/W		XXXXXXXX <sub>B</sub>
000067 <sub>H</sub>	UPS0	UPI0 status register	R/W	R/W		00000000 <sub>B</sub>
000068 <sub>H</sub>	UPDI1/ UPDO1	UPI1 data input register/ data output register	R/W	R/W		XXXXXXXX <sub>B</sub>
000069 <sub>H</sub>	UPS1	UPI1 status register	R/W	R/W		00000000 <sub>B</sub>
00006A <sub>H</sub>	UPDI2/ UPDO2	UPI2 data input register/ data output register	R/W	R/W		XXXXXXXX <sub>B</sub>
00006B <sub>H</sub>	UPS2	UPI2 status register	R/W	R/W		00000000 <sub>B</sub>
00006C <sub>H</sub>	UPDI3/ UPDO3	UPI3 data input register/ data output register	R/W	R/W		XXXXXXXX <sub>B</sub>
00006D <sub>H</sub>	UPS3	UPI3 status register	R/W	R/W		00000000 <sub>B</sub>
00006E <sub>H</sub>	LCR	LPC control register	R/W	R/W	----000 <sub>B</sub>	
00006F <sub>H</sub>	ROMM	ROM mirroring function selection register	W	W	ROM mirroring function	-----1 <sub>B</sub>
000070 <sub>H</sub>	TMCSRL1	Timer control status register CH1 (lower)	R/W	R/W	16-bit reload timer (ch1)	00000000 <sub>B</sub>
000071 <sub>H</sub>	TMCSRH1	Timer control status register CH1 (upper)	R/W	R/W		----0000 <sub>B</sub>
000072 <sub>H</sub>	TMR1/ TMRD1	16-bit timer/reload register CH1	—	R/W		XXXXXXXX <sub>B</sub>
000073 <sub>H</sub>			—	R/W		XXXXXXXX <sub>B</sub>
000074 <sub>H</sub>	TMCSRL2	Timer control status register CH2 (lower)	R/W	R/W	16-bit reload timer (ch2)	00000000 <sub>B</sub>
000075 <sub>H</sub>	TMCSRH2	Timer control status register CH2 (upper)	R/W	R/W		----0000 <sub>B</sub>
000076 <sub>H</sub>	TMR2/ TMRD2	16-bit timer/reload register CH2	—	R/W		XXXXXXXX <sub>B</sub>
000077 <sub>H</sub>			—	R/W		XXXXXXXX <sub>B</sub>

(Continued)

# MB90378 Series

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
000078 <sub>H</sub>	TMCSRL3	Timer control status register CH3 (lower)	R/W	R/W	16-bit reload timer (ch3)	00000000 <sub>B</sub>
000079 <sub>H</sub>	TMCSRH3	Timer control status register CH3 (upper)	R/W	R/W		----0000 <sub>B</sub>
00007A <sub>H</sub>	TMR3/ TMRD3	16-bit timer/reload register CH3	—	R/W		XXXXXXXX <sub>B</sub>
00007B <sub>H</sub>			—	R/W		XXXXXXXX <sub>B</sub>
00007C <sub>H</sub>	TMCSRL4	Timer control status register CH4 (lower)	R/W	R/W	16-bit reload timer (ch4)	00000000 <sub>B</sub>
00007D <sub>H</sub>	TMCSRH4	Timer control status register CH4 (upper)	R/W	R/W		----0000 <sub>B</sub>
00007E <sub>H</sub>	TMR4/ TMRD4	16-bit timer/reload register CH4	—	R/W		XXXXXXXX <sub>B</sub>
00007F <sub>H</sub>			—	R/W		XXXXXXXX <sub>B</sub>
000080 <sub>H</sub>	IBCRL	I <sup>2</sup> C bus control register (lower)	R/W	R/W	I <sup>2</sup> C	----0000 <sub>B</sub>
000081 <sub>H</sub>	IBCRH	I <sup>2</sup> C bus control register (upper)	R/W	R/W		00000000 <sub>B</sub>
000082 <sub>H</sub>	IBSRL	I <sup>2</sup> C bus status register (lower)	R	R		00000000 <sub>B</sub>
000083 <sub>H</sub>	IBSRH	I <sup>2</sup> C bus status register (upper)	R/W	R/W		--000000 <sub>B</sub>
000084 <sub>H</sub>	IDAR	I <sup>2</sup> C data register	R/W	R/W		XXXXXXXX <sub>B</sub>
000085 <sub>H</sub>	IADR	I <sup>2</sup> C address register	R/W	R/W		-XXXXXXXX <sub>B</sub>
000086 <sub>H</sub>	ICCR	I <sup>2</sup> C clock control register	R/W	R/W		0-000000 <sub>B</sub>
000087 <sub>H</sub>	ITCR	I <sup>2</sup> C timeout control register	R/W	R/W		-0-00000 <sub>B</sub>
000088 <sub>H</sub>	ITOC	I <sup>2</sup> C timeout clock register	R/W	R/W		00000000 <sub>B</sub>
000089 <sub>H</sub>	ITOD	I <sup>2</sup> C timeout data register	R/W	R/W		00000000 <sub>B</sub>
00008A <sub>H</sub>	ISTO	I <sup>2</sup> C slave timeout register	R/W	R/W		00000000 <sub>B</sub>
00008B <sub>H</sub>	IMTO	I <sup>2</sup> C master timeout register	R/W	R/W		00000000 <sub>B</sub>
00008C <sub>H</sub>	RDR0	Port 0 pull-up resistor setting register	R/W	R/W		Port 0
00008D <sub>H</sub>	RDR1	Port 1 pull-up resistor setting register	R/W	R/W	Port 1	00000000 <sub>B</sub>
00008E <sub>H</sub>	RDR2	Port 2 pull-up resistor setting register	R/W	R/W	Port 2	00000000 <sub>B</sub>
00008F <sub>H</sub>	RDR3	Port 3 pull-up resistor setting register	R/W	R/W	Port 3	00000000 <sub>B</sub>
000090 <sub>H</sub> to 00009D <sub>H</sub>	Prohibited area					
00009E <sub>H</sub>	PACSR	Program address detect control status register	R/W	R/W	Address match detection	00000000 <sub>B</sub>
00009F <sub>H</sub>	DIRR	Delayed interrupt cause/clear register	R/W	R/W	Delayed interrupt	-----0 <sub>B</sub>

(Continued)

# MB90378 Series

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
0000A0 <sub>H</sub>	LPMCR	Low-power consumption mode register	R/W	R/W	Low-power consumption control register	00011000 <sub>B</sub>
0000A1 <sub>H</sub>	CKSCR	Clock selection register	R/W	R/W		11111100 <sub>B</sub>
0000A2 <sub>H</sub> , 0000A3 <sub>H</sub>	Prohibited area					
0000A4 <sub>H</sub>	CKMC	Clock modulation control register	R/W	R/W	Clock modulation	-----0 <sub>B</sub>
0000A5 <sub>H</sub> to 0000A7 <sub>H</sub>	Prohibited area					
0000A8 <sub>H</sub>	WDTC	Watchdog control register	R/W	R/W	Watchdog timer	X-XXX111 <sub>B</sub>
0000A9 <sub>H</sub>	TBTC	Timebase timer control register	R/W	R/W	Timebase timer	1--00100 <sub>B</sub>
0000AA <sub>H</sub>	WTC	Watch timer control register	R/W	R/W	Watch timer	10001000 <sub>B</sub>
0000AB <sub>H</sub>	Prohibited area					
0000AC <sub>H</sub>	EICR	Wake-up interrupt control register	R/W	R/W	Key-on wake-up interrupt	00000000 <sub>B</sub>
0000AD <sub>H</sub>	EIFR	Wake-up interrupt flag register	R/W	R/W		-----0 <sub>B</sub>
0000AE <sub>H</sub>	FMCS	Flash memory control status register	R/W	R/W	Flash memory interface circuit	000X0000 <sub>B</sub>
0000AF <sub>H</sub>	Prohibited area					
0000B0 <sub>H</sub>	ICR00	Interrupt control register 00	R/W	R/W	Interrupt controller	00000111 <sub>B</sub>
0000B1 <sub>H</sub>	ICR01	Interrupt control register 01	R/W	R/W		00000111 <sub>B</sub>
0000B2 <sub>H</sub>	ICR02	Interrupt control register 02	R/W	R/W		00000111 <sub>B</sub>
0000B3 <sub>H</sub>	ICR03	Interrupt control register 03	R/W	R/W		00000111 <sub>B</sub>
0000B4 <sub>H</sub>	ICR04	Interrupt control register 04	R/W	R/W		00000111 <sub>B</sub>
0000B5 <sub>H</sub>	ICR05	Interrupt control register 05	R/W	R/W		00000111 <sub>B</sub>
0000B6 <sub>H</sub>	ICR06	Interrupt control register 06	R/W	R/W		00000111 <sub>B</sub>
0000B7 <sub>H</sub>	ICR07	Interrupt control register 07	R/W	R/W		00000111 <sub>B</sub>
0000B8 <sub>H</sub>	ICR08	Interrupt control register 08	R/W	R/W		00000111 <sub>B</sub>
0000B9 <sub>H</sub>	ICR09	Interrupt control register 09	R/W	R/W		00000111 <sub>B</sub>
0000BA <sub>H</sub>	ICR10	Interrupt control register 10	R/W	R/W		00000111 <sub>B</sub>
0000BB <sub>H</sub>	ICR11	Interrupt control register 11	R/W	R/W		00000111 <sub>B</sub>
0000BC <sub>H</sub>	ICR12	Interrupt control register 12	R/W	R/W		00000111 <sub>B</sub>
0000BD <sub>H</sub>	ICR13	Interrupt control register 13	R/W	R/W		00000111 <sub>B</sub>
0000BE <sub>H</sub>	ICR14	Interrupt control register 14	R/W	R/W		00000111 <sub>B</sub>
0000BF <sub>H</sub>	ICR15	Interrupt control register 15	R/W	R/W		00000111 <sub>B</sub>

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Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
0000C0 <sub>H</sub>	MBCRL	MI <sup>2</sup> C bus control register (lower)	R/W	R/W	Multi-address I <sup>2</sup> C	----0000 <sub>B</sub>
0000C1 <sub>H</sub>	MBCRH	MI <sup>2</sup> C bus control register (upper)	R/W	R/W		00000000 <sub>B</sub>
0000C2 <sub>H</sub>	MBSRL	MI <sup>2</sup> C bus status register (lower)	R	R		00000000 <sub>B</sub>
0000C3 <sub>H</sub>	MBSRH	MI <sup>2</sup> C bus status register (upper)	R/W	R/W		--000000 <sub>B</sub>
0000C4 <sub>H</sub>	MDAR	MI <sup>2</sup> C data register	R/W	R/W		XXXXXXXX <sub>B</sub>
0000C5 <sub>H</sub>	MALR	MI <sup>2</sup> C alert register	R/W	R/W		----0000 <sub>B</sub>
0000C6 <sub>H</sub>	MADR1	MI <sup>2</sup> C address register 1	R/W	R/W		-XXXXXXXX <sub>B</sub>
0000C7 <sub>H</sub>	MADR2	MI <sup>2</sup> C address register 2	R/W	R/W		-XXXXXXXX <sub>B</sub>
0000C8 <sub>H</sub>	MADR3	MI <sup>2</sup> C address register 3	R/W	R/W		-XXXXXXXX <sub>B</sub>
0000C9 <sub>H</sub>	MADR4	MI <sup>2</sup> C address register 4	R/W	R/W		-XXXXXXXX <sub>B</sub>
0000CA <sub>H</sub>	MADR5	MI <sup>2</sup> C address register 5	R/W	R/W		-XXXXXXXX <sub>B</sub>
0000CB <sub>H</sub>	MADR6	MI <sup>2</sup> C address register 6	R/W	R/W		-XXXXXXXX <sub>B</sub>
0000CC <sub>H</sub>	MCCR	MI <sup>2</sup> C clock control register	R/W	R/W		0-000000 <sub>B</sub>
0000CD <sub>H</sub>	MTCR	MI <sup>2</sup> C timeout control register	R/W	R/W		-0-000000 <sub>B</sub>
0000CE <sub>H</sub>	MTOC	MI <sup>2</sup> C timeout clock register	R/W	R/W		00000000 <sub>B</sub>
0000CF <sub>H</sub>	MTOD	MI <sup>2</sup> C timeout data register	R/W	R/W		00000000 <sub>B</sub>
0000D0 <sub>H</sub>	MSTO	MI <sup>2</sup> C slave timeout register	R/W	R/W		00000000 <sub>B</sub>
0000D1 <sub>H</sub>	MMTO	MI <sup>2</sup> C master timeout register	R/W	R/W		00000000 <sub>B</sub>
0000D2 <sub>H</sub>	SMR2	Serial mode register 2	R/W	R/W	UART2	00000-00 <sub>B</sub>
0000D3 <sub>H</sub>	SCR2	Serial control register 2	R/W	R/W		00000100 <sub>B</sub>
0000D4 <sub>H</sub>	SIDR2/ SODR2	Input data register 2/ output data register 2	R/W	R/W		XXXXXXXX <sub>B</sub>
0000D5 <sub>H</sub>	SSR2	Status register 2	R/W	R/W		00001000 <sub>B</sub>
0000D6 <sub>H</sub>	M2CR2	Mode 2 control register 2	R/W	R/W		----1000 <sub>B</sub>
0000D7 <sub>H</sub>	CDCR2	Clock division control register 2	R/W	R/W	Communication prescaler 2	00--0000 <sub>B</sub>
0000D8 <sub>H</sub>	EENR1	Interrupt enable register	R/W	R/W	Extend External Interrupt 1	00000000 <sub>B</sub>
0000D9 <sub>H</sub>	EERR1	Interrupt cause register	R/W	R/W		XXXXXXXX <sub>B</sub>
0000DA <sub>H</sub> 0000DB <sub>H</sub>	EELR1	Request level setting register	R/W R/W	R/W R/W		00000000 <sub>B</sub> 00000000 <sub>B</sub>
0000DC <sub>H</sub>	EENR2	Interrupt enable register	R/W	R/W	Extend External Interrupt 2	00000000 <sub>B</sub>
0000DD <sub>H</sub>	EERR2	Interrupt cause register	R/W	R/W		XXXXXXXX <sub>B</sub>
0000DE <sub>H</sub> 0000DF <sub>H</sub>	EELR2	Request level setting register	R/W R/W	R/W R/W		00000000 <sub>B</sub> 00000000 <sub>B</sub>
0000E0 <sub>H</sub>	PDL3	Port 3 data latch register	R/W	R/W		Port 3 data latch

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Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
0000E1 <sub>H</sub>	BDR	Bit data register	R/W	R/W	Bit decoder	----XXXX <sub>B</sub>
0000E2 <sub>H</sub>	BRRL	Bit result register (lower)	R	R		XXXXXXXX <sub>B</sub>
0000E3 <sub>H</sub>	BRRH	Bit result register (upper)	R	R		XXXXXXXX <sub>B</sub>
0000E4 <sub>H</sub>	SMR3	Serial mode register 3	R/W	R/W	UART3	00000-00 <sub>B</sub>
0000E5 <sub>H</sub>	SCR3	Serial control register 3	R/W	R/W		00000100 <sub>B</sub>
0000E6 <sub>H</sub>	SIDR3 / SODR3	Input data register 3/ output data register 3	R/W	R/W		XXXXXXXX <sub>B</sub>
0000E7 <sub>H</sub>	SSR3	Status register 3	R/W	R/W		00001000 <sub>B</sub>
0000E8 <sub>H</sub>	M2CR3	Mode 2 control register 3	R/W	R/W		----1000 <sub>B</sub>
0000E9 <sub>H</sub>	CDCR3	Clock division control register 3	R/W	R/W	Communication prescaler 3	00--0000 <sub>B</sub>
0000EA <sub>H</sub>	TMCSRL5	Timer control status register CH5 (lower)	R/W	R/W	16-bit reload timer (ch5)	00000000 <sub>B</sub>
0000EB <sub>H</sub>	TMCSRH5	Timer control status register CH5 (upper)	R/W	R/W		----0000 <sub>B</sub>
0000EC <sub>H</sub>	TMR5/ TMRD5	16-bit timer/reload register CH5	—	R/W		XXXXXXXX <sub>B</sub>
0000ED <sub>H</sub>			—	R/W		XXXXXXXX <sub>B</sub>
0000EE <sub>H</sub>	LCRL	LCD control register 0	R/W	R/W	LCD controller/driver	00010000 <sub>B</sub>
0000EF <sub>H</sub>	LCRH	LCD control register 1	R/W	R/W		00000000 <sub>B</sub>
0000F0 <sub>H</sub> to 0000F4 <sub>H</sub>	VRAM	LCD display RAM	R/W	-		XXXXXXXX <sub>B</sub>
0000F5 <sub>H</sub> to 0000F7 <sub>H</sub>	Prohibited area					
0000F8 <sub>H</sub> to 0000FF <sub>H</sub>	External area					
000100 <sub>H</sub> to 0018FF <sub>H</sub>	Prohibited area (RAM area)					
001FF0 <sub>H</sub>	PADR0	Program address detection register 0	R/W	R/W	Address match detection	XXXXXXXX <sub>B</sub>
001FF1 <sub>H</sub>		Program address detection register 1	R/W	R/W		XXXXXXXX <sub>B</sub>
001FF2 <sub>H</sub>		Program address detection register 2	R/W	R/W		XXXXXXXX <sub>B</sub>

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Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
001FF3 <sub>H</sub>	PADR1	Program address detection register 3	R/W	R/W	Address match detection	XXXXXXXX <sub>B</sub>
001FF4 <sub>H</sub>		Program address detection register 4	R/W	R/W		XXXXXXXX <sub>B</sub>
001FF5 <sub>H</sub>		Program address detection register 5	R/W	R/W		XXXXXXXX <sub>B</sub>
001FF6 <sub>H</sub> to 003F7F <sub>H</sub>	Prohibited area					
003F80 <sub>H</sub>	UDRL10	UP data register 10 (lower)	R/W	R/W	LPC data buffer array-Extend	XXXXXXXX <sub>B</sub>
003F81 <sub>H</sub>	UDRH10	UP data register 10 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F82 <sub>H</sub>	UDRL11	UP data register 11 (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F83 <sub>H</sub>	UDRH11	UP data register 11 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F84 <sub>H</sub>	UDRL12	UP data register 12 (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F85 <sub>H</sub>	UDRH12	UP data register 12 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F86 <sub>H</sub>	UDRL13	UP data register 13 (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F87 <sub>H</sub>	UDRH13	UP data register 13 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F88 <sub>H</sub>	UDRL14	UP data register 14 (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F89 <sub>H</sub>	UDRH14	UP data register 14 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F8A <sub>H</sub>	UDRL15	UP data register 15 (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F8B <sub>H</sub>	UDRH15	UP data register 15 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F8C <sub>H</sub>	UDRL16	UP data register 16 (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F8D <sub>H</sub>	UDRH16	UP data register 16 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F8E <sub>H</sub>	UDRL17	UP data register 17 (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F8F <sub>H</sub>	UDRH17	UP data register 17 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F90 <sub>H</sub>	UDRL18	UP data register 18 (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F91 <sub>H</sub>	UDRH18	UP data register 18 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F92 <sub>H</sub>	UDRL19	UP data register 19 (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F93 <sub>H</sub>	UDRH19	UP data register 19 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F94 <sub>H</sub>	UDRL1A	UP data register 1A (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F95 <sub>H</sub>	UDRH1A	UP data register 1A (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F96 <sub>H</sub>	UDRL1B	UP data register 1B (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F97 <sub>H</sub>	UDRH1B	UP data register 1B (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F98 <sub>H</sub>	UDRL1C	UP data register 1C (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F99 <sub>H</sub>	UDRH1C	UP data register 1C (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F9A <sub>H</sub>	UDRL1D	UP data register 1D (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F9B <sub>H</sub>	UDRH1D	UP data register 1D (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>

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Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
003F9C <sub>H</sub>	UDRL1E	UP data register 1E (lower)	R/W	R/W	LPC data buffer array-Extend	XXXXXXXX <sub>B</sub>
003F9D <sub>H</sub>	UDRH1E	UP data register 1E (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F9E <sub>H</sub>	UDRL1F	UP data register 1F (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003F9F <sub>H</sub>	UDRH1F	UP data register 1F (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FA0 <sub>H</sub>	DBACLR	Data buffer array clear register	R/W	R/W	LPC data buffer array	----000 <sub>B</sub>
003FA1 <sub>H</sub>	Prohibited area					
003FA2 <sub>H</sub>	FWR0	FLASH programming control register 0	R/W	R/W	Dual operating FLASH	00000000 <sub>B</sub>
003FA3 <sub>H</sub>	FWR1	FLASH programming control register 1	R/W	R/W		00000000 <sub>B</sub>
003FA4 <sub>H</sub>	SSR0	Sector switching register	R/W	R/W		00XXXXX0 <sub>B</sub>
003FA5 <sub>H</sub> to 003FAE <sub>H</sub>	Prohibited area					
003FAF <sub>H</sub>	PCKCR	PLL clock control register	W	W	PLL	XXXX0000 <sub>B</sub>
003FB0 <sub>H</sub>	PRL2	PPG reload register (lower)	R/W	R/W	8/16-bit PPG timer 2	XXXXXXXX <sub>B</sub>
003FB1 <sub>H</sub>	PRLH2	PPG reload register (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FB2 <sub>H</sub>	PRL3	PPG reload register (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FB3 <sub>H</sub>	PRLH3	PPG reload register (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FB4 <sub>H</sub>	PPGC2	PPG control register ch2	R/W	R/W		00000001 <sub>B</sub>
003FB5 <sub>H</sub>	PPGC3	PPG control register ch3	R/W	R/W		00000001 <sub>B</sub>
003FB6 <sub>H</sub>	PCS23	PPG clock control register	R/W	R/W		000000XX <sub>B</sub>
003FB7 <sub>H</sub> to 003FBF <sub>H</sub>	Prohibited area					
003FC0 <sub>H</sub>	UDRL0	UP data register 0 (lower)	R/W	R/W	LPC data buffer array	XXXXXXXX <sub>B</sub>
003FC1 <sub>H</sub>	UDRH0	UP data register 0 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FC2 <sub>H</sub>	UDRL1	UP data register 1 (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FC3 <sub>H</sub>	UDRH1	UP data register 1 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FC4 <sub>H</sub>	UDRL2	UP data register 2 (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FC5 <sub>H</sub>	UDRH2	UP data register 2 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FC6 <sub>H</sub>	UDRL3	UP data register 3 (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FC7 <sub>H</sub>	UDRH3	UP data register 3 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FC8 <sub>H</sub>	UDRL4	UP data register 4 (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FC9 <sub>H</sub>	UDRH4	UP data register 4 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>

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Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
003FCA <sub>H</sub>	UDRL5	UP data register 5 (lower)	R/W	R/W	LPC data buffer array	XXXXXXXX <sub>B</sub>
003FCB <sub>H</sub>	UDRH5	UP data register 5 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FCC <sub>H</sub>	UDRL6	UP data register 6 (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FCD <sub>H</sub>	UDRH6	UP data register 6 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FCE <sub>H</sub>	UDRL7	UP data register 7 (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FCF <sub>H</sub>	UDRH7	UP data register 7 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FD0 <sub>H</sub>	UDRL8	UP data register 8 (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FD1 <sub>H</sub>	UDRH8	UP data register 8 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FD2 <sub>H</sub>	UDRL9	UP data register 9 (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FD3 <sub>H</sub>	UDRH9	UP data register 9 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FD4 <sub>H</sub>	UDRLA	UP data register A (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FD5 <sub>H</sub>	UDRHA	UP data register A (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FD6 <sub>H</sub>	UDRLB	UP data register B (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FD7 <sub>H</sub>	UDRHB	UP data register B (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FD8 <sub>H</sub>	UDRLC	UP data register C (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FD9 <sub>H</sub>	UDRHC	UP data register C (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FDA <sub>H</sub>	UDRLD	UP data register D (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FDB <sub>H</sub>	UDRHD	UP data register D (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FDC <sub>H</sub>	UDRLE	UP data register E (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FDD <sub>H</sub>	UDRHE	UP data register E (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FDE <sub>H</sub>	UDRLF	UP data register F (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FDF <sub>H</sub>	UDRHF	UP data register F (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FE0 <sub>H</sub>	DNDL0	DOWN data register 0 (lower)	R	R		XXXXXXXX <sub>B</sub>
003FE1 <sub>H</sub>	DNDH0	DOWN data register 0 (upper)	R	R		XXXXXXXX <sub>B</sub>
003FE2 <sub>H</sub>	DNDL1	DOWN data register 1 (lower)	R	R		XXXXXXXX <sub>B</sub>
003FE3 <sub>H</sub>	DNDH1	DOWN data register 1 (upper)	R	R		XXXXXXXX <sub>B</sub>
003FE4 <sub>H</sub>	DNDL2	DOWN data register 2 (lower)	R	R		XXXXXXXX <sub>B</sub>
003FE5 <sub>H</sub>	DNDH2	DOWN data register 2 (upper)	R	R		XXXXXXXX <sub>B</sub>
003FE6 <sub>H</sub>	DNDL3	DOWN data register 3 (lower)	R	R		XXXXXXXX <sub>B</sub>
003FE7 <sub>H</sub>	DNDH3	DOWN data register 3 (upper)	R	R		XXXXXXXX <sub>B</sub>
003FE8 <sub>H</sub>	DNDL4	DOWN data register 4 (lower)	R	R		XXXXXXXX <sub>B</sub>
003FE9 <sub>H</sub>	DNDH4	DOWN data register 4 (upper)	R	R		XXXXXXXX <sub>B</sub>
003FEA <sub>H</sub>	DNDL5	DOWN data register 5 (lower)	R	R	XXXXXXXX <sub>B</sub>	
003FEB <sub>H</sub>	DNDH5	DOWN data register 5 (upper)	R	R	XXXXXXXX <sub>B</sub>	
003FEC <sub>H</sub>	DNDL6	DOWN data register 6 (lower)	R	R	XXXXXXXX <sub>B</sub>	
003FED <sub>H</sub>	DNDH6	DOWN data register 6 (upper)	R	R	XXXXXXXX <sub>B</sub>	

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Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
003FEE <sub>H</sub>	DNDL7	DOWN data register 7 (lower)	R	R	LPC data buffer array	XXXXXXXX <sub>B</sub>
003FEF <sub>H</sub>	DNDH7	DOWN data register 7 (upper)	R	R		XXXXXXXX <sub>B</sub>
003FF0 <sub>H</sub>	DBAAL	Data buffer array address register (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FF1 <sub>H</sub>	DBAAH	Data buffer array address register (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FF2 <sub>H</sub> , 003FF3 <sub>H</sub>	Prohibited area					
003FF4 <sub>H</sub>	TMCSRL6	Timer control status register CH6 (lower)	R/W	R/W	16-bit reload timer (ch6)	0000000 <sub>B</sub>
003FF5 <sub>H</sub>	TMCSRH6	Timer control status register CH6 (upper)	R/W	R/W		----0000 <sub>B</sub>
003FF6 <sub>H</sub>	TMR6/ TMRD6	16-bit timer/reload register CH6	—	R/W		XXXXXXXX <sub>B</sub>
003FF7 <sub>H</sub>			—	R/W		XXXXXXXX <sub>B</sub>
003FF8 <sub>H</sub>	PRLLO	PPG reload register (lower)	R/W	R/W	8/16-bit PPG timer 1	XXXXXXXX <sub>B</sub>
003FF9 <sub>H</sub>	PRLHO	PPG reload register (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FFA <sub>H</sub>	PRLLO	PPG reload register (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FFB <sub>H</sub>	PRLHO	PPG reload register (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FFC <sub>H</sub>	PPGC0	PPG control register ch0	R/W	R/W		0000001 <sub>B</sub>
003FFD <sub>H</sub>	PPGC1	PPG control register ch1	R/W	R/W		0000001 <sub>B</sub>
003FFE <sub>H</sub>	PCS01	PPG clock control register	R/W	R/W		000000X <sub>B</sub>
003FFF <sub>H</sub>	Prohibited area					

- Meaning of abbreviations used for reading and writing
  - R/W : Readable and writable
  - R : Read-only
  - W : Write-only
- Explanation of initial values
  - 0 : The bit is initialized to 0.
  - 1 : The bit is initialized to 1.
  - X : The initial value of the bit is undefined.
  - : The bit is not used. Its initial value is undefined.
- Instruction using IO addressing e.g. MOV A, io, is not supported for registers area 003F80<sub>H</sub> to 003FFF<sub>H</sub>.

# MB90378 Series

## ■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt cause	EI <sup>2</sup> OS support	Interrupt vector		Interrupt control register		Priority*2	
		Number	Address	ICR	Address		
Reset	×	#08	08 <sub>H</sub>	FFFFDC <sub>H</sub>	—	<div style="display: flex; align-items: center; justify-content: center;"> <span style="font-size: 2em;">↑</span> <div style="margin: 0 10px;">High</div> <span style="font-size: 2em;">↓</span> </div> <div style="margin-top: 10px; text-align: center;">Low</div>	
INT9 instruction	×	#09	09 <sub>H</sub>	FFFFD8 <sub>H</sub>	—		
Exception processing	×	#10	0A <sub>H</sub>	FFFFD4 <sub>H</sub>	—		
A/D converter conversion termination	○	#11	0B <sub>H</sub>	FFFFD0 <sub>H</sub>	ICR00		0000B0 <sub>H</sub> *1
Timebase timer	△	#12	0C <sub>H</sub>	FFFFCC <sub>H</sub>	ICR01		0000B1 <sub>H</sub> *1
UPI0 IBF/LPC reset	△	#13	0D <sub>H</sub>	FFFFC8 <sub>H</sub>			
UPI1 IBF	△	#14	0E <sub>H</sub>	FFFFC4 <sub>H</sub>			
UPI2 IBF	△	#15	0F <sub>H</sub>	FFFFC0 <sub>H</sub>	ICR02		0000B2 <sub>H</sub> *1
UPI3 IBF	△	#16	10 <sub>H</sub>	FFFFBC <sub>H</sub>			
DTP/ext. interrupt channels 0/1 detection	○	#17	11 <sub>H</sub>	FFFFB8 <sub>H</sub>	ICR03		0000B3 <sub>H</sub> *1
DTP/ext. interrupt channels 2/3 detection	○	#18	12 <sub>H</sub>	FFFFB4 <sub>H</sub>			
DTP/ext. interrupt channels 4/5 detection	○	#19	13 <sub>H</sub>	FFFFB0 <sub>H</sub>			
Key-on wake-up interrupt detection	△	#20	14 <sub>H</sub>	FFFFAC <sub>H</sub>	ICR04		0000B4 <sub>H</sub> *1
UPI0/1/2/3 OBE	△	#21	15 <sub>H</sub>	FFFFA8 <sub>H</sub>			
16-bit PPG timer 1 / 8/16-bit PPG timer 0/1	△	#22	16 <sub>H</sub>	FFFFA4 <sub>H</sub>	ICR05		0000B5 <sub>H</sub> *2
PS/2 interface 0/1	△	#23	17 <sub>H</sub>	FFFFA0 <sub>H</sub>			
PS/2 interface 2	△	#24	18 <sub>H</sub>	FFFF9C <sub>H</sub>	ICR06		0000B6 <sub>H</sub> *1
Watch timer	△	#25	19 <sub>H</sub>	FFFF98 <sub>H</sub>			
I <sup>2</sup> C transfer complete / bus error	△	#26	1A <sub>H</sub>	FFFF94 <sub>H</sub>	ICR07		0000B7 <sub>H</sub> *1
16-bit PPG timer 2/3	○	#27	1B <sub>H</sub>	FFFF90 <sub>H</sub>			
DTP/ext. interrupt channels 6/7 detection	○	#28	1C <sub>H</sub>	FFFF8C <sub>H</sub>			
Multi-address I <sup>2</sup> C transfer complete / bus error	△	#29	1D <sub>H</sub>	FFFF88 <sub>H</sub>	ICR09		0000B9 <sub>H</sub> *1
Extend External Interrupt 00 to 07/08 to 15	○	#30	1E <sub>H</sub>	FFFF84 <sub>H</sub>			
I <sup>2</sup> C timeout / standby wake-up	△	#31	1F <sub>H</sub>	FFFF80 <sub>H</sub>	ICR10		0000BA <sub>H</sub> *1
16-bit reload timer 1/2/5 underflow	○	#32	20 <sub>H</sub>	FFFF7C <sub>H</sub>			
Multi-address I <sup>2</sup> C timeout / standby wake-up	△	#33	21 <sub>H</sub>	FFFF78 <sub>H</sub>	ICR11		0000BB <sub>H</sub> *1
16-bit reload timer 3/4/6 underflow	○	#34	22 <sub>H</sub>	FFFF74 <sub>H</sub>			
UART1 receive	◎	#35	23 <sub>H</sub>	FFFF70 <sub>H</sub>	ICR12		0000BC <sub>H</sub> *1
UART1 send	△	#36	24 <sub>H</sub>	FFFF6C <sub>H</sub>			
UART2 receive	◎	#37	25 <sub>H</sub>	FFFF68 <sub>H</sub>	ICR13		0000BD <sub>H</sub> *1
UART2 send	△	#38	26 <sub>H</sub>	FFFF64 <sub>H</sub>			
UART3 receive	◎	#39	27 <sub>H</sub>	FFFF60 <sub>H</sub>	ICR14		0000BE <sub>H</sub> *1
UART3 send	△	#40	28 <sub>H</sub>	FFFF5C <sub>H</sub>			
Flash memory status	△	#41	29 <sub>H</sub>	FFFF58 <sub>H</sub>	ICR15		0000BF <sub>H</sub> *1
Delayed interrupt generator module	△	#42	2A <sub>H</sub>	FFFF54 <sub>H</sub>			

(Continued)

(Continued)

- : Can be used and interrupt request flag is cleared by EI<sup>2</sup>OS interrupt clear signal.
- × : Cannot be used.
- ◎ : Can be used and support the EI<sup>2</sup>OS stop request.
- △ : Can be used.

\*1 : • For peripheral functions that share the ICR register, the interrupt level will be the same.  
• If the extended intelligent I/O service is to be used with a peripheral function that shares the ICR register with another peripheral function, the service can be started by either of the function. And if EI<sup>2</sup>OS clear is supported, both interrupt request flags for the two interrupt causes are cleared by EI<sup>2</sup>OS interrupt clear signal. It is recommended to mask either of the interrupt request during the use of EI<sup>2</sup>OS.  
• EI<sup>2</sup>OS service cannot be started multiple times simultaneously. Interrupt other than the operating interrupt is masked during EI<sup>2</sup>OS operation. It is recommended to mask either of the interrupt requests during the use of EI<sup>2</sup>OS.

\*2 : This priority is applied when interrupts of the same level occur simultaneously.

# MB90378 Series

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Rating

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V <sub>CC</sub>	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 4.0	V	
	AV <sub>CC</sub>	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 4.0	V	V <sub>CC</sub> ≥ AV <sub>CC</sub> *2
A/D converter reference input voltage*1	AVR	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 4.0	V	AV <sub>CC</sub> ≥ AVR, AVR ≥ AV <sub>SS</sub>
LCD power supply voltage*1	V1 to V3	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 4.0	V	V1 to V3 must not exceed V <sub>CC</sub>
Input voltage*1	V <sub>I1</sub>	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 4.0	V	All pins except P40 to P45, P80 to P82, P90 to P95 *3
	V <sub>I2</sub>	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 6.0	V	P40 to P45, P80 to P82, P90 to P95
Output voltage*1	V <sub>O</sub>	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 4.0	V	*3
Maximum clamp current	I <sub>CLAMP</sub>	- 2.0	+ 2.0	mA	*5
Total maximum clamp current	Σ I <sub>CLAMP</sub>	—	20	mA	*5
“L” level maximum output current	I <sub>OL1</sub>	—	10	mA	All pins except PF0 to PF7 *4
	I <sub>OL2</sub>	—	20	mA	PF0 to PF7 *4
“L” level average output current	I <sub>OLAV1</sub>	—	4	mA	All pins except PF0 to PF7 Average output current = operating current × operating efficiency
	I <sub>OLAV2</sub>	—	12	mA	PF0 to PF7 Average output current = operating current × operating efficiency
“L” level total maximum output current	ΣI <sub>OL</sub>	—	100	mA	
“L” level total average output current	ΣI <sub>OLAV</sub>	—	50	mA	Average output current = operating current × operating efficiency
“H” level maximum output current	I <sub>OH</sub>	—	- 10	mA	*4
“H” level average output current	I <sub>OHAV</sub>	—	- 3	mA	Average output current = operating current × operating efficiency
“H” level total maximum output current	ΣI <sub>OH</sub>	—	- 100	mA	
“H” level total average output current	ΣI <sub>OHAV</sub>	—	- 50	mA	Average output current = operating current × operating efficiency
Power consumption	P <sub>D</sub>	—	200	mW	
Operating temperature	T <sub>A</sub>	- 40	+ 85	°C	
Storage temperature	T <sub>stg</sub>	- 55	+ 150	°C	

(Continued)

# MB90378 Series

(Continued)

\*1 : This parameter is based on  $V_{SS} = AV_{SS} = 0.0$  V.

\*2 : Set  $AV_{CC}$  and  $V_{CC}$  at the same voltage. Take care so that AVR does not exceed  $V_{CC} + 0.3$  V when the power is turned on.

\*3 :  $V_I$  and  $V_O$  shall never exceed  $V_{CC} + 0.3$  V.

\*4 : The maximum output current is a peak value for a corresponding pin.

\*5 :

- Use within recommended operating conditions.

- Use at DC voltage (current).

- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.

- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.

- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the  $V_{CC}$  pin, and this may affect other devices.

- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.

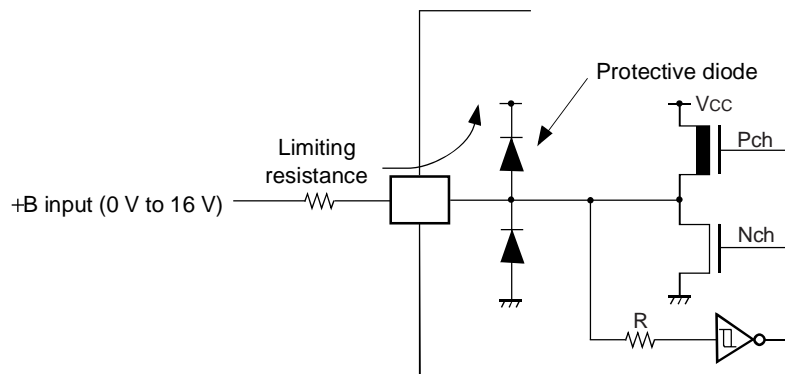
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.

- Care must be taken not to leave the +B input pin open.

- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, etc.) cannot accept +B signal input.

- Sample recommended circuits :

• Input/output equivalent circuits



**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

# MB90378 Series

## 2. Recommended Operating Conditions

( $V_{SS} = AV_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage *2	$V_{CC}$	2.7 *1	3.6	V	Normal operation assurance range
	$V_{CC}$	1.8	3.6	V	Retains the RAM state in stop mode
A/D converter reference input voltage *3	AVR	0	$AV_{CC}$	V	Normal operation assurance range
LCD power supply voltage	V1 to V3	$V_{SS}$	$V_{CC}$	V	V1 to V3 pins (The optimum value is dependent on the LCD element in use.)
Operating temperature	$T_A$	- 40	+ 85	°C	

\*1 : The operating voltage varies with the operation frequency.

\*2 : Set  $AV_{CC}$  and  $V_{CC}$  at the same voltage.

\*3 : Take care so that AVR does not exceed  $V_{CC} + 0.3\text{ V}$  when power is turned on.

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

# MB90378 Series

## 3. DC Characteristics

( $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $AV_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
“H” level input voltage	$V_{IH}$	P10 to P17, P20 to P27, P30 to P37, P46, P47, P51 to P57, PC0 to PC7, PD0 to PD7	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	CMOS input pins
	$V_{IHS}$	P00 to P07, P60 to P67, P70 to P77, P83 to P86, PA0 to PA7, PB0 to PB7, PE0 to PE7, PF0 to PF7, $\overline{RST}$		$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	CMOS hysteresis input pins
	$V_{IHSS}$	P40 to P45		$0.8 V_{CC}$	—	$V_{SS} + 5.5$	V	5 V tolerant CMOS hysteresis input pins
	$V_{IH5}$	P50, P82		$0.7 V_{CC}$	—	$V_{SS} + 5.5$	V	5 V tolerant CMOS input pins
	$V_{IHSM}$	P80, P81, P90 to P95		2.1	—	$V_{SS} + 5.5$	V	SMBus input pins
	$V_{IHM}$	MD0 to MD2		$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	Mode pins
“L” level input voltage	$V_{IL}$	P10 to P17, P20 to P27, P30 to P37, P46, P47, P50 to P57, P82, PC0 to PC7, PD0 to PD7	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	CMOS input pins
	$V_{ILS}$	P00 to P07, P40 to P45, P60 to P67, P70 to P77, P83 to P86, PA0 to PA7, PB0 to PB7, PE0 to PE7, PF0 to PF7, $\overline{RST}$		$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	CMOS hysteresis input pins
	$V_{ILSM}$	P80, P81, P90 to P95		$V_{SS} - 0.3$	—	0.8	V	SMBus input pins
	$V_{ILM}$	MD0 to MD2		$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	Mode pins
Open-drain output pin application voltage	$V_{D5}$	P40 to P45, P50, P80 to P82, P90 to P95	—	$V_{SS} - 0.3$	—	$V_{SS} + 5.5$	V	
	$V_D$	P46, PF0 to PF7		$V_{SS} - 0.3$	—	$V_{CC} + 0.3$	V	
“H” level output voltage	$V_{OH1}$	All port pins except P40 to P46, P50, P80 to P82, P90 to P95, PF0 to PF7	$V_{CC} = 3.0\text{ V}$ $I_{OH1} = -4.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
“L” level output voltage	$V_{OL1}$	All port pins except PF0 to PF7	$I_{OL1} = 4.0\text{ mA}$	—	—	0.4	V	
	$V_{OL2}$	PF0 to PF7	$I_{OL2} = 12.0\text{ mA}$	—	—	0.4	V	

(Continued)

# MB90378 Series

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leakage current (Hi-Z output leakage current)	$I_{IL}$	All input pins	$V_{CC} = 3.3\text{ V}$ , $V_{SS} < V_I < V_{CC}$	-5	—	5	$\mu\text{A}$	
Open-drain output leakage current	$I_{LEAK}$	P40 to P46, P50, P80 to P82, P90 to P95, PF0 to PF7	—	—	—	5	$\mu\text{A}$	
Power supply current*	$I_{CC}$	$V_{CC}$	$V_{CC} = 3.3\text{ V}$ , Internal operation at 20 MHz	—	56	68	$\text{mA}$	
	$I_{CCS}$		$V_{CC} = 3.3\text{ V}$ , Internal operation at 20 MHz, In sleep mode	—	23	30	$\text{mA}$	
	$I_{CCL}$		$V_{CC} = 3.3\text{ V}$ , External 32 kHz, Internal operation at 8 kHz, In sub-clock mode, $T_A = +25\text{ }^\circ\text{C}$	—	23	80	$\mu\text{A}$	
	$I_{CCLS}$		$V_{CC} = 3.3\text{ V}$ , External 32 kHz, Internal operation at 8 kHz, In sub-clock sleep mode, $T_A = +25\text{ }^\circ\text{C}$	—	10	50	$\mu\text{A}$	
	$I_{CCWAT}$		$V_{CC} = 3.3\text{ V}$ , External 32 kHz, Internal operation at 8 kHz, In watch mode, $T_A = +25\text{ }^\circ\text{C}$	—	1.5	30	$\mu\text{A}$	
Power supply current*	$I_{CCT}$	$V_{CC}$	$V_{CC} = 3.3\text{ V}$ , Internal operation at 20 MHz, In timebase timer mode	—	2.0	3	$\text{mA}$	
	$I_{CCH}$		$V_{CC} = 3.3\text{ V}$ , In stop mode, $T_A = +25\text{ }^\circ\text{C}$	—	1	20	$\mu\text{A}$	
Input capacitance	$C_{IN}$	All input pins except $V_{CC}$ , $AV_{CC}$ , $V_{SS}$ , $AV_{SS}$	—	—	10	80	$\text{pF}$	

(Continued)



# MB90378 Series

(Continued)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
LCD divided resistance	R <sub>LCD</sub>	—	Between V <sub>CC</sub> and V3 at V <sub>CC</sub> = 3.3 V	100	200	400	kΩ	
			Between V3 and V2 Between V2 and V1 Between V1 and V <sub>SS</sub> at V <sub>CC</sub> = 3.3 V	50	100	200		
COM0 to COM3 output impedance	R <sub>VCOM</sub>	COM0 to COM3	V1 to V3 = 3.3 V	—	—	5	kΩ	
SEG0 to SEG8 output impedance	R <sub>VSEG</sub>	SEG0 to SEG8		—	—	5	kΩ	
LCD leakage current	L <sub>LCDL</sub>	V1 to V3, COM0 to COM3, SEG0 to SEG8	—	—	±1	μA		
Pull-up resistance	R <sub>UP</sub>	P00 to P07,P10 to P17, P20 to P27,P30 to P37, RST	—	25	50	100	kΩ	
Pull-down resistance	R <sub>DOWN</sub>	MD2	—	25	50	100	kΩ	MB90V378 only

\* : The current value is preliminary value and may be subject to change for enhanced characteristics without previous notice. The power supply current is measured with an external clock.

# MB90378 Series

## 4. AC Characteristics

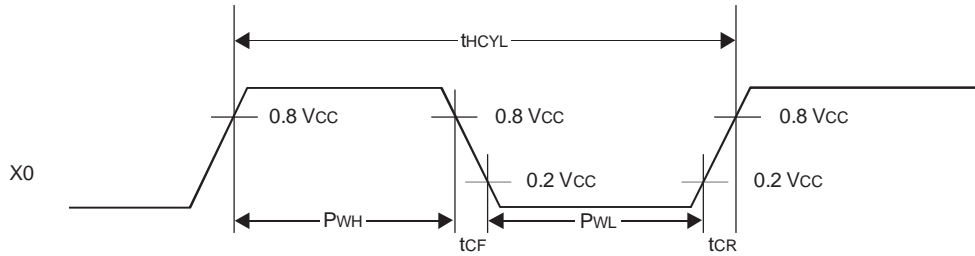
### (1) Clock Timings

( $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $AV_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

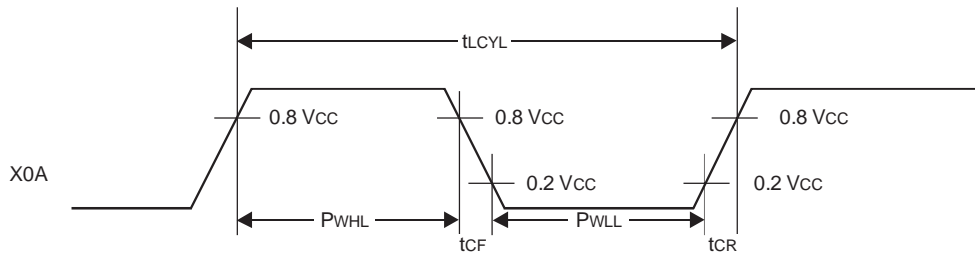
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	$f_{CH}$	X0, X1	—	3	—	16	MHz	$\times 1/2$ (When PLL stops) When using an oscillation circuit
				4	—	16	MHz	PLL $\times 1$ When using an oscillation circuit
				4	—	10	MHz	PLL $\times 2$ When using an oscillation circuit
				4	—	6.67	MHz	PLL $\times 3$ When using an oscillation circuit
				4	—	5	MHz	PLL $\times 4$ When using an oscillation circuit
				3	—	32	MHz	$\times 1/2$ (When PLL stops) When using an external clock
				4	—	20	MHz	PLL $\times 1$ When using an external clock
				4	—	10	MHz	PLL $\times 2$ When using an external clock
				4	—	6.67	MHz	PLL $\times 3$ When using an external clock
				4	—	5	MHz	PLL $\times 4$ When using an external clock
	$f_{CL}$	X0A, X1A	—	—	32.768	—	kHz	
Clock cycle time	$t_{HCYL}$	X0, X1	—	31.25	—	333	ns	
	$t_{LCYL}$	X0A, X1A	—	—	30.5	—	$\mu\text{s}$	
Frequency fluctuation rate locked*	$\Delta f$	—	—	—	—	5	%	
Input clock pulse width	$P_{WH}$ $P_{WL}$	X0	—	5	—	—	ns	Recommend duty ratio of 30% to 70%
	$P_{WHL}$ $P_{WLL}$	X0A	—	—	15.2	—	$\mu\text{s}$	Recommend duty ratio of 30% to 70%
Input clock rise/fall time	$t_{CR}$ $t_{CF}$	X0	—	—	—	5	ns	External clock operation
Internal operating clock frequency	$f_{CP}$	—	—	1.5	—	20	MHz	Main clock operation
	$f_{LCP}$	—	—	—	8.192	—	kHz	Sub-clock operation
Internal operating clock cycle time	$t_{CP}$	—	—	50	—	666	ns	Main clock operation
	$t_{LCP}$	—	—	—	122.1	—	$\mu\text{s}$	Sub-clock operation

# MB90378 Series

- X0, X1 clock timing



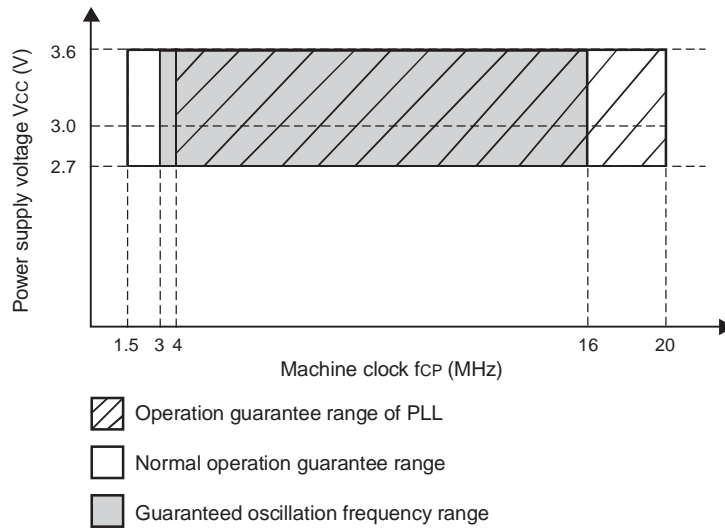
- X0A, X1A clock timing



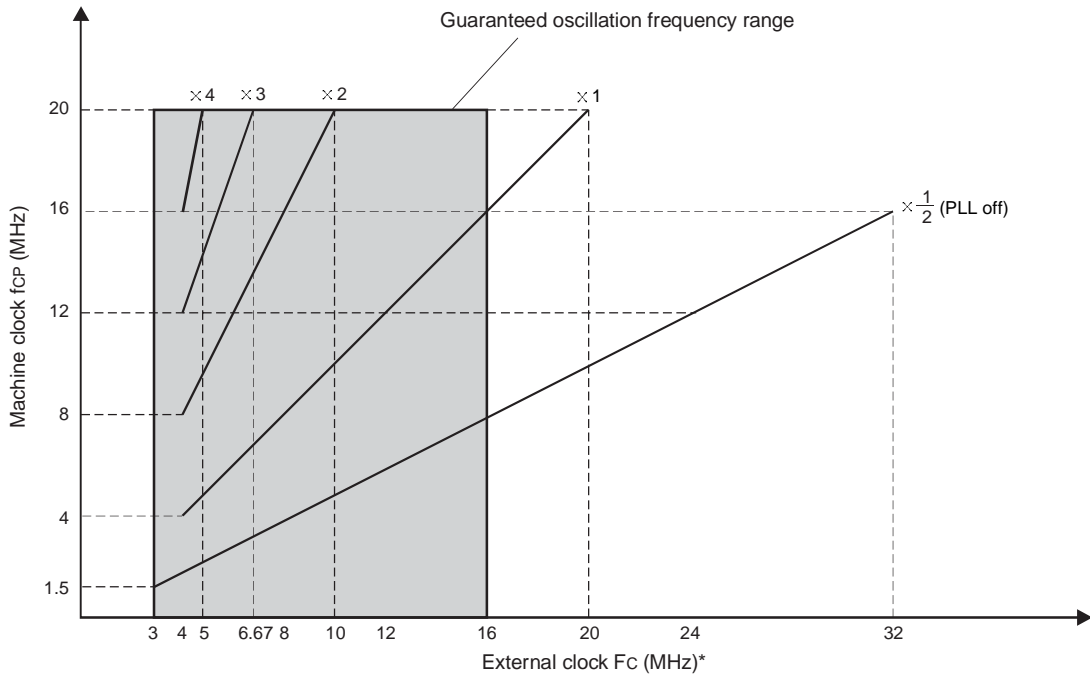
# MB90378 Series

• PLL operation guarantee range

Relationship between machine clock frequency and power supply voltage



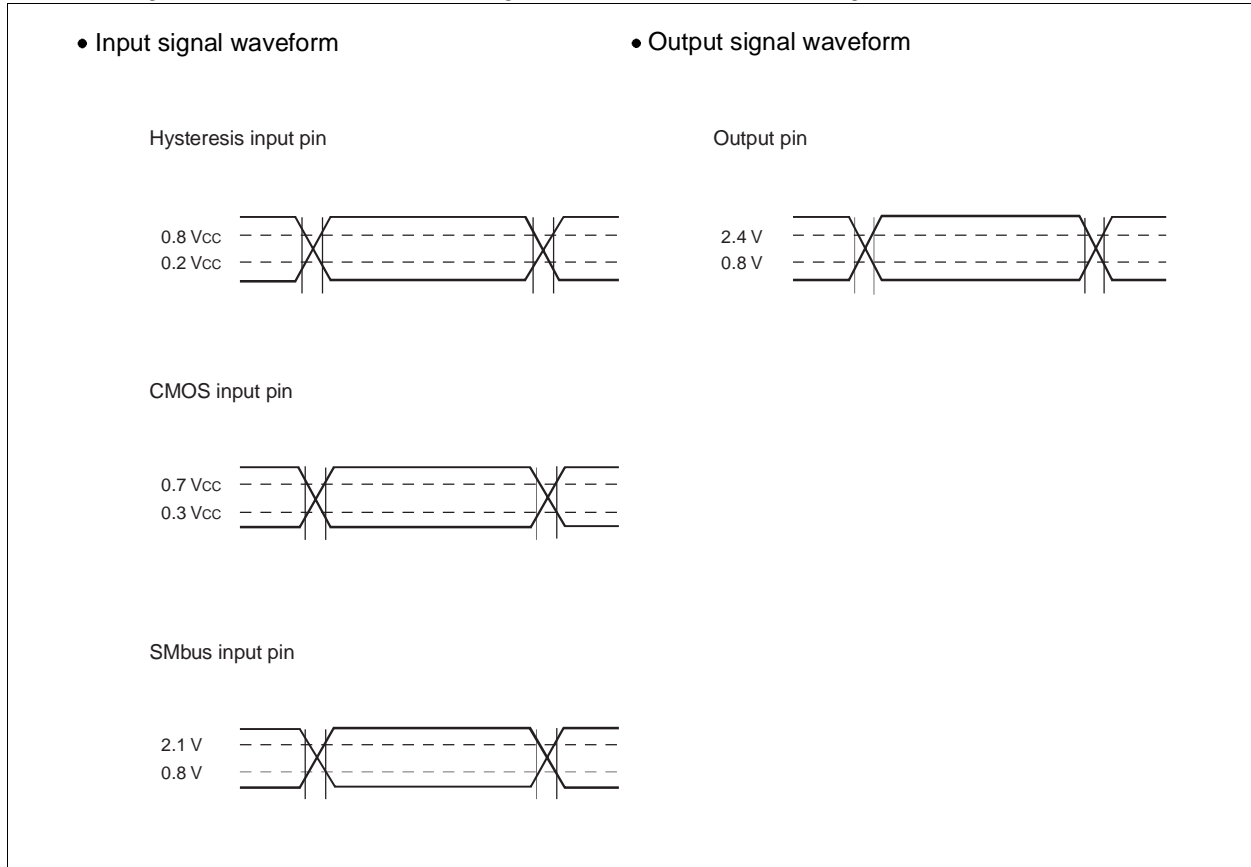
Relationship between external clock frequency and machine clock frequency



\* : When using a crystal oscillator or a ceramic oscillator, the maximum oscillation clock frequency is 16 MHz.

# MB90378 Series

The AC ratings are measured for the following measurement reference voltages :



# MB90378 Series

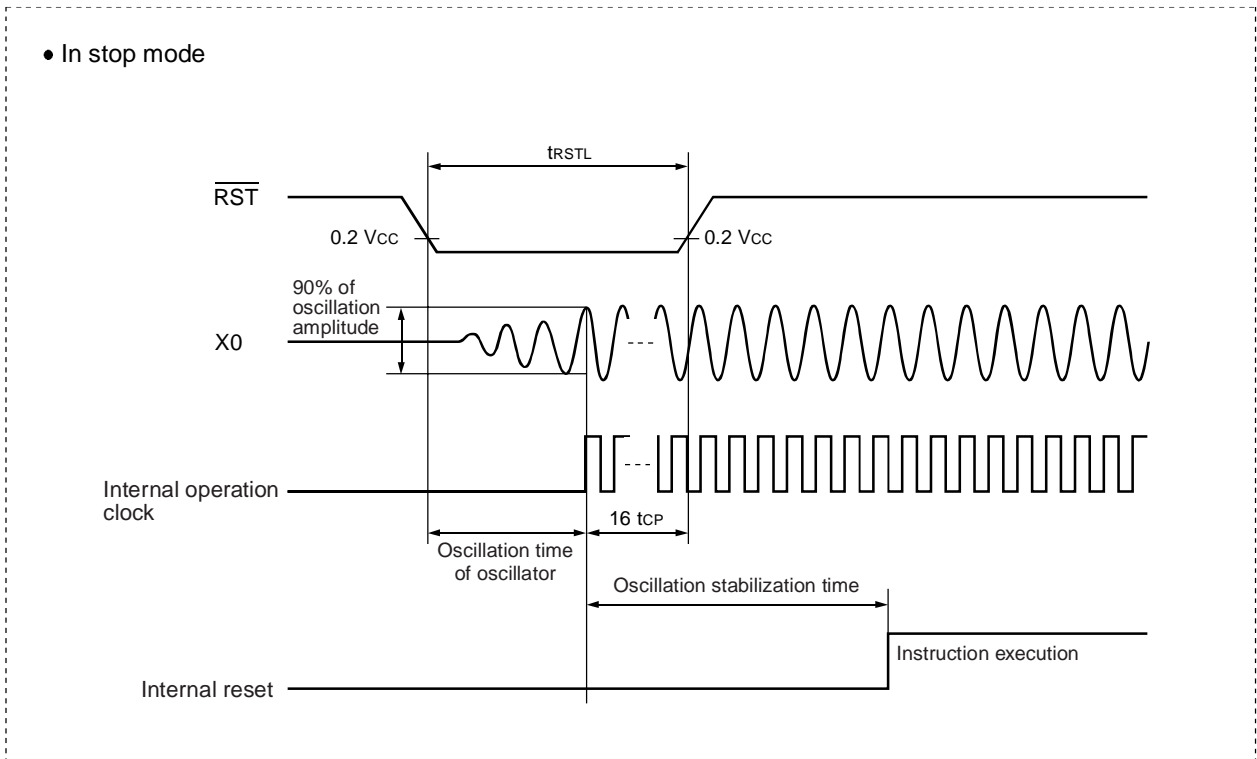
## (2) Reset Input Timing

( $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $AV_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Reset input time	$t_{RSTL}$	$\overline{RST}$	—	16 $t_{CP}$	—	ns	Normal operation
				Oscillation time of oscillator* + 16 $t_{CP}$	—	ms	In stop mode and sub-clock mode

\* : Oscillation time of oscillator is the time to reach to 90% of the oscillation amplitude from stand still. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In FAR/ceramic oscillator, the oscillation time is between hundreds of  $\mu\text{s}$  to several ms. In the external clock, the oscillation time is 0 ms.

Note :  $t_{CP}$  is the internal operating clock cycle time. Refer to “(1) Clock Timings” rating for  $t_{CP}$ .



# MB90378 Series

## (3) Power-on Reset

( $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $AV_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

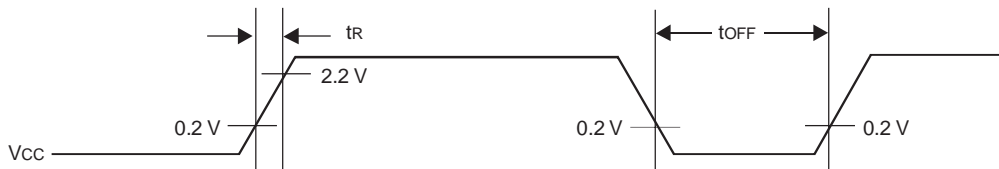
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Power supply rise time	$t_R$	$V_{CC}^*$	—	—	50	ms	
Power supply cut-off time	$t_{OFF}$	$V_{CC}^*$	—	1	—	ms	Due to repeated operations

\* :  $V_{CC}$  must be kept lower than 0.2 V before power-on.

Notes : • The above values are used for causing a power-on reset.

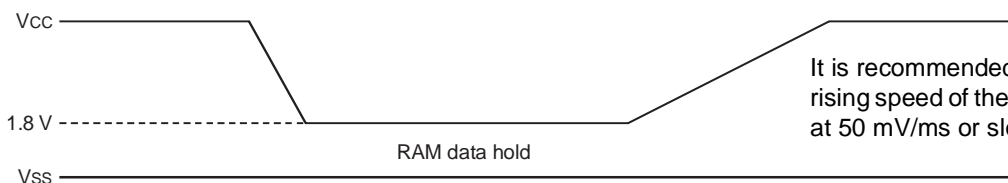
Some registers in the device are initialized only upon a power-on reset. To initialize these registers, turn on the power supply using the above values.

- Make sure that power supply rises within the selected oscillation stabilization time. If the power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.



Sudden changes in the power supply voltage may cause a power-on reset.

To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below. In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 V or fewer per second, however, you can use the PLL clock.



# MB90378 Series

## (4) UART1 to UART3

( $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $AV_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ °C to }+85\text{ °C}$ )

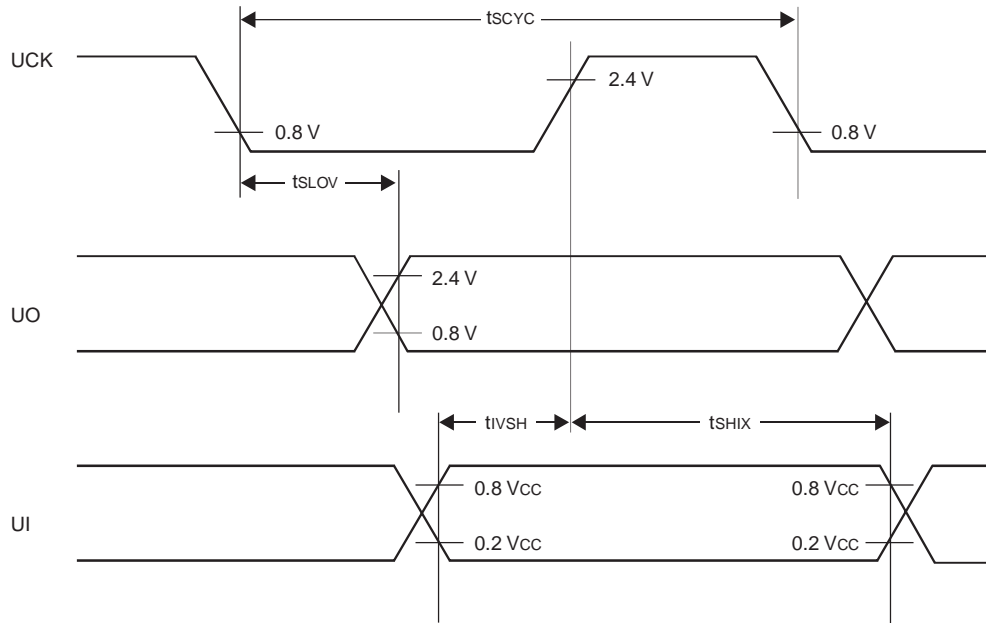
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	$t_{SCYC}$	UCK1 to UCK3	$C_L = 80\text{ pF} + 1\text{ TTL}$ for an output pin of internal shift clock mode	4 $t_{CP}$	—	ns	
UCK ↓ → UO delay time	$t_{SLOV}$	UCK1 to UCK3, UO1 to UO3		-80	80	ns	
Valid UI → UCK ↑	$t_{IVSH}$	UCK1 to UCK3, UI1 to UI3		100	—	ns	
UCK ↑ → valid UI hold time	$t_{SHIX}$	UCK1 to UCK3, UI1 to UI3		$t_{CP}$	—	ns	
Serial clock "H" pulse width	$t_{SHSL}$	UCK1 to UCK3	$C_L = 80\text{ pF} + 1\text{ TTL}$ for an output pin of external shift clock mode	4 $t_{CP}$	—	ns	
Serial clock "L" pulse width	$t_{SLSH}$	UCK1 to UCK3		4 $t_{CP}$	—	ns	
UCK ↓ → UO delay time	$t_{SLOV}$	UCK1 to UCK3, UO1 to UO3		—	150	ns	
Valid UI → UCK ↑	$t_{IVSH}$	UCK1 to UCK3, UI1 to UI3		60	—	ns	
UCK ↑ → valid UI hold time	$t_{SHIX}$	UCK1 to UCK3, UI1 to UI3		60	—	ns	

- Notes :
- These are AC ratings in the CLK synchronous mode.
  - $C_L$  is the load capacitance value connected to pins while testing.
  - $t_{CP}$  is the internal operating clock cycle time. Refer to "(1) Clock Timings" rating for  $t_{CP}$ .

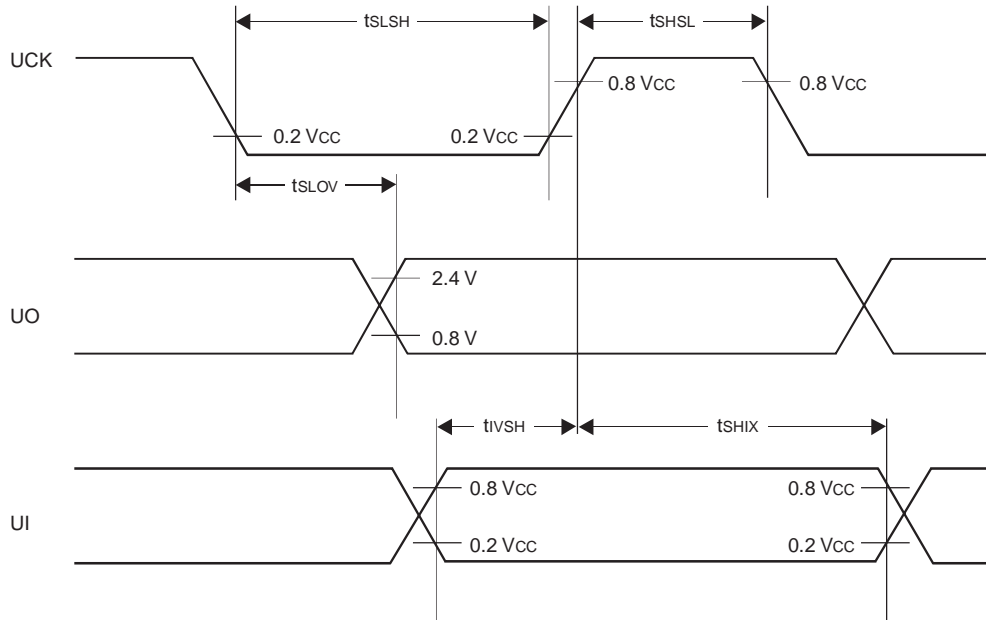


# MB90378 Series

## • Internal shift clock mode



## • Internal shift clock mode



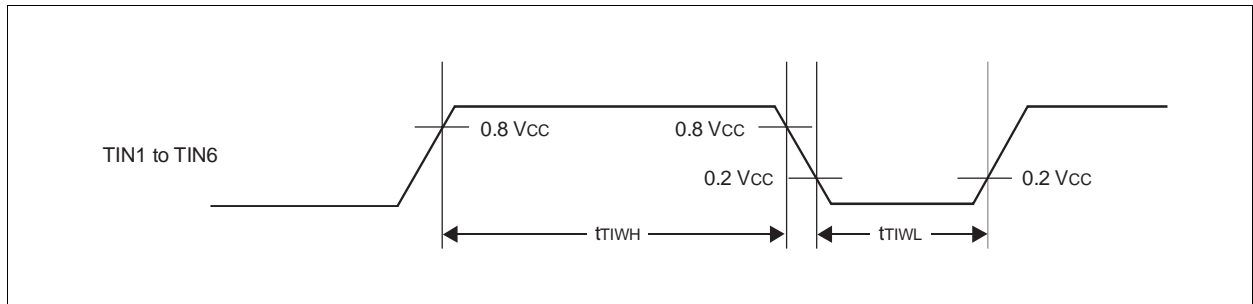
# MB90378 Series

## (5) Resources Input Timing

( $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $AV_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Timer input pulse width	$t_{TIWH}$ $t_{TIWL}$	TIN1 to TIN6	—	$4 t_{CP}$	—	ns	

Note :  $t_{CP}$  is the internal operating clock cycle time. Refer to “(1) Clock Timings” rating for  $t_{CP}$ .

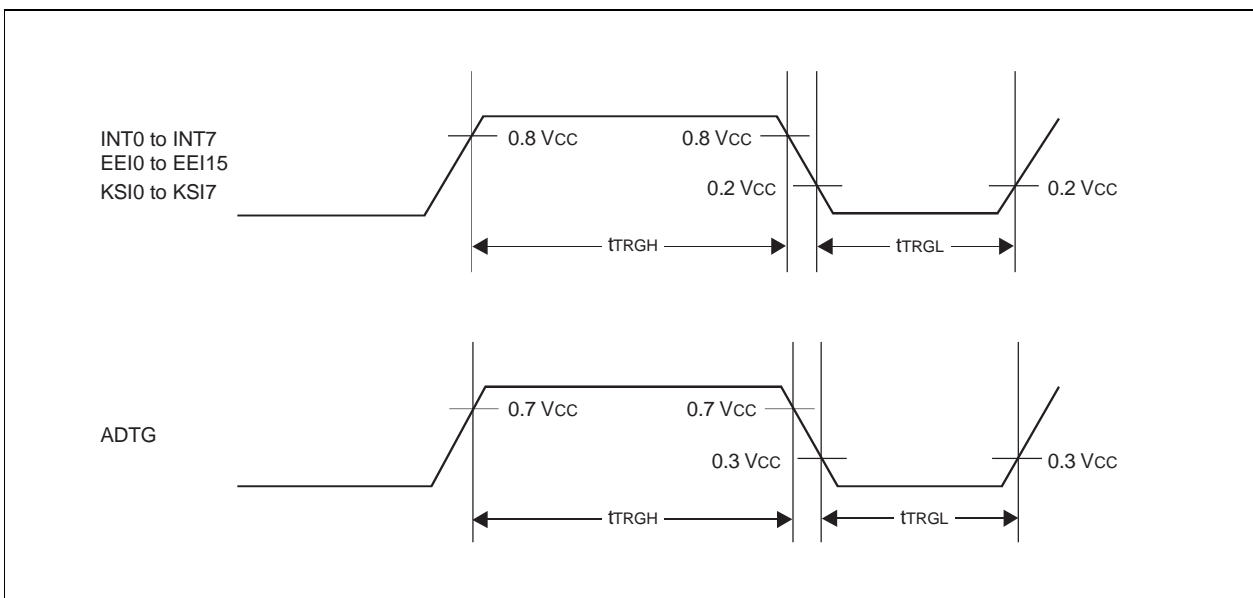


## (6) Trigger Input Timing

( $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $AV_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{TRGH}$	ADTG, INT0 to INT7, EEI0 to EEI15, KSI0 to KSI7	—	$5 t_{CP}$	—	ns	Normal operation
	$t_{TRGL}$			1	—	$\mu\text{s}$	Stop mode

Note :  $t_{CP}$  is the internal operating clock cycle time. Refer to “(1) Clock Timings” rating for  $t_{CP}$ .



# MB90378 Series

## (7) I<sup>2</sup>C / Multi-address I<sup>2</sup>C Timing

(V<sub>CC</sub> = 2.7 V to 3.6 V, AV<sub>CC</sub> = 2.7 V to 3.6 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40 °C to +85 °C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Start condition output	t <sub>STA</sub>	SCL, SDA	t <sub>CP</sub> (m × n/2 - 1) - 20	t <sub>CP</sub> (m × n/2 - 1) + 20	ns	Master mode
Stop condition output	t <sub>STO</sub>	SCL, SDA	t <sub>CP</sub> (m × n/2 + 3) - 20	t <sub>CP</sub> (m × n/2 + 3) + 20	ns	Master mode
Start condition detect	t <sub>STA</sub>	SCL, SDA	t <sub>CP</sub> + 40	—	ns	
Stop condition detect	t <sub>STO</sub>	SCL, SDA	t <sub>CP</sub> + 40	—	ns	
Restart condition output	t <sub>STASU</sub>	SCL, SDA	t <sub>CP</sub> (m × n/2 + 3) - 20	t <sub>CP</sub> (m × n/2 + 3) + 20	ns	Master mode
Restart condition detect	t <sub>STASU</sub>	SCL, SDA	t <sub>CP</sub> + 40	—	ns	
SCL output "L" width	t <sub>LOW</sub>	SCL	t <sub>CP</sub> × m × n/2 - 20	t <sub>CP</sub> × m × n/2 + 20	ns	Master mode
SCL output "H" width	t <sub>HIGH</sub>	SCL	t <sub>CP</sub> (m × n/2 + 2) - 20	t <sub>CP</sub> (m × n/2 + 2) + 20	ns	Master mode
SDA output delay	t <sub>DO</sub>	SDA	t <sub>CP</sub> × 3 - 20	t <sub>CP</sub> × 3 + 20	ns	
SDA output setup time after interrupt	t <sub>DOSU</sub>	SDA	t <sub>CP</sub> × m × n/2 - 20	—	ns	*1
			t <sub>CP</sub> × 4 - 20	—	ns	*2
SCL input "L" pulse	t <sub>LOW</sub>	SCL	t <sub>CP</sub> × 3 + 40	—	ns	
SCL input "H" pulse	t <sub>HIGH</sub>	SCL	t <sub>CP</sub> + 40	—	ns	
SDA output setup time	t <sub>SU</sub>	SDA	40	—	ns	
SDA hold time	t <sub>HO</sub>	SDA	0	—	ns	

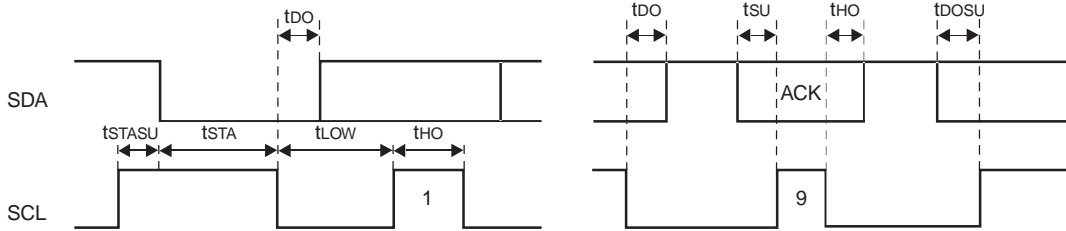
- Notes :
- t<sub>CP</sub> is the internal operating clock cycle time. Refer to "(1) Clock Timings" rating for t<sub>CP</sub>.
  - m is the setting bit of shift clock oscillation defined in the "ICCR register (CS4, CS3)" and "MCCR register (CS4, CS3)". Please refer to the MB90378 series H/W manual for details.
  - n is the setting bit of shift clock oscillation defined in the "ICCR register (CS2 to CS0)" and "MCCR register (CS2 to CS0)". Please refer to the MB90378 series H/W manual for details.
  - t<sub>DOSU</sub> is shown in the interrupt time is longer than the "L" width of SCL.
  - SDA and SCL output value is specified on condition that the rise/fall time is "0 ns".

\*1 : At the stop condition or transferring of next byte.

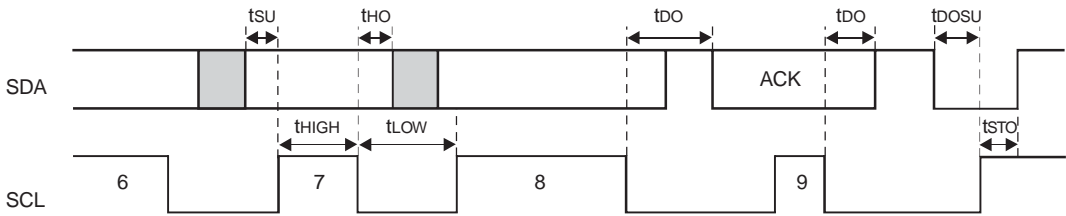
\*2 : After setting register bit IBCRH : SCC at restart.

# MB90378 Series

- Data transmit (master/slave)



- Data receive (master/slave)



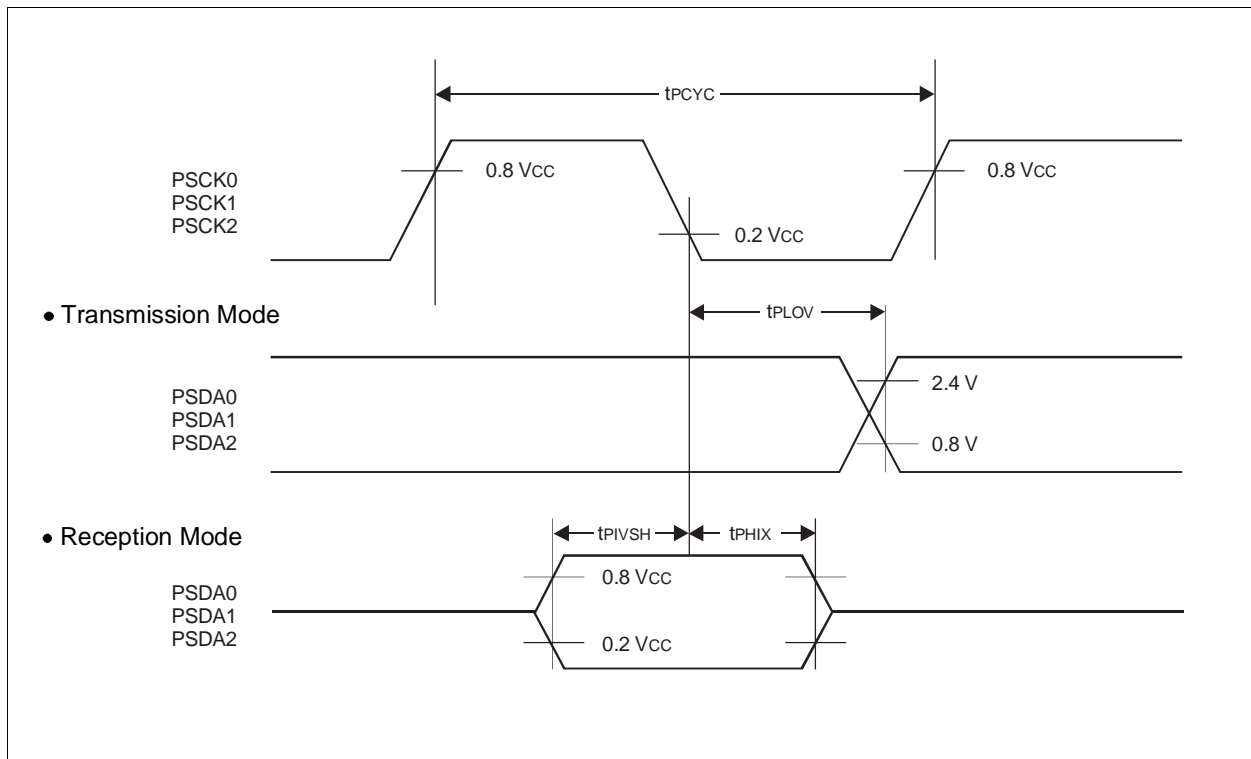
# MB90378 Series

## (8) PS/2 Interface Timing

( $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $AV_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
PSCK clock cycle time	$t_{PCYC}$	PSCK0 to PSCK2, PSDA0 to PSDA2	—	$4 t_{CP}$	—	—	ns	
PSCK $\downarrow$ $\rightarrow$ PSDA	$t_{PLOV}$	PSCK0 to PSCK2, PSDA0 to PSDA2	Transmission Mode	$2 t_{CP}$	—	—	ns	
Valid PSDA $\rightarrow$ PSCK $\downarrow$	$t_{PIVSH}$	PSCK0 to PSCK2, PSDA0 to PSDA2	Reception Mode	$1 t_{CP}$	—	—	ns	
PSCK $\downarrow$ $\rightarrow$ valid PSDA hold time	$t_{PHIX}$	PSCK0 to PSCK2, PSDA0 to PSDA2		$1 t_{CP}$	—	—	ns	
PSCK clock "H" pulse width	$t_{PHSL}$	PSCK0 to PSCK2, PSDA0 to PSDA2	—	$2 t_{CP}$	—	—	ns	
PSCK clock "L" pulse width	$t_{PLSH}$	PSCK0 to PSCK2, PSDA0 to PSDA2		$2 t_{CP}$	—	—	ns	

Note :  $t_{CP}$  is the internal operating clock cycle time. Refer to "(1) Clock Timings" rating for  $t_{CP}$ .



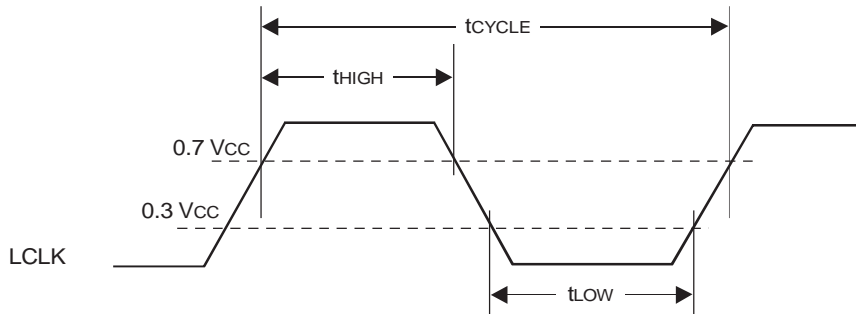
# MB90378 Series

## (9) LPC Timing

( $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $AV_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
LCLK cycle time	$t_{CYCLE}$	—	—	30	—	—	ns	
LCLK high time	$t_{HIGH}$	—	—	12	—	—	ns	
LCLK low time	$t_{LOW}$	—	—	12	—	—	ns	

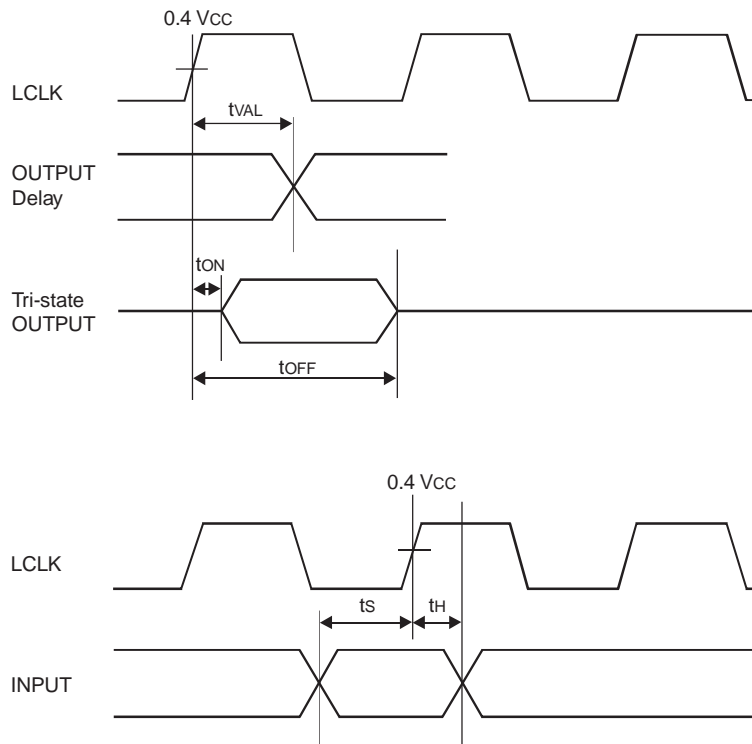
### • LCLK AC timing



# MB90378 Series

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output valid delay	$t_{VAL}$	—	—	2	—	12	ns	
Float to active delay	$t_{ON}$	—	—	2	—	—	ns	
Active to float delay	$t_{OFF}$	—	—	—	—	28	ns	
Input setup time	$t_s$	—	—	7	—	—	ns	
Input hold time	$t_H$	—	—	0	—	—	ns	

• LAD,  $\overline{LFRAME}$ , GA20 AC timing



# MB90378 Series

## 5. A/D Converter Electrical Characteristics

( $2.7\text{ V} \leq \text{AVR} - \text{AV}_{\text{SS}}$ ,  $V_{\text{CC}} = \text{AV}_{\text{CC}} = 2.7\text{ V}$  to  $3.6\text{ V}$ ,  $V_{\text{SS}} = \text{AV}_{\text{SS}} = 0.0\text{ V}$ ,  $T_{\text{A}} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ )

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	$\pm 3.0$	LSB	
Non-linear error	—	—	—	—	$\pm 2.5$	LSB	
Differential linearity error	—	—	—	—	$\pm 1.9$	LSB	
Zero transition voltage	$V_{\text{OT}}$	AN0 to AN11	$\text{AV}_{\text{SS}} - 1.5\text{ LSB}$	$\text{AV}_{\text{SS}} + 0.5\text{ LSB}$	$\text{AV}_{\text{SS}} + 5.5\text{ LSB}$	mV	For MB90V378
					$\text{AV}_{\text{SS}} + 2.5\text{ LSB}$		For MB90F378
Full-scale transition voltage	$V_{\text{FST}}$	AN0 to AN11	$\text{AVR} - 3.5\text{ LSB}$	$\text{AVR} - 1.5\text{ LSB}$	$\text{AVR} + 0.5\text{ LSB}$	mV	
Conversion time	—	—	3.1	—	—	$\mu\text{s}$	Actual value is specified as a sum of values specified in ADCR0 : CT1, CT0 and ADCR0 : ST1, ST0. Be sure that the setting value is greater than the min value
Sampling period	—	—	2	—	—	$\mu\text{s}$	Actual value is specified in ADCR0 : ST1, ST0 bits. Be sure that the setting value is greater than the min value
Analog port input current	$I_{\text{AIN}}$	AN0 to AN11	—	0.1	10	$\mu\text{A}$	
Analog input voltage	$V_{\text{AIN}}$	AN0 to AN11	$\text{AV}_{\text{SS}}$	—	AVR	V	
Reference voltage	—	AVR	$\text{AV}_{\text{SS}} + 2.7$	—	$\text{AV}_{\text{CC}}$	V	
Power supply current	$I_{\text{A}}$	$\text{AV}_{\text{CC}}$	—	1.4	6.4	mA	
	$I_{\text{AH}}$		—	—	5	$\mu\text{A}$	*
Reference voltage supply current	$I_{\text{R}}$	AVR	—	94	300	$\mu\text{A}$	
	$I_{\text{RH}}$		—	—	5	$\mu\text{A}$	*
Offset between channels	—	AN0 to AN11	—	—	4	LSB	

\*: The current when the A/D converter is not operating or the CPU is in stop mode (for  $V_{\text{CC}} = \text{AV}_{\text{CC}} = \text{AVR} = 3.0\text{ V}$ ).



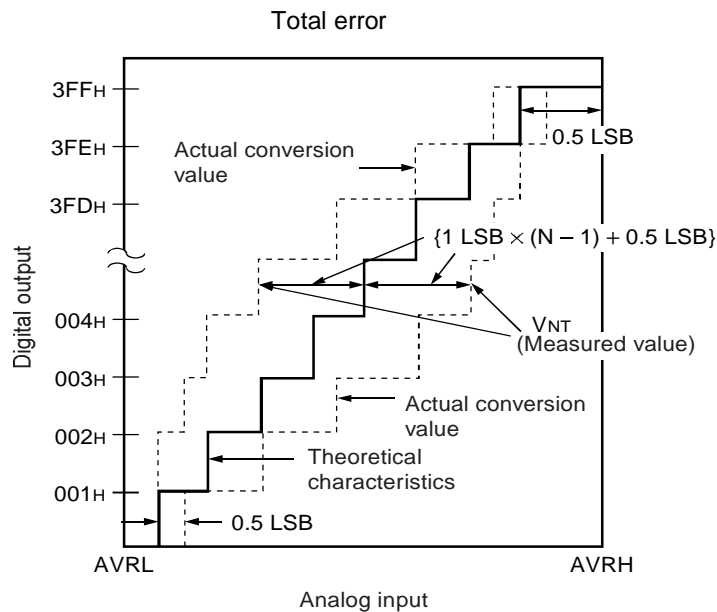
## 6. A/D Converter Glossary

Resolution : Analog changes that are identifiable with the A/D converter.

Linearity error : The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics.

Differential linearity error : The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value.

Total error : The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



$$\text{Total error for digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$1 \text{ LSB (Theoretical value)} = \frac{AVR - AVss}{1024} \text{ [V]}$$

$$V_{OT} \text{ (Theoretical value)} = AVss + 0.5 \text{ LSB [V]}$$

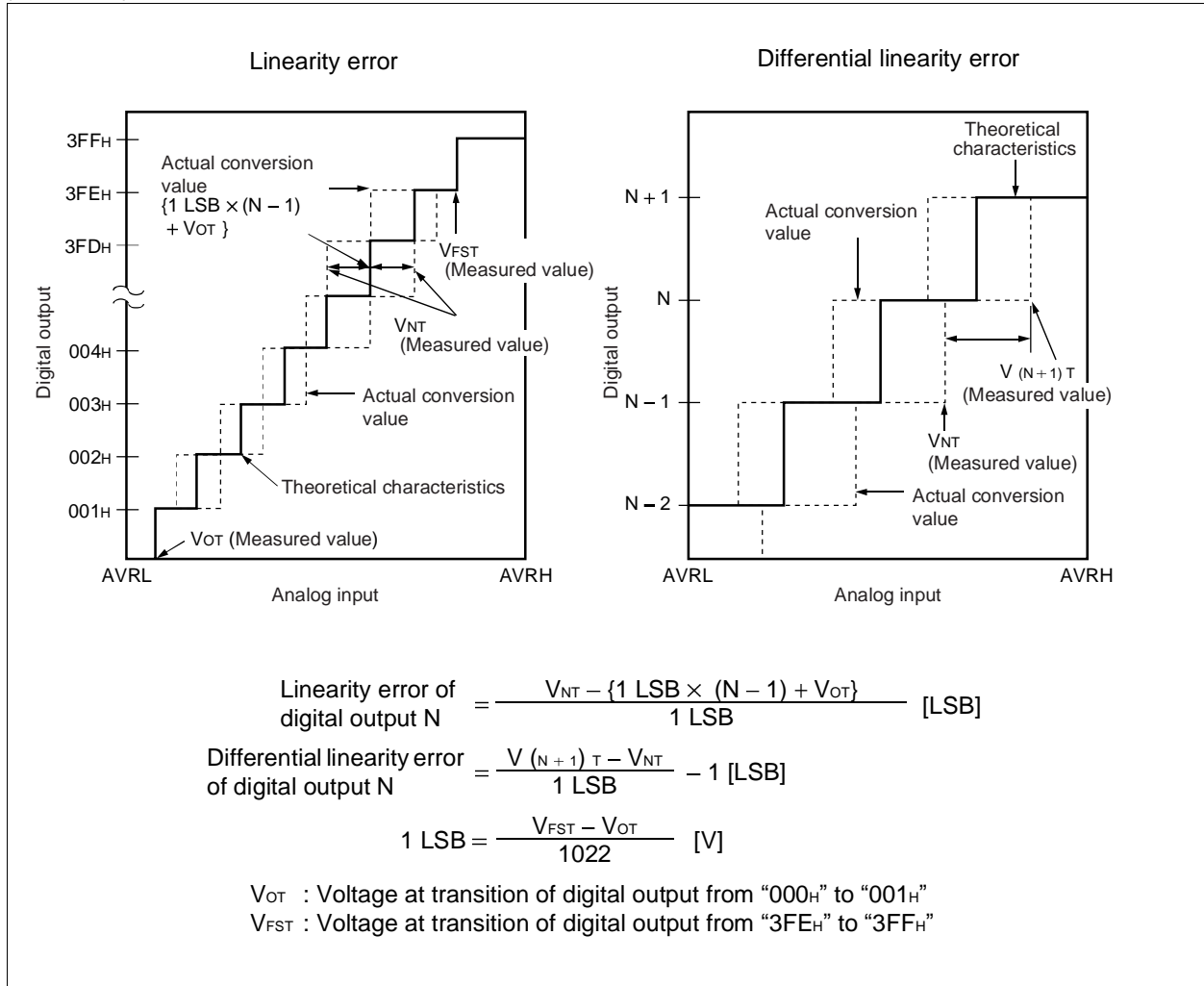
$$V_{FST} \text{ (Theoretical value)} = AVR - 1.5 \text{ LSB [V]}$$

$V_{NT}$  : Voltage at a transition of digital output from  $(N - 1)$  to  $N$

(Continued)

# MB90378 Series

(Continued)



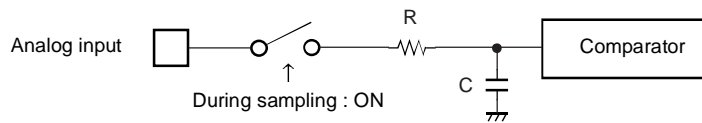
# MB90378 Series

## 7. Notes on Using A/D Converter

### • About the external impedance of the analog input and its sampling time

- A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sampling and hold capacitor is insufficient, adversely affecting A/D conversion precision.

#### • Analog input circuit model

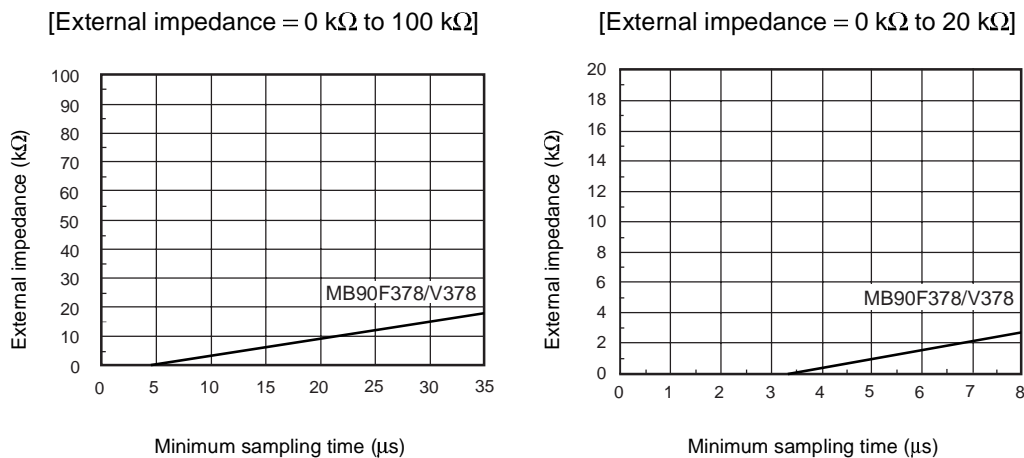


Note : The values are reference values.

	R	C
MB90F378/V378	1.9 kΩ (Max)	25 pF (Max)

- To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

#### • The relationship between the external impedance and minimum sampling time



- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

### • About errors

As  $|AVR - AV_{SS}|$  becomes smaller, values of relative errors grow larger.

# MB90378 Series

## 8. D/A Electrical Characteristics

( $V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Resolution	—	—	—	—	8	—	bit	
Differential linearity error	—	—		—	—	$\pm 0.9$	LSB	
Non-linearity error	—	—		—	—	$\pm 1.5$	LSB	
Conversion time	—	—		—	0.6	—	$\mu\text{s}$	*
Analog output impedance	—	—		2.0	2.9	3.8	$\text{k}\Omega$	
Power supply current	$I_{DVR}$	$AV_{CC}$		—	—	460	$\mu\text{A}$	
	$I_{DVRS}$	$AV_{CC}$	—	0.1	—	$\mu\text{A}$	D/A stops	

\* : With load capacitance is 20 pF.

## 9. Serial IRQ Electrical Characteristics

( $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $AV_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	$V_{IH}$	—	—	$0.7 V_{CC}$	—	$V_{CC}$	V	
"L" level input voltage	$V_{IL}$	—	—	$V_{SS}$	—	$0.3 V_{CC}$	V	
"H" level output voltage	$V_{OH}$	—	—	$V_{CC} - 0.5$	—	—	V	
"L" level output voltage	$V_{OL}$	—	—	—	—	0.4	V	

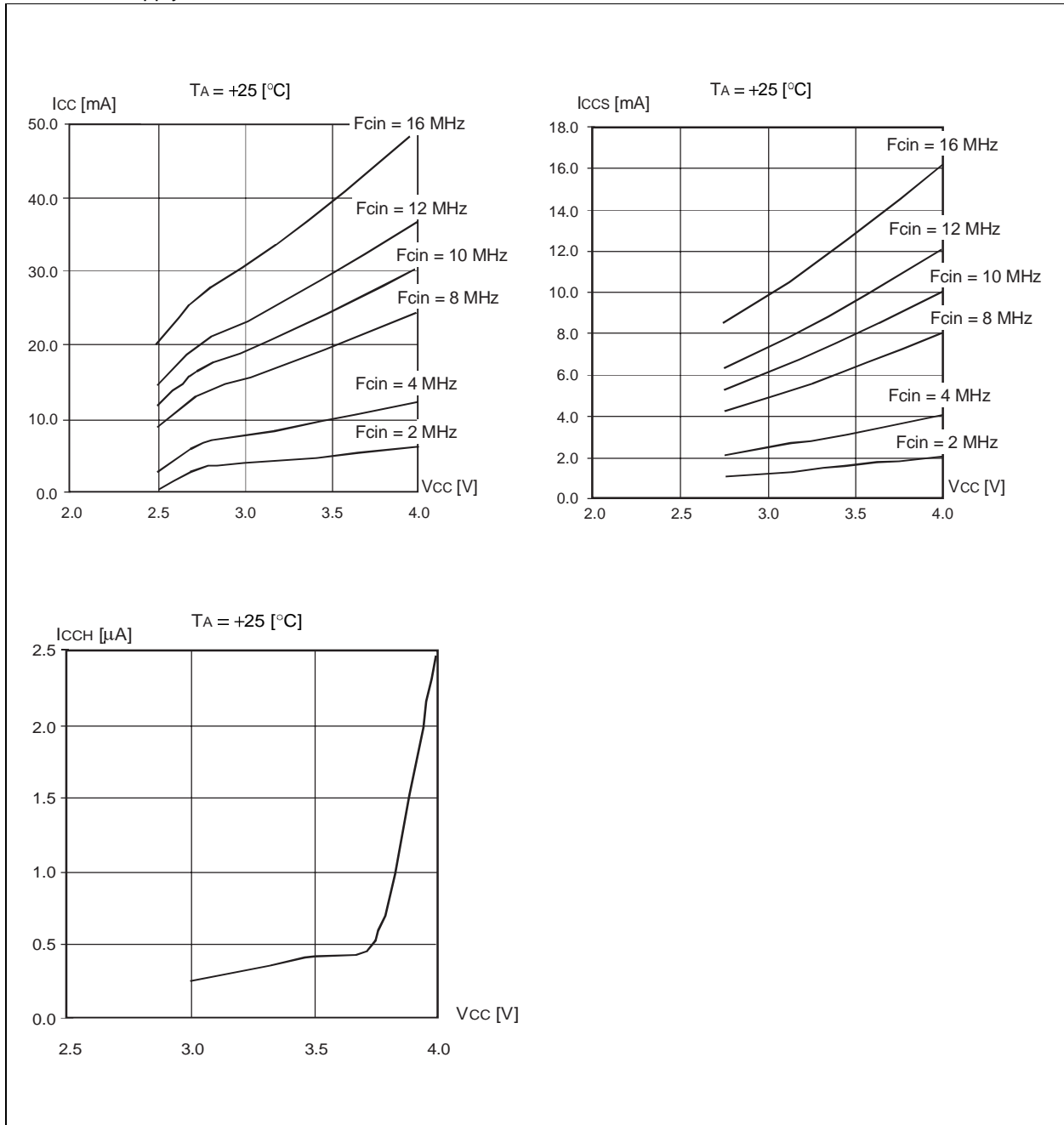
## 10. Flash Memory Program/Erase Characteristics

Parameter	Condition	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time (4 Kbytes sector)	$T_A = +25\text{ }^\circ\text{C}$ $V_{CC} = 3.0\text{ V}$	—	0.2	0.5	s	Excludes 00 <sub>H</sub> programming prior to erasure
Sector erase time (16 Kbytes sector)		—	0.5	7.5	s	Excludes 00 <sub>H</sub> programming prior to erasure
Chip erase time		—	4.6	—	s	Excludes 00 <sub>H</sub> programming prior to erasure
Byte (8-bit width) programming time		—	32	3,600	$\mu\text{s}$	Except for the over head time of the system
Program/Erase cycle	—	10,000	—	—	cycle	

# MB90378 Series

## EXAMPLE CHARACTERISTICS (MB90F378)

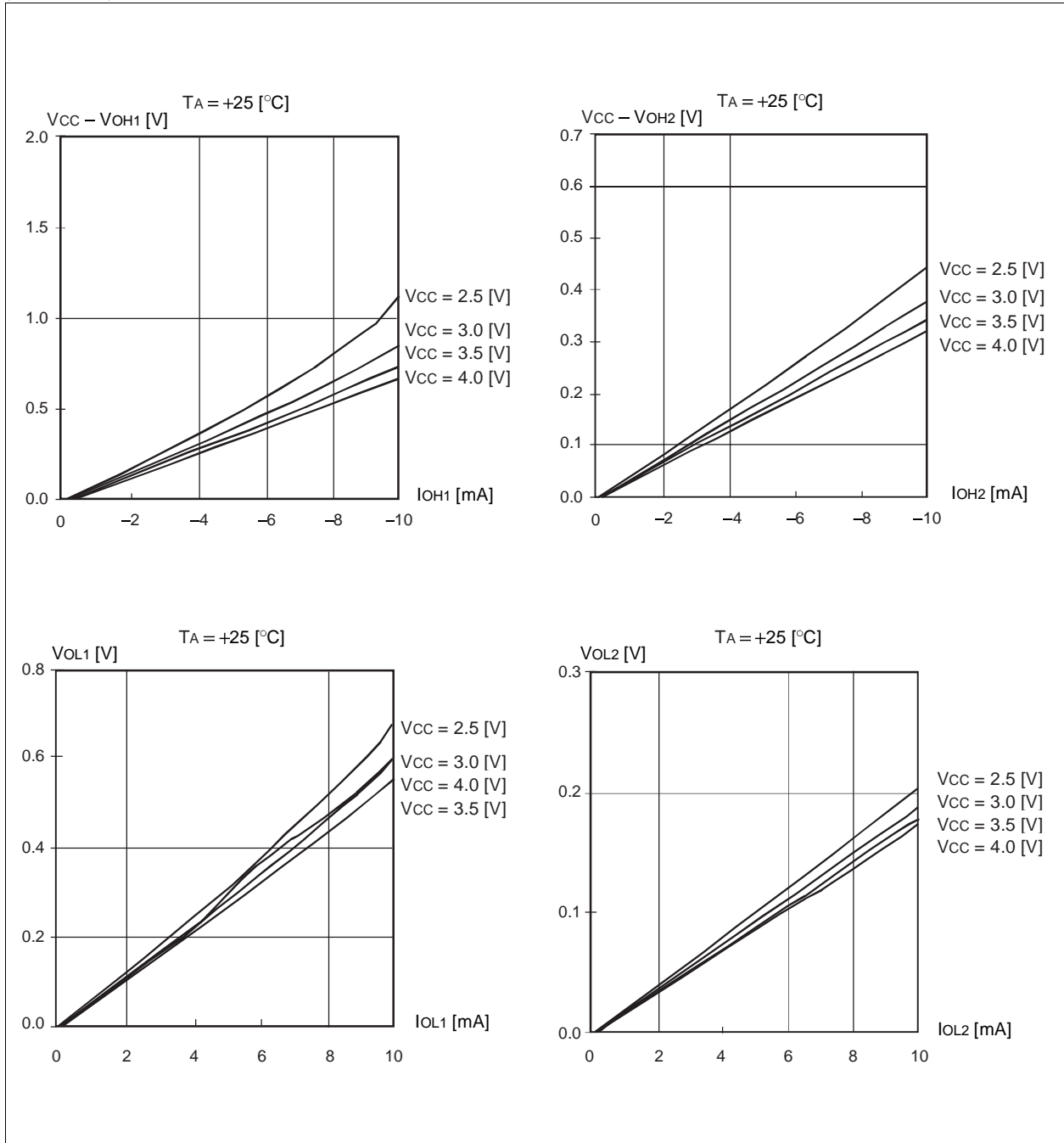
- Power Supply Current



(Continued)

# MB90378 Series

(Continued)



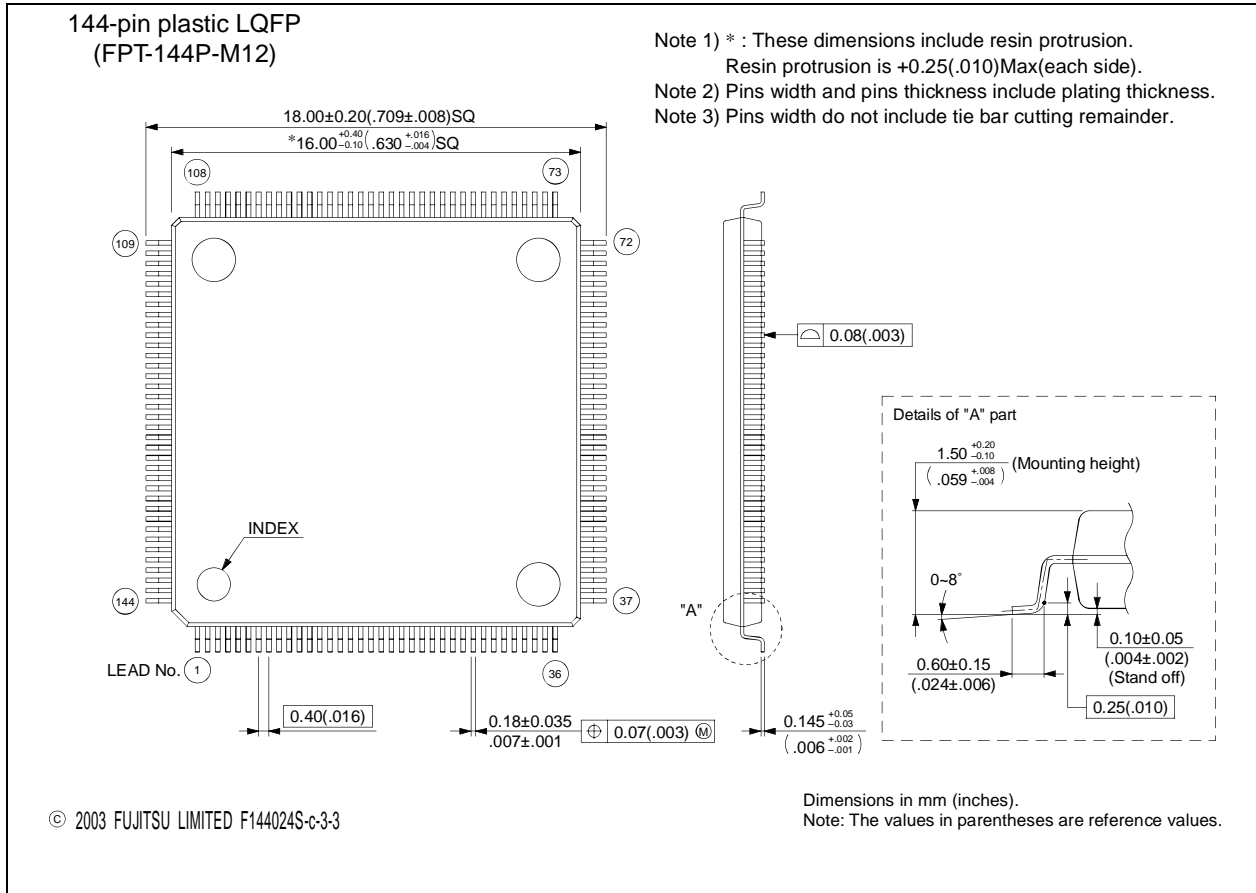
# MB90378 Series

## ■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F378PFF-GE1	144-pin Plastic LQFP (FPT-144P-M12)	

# MB90378 Series

## ■ PACKAGE DIMENSION





# MB90378 Series

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