## *Advance Product Information*

# *VSC7124*

*Quad Port Bypass Circuit*

## *Features*

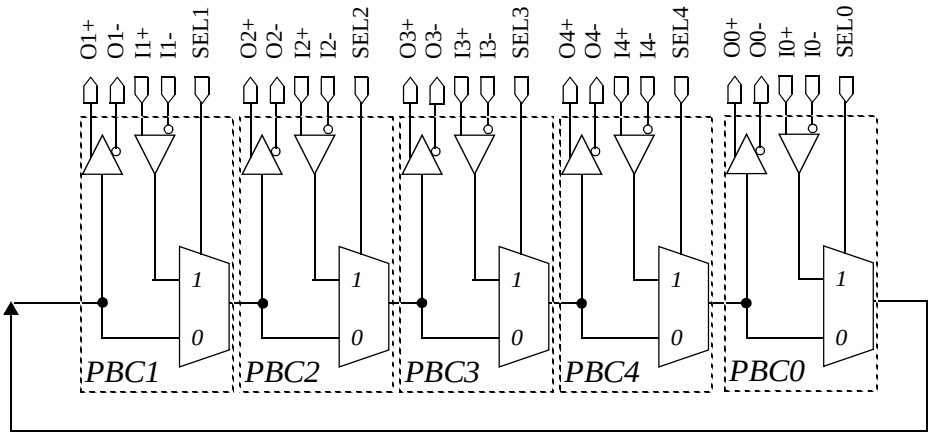
- ANSI X3T11 Fibre Channel Compliant at 1.0625Gb/s
- IEEE 802.3z Gigabit Ethernet Compliant at 1.25Gb/s
- Five Port Bypass Circuits (PBCs)
- On-Chip Transmit Termination
- 3.3V, 0.25W Typical Power
- 0.35um CMOS, a Velocity Family Member
- 44-Pin, 10mm PQFP Package

## *General Description*

The VSC7124 contains five cascaded Port Bypass Circuits (PBCs) used to steer serial signals. This part is typically used in distributing Fibre Channel signals to an array of disk drives in an FC-AL loop as illustrated in Figure 1. The VSC7124 can be used with any of the Vitesse JBOD circuits to implement FC-AL JBODs of virtually any size. In Figure 1, the first VSC7127's CRU is configured as a Repeater to attenuate jitter. The VSC7124 does not contain a CRU in order to reduce power and cost. The second VSC7127's CRU is configured as a retimer so that the output of the device is a jitter compliance point.

Each PBC is a multiplexer that is controlled by the corresponding SELx line which, if HIGH, selects the external input or, if LOW, selects the output of the previous PBC.

## *VSC7124 Block Diagram*



## Application Example

A 12-port JBOD is shown in Figure 1. This dual loop application uses one VSC7127R, one VSC7127T and one VSC7124 on each loop in order to configure the FC-AL disk array. Functional drives are included in the FC-AL loop while nonfunctional or missing drives (numbers 2, 7, 9) are excluded.

**Figure 1: 12-Drive FC-AL JBOD Application**

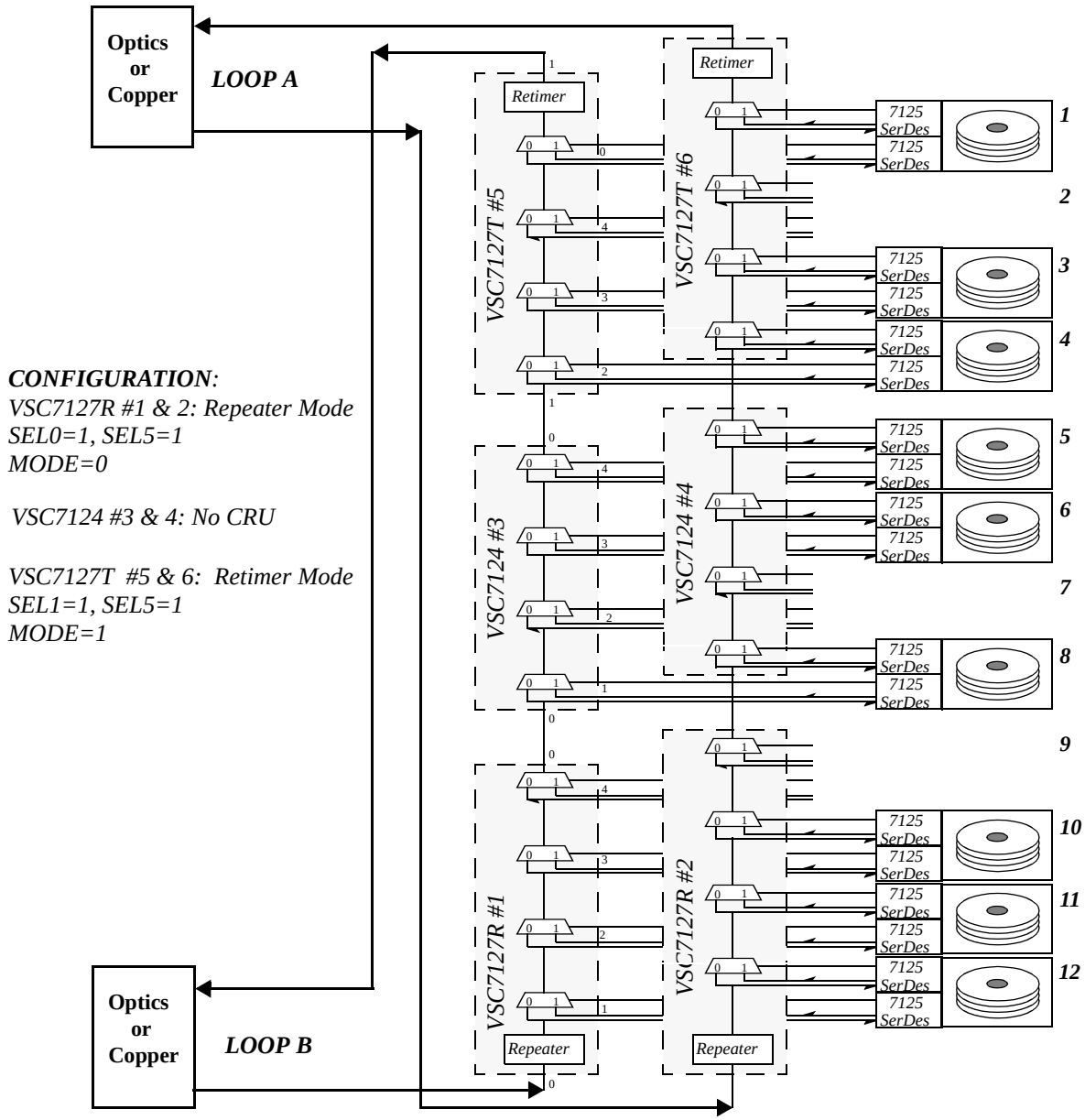
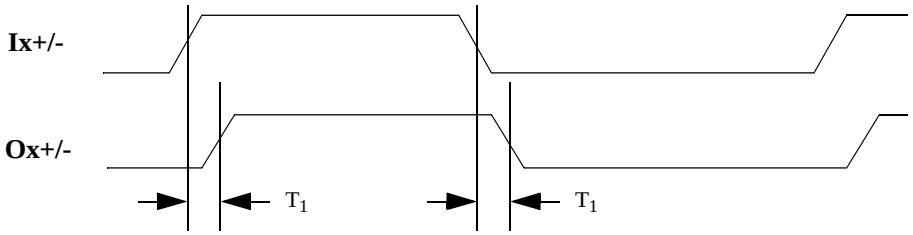


**Figure 2: Timing Waveforms**




## AC Characteristics *(Over Recommended Operating Conditions)*

| *Parameters* | *Description* | *Min* | *Typ* | *Max* | *Units* | *Conditions* |
|---|---|---|---|---|---|---|
| $T_1$ | Propagation Delay | | | 7.0 | ns | Delay with all circuits bypassed. |
| $T_R$, $T_F$ | Serial Data Rise and Fall Time | | | 300 | ps | At $\Delta V_{IN}$ minimum levels |
| $T_{j(PBC)}$ | Data Jitter Accummulation | | | 120 | ps | Peak-to-Peak on Ox+/- |

## DC Characteristics *(Over Recommended Operating Conditions)*

| *Parameters* | *Description* | *Min* | *Typ* | *Max* | *Units* | *Conditions* |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH voltage (TTL) | 2.4 | | | V | $I_{OH}$ = -1.0 mA |
| $V_{OL}$ | Output LOW voltage (TTL) | | | 0.5 | V | $I_{OL}$ = +1.0 mA |
| $V_{IH}$ | Input HIGH voltage (TTL) | 2.0 | | 5.5 | V | |
| $V_{IL}$ | Input LOW voltage (TTL) | 0 | | 0.8 | V | |
| $I_{IH}$ | Input HIGH current (TTL) | | 50 | 500 | µA | $V_{IN}$ =2.4V |
| $I_{IL}$ | Input LOW current (TTL) | | | -500 | µA | $V_{IN}$ =0.5V |
| $\Delta V_{OUT75}$(1) | TX output differential peak-to-peak voltage swing | 1200 | | 2200 | mVp-p | 75Ω to $V_{DD}$ – 2.0 V |
| $\Delta V_{OUT50}$(1) | TX output differential peak-to-peak voltage swing | 1000 | | 2200 | mVp-p | 50Ω to $V_{DD}$ – 2.0 V |
| $\Delta V_{IN}$(1) | Receiver differential peak-to-peak Input Sensitivity RX | 400 | | 2600 | mVp-p | Internally biased to $V_{DD}$/2 |
| $V_{DD}$ | Supply voltage | 3.14 | | 3.47 | V | 3.3V±5% |
| $P_D$ | Power dissipation | | 250 | 555 | mW | Outputs open, $V_{DD}$ = $V_{DD}$ max ±2% |
| $I_{DD}$ | Power Supply Current | | 76 | 160 | mA | Outputs open, $V_{DD}$ = $V_{DD}$ max |

*NOTE: (1) Refer to Application Note AN-37 for details regarding differential voltage measurements.*

## Absolute Maximum Ratings (1)

TTL Power Supply Voltage ($V_{DD}$) ..... 0.5V to +4V
PECL DC Input Voltage ($V_{INP}$) ..... -0.5V to $V_{DD}$ +0.5V
TTL DC Input Voltage, ($V_{INT}$) ..... -0.5V to 5.5V
DC Voltage Applied to Outputs for High Output State ($V_{IN\ TTL}$) ..... -0.5V to $V_{DD}$ + 0.5V
TTL Output Current ($I_{OUT}$), (DC, Output High) ..... 50mA
PECL Output Current ($I_{OUT}$), (DC, Output High) ..... -50mA
Case Temperature Under Bias, ($T_C$) ..... -55°C to +125°C
Storage Temperature ($T_{STG}$) ..... -65°C to + 150°C

## Recommended Operating Conditions (2)

Power Supply Voltage ($V_{DD}$) . ..... +3.14V to 3.47V
Ambient Operating Temperature Range (T) ..... 0°C to +85°C Ambient

*NOTES: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.*

*(2) Vitesse guarantees the functional and parametric operation of the part under "Recommended Operating Conditions" except where specifically noted in the AC and DC Parametric tables.*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## Package Pin Descriptions

**Figure 3: Pin Diagram**

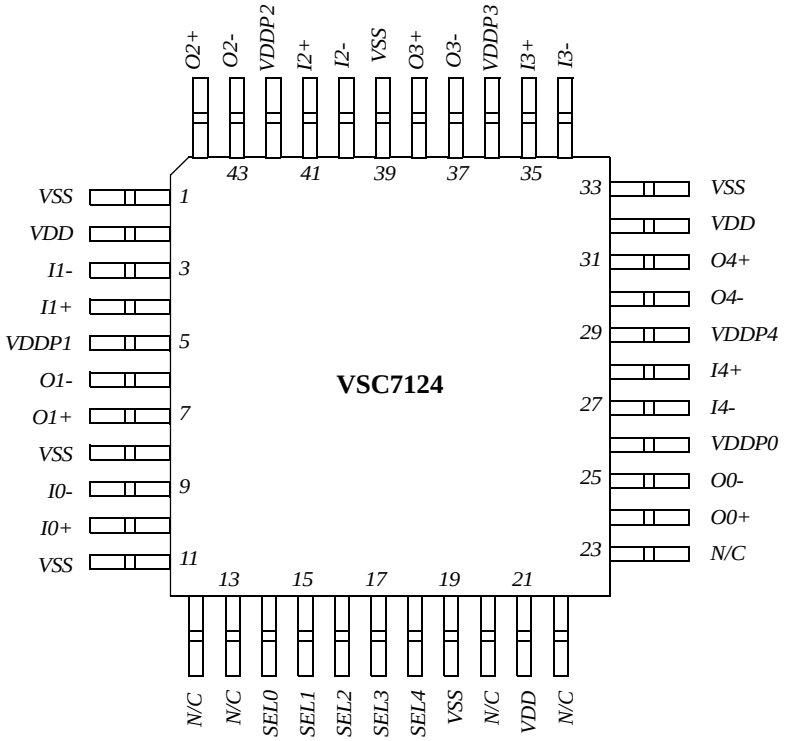
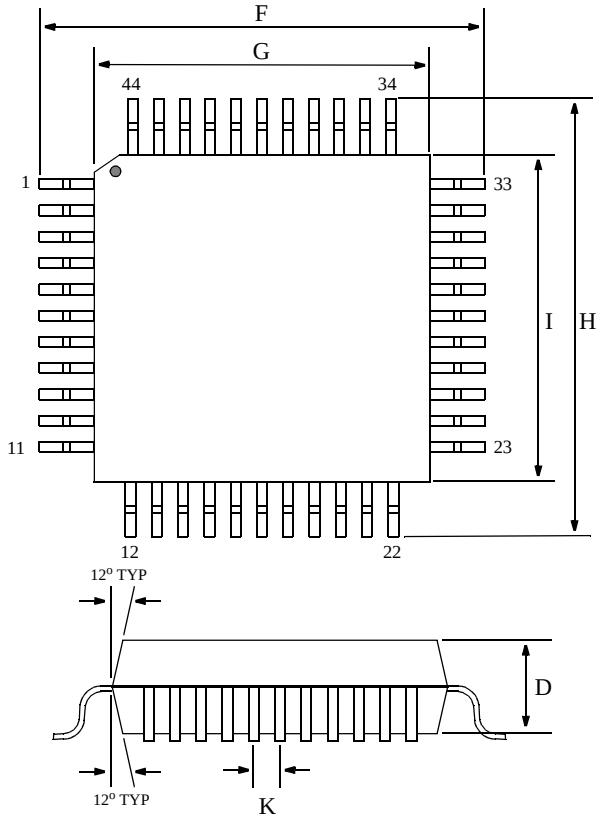



**Table 1: Pin Identifications**

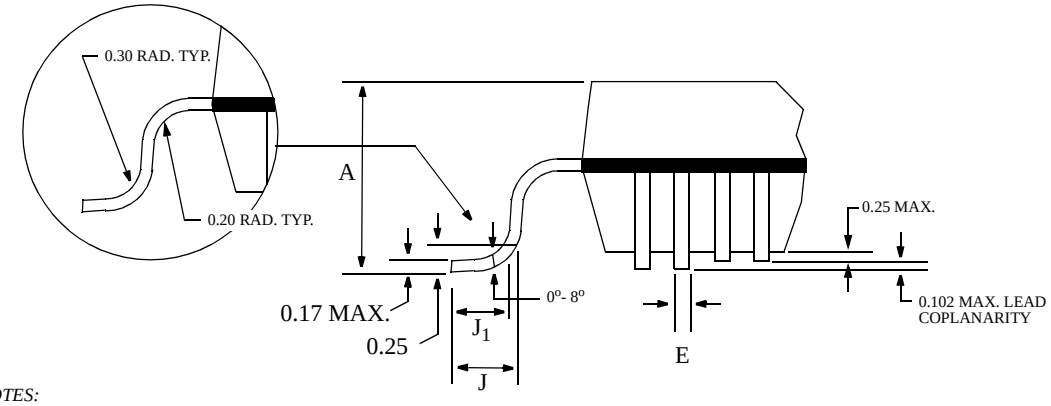
| *Pin #* | *Name* | *Description* |
|---|---|---|
| 4, 3, 41, 40<br>35, 34, 28, 27<br>10, 9 | I1+, I1-, I2+, I2-<br>I3+, I3-, I4+, I4-<br>I0+, I 0- | INPUT - Differential, Internally Biased to $V_{DD}/2$<br>Ix+/Ix- is the serial input to PBCx. |
| 15, 16,<br>17, 18<br>14 | SEL1, SEL2<br>SEL3, SEL4<br>SEL0 | INPUT - TTL<br>Port Bypass Mux SELect lines. A HIGH selects Ix. A LOW selects the output of the previous internal device. |
| 7, 6, 44, 43<br>38, 37, 31, 30<br>24, 25 | O1+, O1-, O2+, O2-<br>O3+, O3-, O4+, O4-<br>O0+, O0- | OUTPUT - Differential<br>Ox+/Ox- is the serial output from PBCx. |
| 2, 21, 32 | VDD | Digital Logic Power Supply. |
| 5<br>42<br>36<br>29<br>26 | VDDP1<br>VDDP2<br>VDDP3<br>VDDP4<br>VDDP0 | Power Supply (3.3V) for O1+/-. If unused, connect to VSS.<br>Power Supply (3.3V) for O2+/-. If unused, connect to VSS.<br>Power Supply (3.3V) for O3+/-. If unused, connect to VSS.<br>Power Supply (3.3V) for O4+/-. If unused, connect to VSS.<br>Power Supply (3.3V) for O0+/-. If unused, connect to VSS |
| 12, 13, 20, 22, 23 | N/C | Not Connected |
| 1, 8, 11, 19, 33, 39 | VSS | Ground |

## Package Information

***44-Pin PQFP 10 x 10 mm***




| *Item* | *mm* | *Tol.* |
|---|---|---|
| A | 2.45 | MAX |
| D | 2.00 | +0.10 |
| E | 0.35 | ±.05 |
| F | 13.20 | ±.25 |
| G | 10.00 | ±.10 |
| H | 13.20 | ±.25 |
| I | 10.00 | ±.10 |
| J | 0.88 | +.15 / -.10 |
| K | 0.80 | BASIC |




*NOTES:*
*Drawing not to scale.*
*Cavity up*
*All units in mm unless otherwise noted.*

## Package Thermal Characteristics

The VSC7124 is packaged in a standard plastic quad flatpack, PQFP. This package adheres to industry-standard EIAJ footprints for a 10mm body, 44-pin PQFP. The package construction is shown in Figure 4. The 44-pin PQFP with embedded slug has the thermal properties listed in Table 2.

**Figure 4: Package Cross Section**

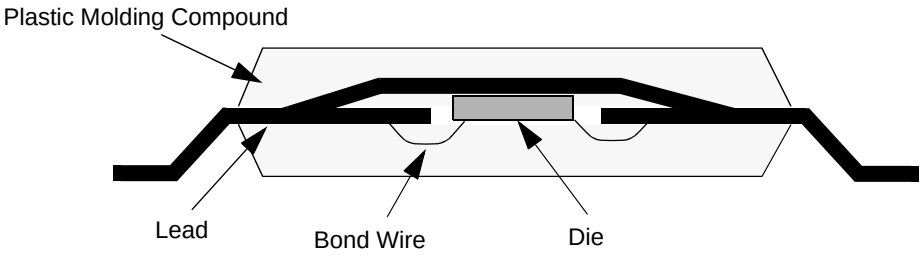



**Table 2: 44 PQFP Thermal Resistance**

| *Symbol* | *Description* | *Value* | *Units* |
|---|---|---|---|
| $\theta_{CA-0}$ | Thermal resistance from case-to-ambient, still air | 50 | $^{o}$C/W |
| $\theta_{CA-100}$ | Thermal resistance from case-to-ambient, 100 LFPM air | 43 | $^{o}$C/W |
| $\theta_{CA-200}$ | Thermal resistance from case-to-ambient, 200 LFPM air | 39 | $^{o}$C/W |
| $\theta_{CA-400}$ | Thermal resistance from case-to-ambient, 400 LFPM air | 36 | $^{o}$C/W |
| $\theta_{CA-600}$ | Thermal resistance from case-to-ambient, 600 LFPM air | 34 | $^{o}$C/W |

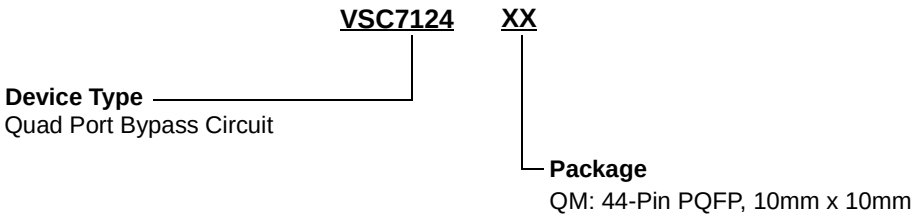
The VSC7124 is designed to operate with an ambient temperature up to +70$^{o}$C.

## Moisture Sensitivity Level

This device is rated at a Moisture Sensitivity Level 3 rating with maximum floor life of 168 hours at 30ºC, 60% relative humidity. Please refer to Application Note AN-20 for appropriate handling procedures.

## Ordering Information

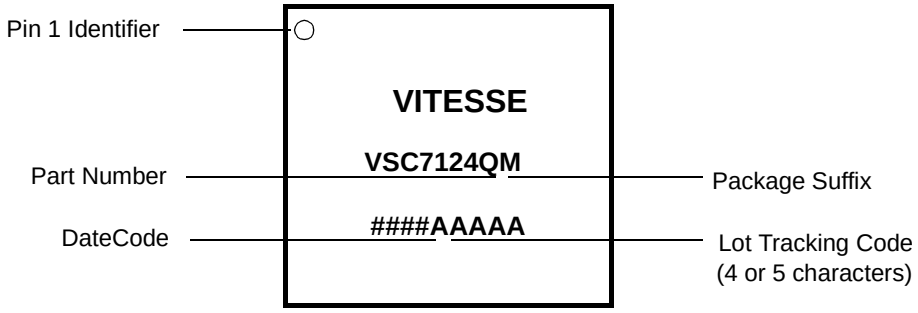
The order number for this product is formed by a combination of the device number and package type.




## Marking Information

The package is marked with three lines of text as shown in Figure 5.

**Figure 5: Package Marking Information**





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