![hynix logo]

HY29DS322/HY29DS323

32 Megabit (4M x 8/2M x16) Super-Low Voltage,
Dual Bank, Simultaneous Read/Write, Flash Memory

KEY FEATURES

- **Single Power Supply Operation**
  - Read, program, and erase operations from 1.8 to 2.2 V (2.0V ± 10%)
  - Ideal for battery-powered applications
- **Simultaneous Read/Write Operations**
  - Host system can program or erase in one bank while simultaneously reading from any sector in the other bank with zero latency between read and write operations
- **High Performance**
  - 100, 110 and 120 ns access time versions
- **Ultra Low Power Consumption (Typical Values)**
  - Automatic sleep mode current: 5 µA
  - Standby mode current: 5 µA
  - Read current: 5 mA (at 5 MHz)
  - Program/erase current: 20 mA
- **Boot-Block Sector Architecture with 71 Sectors in Two Banks for Fast In-System Code Changes**
- **Secured Sector: An Extra 64 Kbyte Sector that Can Be:**
  - <u>Factory locked and identifiable:</u> 16 bytes available for a secure, random factory Electronic Serial Number
  - <u>Customer lockable:</u> Can be read, programmed, or erased just like other sectors
- **Flexible Sector Architecture**
  - Sector Protection allows locking of a sector or sectors to prevent program or erase operations within that sector
  - Temporary Sector Unprotect allows changes in locked sectors (requires high voltage on RESET# pin)
- **Automatic Erase Algorithm Erases Any Combination of Sectors or the Entire Chip**
- **Automatic Program Algorithm Writes and Verifies Data at Specified Addresses**
- **Compliant with Common Flash Memory Interface (CFI) Specification**
- **Minimum 100,000 Write Cycles per Byte/ Word**
- **Compatible with JEDEC Standards**
  - Pinout and software compatible with single-power supply Flash devices
  - Superior inadvertent write protection

- **Data# Polling and Toggle Bits**
  - Provide software confirmation of completion of program or erase operations
- **Ready/Busy# Pin**
  - Provides hardware confirmation of completion of program or erase operations
- **Erase Suspend**
  - Suspends an erase operation to allow programming data to or reading data from a sector in the same bank
  - Erase Resume can then be invoked to complete the suspended erasure
- **Hardware Reset Pin (RESET#) Resets the Device to Reading Array Data**
- **WP#/ACC Input Pin**
  - Write protect (WP#) function allows hardware protection of two outermost boot sectors, regardless of sector protect status
  - Acceleration (ACC) function provides accelerated program times
- **Fast Program and Erase Times**
  - Sector erase time: 2 sec typical
  - Byte/Word program time utilizing Acceleration function: 10 µs typical
- **Space Efficient Packaging**
  - 48-pin TSOP and 48-ball FBGA packages

LOGIC DIAGRAM
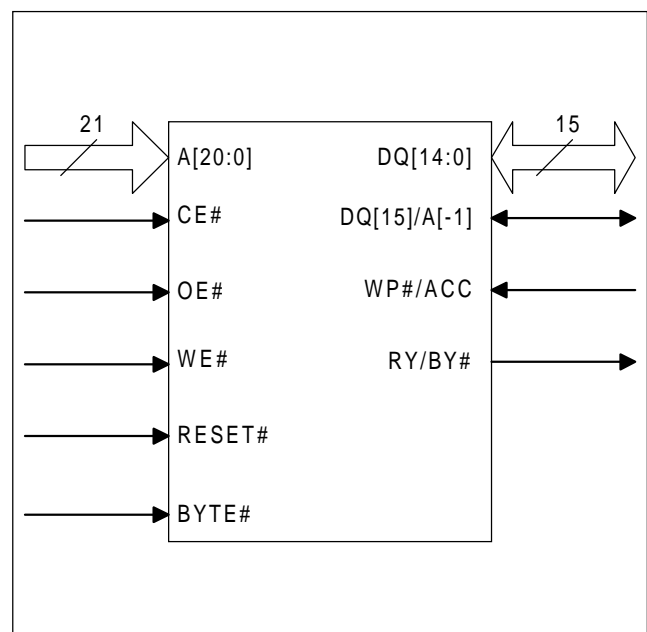
GENERAL DESCRIPTION

The HY29DS322/HY29DS323 (HY29DS32x) is a 32 Mbit, 2.0 volt-only CMOS Flash memory organized as 4,194,304 (4M) bytes or 2,097,152 (2M) words. The device is available in 48-pin TSOP and 48-ball FBGA packages. Word-wide data (x16) appears on DQ[15:0] and byte-wide (x8) data appears on DQ[7:0].

The HY29DS32x Flash memory array is organized into 71 sectors in two banks. Bank 1 contains eight 8 KByte boot/parameter sectors and 7 or 15 larger sectors of 64 KBytes each, depending on the version of the device. Bank 2 contains the rest of the memory array, organized as 56 or 48 sectors of 64 KBytes:

	Bank 1	Bank 2
HY29DS322	8 x 8KB/4KW	56 x 64KB/32KW
	7 x 64KB/32KW	
HY29DS323	8 x 8KB/4KW	48 x 64KB/32KW
	15 x 64KB/32KW	

The device features simultaneous read/write operation, which allows the host system to invoke a program or erase operation in one bank and immediately and simultaneously read data from the other bank, except if that bank has any sectors marked for erasure, with zero latency. This releases the system from waiting for the completion of program or erase operations, thus improving overall system performance.

The HY29DS32x can be programmed and erased in-system with a single 2.0 volt ± 10% V_{CC} supply. Internally generated and regulated voltages are provided for program and erase operations, so that the device does not require a higher voltage V_{PP} power supply to perform those functions. The device can also be programmed in standard EPROM programmers. Access times as low as 100ns are offered for timing compatibility with the zero wait state requirements of high speed microprocessors. To eliminate bus contention, the HY29DS32x has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device is compatible with the JEDEC single-power-supply Flash command set standard. Commands are written to the command register using standard microprocessor write timings, from where they are routed to an internal state-machine that controls the erase and programming circuits.

Device programming is performed a byte/word at a time by executing the four-cycle Program Command write sequence. This initiates an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Faster programming times can be achieved by placing the HY29DS32x in the Unlock Bypass mode, which requires only two write cycles to program data instead of four.

The HY29DS32x's sector erase architecture allows any number of array sectors, in one or both banks, to be erased and reprogrammed without affecting the data contents of other sectors. Device erasure is initiated by executing the Erase Command sequence. This initiates an internal algorithm that automatically preprograms the sector before executing the erase operation. As during programming cycles, the device automatically times the erase pulse widths and verifies proper cell margin. Hardware Sector Group Protection optionally disables both program and erase operations in any combination of the sector groups, while Temporary Sector Group Unprotect, which requires a high voltage on one pin, allows in-system erasure and code changes in previously protected sector groups. Erase Suspend enables the user to put erase on hold in a bank for any period of time to read data from or program data to any sector in that bank that is not selected for erasure. True background erase can thus be achieved. Because the HY29DS32x features simultaneous read/write capability, there is no need to suspend to read from a sector located within a bank that does not contain sectors marked for erasure. The device is fully erased when shipped from the factory.

Addresses and data needed for the programming and erase operations are internally latched during write cycles. The host system can detect completion of a program or erase operation by observing the RY/BY# pin or by reading the DQ[7] (Data# Polling) and DQ[6] (Toggle) status bits. Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions.

After a program or erase cycle has been completed, or after assertion of the RESET# pin (which terminates any operation in progress), the device is ready to read data or to accept another com

mand. Reading data out of the device is similar to reading from other Flash or EPROM devices.

The Secured Sector is an extra 64 Kbyte sector capable of being permanently locked at the factory or by customers. The Secured Indicator Bit (accessed via the Electronic ID mode) is permanently set to a 1 if the part is factory locked, and permanently set to a 0 if customer lockable. This way, customer lockable parts can never be used to replace a factory locked part. Factory locked parts provide several options. The Secured Sector may store a secure, random 16-byte ESN (Electronic Serial Number), customer code programmed at the factory, or both. Customer Lockable parts may utilize the Secured Sector as bonus space, reading and writing like any other Flash sector, or may permanently lock their own code there.
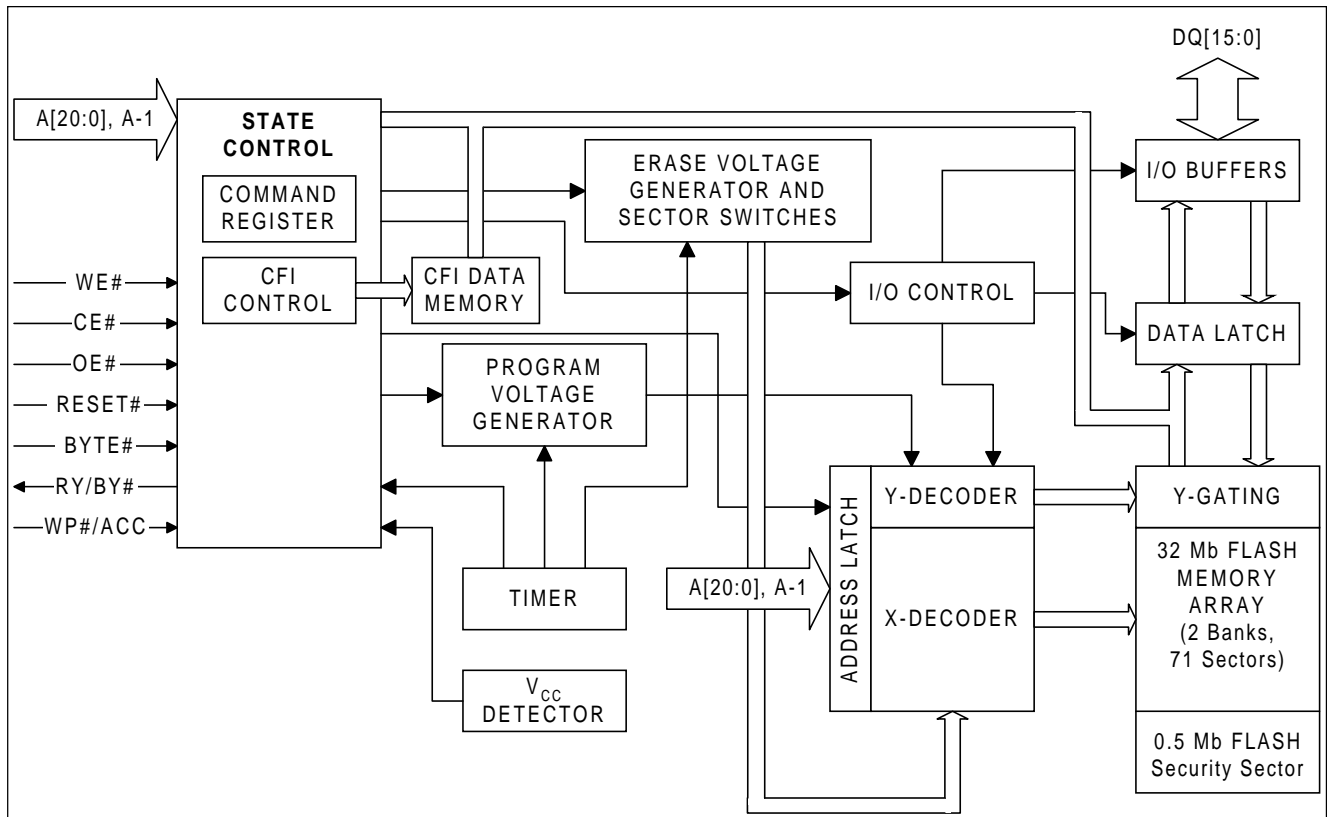
The WP#/ACC pin provides access to two functions. The Write Protect function provides a hardware method of protecting certain boot sectors without using a high voltage. The Accelerate function speeds up programming operations, and is intended primarily to allow faster manufacturing throughput.

Two power-saving features are embodied in the HY29DS32x. When addresses have been stable for a specified amount of time, the device enters the automatic sleep mode. The host can also place the device into the standby mode. Power consumption is greatly reduced in both these modes.

Common Flash Memory Interface (CFI)

To make Flash memories interchangeable and to encourage adoption of new Flash technologies, major Flash memory suppliers developed a flexible method of identifying Flash memory sizes and configurations in which all necessary Flash device parameters are stored directly on the device. Parameters stored include memory size, byte/word configuration, sector configuration, necessary voltages and timing information. This allows one set of software drivers to identify and use a variety of different, current and future Flash products. The standard which details the software interface necessary to access the device to identify it and to determine its characteristics is the Common Flash Memory Interface (CFI) Specification. The HY29DS32x is fully compliant with this specification.
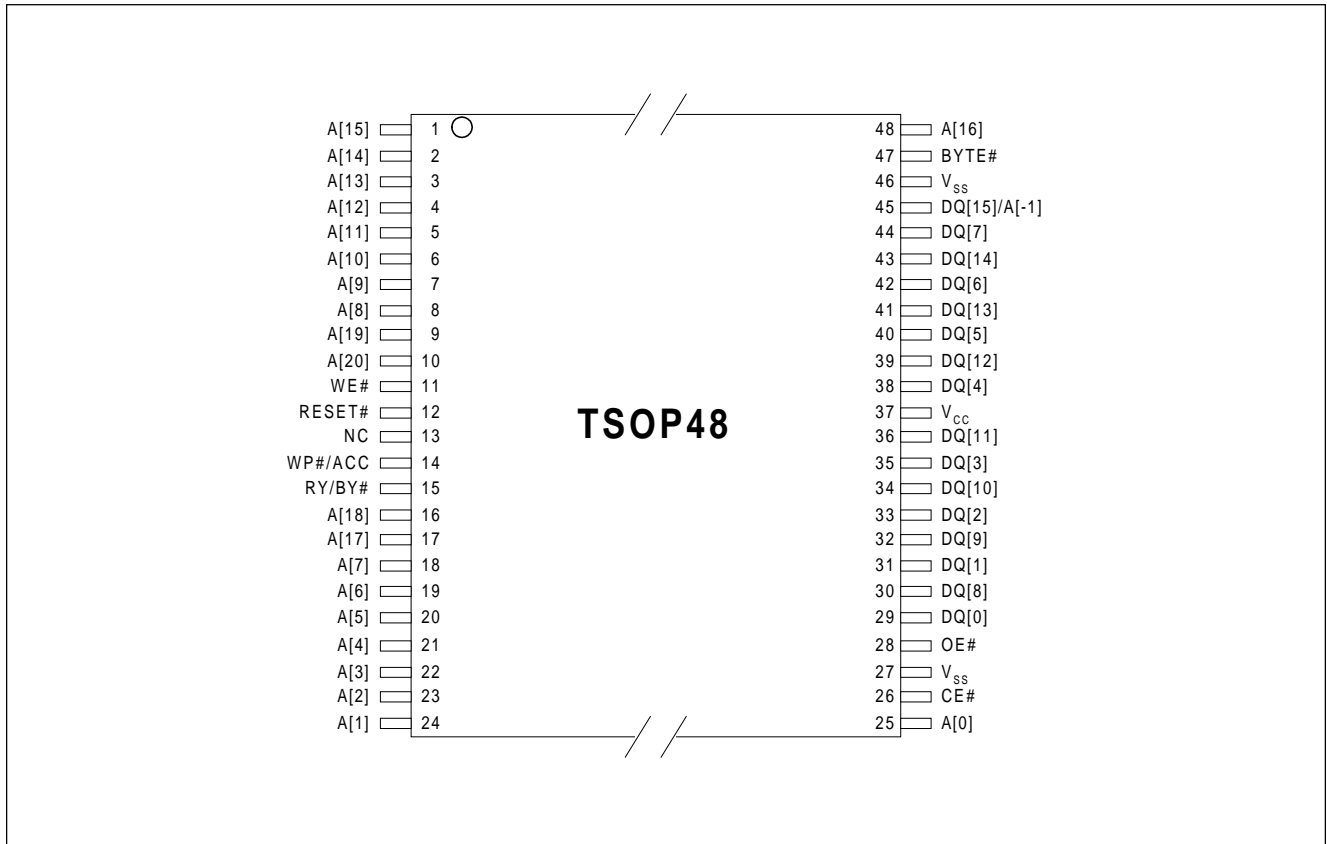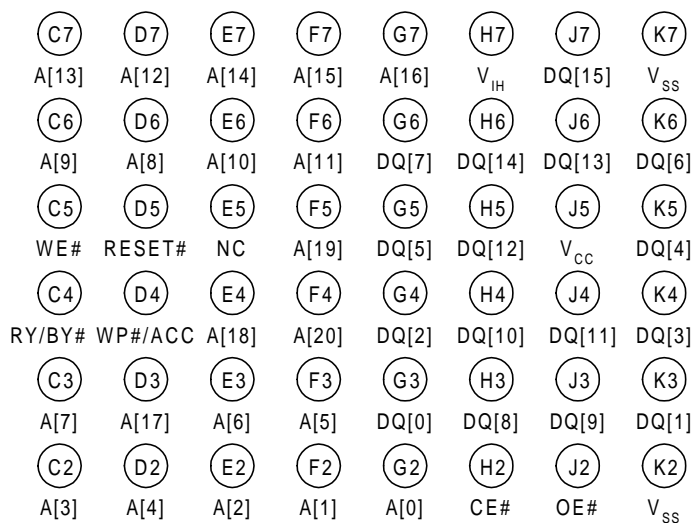
BLOCK DIAGRAM

SIGNAL DESCRIPTIONS

Name	Type	Description
A[20:0]	Inputs	**Address, active High.** In word mode, these 21 inputs select one of 2,097,152 (2M) words within the array for read or write operations. In byte mode, these inputs are combined with the DQ[15]/A[-1] input (LSB) to select one of 4,194,304 (4M) bytes within the array for read or write operations.
DQ[15]/A[-1], DQ[14:0]	Inputs/Outputs Tri-state	**Data Bus, active High**. In word mode, these pins provide a 16-bit data path for read and write operations. In byte mode, DQ[7:0] provide an 8-bit data path and DQ[15]/A[-1] is used as the LSB of the 22-bit byte address input. DQ[14:8] are unused and remain tri-stated in byte mode..
BYTE#	Input	**Byte Mode, active Low.** Low selects byte mode, High selects word mode.
CE#	Input	**Chip Enable, active Low.** This input must be asserted to read data from or write data to the HY29DS32x. When High, the data bus is tri-stated and the device is placed in the Standby mode.
OE#	Input	**Output Enable, active Low**. This input must be asserted for read operations and negated for write operations. When High, data outputs from the device are disabled and the data bus pins are placed in the high impedance state.
WE#	Input	**Write Enable, active Low.** Controls writing of commands or command sequences for various device operations. A write operation takes place when WE# is asserted while CE# is also Low and OE# is High.
RESET#	Input	**Hardware Reset, active Low.** Provides a hardware method of resetting the HY29DS32x to the read array state. When the device is reset, it immediately terminates any operation in progress. The data bus is tri-stated and all read/write commands are ignored while the input is asserted. While RESET# is asserted the device will be in the Standby mode.
RY/BY#	Output Open Drain	**Ready/Busy Status.** Indicates whether a write or erase command is in progress or has been completed. Valid after the rising edge of the final WE# pulse of a command sequence. Remains Low while the device is actively programming data or erasing, and goes High when it is ready to read array data.
WP#/ACC	Input	**Write Protect, active Low/Accelerate (V_{HH}).** Write Protect Function: Placing this pin at V_{IL} disables program and erase operations in two of the eight 8 KByte boot sectors. The affected sectors are sectors S0 and S1 in a bottom-boot device, or S69 and S70 in a top-boot device. If the pin is placed at V_{IH}, the protection state of those two sectors reverts to whether they were last set to be protected or unprotected using the Sector Group Protection and Unprotection capability of the HY29DS32x. Accelerate Function: If V_{HH} is applied to this input, the device enters the Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. (The system would then use the two-cycle program command sequence as required by the Unlock Bypass mode.) Removing V_{HH} from the pin returns the device to normal operation. This pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. Leaving the pin floating or unconnected may result in inconsistent device operation.
V_{CC}	--	**2-volt power supply.**
V_{SS}	--	**Power and signal ground.**

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PIN CONFIGURATIONS

A[15]	1		48	A[16]
A[14]	2		47	BYTE#
A[13]	3		46	V_{SS}

A[15] 1 — 48 A[16]
A[14] 2 — 47 BYTE#
A[13] 3 — 46 V$_{SS}$
A[12] 4 — 45 DQ[15]/A[-1]
A[11] 5 — 44 DQ[7]
A[10] 6 — 43 DQ[14]
A[9] 7 — 42 DQ[6]
A[8] 8 — 41 DQ[13]
A[19] 9 — 40 DQ[5]
A[20] 10 — 39 DQ[12]
WE# 11 — 38 DQ[4]
RESET# 12 — 37 V$_{CC}$
NC 13 — 36 DQ[11]
WP#/ACC 14 — 35 DQ[3]
RY/BY# 15 — 34 DQ[10]
A[18] 16 — 33 DQ[2]
A[17] 17 — 32 DQ[9]
A[7] 18 — 31 DQ[1]
A[6] 19 — 30 DQ[8]
A[5] 20 — 29 DQ[0]
A[4] 21 — 28 OE#
A[3] 22 — 27 V$_{SS}$
A[2] 23 — 26 CE#
A[1] 24 — 25 A[0]

TSOP48

48-Ball FBGA - Top View, Balls Facing Down

C7 A[13]	D7 A[12]	E7 A[14]	F7 A[15]	G7 A[16]	H7 V$_{IH}$	J7 DQ[15]	K7 V$_{SS}$
C6 A[9]	D6 A[8]	E6 A[10]	F6 A[11]	G6 DQ[7]	H6 DQ[14]	J6 DQ[13]	K6 DQ[6]
C5 WE#	D5 RESET#	E5 NC	F5 A[19]	G5 DQ[5]	H5 DQ[12]	J5 V$_{CC}$	K5 DQ[4]
C4 RY/BY#	D4 WP#/ACC	E4 A[18]	F4 A[20]	G4 DQ[2]	H4 DQ[10]	J4 DQ[11]	K4 DQ[3]
C3 A[7]	D3 A[17]	E3 A[6]	F3 A[5]	G3 DQ[0]	H3 DQ[8]	J3 DQ[9]	K3 DQ[1]
C2 A[3]	D2 A[4]	E2 A[2]	F2 A[1]	G2 A[0]	H2 CE#	J2 OE#	K2 V$_{SS}$

IMPORTANT NOTICE

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