MELPS740

MITSUBISHI SINGLE-CHIP
8 bit MICROCOMPUTERS

M37428M4-XXXFP

M37428M4-XXXFP SINGLE-CHIP 8-bit MICROCONTROLLER

PRELIMINARY SPECIFICATIONS

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Rev. D

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1.0 DESCRIPTION

The M37428M4-XXXFP is a single-chip microcomputer designed with high-speed CMOS silicon gate technology. It is housed in an 80-pin shrink plastic molded quad flat package. The M37428RFS is an EPROM mounted-type (piggyback version) microcomputer designed to simplify program development. The piggyback is ideal for prototype development.

This microcontroller's internal architecture and instruction set makes it ideal for business and office automation equipment. In addition to its simple instruction set, the ROM, RAM and I/O addresses are placed on the same memory map to enable easy programming.

This microcontroller is also suitable for applications which require control of LCD panels. The difference between the M37428M4-XXXFP and M37428RFS is that the piggyback version has no built-in ROM. The M37428RFS is used for development purposes.

2.0 DISTINCTIVE FEATURES

- CPU: Compatible with MELPS740 CPU (8MHz)
- Number of basic instructions 69
- ROM ..... 8K bytes
- RAM ..... 384 bytes
- Instruction execution time
  (shortest instruction at 8MHz) ..... 1μsec.
- Power dissipation
  normal operation mode (at 8MHz) ..... 15mW(Vcc=5V, Typ.)
  low speed operation mode (at 32KHz) ..... 225μW(Vcc=5V, Typ.)
  55μW(Vcc=3V, Typ.)
  stop mode (at 25°C) ..... 5μW(Vcc=5V, Max.)
- RAM retention voltage (stop mode) ..... 2.0V≤Vram≤5.5V
- Subroutine nesting ..... 96(max.)
- Interrupt ..... 10 types, 5 vectors
- Single power supply
  f(Xin)=8MHz ..... 5V±10%
  f(Xcin)=32KHz ..... 2.8V≤Vcc≤5.5V(Typ.)
- Timers
  8-bit timers with prescalers and reload latches 2
  8-bit timer with reload latches 3
- UART with Baud Rate Generator (8-bit) 1
- Programmable I/O Ports
  (Port P0, P1, P2, P3) 32
- Input Ports
  (Port P4) 8
- LCD controller/driver (1/2, 1/3 bias, 1/2, 1/3, 1/4 duty)
  segment output 32
  common output 4
- Process Technology ..... High-speed silicon gate CMOS
- Package ..... 80P6N QFP

Figure 2.1 M37428M4-XXXFP Pin Outline

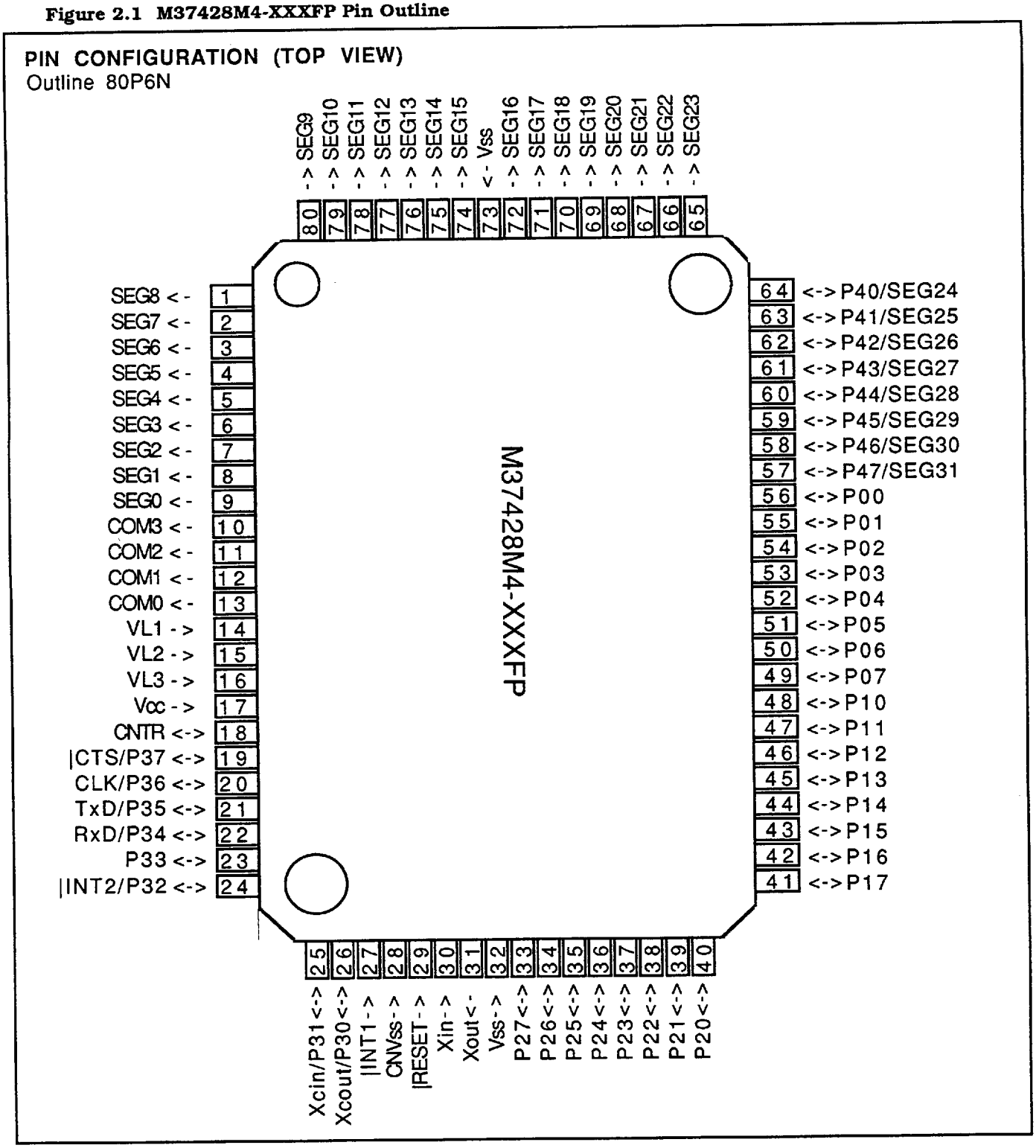


Figure 2.2 M37428RFS Pin Outline

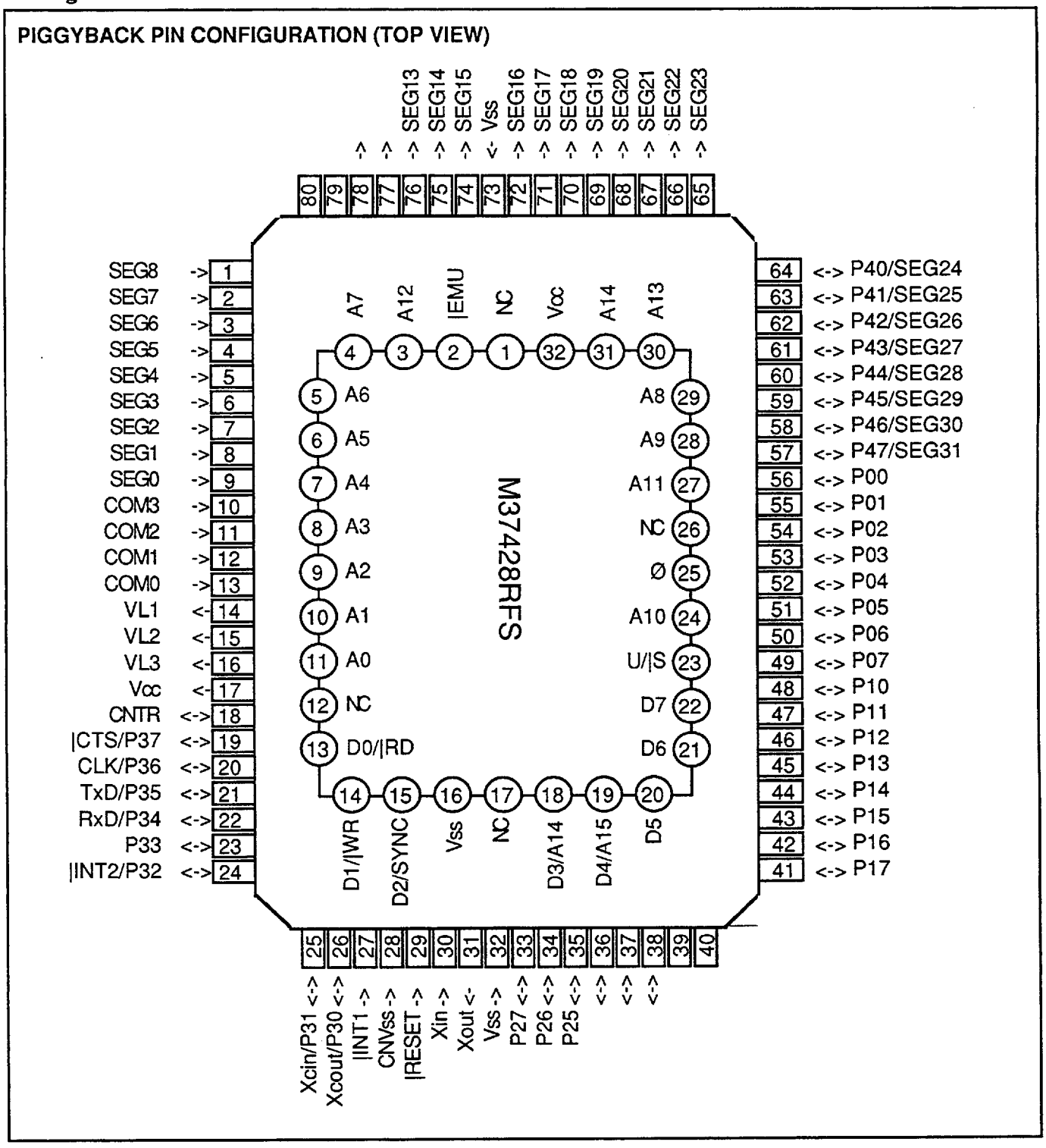
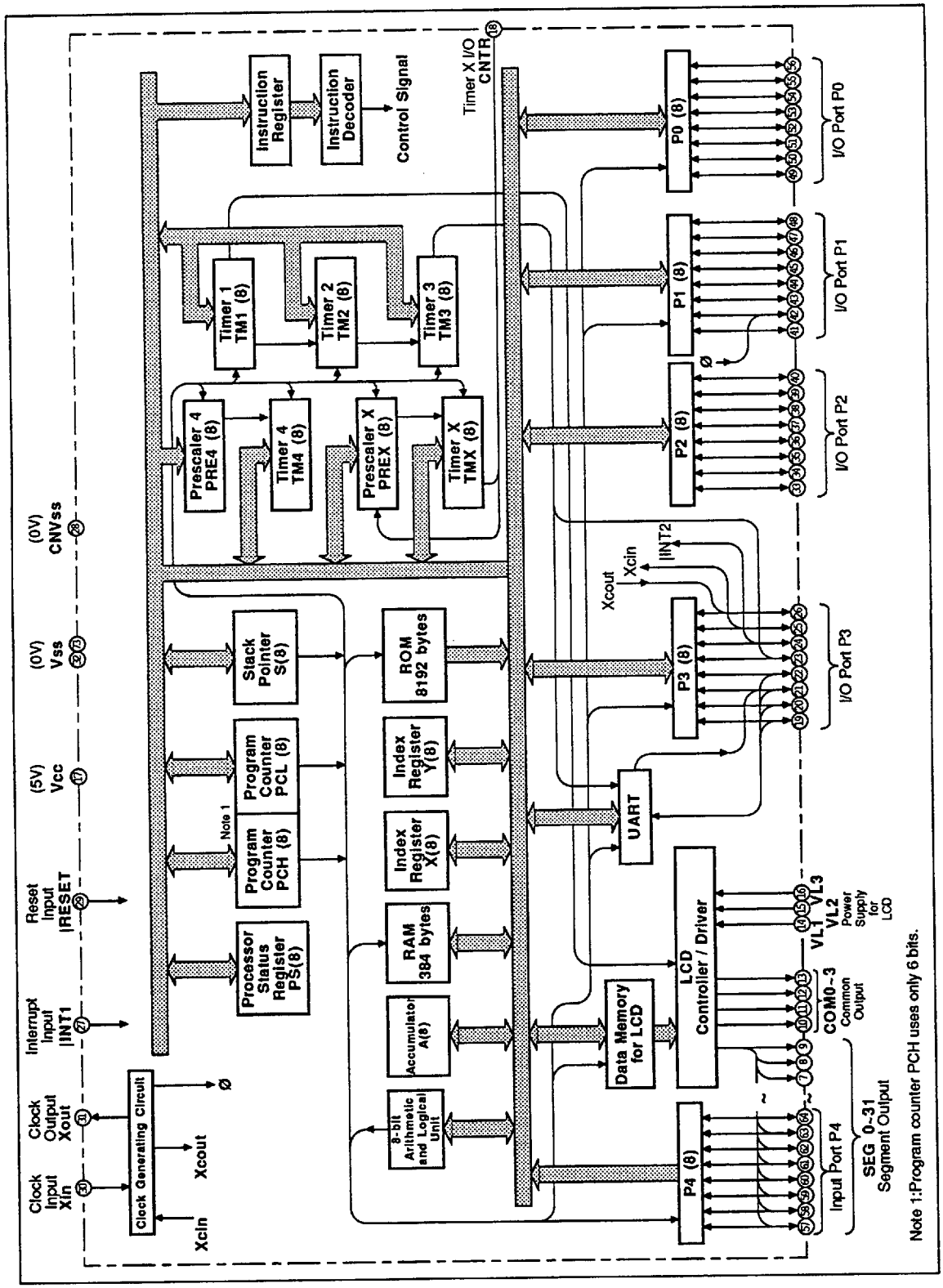


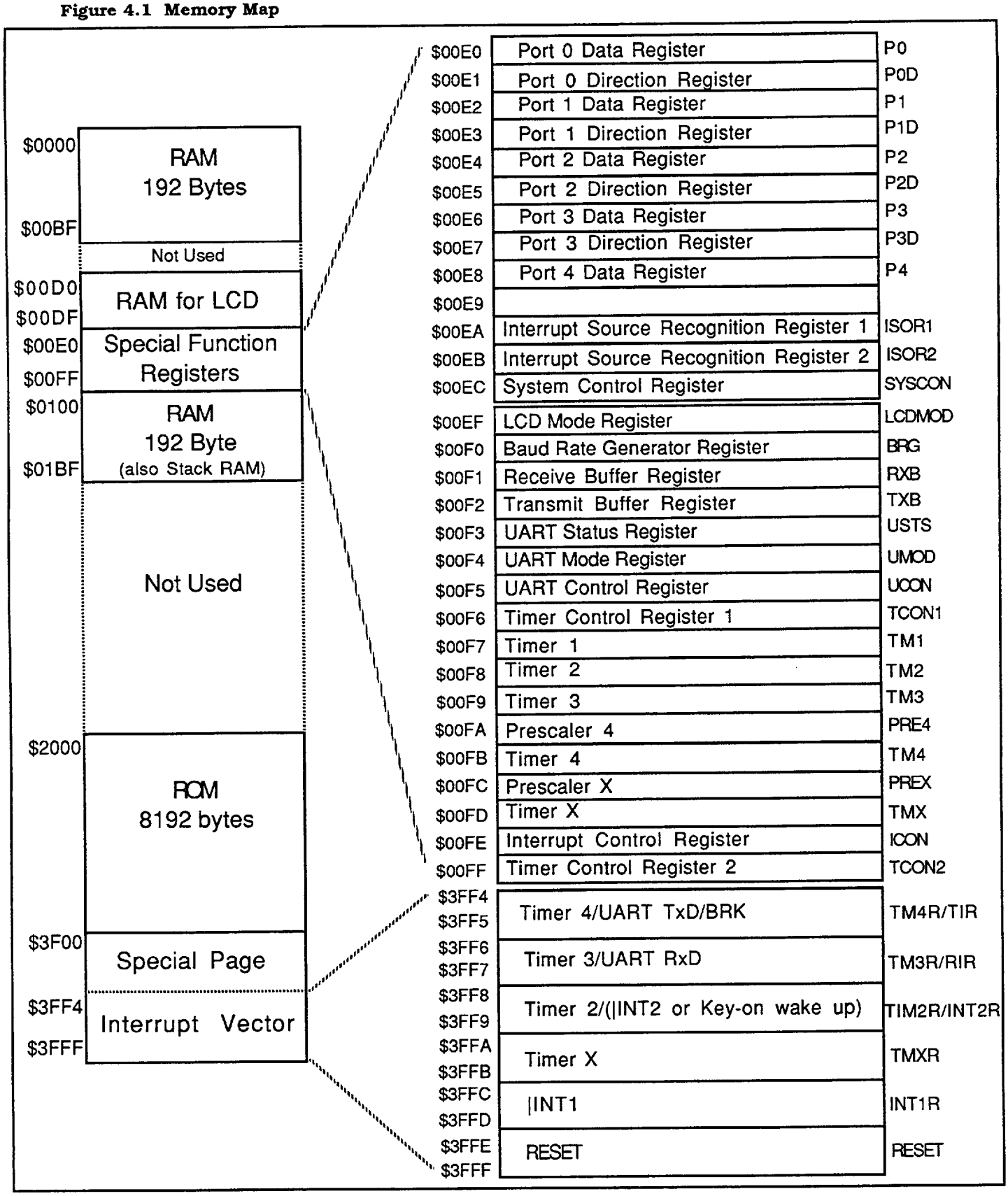
Figure 2.3 M37428M4 Block Diagram



3.0 PIN DESCRIPTION

Pin	Name	Input/ Output	Function
Vcc Vss	Power supply	---	Connect Vcc to 5V±10%. Connect Vss to 0V.
CNVss	CNVss input	Input	Connect to 0V to ensure proper operation in the single-chip mode.
¦RESET	RESET input	Input	To reset the CPU, keep the RESET input terminal low for at least 2µsec under normal Vcc conditions.
Xin	Clock input	Input	Connect a ceramic or crystal oscillator between Xin and Xout for clock oscillation. If an external clock input is used, connect the clock input to the Xin pin and leave the Xout pin opened.
Xout	Clock output	Output	
¦INT1	Interrupt Input	Input	This is the highest priority interrupt input pin (except for RESET).
P0.0~P0.7	I/O Port P0	Input/ Output	Port P0 is an 8-bit I/O port with directional registers allowing each bit to be individually programmed as input or output. At reset, this port is set as input. The I/O port structure is CMOS compatible.
P1.0~P1.7	I/O Port P1	Input/ Output	Port P1 is an 8-bit I/O port with the same function as Port P0.
P2.0~P2.7	I/O Port P2	Input/ Output	Port P2 is an 8-bit I/O port with the same function as Port P0. It can also be used as input pins for key-on wake up.The output is CMOS compatible.
P3.0~P3.7	I/O Port P3	Input/ Output	Port P3 is an 8-bit I/O port with the same function as Port P0. P34, P35, P36 and P37 can operate as RxD, TxD, CLK and ¦CTS, respectively, for the UART function. P32 can be set to work as an external interrupt input pin ¦INT2. P31 and P30 can function as Xcin and Xcout, respectively, which are the input pins for the low-power dissipation mode clock.
P4.0~P4.7	I/O Port P4	Input/ Output	Port P4 is an 8-bit input port which can operate as the LCD segment output pins SEG24~SEG31.
VL1~VL3	Supply Voltage for LCD	Input	For LCD operation, these pins must be connected to power such that 0V≤VL1≤VL2≤VL3≤Vcc.
COM0~ COM3	Common Output	Output	These are LCD common output pins. At 1/2 duty, COM2 and COM3 are not used. At 1/3 duty, COM3 is not used. See table 9.2.
SEG0~ SEG31	Segment Output	Output	These are LCD segment output pins.
CNTR	Counter I/O	Input/ Output	This pin is used together with timer X for event counter, pulse output or PWM mode.

Figure 4.1 Memory Map



4.0 MEMORY MAP

A memory map for M37428 is shown in Figure 4.1.

Addresses $2000 to $3FFF are assigned to the built-in ROM which consists of 8192 bytes. In the piggyback version this ROM does not exist internally. Instead an EPROM can be attached externally. Addressess $3F00 to $3FFF are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addresses $3FF4 to $3FFF are vector addresses used for the reset and interrupts (see section 10.0 INTERRUPTS). Addresses $00 to $FF are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing modes will greatly reduce the program code size. A total of 384 bytes of RAM are built-in as two separate blocks. The first block of 192 bytes is located between addresses $00 and $BF, and the second block is located between addresses $100 and $1BF. In addition to data storage the second block is also used for the stack during subroutine calls and interrupts. The stack must always be located within the second RAM block between addresses $100~$1BF. Refer to section 6.4 for more details on the use of the stack.

The special function registers (SFRs) for I/O ports and other peripheral control are located within the zero page from address $E0 to $FF. Registers $E9, $ED and $EE are reserved for possible future expansion and can not be used. A complete SFR memory map is included in Figure 4.1. The SPECIAL FUNCTION REGISTER BIT STRUCTURE section gives a detailed description of each bit located whithin the SFRs, except for the I/O ports registers which are explained in the INPUT/OUTPUT PORTS section.

5.0 PROCESSOR MODES

The M37428 microcontroller operates in the single-chip mode. To insure proper operation the CNVss pin should be connected to Vss and bits PMOD1 and PMOD0 located in the Timer Control Register 2 (TCON2 at address $FF) must always be equal to '00'.

The memory map for M37428M4 is the same as the one shown in Figure 4.1.

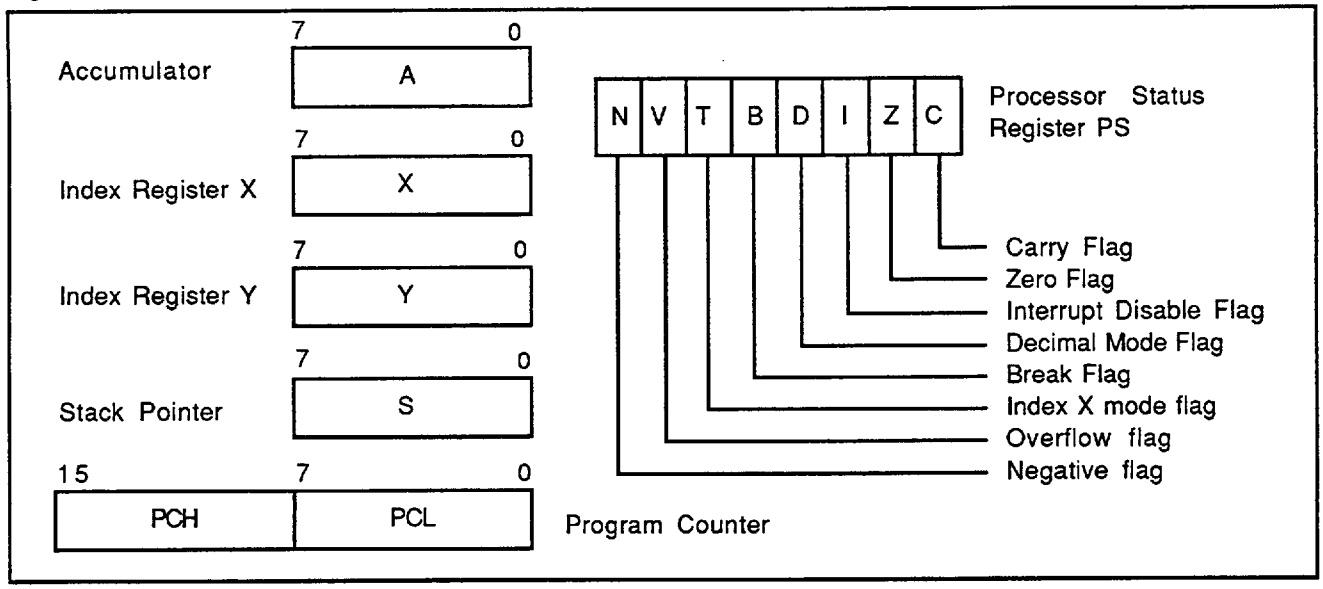
6.0 CENTRAL PROCESSING UNIT (CPU)

Six main registers are built into the CPU of the M37428.

The program counter (PC) has a 16-bit configuration but the other five registers: the accumulator (A), index register X (X), index register Y (Y), stack pointer (S) and processor status register (PS), all have an 8-bit configuration.

Except for the I flag, the contents of these registers are indeterminate after a hardware reset. Therefore, initialization is required with some programs. Upon hardware reset the I flag is automatically set to "1".

Figure 6.1 Register Configuration



6.1 Accumulator (A)

The accumulator is the central register of the microcomputer and has an 8-bit configuration. Data operations such as data transfers, Input/Output, etc., are executed mainly through the accumulator.

6.2 Index Register X (X), Index Register Y (Y)

The M37428 has an index register X and an index register Y, both of which have an 8-bit configuration.

In the addressing modes which use these index registers, the actual address is formed by adding the index register contents to the specified address. These modes are extremely effective for referencing subroutine tables and memory tables.

The index registers also have increment, decrement, compare and data transfer functions allowing them to be used as simple accumulators.

6.3 Stack Pointer (S)

The stack pointer is an 8-bit register which contains the address of the top of the stack. It is mostly used during interrupts and subroutines calls. The stack pointer is not automatically initialized after reset and should be initialized at the beginning of the program using the TXS instruction. The stack will always be located in the RAM between addresses $0100~$01BF. The higher address byte "$01" is hardware set and never changes. The user must load the lowest byte into the 8-bit stack pointer to decide the bottom of the

stack. This lowest byte must be between $00~$BF, such that the stack is always located between addresses $100~$1BF. When an interrupt occurs the program counter and the processor status register are pushed onto the stack. When the return from interrupt instruction (RTI) is executed the processor status register and the program counter are popped off the stack. During a subroutine call only the program counter is pushed onto the stack automatically.

When an interrupt is received, the following procedure is performed automatically in the following sequence :

(1) The contents of the higher 8 bits of the program counter (PCH) are saved to an address determined by using the value $01 for the higher 8 bits and the stack pointer contents for the lower 8 bits.
(2) The stack pointer contents are decremented by 1.
(3) The contents of the lower 8 bits of the program counter (PCL) are saved to an address determined by using the value $01 for the higher 8 bits and the stack pointer contents for the lower 8 bits.
(4) The stack pointer contents are decremented by 1.
(5) The contents of the processor status register (PS) are saved to an address determined by using the value $01 for the higher 8 bits and the stack pointer contents for the lower 8 bits.
(6) The stack pointer contents are decremented by 1.

Before performing a subroutine call only the first 4 steps mentioned above are automatically executed. The PHP instruction can be used to compensate for steps (5) and (6).
To prevent data loss during interrupt servicing and subroutine calls, it is recommended to save the other registers onto the stack as well. For example, the PHA instruction is executed to store the contents of the accumulator onto the stack. Executing the PHA instruction saves the accumulator contents to an address determined by using the value $01 for the higher 8 bits and the stack pointer contents for the lower 8 bits, after which the stack pointer contents are decremented by 1.

The RTI instruction is executed to return from an interrupt routine. When the RTI instruction is executed, the following steps are automatically executed:

(1) The stack pointer contents are incremented by 1.
(2) The contents at the address specified by using $01 as the higher 8 bits and the stack pointer contents as the lower 8 bits are returned to the processor status register.
(3) The stack pointer contents are incremented by 1.
(4) The contents at the address specified by using $01 as the higher 8 bits and the stack pointer contents as the higher 8 bits are returned to the lower 8 bits of the program counter (PCL)
(5) The stack pointer contents are incremented by 1.
(6) The contents at the address specified by using $01 as the higher 8 bits and the stack pointer contents as the higher 8 bits are returned to the lower 8 bits of the program counter (PCH).

Steps (1) and (2) above are not executed when returning from a subroutine. Returning from a subroutine is done with the RTS instruction.

The processor status register is popped by the PLP instruction and the accumulator is popped by the PLA instruction. Executing the PLP (PLA) instruction increments the stack pointer by 1 and returns the contents at the address specified by using $01 as the higher 8 bits and the stack pointer contents as the lower 8 bits to the processor status register (accumulator).
Saving data in the stack area gradually fills the RAM area with saved data. Therefore, caution must be taken concerning the number of interrupt levels and subroutine nesting.

6.4 Program Counter (PC)

The program counter is a 16-bit counter consisting of two 8-bit registers PCH and PCL. The program counter indicates the address of the next instruction to be executed.

6.5.0 Processor Status Register (PS)

The processor status register is an 8-bit register consisting entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the carry flag (C), zero flag (Z), overflow flag (V) or the negative flag (N). Each of these flags is described below. Refer to the "Series MELPS 740 Programming Manual" for instructions which alter these flags.

6.5.1 Carry Flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic and Logical Operation Unit (ALU) immediately after an operation. It can also be changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

6.5.2 Zero Flag (Z)

This flag is used to indicate if the previous operation generated a zero result or not. If the result is zero, the zero flag will be set to "1". If the result is not zero, the zero flag will be set to "0".

6.5.3 Interrupt Disable Flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt occurs, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

6.5.4 Decimal Mode Flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal; if the flag is set to "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

6.5.5 Break Flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag pushed onto the stack can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, bit 4 of SP+1 (break flag in the PS on the stack) will be "1", otherwise it will be "0". The break flag in the actual PS will remain a "0".

6.5.6 Index X Mode Flag (T)

When the T flag is "1", operations between the memories are executed directly without passing through the accumulator. Operations between memories through the accumulator are executed when the T flag is "0". The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the index X mode flag, respectively.

T=0	Acc <- Acc*M2	*	= operation
		Acc	= accumulator
		M2	= memory addressed by operation addressing
T=1	M1 <- M1*M2	*	= operation
		M1	= zero page memory addressed by index register X
		M2	= memory addressed by operation addressing

6.5.7 Overflow Flag (V)

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or -128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the overflow flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

6.5.8 Negative Flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit7 is set to "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the negative flag. There are no instructions for directly setting or resetting the negative flag.

7.0 TIMERS

The M37428 has 5 timers: Timer 1, 2, 3, 4, and Timer X.

Timer 1, 2 and 3 are 8-bit timers with reload latches. Timer 4 is an 8-bit timer with an 8-bit prescaler and reload latches. Timer X is the same as timer 4 and it can operate in four different modes. The input clock source frequency can be selected between Xin or Xcin individually for each timer. Each timer has its own stop bit which enables controlling the exact time when the timer starts or stops counting.

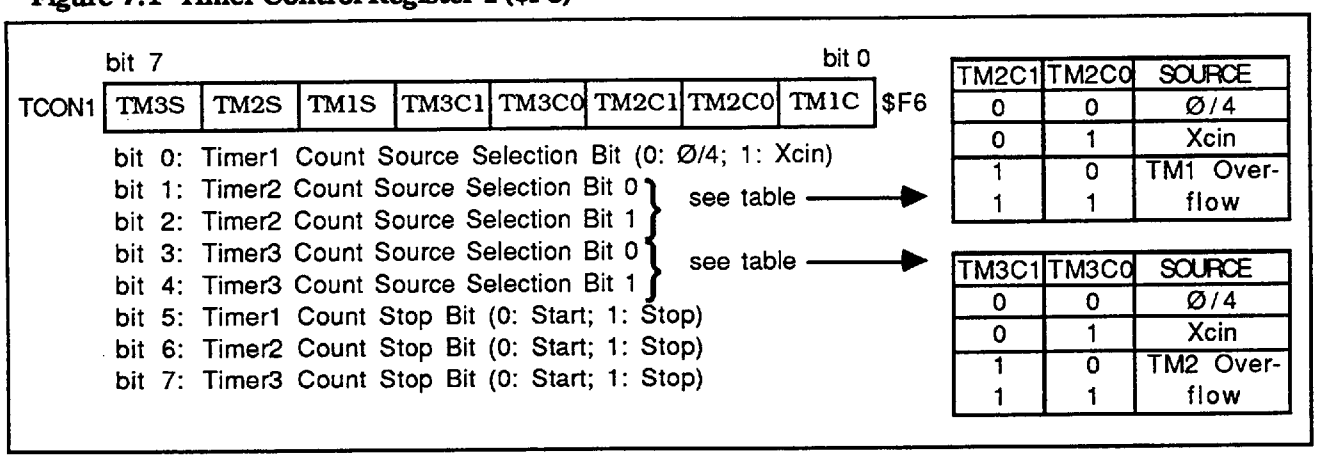
When the timer 2, 3, 4 or X contents reach 0, a timer interrupt is generated. The reload action is performed during the next Ø cycle. For all the timers and the prescalers the counting ratio is [1/(n+1)], where n is the value loaded in the timer or prescaler (n=0~255). Timer 2, 3 and 4 interrupts share the same interrupt vector address as INT2, UART RxD and UART TxD, respectively. Please refer to the INTERRUPT section for a detailed description about using these interrupts.

Timer 1 is used for generating the LCD clock frequency and can not create an interrupt. However, timer 1, 2 and 3 can be cascaded to create a larger divide value. The Timer Control Register 1 (TCON1) located at address $F6 contains the clock source selection bits and the stop bits for timers 1, 2 and 3. By manipulating these bits it is possible to operate each one of timers 1, 2 or 3 either individually or cascaded. The timer block diagram in Figure 7.2 shows the configuration of all the timer control circuitry and indicates the bits to be changed for different timer operation. The control bits for timer 4 are located in LCDMOD register at address $EF and for timer X in TCON2 at address $FF.

After RESET the prescaler X and timer X are loaded with $FF and $01, respectively. Timer 1, 2, 3 and 4 are loaded with random values. During a STP instruction the timer contents will not change. The RESET CIRCUIT section includes a list of the states of the Special Function Register bits (SFRs) after RESET. This list shows that after RESET all timers are started and Xin is the main input clock source frequency. As seen in the Timer Block Diagram, Ø = Xin/4 and the actual timer count source is Ø/4, after RESET.

Timer 1, 2, 3 and 4 can only operate in timer mode which is the same as the timer X timer mode described below. Timer X can function in four different modes selected by TMOD1 and TMOD0, bits 3 and 2 of Timer Control Register 2 (TCON2 address $FF).

Figure 7.1 Timer Control Register 1 ($F6)



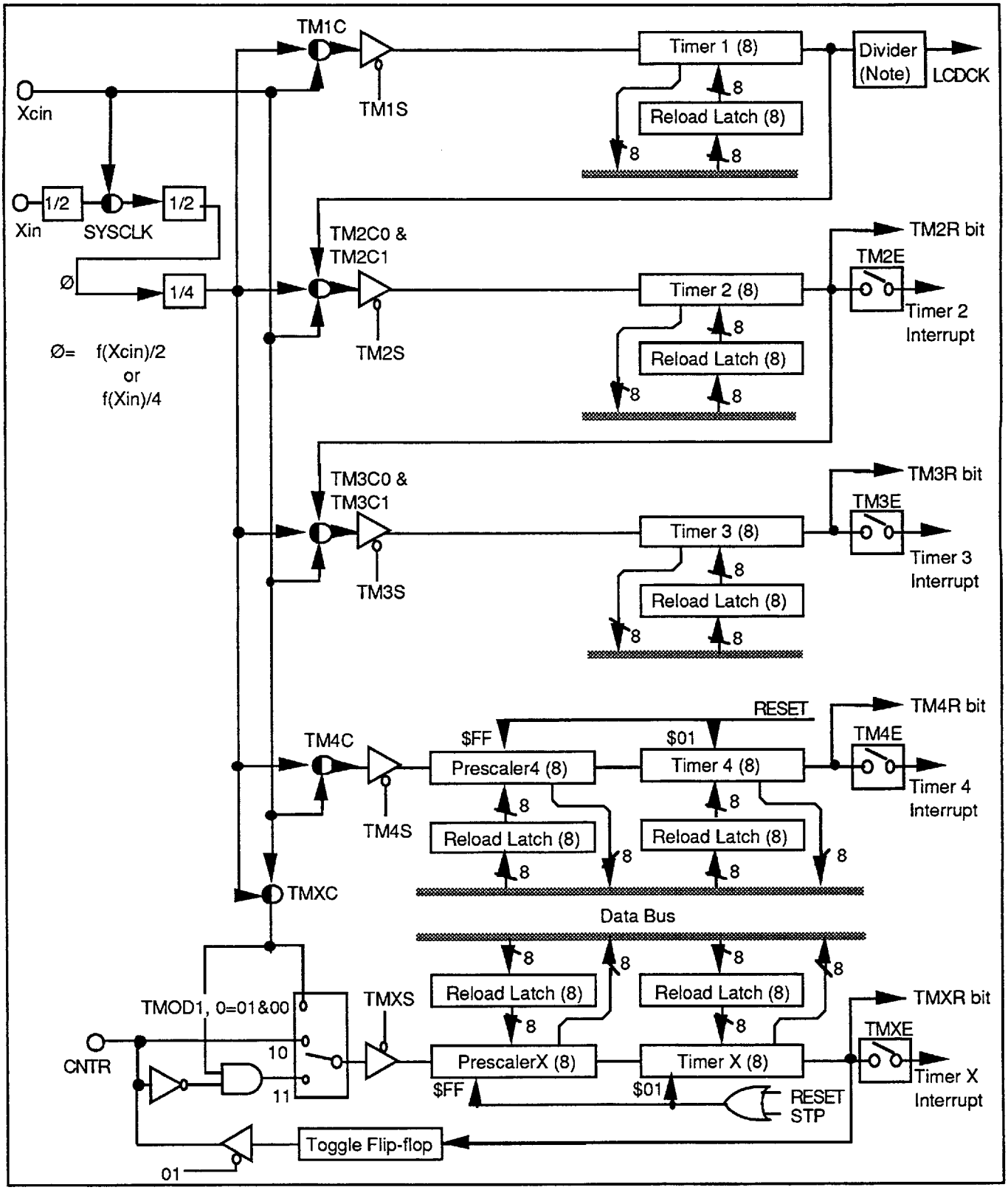
TM2C1	TM2C0	SOURCE
0	0	Ø/4
0	1	Xcin
1	0	TM1 Over-
1	1	flow

TM3C1	TM3C0	SOURCE
0	0	Ø/4
0	1	Xcin
1	0	TM2 Over-
1	1	flow

7.1 Timer Mode (TMOD1=0, TMOD0=0)

When bits 3 and 2 of TCON2 ($FF) are set to '00', timer X enters the timer mode. In this mode the timer counts down from the timer latch value. When the timer underflows, the timer interrupt request bit (TMXR of TCON2 $FF) is set to "1", the contents of the reload register are transferred to the timer and the cycle starts over again. In order for an interrupt to occur, the timer interrupt enable bit must be set to "1". The count source (Ø/4 or Xcin) can be selected with TMXC bit 4 of TCON2 (address $FF). A block diagram is shown in Figure 7.4

Figure 7.2 Timer Block Diagram



Note: The Divider is explained in detail in Figure 9.4 (LCD section)

Figure 7.3 Timer Control Register 2 ($FF)

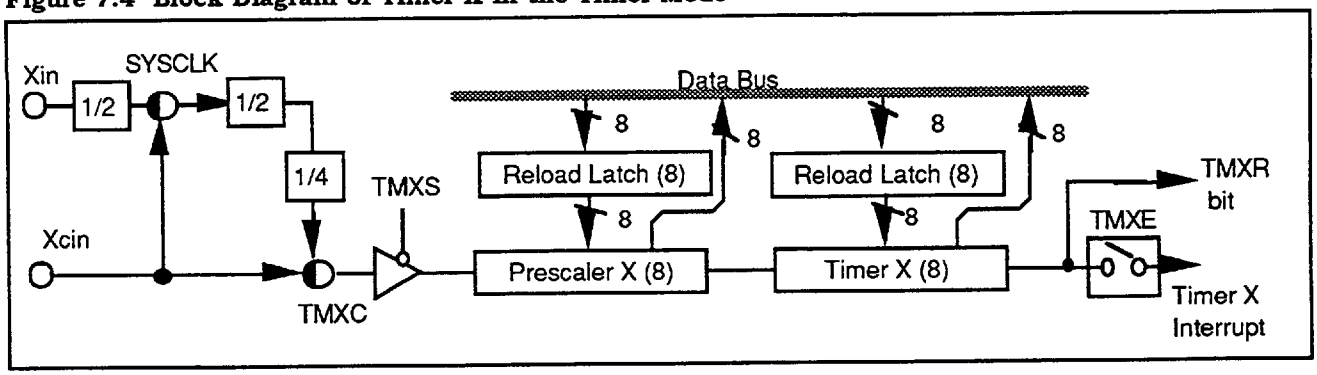
	bit 7							bit 0	
TCON2	TMXR	TMXE	TMXS	TMXC	TMOD1	TMOD0	PMOD1	PMOD0	$FF

bit 0: Processor Mode Bit 0
bit 1: Processor Mode Bit 1
bit 2: Timer X Mode Bit 0
bit 3: Timer X Mode Bit 1
bit 4: Timer X Count Source Selection Bit (0: Ø/4; 1: Xcin)
bit 5: Timer X Count Stop (0: Start; 1: Stop)
bit 6: Timer X Interrupt Enable (1: Enable)
bit 7: Timer X Interrupt Request (1: Request)

PMOD		Processor Mode
1	0	
0	0	Single-Chip Mode
Note: PMOD0 and PMOD1 must always be equal to "0".		

TMOD		Timer X Function Mode
1	0	
0	0	Timer Mode
0	1	Pulse Output Mode
1	0	Event Counter Mode
1	1	Pulse Width Measurement Mode

Figure 7.4 Block Diagram of Timer X in the Timer Mode



7.2 Event Counter Mode (TMOD1=1, TMOD0=0)

When bits 3 and 2 of TCON2 ($FF) are set to '1' and '0', respectively, timer X enters the event counter mode. This mode has the same function as the timer mode except that the count source is provided through the external CNTR pin. The maximum input frequency of the event clock source is 1MHz. Figure 7.5 represents the timer X block diagram in the event counter mode.

7.3 Pulse Output Mode (TMOD1=0, TMOD0=1)

When bits 3 and 2 of TCON2 ($FF) are set to '0' and '1', respectively, timer X enters the pulse output mode. In this mode the polarity of CNTR pin is inverted each time the timer counts down to zero. When timer x is written to, the CNTR pin is forced to '1' and pulse output mode continues. The count source can be selected with bit TMXC located within TCON2 ($FF). Figure 7.6 represents the timer X block diagram in the pulse output mode.

Figure 7.5 Block Diagram of Timer X in the Event Counter Mode

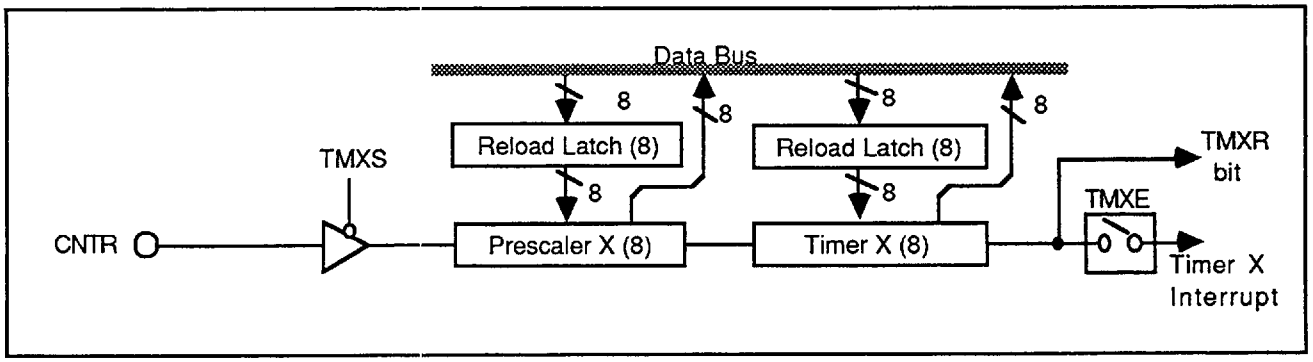
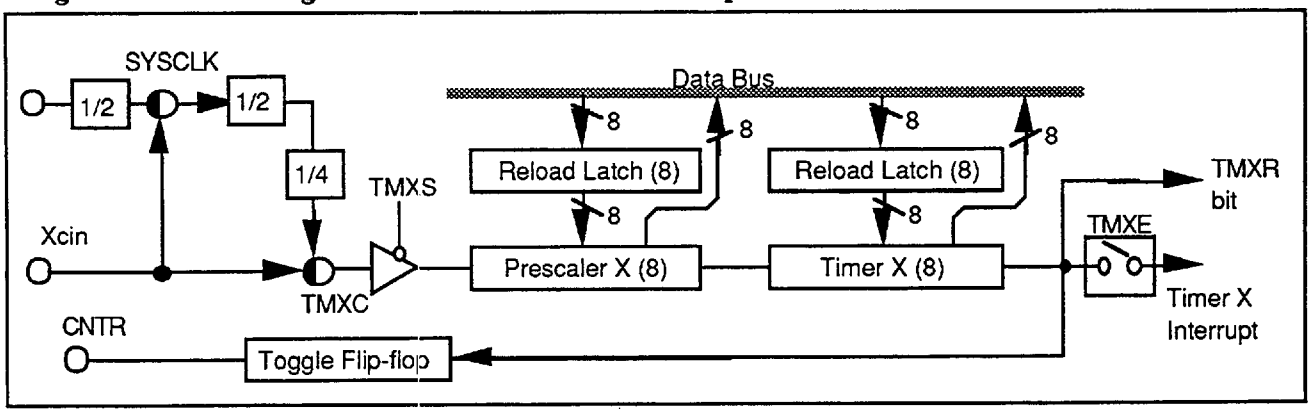


Figure 7.6 Block Diagram of Timer X in the Pulse Output Mode



7.4 Pulse Width Measurement Mode (TMOD1=1, TMOD0=1)

When bits 3 and 2 of TCON2 ($FF) are both set to '1', timer X enters the pulse width measurement mode PWM. This mode is used to measure the pulse width (low period) input to CNTR pin. The count source can be selected with bit TMXC of TCON2 register ($FF). When the timer reaches zero, the timer X interrupt request bit is set and the reload latch contents are transferred to the timer. Then the timer starts counting again while the input to the CNTR pin is low. Figure 7.7 shows the block diagram of timer X in PWM mode.

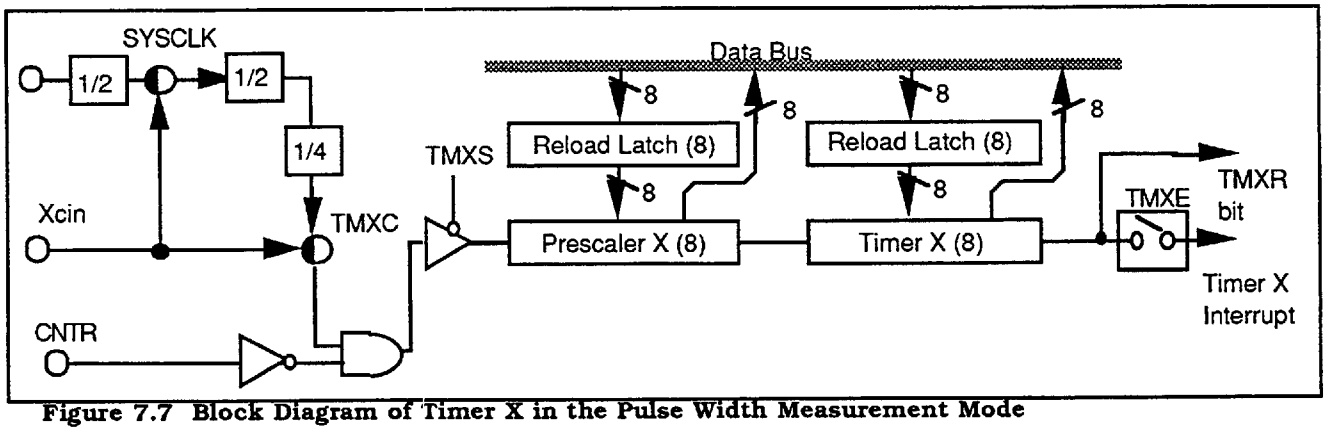


Figure 7.7 Block Diagram of Timer X in the Pulse Width Measurement Mode

8.0 UART

The M37428 contains an independent full-duplex UART (Universal Asynchronous Receiver/Transmitter). The UART contains its own Baud Rate Generator, as well as an interrupt request flag, interrupt control flag and interrupt vectors for both receive and transmit interrupts.
The UART has three external signals: RXD (Receiver Input), TXD (Transmitter Output) and |CTS (Clear To Send) which are multiplexed with P3.4, P3.5 and P3.7, respectively. The UART function is selected by setting bit 7 (UARTE) of UART Mode Register (UMOD at address $F4) to "1". There are six registers for control and data transfer: Baud Rate Generator Register (BRG at address $F0), Receiver Buffer Register (RXB $F1), Transmitter Buffer Register (TXB $F2), UART Status Register (USTS $F3), UART Mode Register (UMOD $F4) and UART Control Register (UCON $F5).There is also an external clock terminal CLK, multiplexed with port P3.6 which can be selected as the baud rate generator clock by setting bit 5 (EX) of the UART mode register (UMOD $F4) to "1".

Figure 8.1 UART Block Diagram

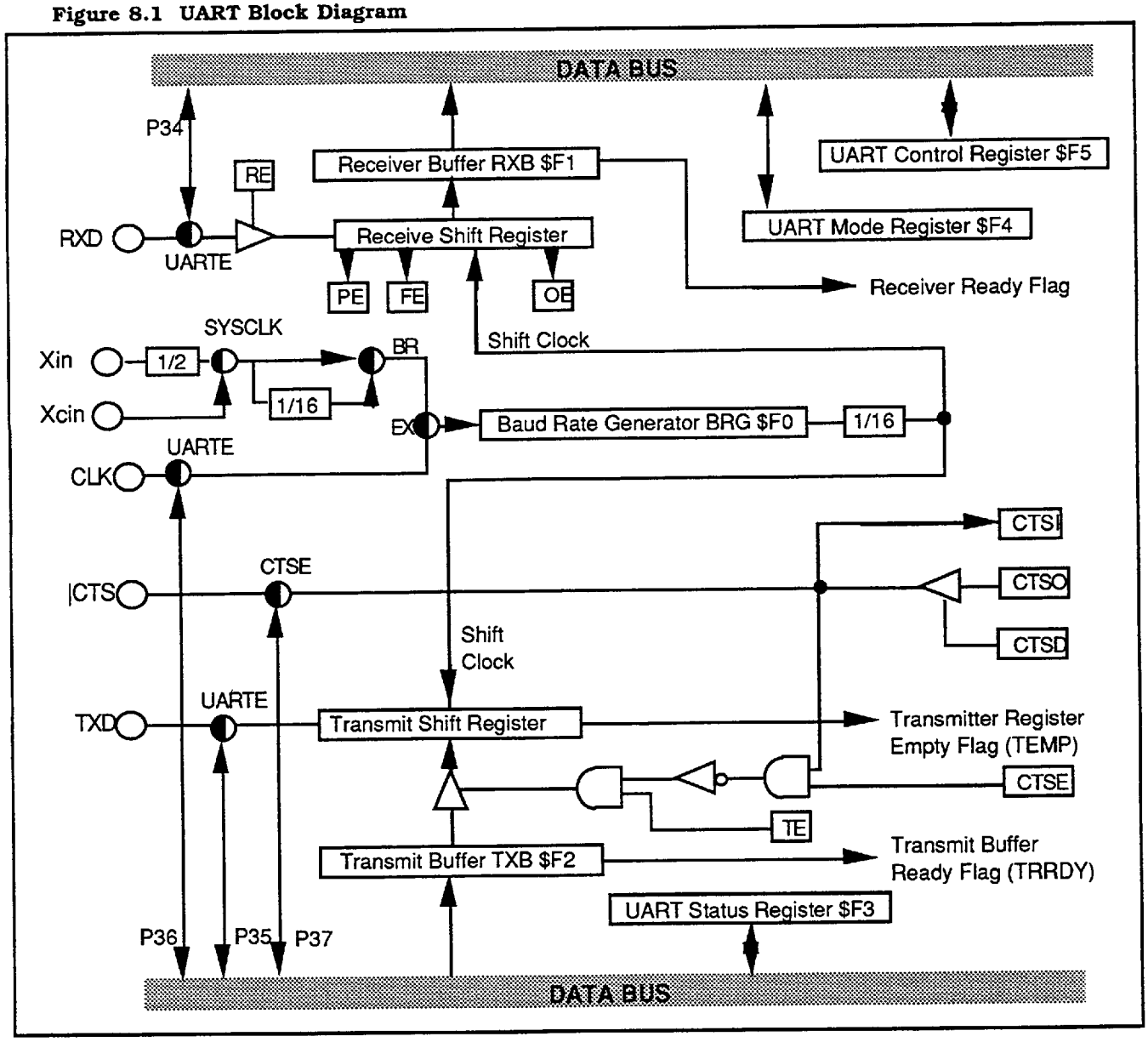


Figure 8.2 UART Special Function Registers: USTS, UMOD, UCON

UART Status Register ($F3)

	bit 7							bit 0	
USTS	CTSI	X	FE	OE	PE	TEMP	RRDY	TRRDY	$F3

bit 0: Transmitter Buffer Ready ("1" when TXB is empty and ready for another byte)
bit 1: Receiver Ready ("1" when the RXB has finished receiving a byte)
bit 2: Transmitter Register Empty ("1" when the transmitter shift register and TXB are empty)
bit 3: Parity Error ("1" when a parity error is detected in the received data)
bit 4: Overrun Error ("1" when a character is not finished being read from RXB before the next one becomes available)
bit 5: Framing Error ("1" when a valid stop bit is not detected)
bit 6: X : Not Used
bit 7: |CTS Input Status Bit (0: at "L" level; 1: at "H" level)

UART Mode Register ($F4)

	bit 7							bit 0	
UMOD	CTSD	UARTE	EX	BR	ST	CHL	EVN	PEN	$F4

bit 0: Parity Enable Bit (1: Enable)
bit 1: Even/Odd Parity Selection Bit (1: Even, 0: Odd)
bit 2: Character Length Selection (1: 8 bits; 0: 7 bits)
bit 3: Stop Bit Number Selection (1: 2 bits; 0: 1 bit)
bit 4: Baud Rate Oscillation Selection (1: 1/32; 0: 1/2)
bit 5: Baud Rate Clock Source Selection (1: External; 0: Internal)
bit 6: UART Enable (1: Enable; 0: Disable)
bit 7: |CTS Direction Selection (1: output; 0: input)

UART Control Register ($F5)

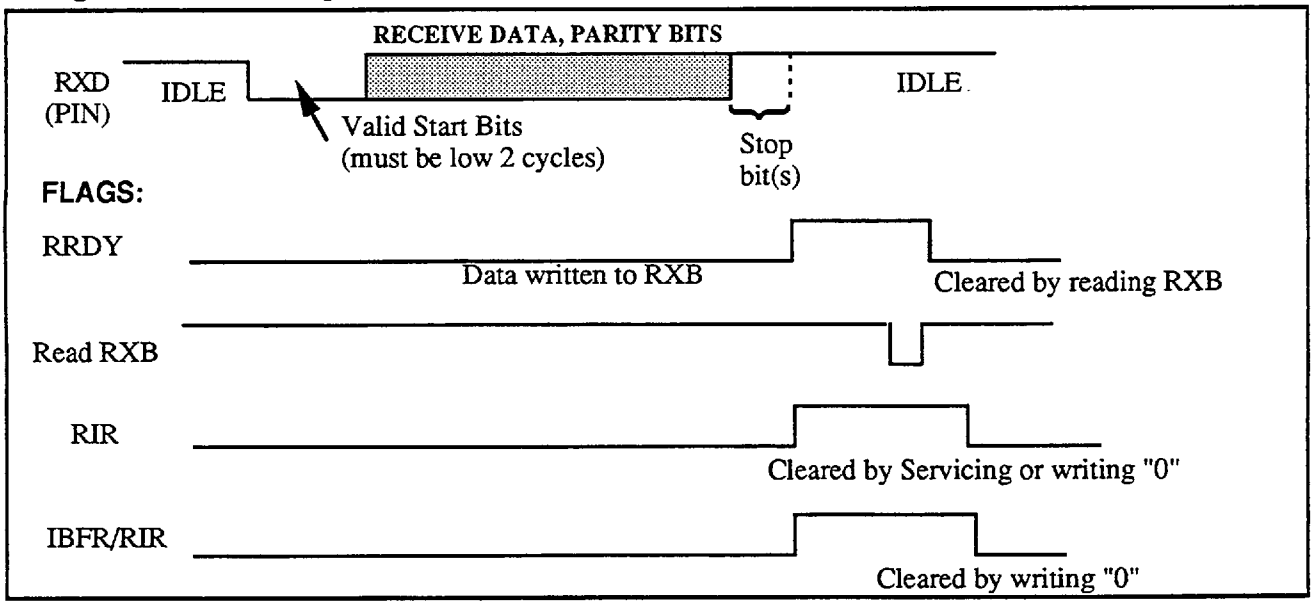
	bit 7							bit 0	
UCON	ERST	MR	CTSO	CTSE	RIE	RE	UTIE	TE	$F5

bit 0: Transmit Enable (1: Enable)
bit 1: UART Transmit Interrupt Enable (1: Enable)
bit 2: Receive Enable (1: Enable)
bit 3: Receive Interrupt Enable (1:Enable)
bit 4: |CTS Control Enable (1:Enable)
bit 5: |CTS Output Data Register
bit 6: Transmitter Master Reset (1: Enable; 0: Reset)
bit 7: Error Reset (1: Reset; 0: Invalid)

8.1. UART Receiver Operation

The UART receiver is equipped with a Receive Shift Register and a Receive Buffer (RXB $F1). Data is received through the RxD pin. When this pin is not receiving data the external signal must remain at a high level. In order to receive data, the receive enable bit (bit 2 RE of UCON $F5) must be set. The receiver samples RxD pin at an internal clock rate of 16 times the baud rate. When RxD goes low for two consecutive clock cycles, a valid start bit is assumed to be received. The UART samples the expected center of the start bit three times. If the samples are low at least twice then this is considered the start bit. If the samples are low only once or not at all, the receiver declares the start bit invalid and goes back to waiting for a start bit. The data bits, parity bit and one stop bit are sampled in the same manner, three times at the assumed center of each bit. If two or more samples are high, then the bit is assumed to be high. If two or more samples are low then the bit is assumed to be low. When the first stop bit is received, the received data is written from the shift register to the RXB. The UART Receiver uses only the first stop bit. The Receiver Ready Flag (bit 1 RRDY of USTS $F3) is set to indicate that RXB is full. (This flag is cleared when the data in RXB is read.)

Figure 8.3 Receive Operation



Based on the values of bits 0-3 of UMOD ($F4), the receiver operation can flag three different errors. The status of these errors is determined by reading bits 3-7 of USTS ($F3). If a parity error occurs, The Parity Error Flag (PE) is set. If the first stop bit is low, the Framing Error Flag (FE) is set; the second stop bit does not effect FE. If RXB has unread data and another stop bit is received into the shift register, the Overrun Error Flag (OE) is set and the unread data is written over. To reset any error flag a "1" must be written to the Error Reset Flag (bit 7 ERST of UCON $F5). ERST automatically reverts to "0". None of the errors effect the receiver operation.

When RXB is full (RRDY=1), the Receive Interrupt Request flag (bit 1 RIR) of the Interrupt Source Recognition Register 2 (ISOR2 $EB) is set. An interrupt will occur if the Receive Interrupt Enable flag (bit 3 RIE of UCON) and the Receive Interrupt Enable bit (TM3E/RIE) of the Interrupt Control Register (ICON $FE) are set, and the Interrupt Inhibit flag I in the Processor Status Register (PS) is clear. The Receive Interrupt Request flag (TM3R/RIR of ICON at $FE) can be cleared by servicing the interrupt or by writing "0" to this flag. However, the RIR flag (in ISOR2) can only be cleared by writing "0" to it. Further receive interrupts can be detected only after both of these flags have been cleared.

When the Receiver Enable Flag is set to "0" the receiver operation is reset. In this state RRDY is cleared and the receiver is idle. The receiver will not start searching for a start bit until RE is set to "1".

8.2 UART Transmitter Operation

The UART transmitter has a Transmit Buffer (TXB $F2) and a transmit shift register. Data is transferred through the TxD pin. When no data is being transmitted, TxD is held high. In order to transmit data, the transmit enable bit (bit 0 TE of UCON $F5) must be set. Transmit data is written to TXB. If the transmit shift register is empty, the data in TXB is read into the shift register along with the start bit, the stop bit and parity information. The Transmit Ready flag (bit 0 TRRDY of USTS $F3) is set and the shift register begins to shift data through the TxD pin. Please note that TRRDY=1 when TXB is empty and data can be written to it; TRRDY=0 when TXB is full and data cannot be written to it. The number of stop bits, character length, parity polarity, and parity enable information are read from bits 0-3 of the UART Mode Register (UMOD $F4). If new data is written to TXB during transmission, TRRDY is cleared, preventing further writes to TXB. Once transmission completes, the new data in TXB is read into the shift register and TRRDY set, allowing further writes to TXB.

Clearing the TE bit will have no effect on data that was already written to TXB while TE was set.

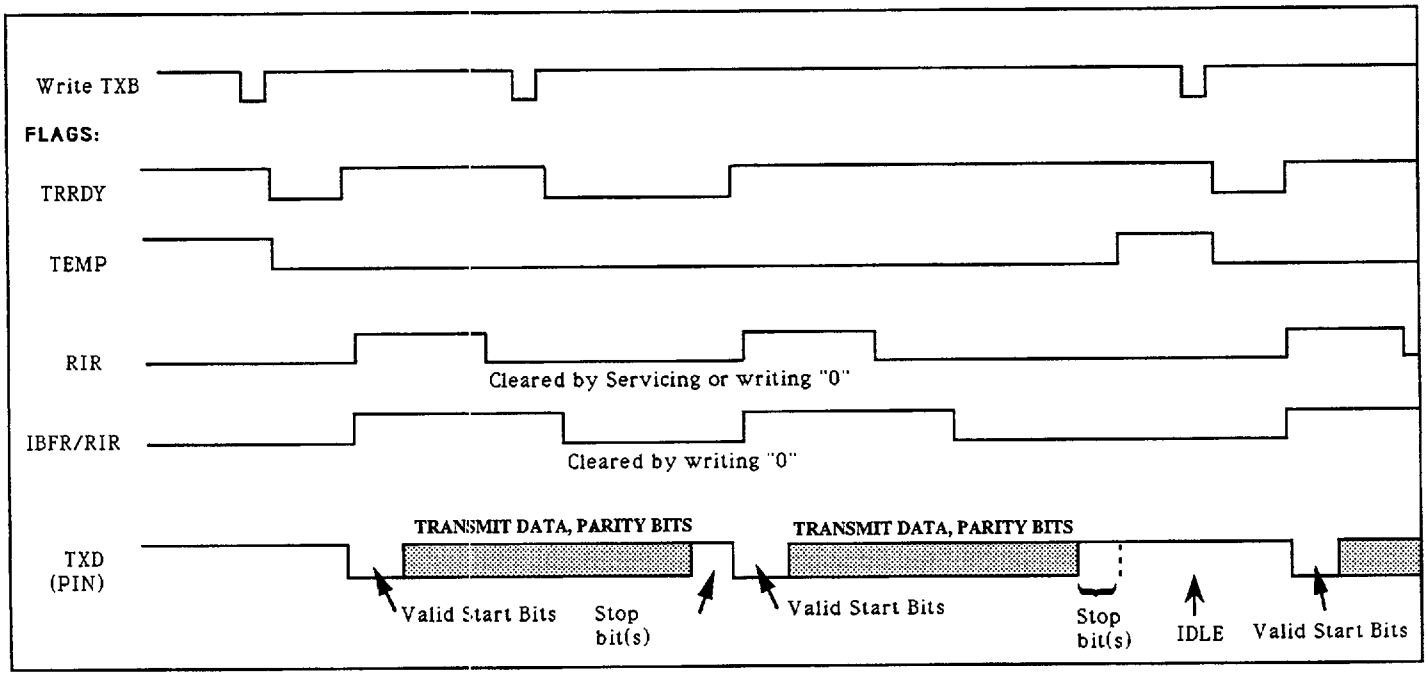
It is possible to transmit data in a continuous flow without any idle time between transmissions. This can be done as long as the new data is written to TXB before the 16th internal clock cycle of the stop bit is received (An internal UART clock is running at 16 times the baud rate). When all data has been transmitted through the shift register and no new data has been written to TXB (to be read into the shift register), the Transmitter Buffer Empty flag (bit 2 TEMP of USTS $F3) is set. This flag is cleared when further data is written to TXB.

Refer to Figure 8.4 for timing of the previous two examples.

When TXB is empty (TRRDY=1), i.e. when the data in TXB transfers to the shift register, the Transmit Interrupt Request flag (bit 5 TIR) of the Interrupt Source Recognition Register 2 (ISOR2 $EB) is set. An interrupt will occur if the Transmit Interrupt Enable flag (bit 1 UTIE of UCON $F5) and the Transmit Interrupt Enable bit (TM4E/TIE) of the Interrupt Control Register (ICON $FE) are set, and the Interrupt Inhibit flag I in the Processor Status Register (PS) is clear. The Transmit Interrupt Request flag (TM4R/TIR of ICON at $FE) can be cleared by servicing the interrupt or by writing "0" to this flag. However, the TIR flag (in ISOR2) can only be cleared by writing "0" to it. Further transmit interrupts can be detected only after both of these flags have been cleared.

Writing "0" to the Transmitter Master Reset (bit 6 of UCON $F5) restores the transmitter to its state at RESET. Writing a "1" to this bit allows the transmitter to begin operation.

Figure 8.4 Transmit Operation



8.3 UART Transmitter Operation Using CTS

The transmitter has a Clear-To-Send (CTS) pin which can be used to control transmission externally or indicate the start of transmission to an external source. The mode of operation is determined by the values of CTSE and CTSO (bits 4, 5 of UCON $F5), and CTSD (bit 7 of UMOD $F4).

Setting CTSE to "1" and CTSD to "0" allows for external control of the transmitter. If the CTS pin is "H" data written to TXB is not allowed into the shift register to be transmitted. Bringing the CTS pin "L" allows the data in TXB into the shift register and transmission begins. Bringing CTS "H" once transmission has started will have no effect on the data.

Setting CTSE to "1" and CTSD to "1" allows CTS to be used as an output pin to indicate the start of data transmission. In this mode the value of the CTS pin is equal to the value of CTSO. Writing a "1" to CTSO will not allow data written to TXB into the shift register to be transmitted. Setting CTSO to "0" brings the CTS pin low, causing the data in TXB to be read into the shift register and transmission to begin. Setting CTSO to "1" once transmission has started will have no effect on the data.

Both of the above cases require that CTS be high to inhibit transmission and low to start transmission. CTS can also be used in output mode to signal an external source to begin transmitting data to the UART through RxD. If the intent is only to signal the external source and not also trigger the start of data transmission through TxD, CTSE must be set to "0" and CTSD to "1". Writing the appropriate value to CTSO will signal the external source to begin transmission.

8.4 UART Baud Rate Generator

The UART has a programmable baud rate generator which provides the clock for the UART receiver and transmitter. The clock divide ratio is written to the UART Baud Rate Generator Register BRG at address $F0. The divide ratio, n, must be in the range $0 \le n \le 255$. BRG should only be written to when RE and MR are both "0".

An external clock can be selected by setting the EX flag in the UART Mode Register (UMOD $F4). This external clock should not exceed 1.6MHz.

The baud rate of the UART can be determined by dividing the input clock (f(Xin)/2, f(Xin)/32 or the external clock) by the BRG value n+1 and then by 16. By setting bit BR (UMOD $F4) to "0" f(Xin)/2 is selected. Below, three different cases of setting the baud rate are illustrated. Also, the examples below show how to achieve different baud rates with commercially available oscillators.

Case1 EX=0 BR=0 $\quad \text{BAUD RATE} = \frac{f(Xin)}{2} \times \frac{1}{(16)(n+1)}$

Case 2 EX=0 BR=1 $\quad \text{BAUD RATE} = \frac{f(Xin)}{32} \times \frac{1}{(16)(n+1)}$

Case 3 EX=1 $\quad \text{BAUD RATE} = \frac{CLK}{(16)(n+1)}$

Examples

(EX=0, BR=0) f(Xin): 7.3728MHz → Baud Rate = $\frac{7372800}{(2)(16)(191+1)}$ = 1,200 bps

(EX=0, BR=0) f(Xin): 7.3728MHz → Baud Rate = $\frac{7372800}{(2)(16)(47+1)}$ = 4,800 bps

(EX=0, BR=0) f(Xin): 7.3728MHz → Baud Rate = $\frac{7372800}{(2)(16)(23+1)}$ = 9,600 bps

(EX=0, BR=0) f(Xin): 7.3728MHz → Baud Rate = $\frac{7372800}{(2)(16)(11+1)}$ = 19,200 bps

(EX=1) External clock: 1.2288MHz → Baud Rate = $\frac{1228800}{(16)(63+1)}$ = 1,200 bps

(EX=1) External clock: 1.2288MHz → Baud Rate = $\frac{1228800}{(16)(15+1)}$ = 4,800 bps

(EX=1) External clock: 1.2288MHz → Baud Rate = $\frac{1228800}{(16)(7+1)}$ = 9,600 bps

(EX=1) External clock: 1.2288MHz → Baud Rate = $\frac{1228800}{(16)(3+1)}$ = 19,200 bps

8.5 Notes for Programming

The UART mode register UMOD is a "write" only register. Only bit 7 (UARTE) can be read and written to. When writing to the UART mode register, only the load memory LDM instruction should be used. Using individual bit manipulation instructions (ex: CLB i,$F4 or SEB i,$F4) might result in incorrect bit setting.

9.0 LCD CONTROLLER/DRIVER

9.1 LCD Controller/Driver Function

The M37428 has a built-in LCD (Liquid Crystal Display device) controller/driver which consists of an LCD mode register, LCD display RAM, selector, timing controller, common driver, segment driver and bias control circuit. A block diagram of the LCD Controller/Driver is shown in Figure 9.1. When an appropriate voltage is applied to the LCD power supply input pins (VL1~VL3) and data is loaded into the LCD mode register, timer 1, LCD display RAM and the controller/driver automatically reads the display data and performs bias and duty control.

The external LCD panel is controlled by four common signal output pins (COM0~COM3) and thirty-two segment signal output pins (SEG0~SEG31). When twenty-four or fewer segment signal output pins are enough, SEG24~SEG31 can be used as input port P4. Bit 4 of the LCD mode register ($EF)is used to make this selection. Table 9.1 shows the maximum number of display pixels for each duty ratio.

Table 9.1 Maximum Number of Display Pixels for each duty

Duty	Max. Number of Display Pixels
1/2	64 dots or 8 LCD segment x 8 digits
1/3	96 dots or 8 LCD segment x 10 digits
1/4	128 dots or 8 LCD segment x 16 digits

The LCD mode register LCDMOD is an 8 bit register located at address $EF. The LCDMOD bit structure is shown at the end of this section and each bit is explained in section SPECIAL FUNCTION REGISTER BIT STRUCTURE. The LCD controller/driver operation and the proper bias and duty ratio values for the LCD panel used are controlled by the five lower bits of this register.

The 16 bytes from address $D0 to address $DF are the dedicated LCD display RAM. Writing "1" to the bits lights the corresponding segment on the LCD panel and writing "0" turns it off. Table 9.2 shows the LCD display RAM map and Figure 9.2 shows a typical LCD panel display pattern. For example, bits 4~7 of address $D0 correspond to segment port 1 (SEG1) and the respective bits correspond to COM0~COM3.

Table 9.2 LCD Display RAM

Pin Name / Address \ Bit	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0
	7	6	5	4	3	2	1	0
$D0	SEG1				SEG0			
$D1	SEG3				SEG2			
$D2	SEG5				SEG4			
$D3	SEG7				SEG6			
$D4	SEG9				SEG8			
$D5	SEG11				SEG10			
$D6	SEG13				SEG12			
$D7	SEG15				SEG14			
$D8	SEG17				SEG16			
$D9	SEG19				SEG18			
$DA	SEG21				SEG20			
$DB	SEG23				SEG22			
$DC	SEG25				SEG24			
$DD	SEG27				SEG26			
$DE	SEG29				SEG28			
$DF	SEG31				SEG30			

Figure 9.1 Block Diagram of LCD Controller/Driver

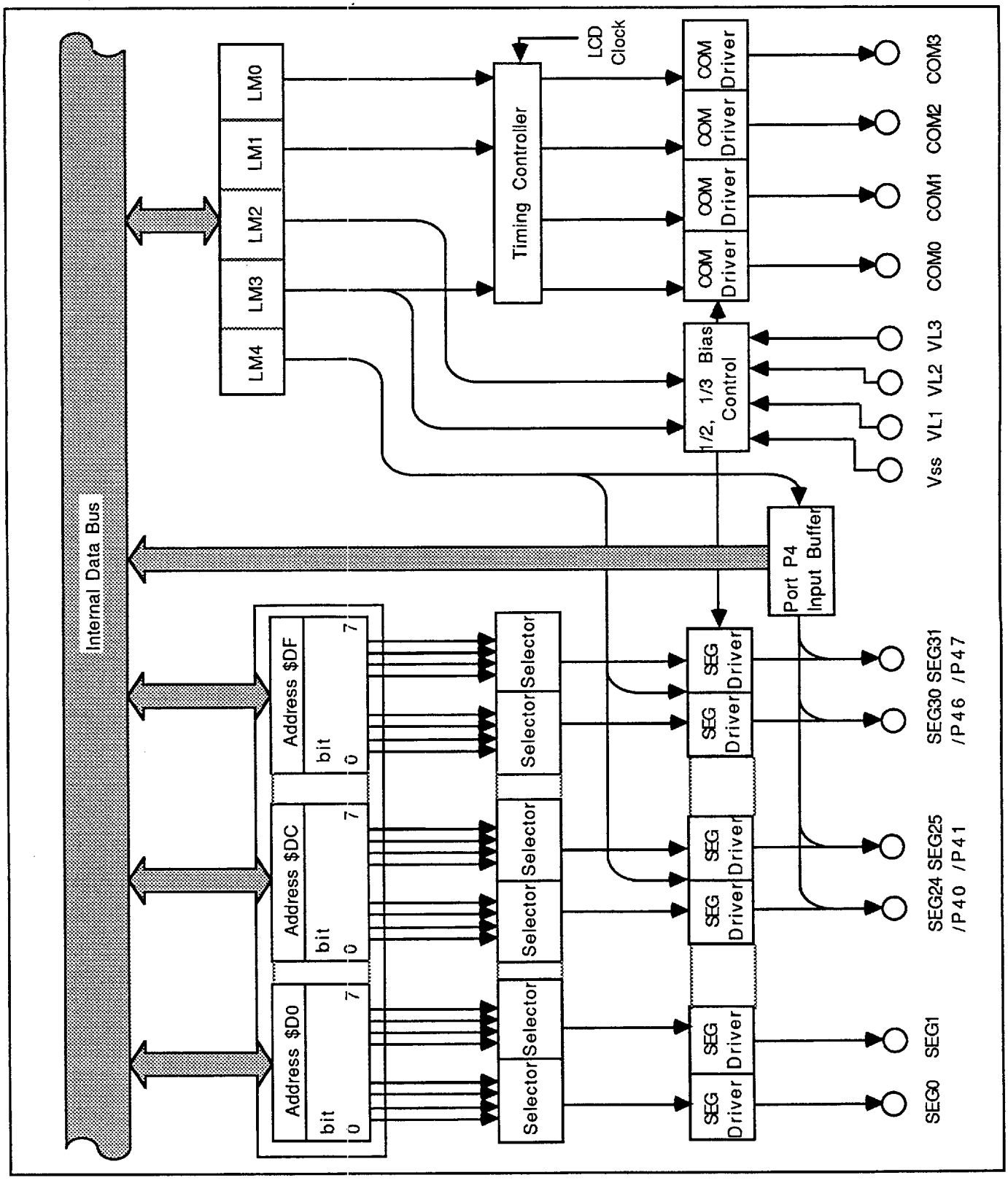
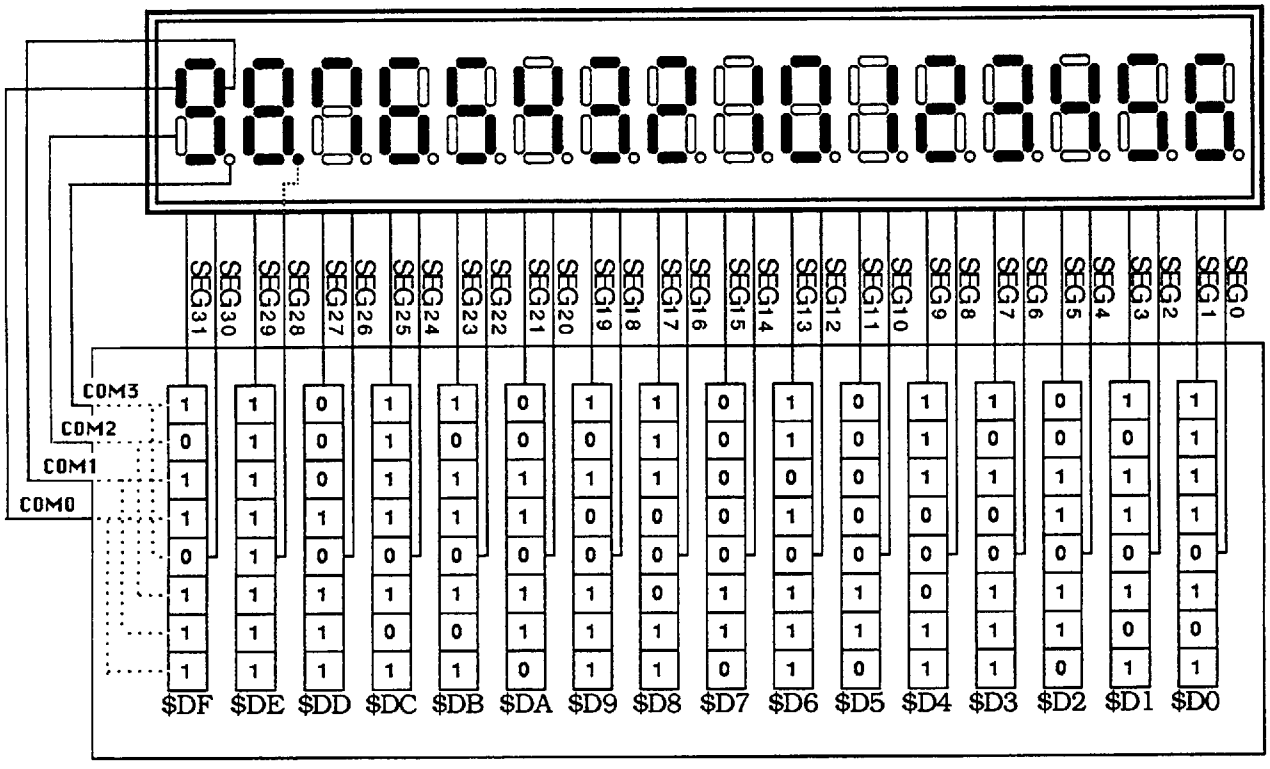
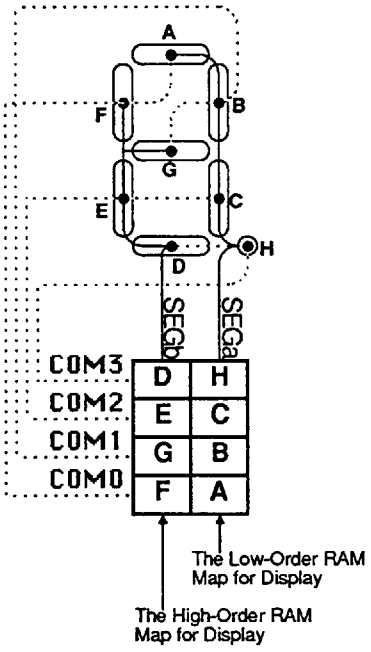


Figure 9.3 Example of LCD Display Pattern





9.2 Bias and Duty Control

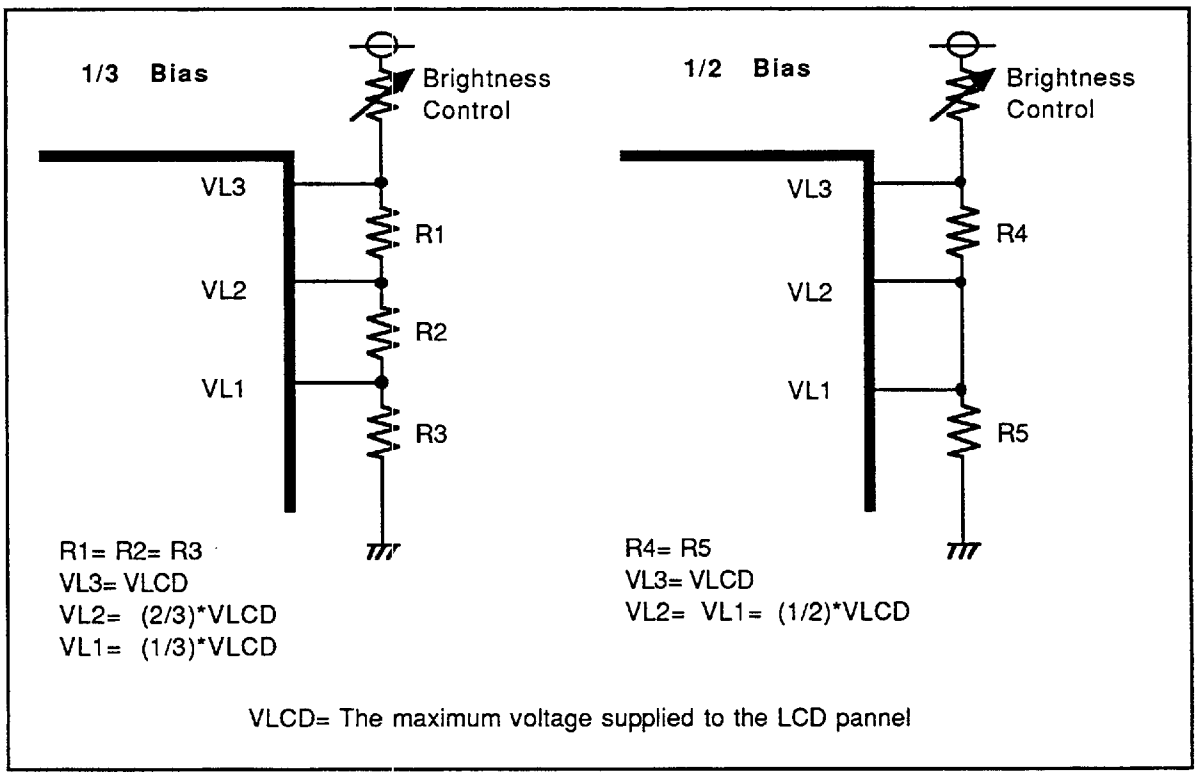
The M37428 can be set for two different bias values: 1/2 bias or 1/3 bias, dependent upon the LCD panel used. The bias setting is made using the bias selection bit (bit 2) of the LCD mode register ($EF). Figure 9.3 shows the internal circuitry of the LCD power supply input pins. The common signal output pins (COM0~COM3) used are determined by the duty ratio selected. Bits 0 and 1 of the LCD mode register LCDMOD ($EF) are used to set duty ratio. Table 9.3 shows the common COM pin names and duty ratio selection bits values for each duty ratio.

Table 9.3 Duty Ratio Control

Duty	Duty Ratio Selection Bits		COM Pins Used
	LM1	LM0	
1/2	0	1	COM0, COM1 (Note1)
1/3	1	0	COM0~ COM2 (Note2)
1/4	1	1	COM0~ COM3

Note1: COM2 and COM3 pins are to be left unconnected
Note2: COM3 is to be left unconnected

Figure 9.3 Example of Circuit at 1/3 Bias and 1/2 Bias



9.3 LCD Drive Timing

Figure 9.4 shows a block diagram of the LCD drive timing circuit. Figure 9.5 shows typical waveforms with 1/2 bias and 1/4 duty ratio and the voltage difference between SEGn and COMn. The display segment controlled by SEGn and COMn lights when the potential difference across the common pin and segment pins is |VLCD|. Figure 9.6 shows typical waveforms for each bias and duty ratio.

Figure 9.6 Typical Waveform For Various Setting Values

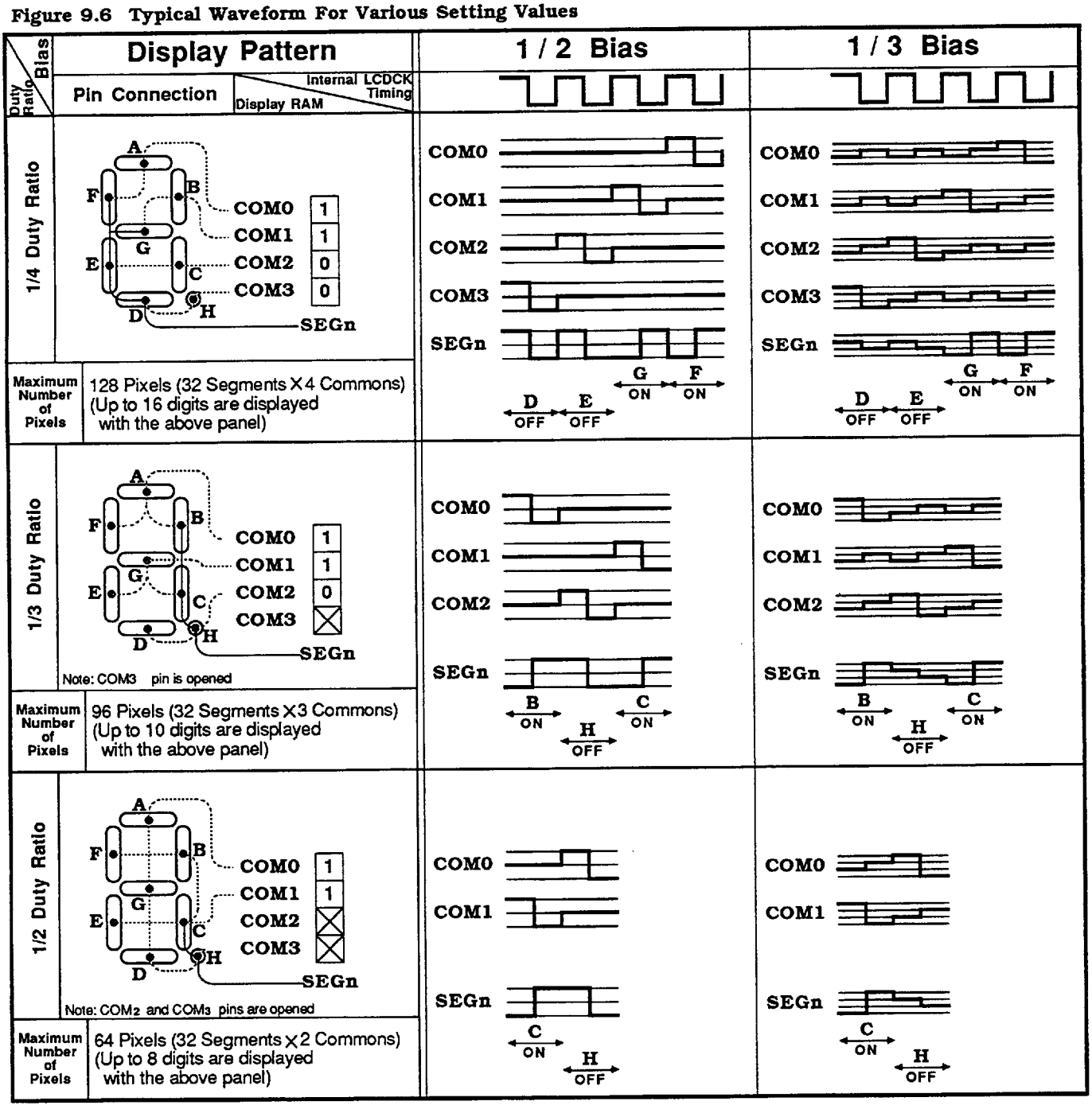


Figure 9.4 LCD Drive Timing Circuit Block Diagram

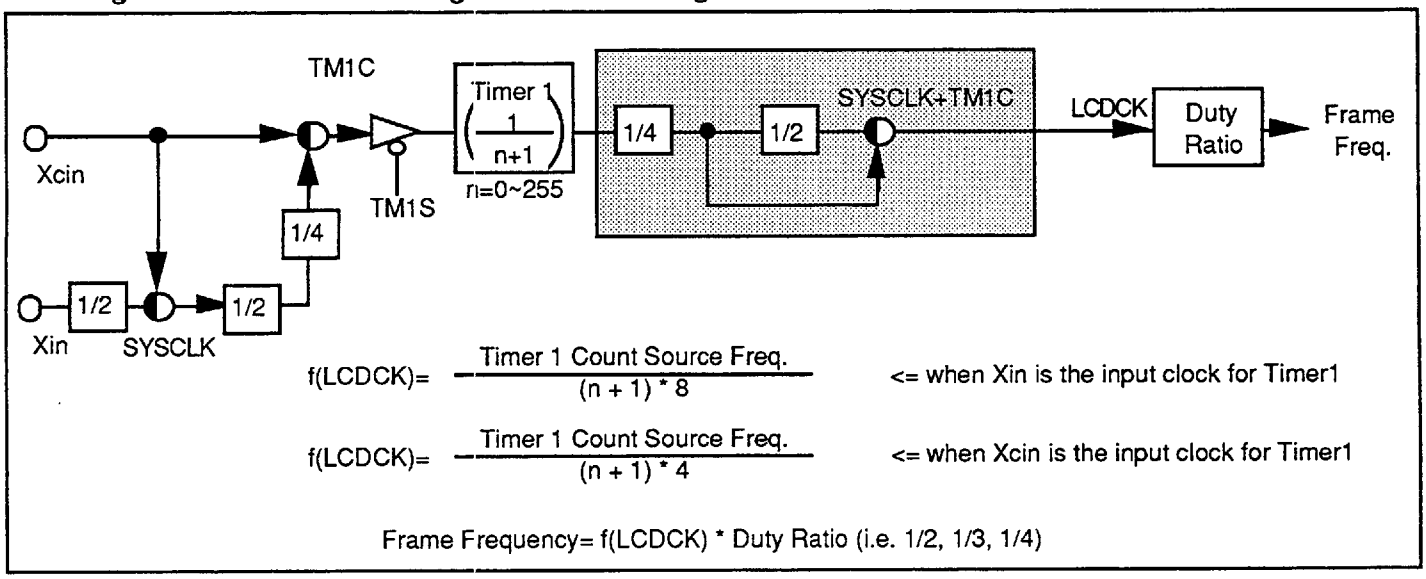


Figure 9.5 Typical Drive Waveform with 1/2 Bias and 1/4 Duty Ratio and the Voltage Difference between SEGn and COMn.

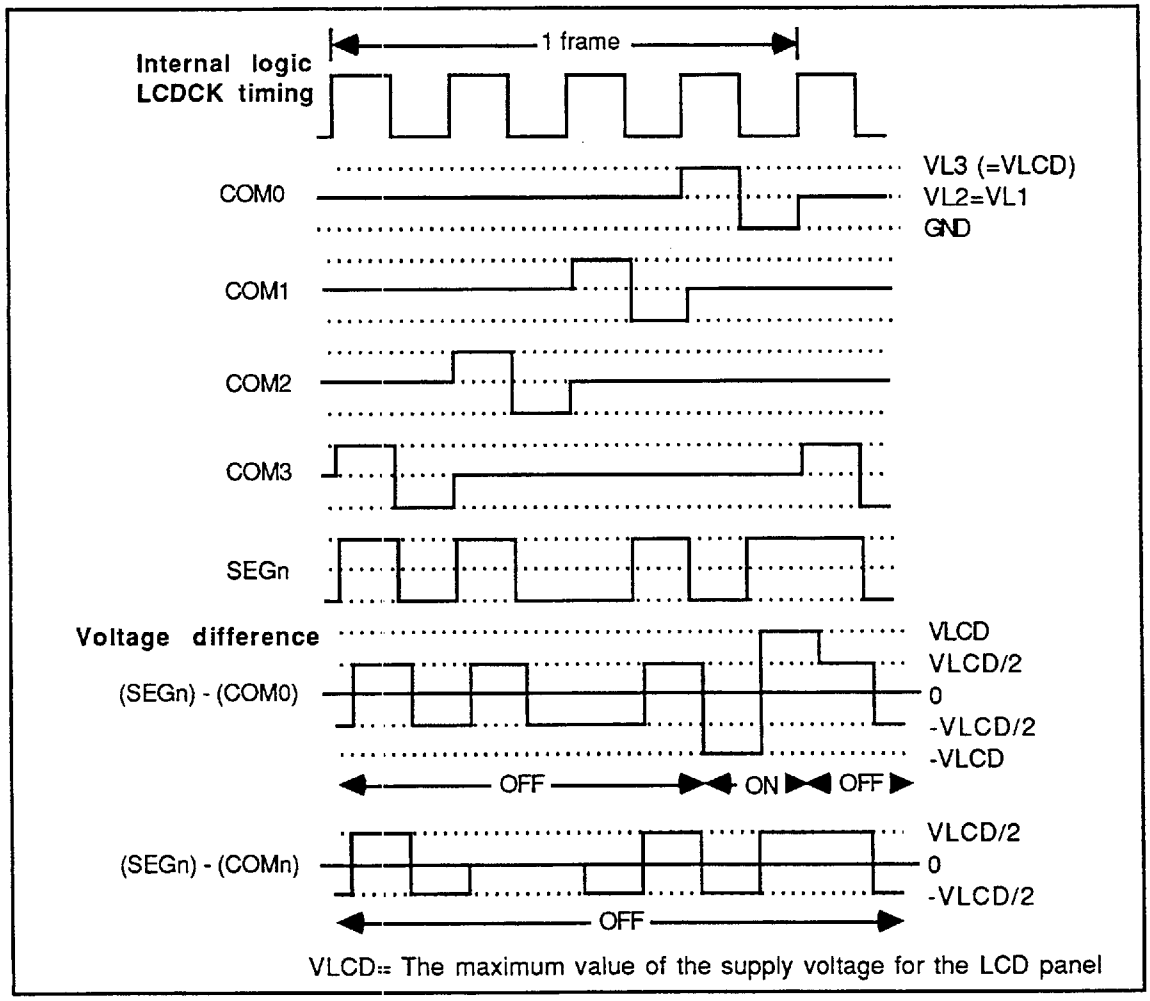
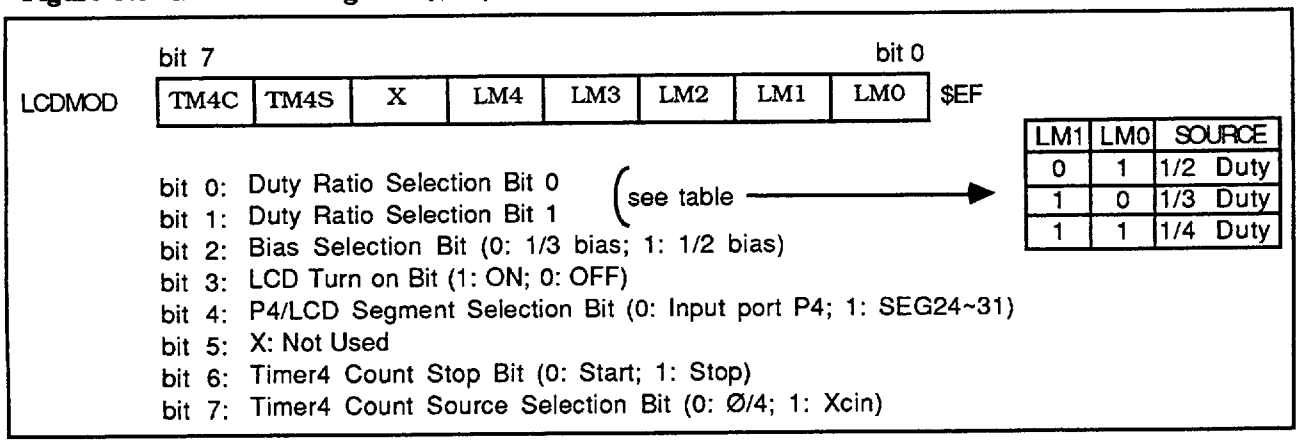


Figure 9.7 LCD Mode Register ($EF)



LM1	LM0	SOURCE
0	1	1/2 Duty
1	0	1/3 Duty
1	1	1/4 Duty

10.0 INTERRUPTS

The M37428 has 11 interrupts which include RESET and BRK instruction interrupt. All interrupts except RESET and BRK interrupts are maskable by I flag. When the I flag is cleared to '0', all maskable interrupts are enabled. Once an interrupt is accepted, the interrupt routine is processed. The interrupt request flag located in ICON register($FE) or TCON2 ($FF) is automatically cleared. Some interrupts have the same interrupt vector, as seen in Table 10.1. When one of these interrupts occur, the user should examine the interrupt request flags located in the Interrupt Source Recognition Register 1 and 2, ISOR1 and ISOR2 at addresses $EA and $EB, respectively, to check which interrupt occurred and then jump to the respective interrupt routine. The user must clear the interrupt request flag located in ISOR1 or ISOR2 in order for future interrupts sharing the same address to be accepted. When an interrupt is accepted the I flag is set to "1". The I flag must be cleared before any other interrupts could be accepted. After a RTI instruction the processor status word is pulled from the stack and the I flag is automatically restored to its original value.

Table 10.1 Interrupt Vector Address and Priority

Priority	Interrupt	Vector Address
1	|RESET	$3FFF~$3FFE
2	|INT1	$3FFD~$3FFC
3	Timer X	$3FFB~$3FFA
4	Timer 2 / (|INT2 or Key-on wake up)	$3FF9~$3FF8
5	Timer 3 / UART RxD	$3FF7~$3FF6
6	Timer 4 / UART TxD / BRK	$3FF5~$3FF4

Figure 10.1 Interrupt Control

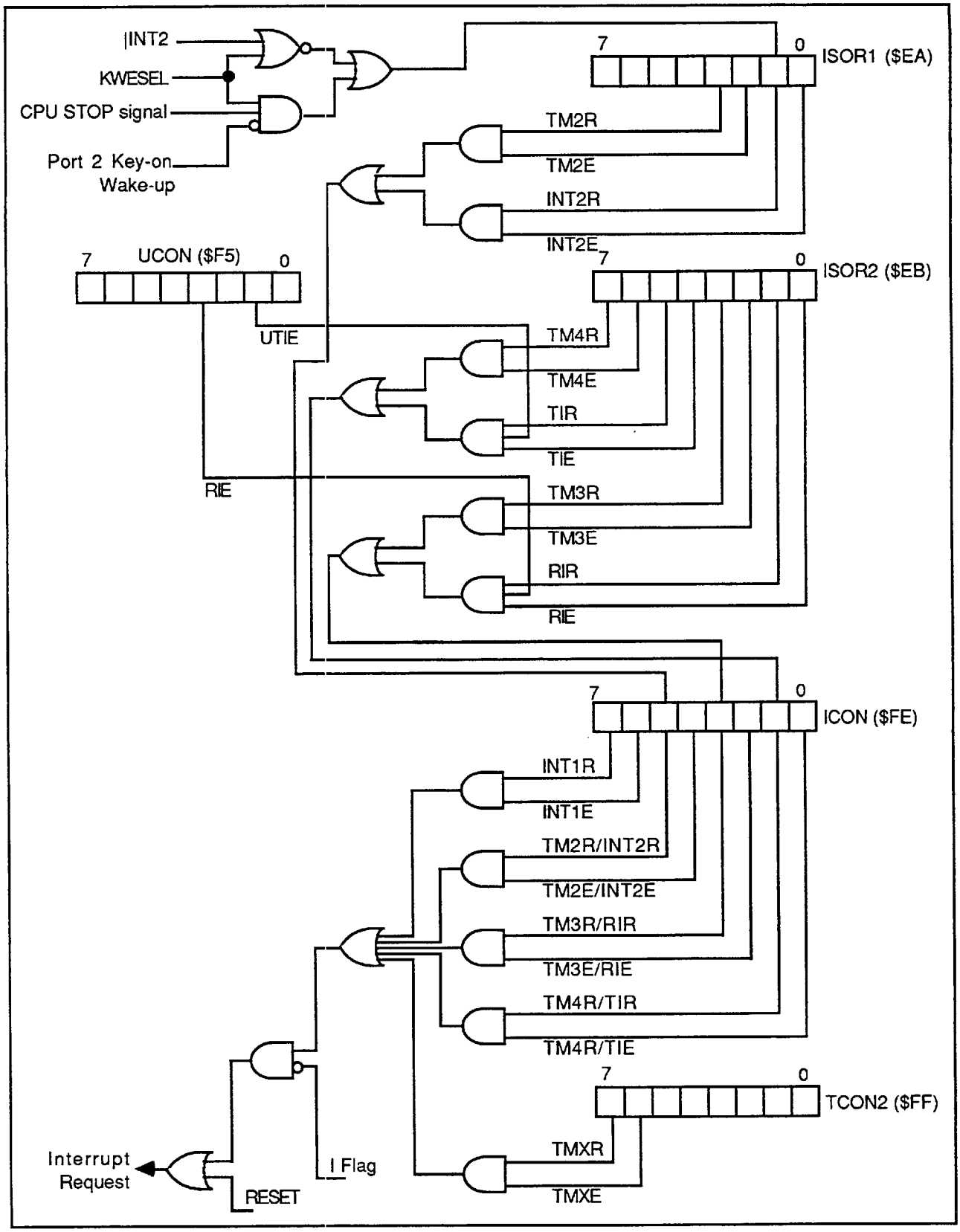


Figure 10.2 Interrupt Special Function Registers: ISOR1, ISOR2, ICON

Interrupt Source Recognition Register 1 ($EA)

	bit 7							bit 0	
ISOR1	X	CNTRS	INT2S	INT1S	TM2R	TM2E	INT2R	INT2E	$EA

bit 0: |INT2 Interrupt Enable (1: Enable)
bit 1: |INT2 Interrupt Request (1: Request)
bit 2: Timer2 Interrupt Enable (1: Enable)
bit 3: Timer2 Interrupt Request (1: Request)
bit 4: |INT1 Status Bit (0: at "L" level; 1: at "H" level)
bit 5: |INT2 Status Bit (0: at "L" level; 1: at "H" level)
bit 6: CNTR Status Bit (0: at "L" level; 1: at "H" level)
bit 7: X: Not Used

Interrupt Source Recognition Register 2 ($EB)

	bit 7							bit 0	
ISOR2	TM4R	TM4E	TIR	TIE	TM3R	TM3E	RIR	RIE	$EB

bit 0: UART Receive Interrupt Enable (1: Enable)
bit 1: UART Receive Interrupt Request (1: Request)
bit 2: Timer3 Interrupt Enable (1: Enable)
bit 3: Timer3 Interrupt Request (1: Request)
bit 4: UART Transmit Interrupt Enable (1: Enable)
bit 5: UART Transmit Interrupt Request (1: Request)
bit 6: Timer4 Interrupt Enable (1: Enable)
bit 7: Timer4 Interrupt Request (1: Request)

Interrupt Control Register ($FE)

	bit 7							bit 0	
ICON	INT1R	INT1E	TM2R/INT2R	TM2E/INT2E	TM3R/RIR	TM3E/RIE	TM4R/TIR	TM4E/TIE	$FE

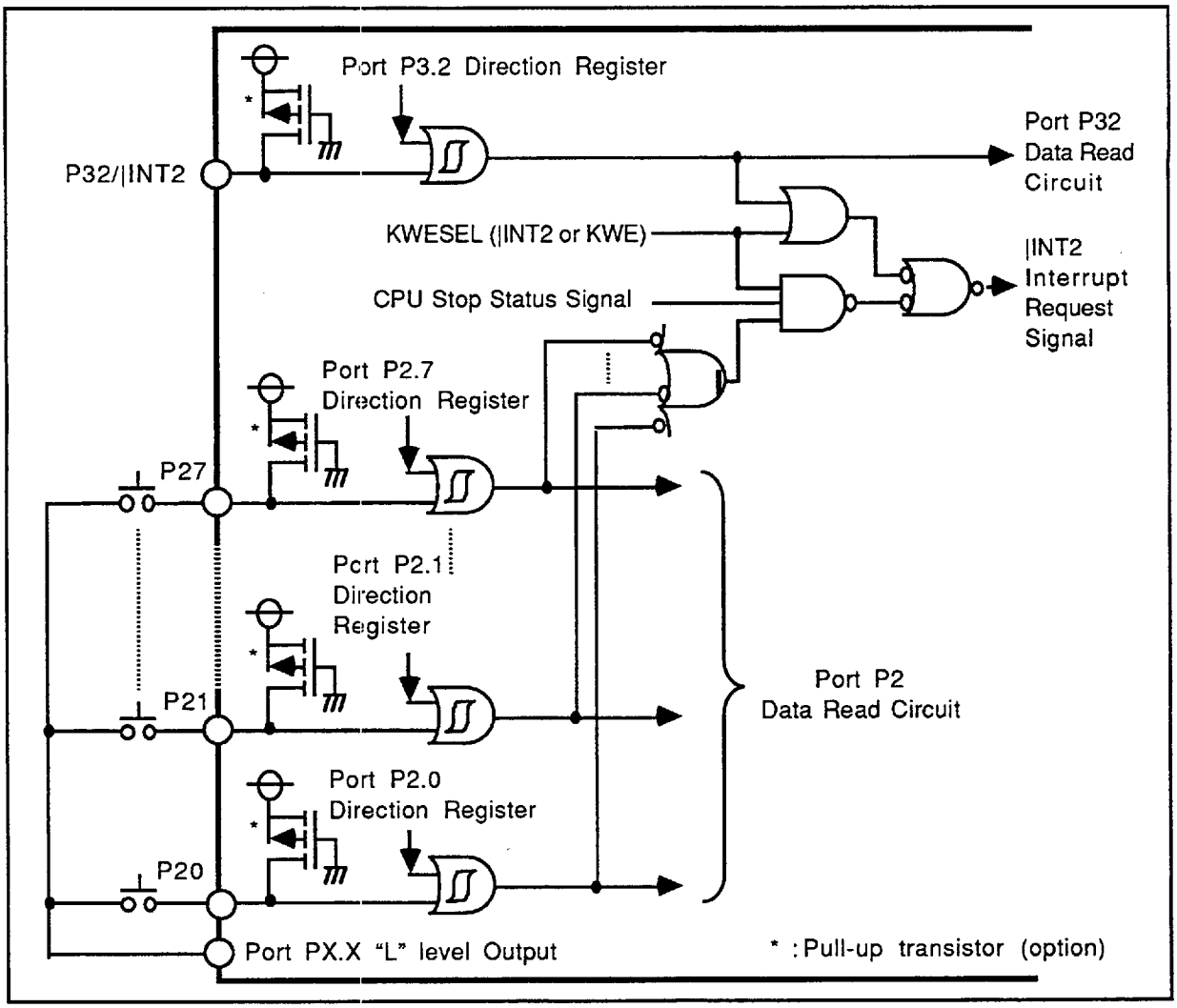
bit 0: Double Function= Timer4 or UART: see ISOR2 $EB (1: Enable)
bit 1: Double Function= Timer4 or UART: see ISOR2 $EB (1: Request)
bit 2: Double Function= Timer3 or UART: see ISOR2 $EB (1: Enable)
bit 3: Double Function= Timer3 or UART: see ISOR2 $EB (1: Request)
bit 4: Double Function= Timer2 or INT2: see ISOR1 $EA (1: Enable)
bit 5: Double Function= Timer2 or INT2: see ISOR1 $EA (1: Request)
bit 6: External Interrupt INT1 Enable (1:Enable)
bit 7: External Interrupt INT1 Request (1:Request)

11.0 KEY-ON WAKE UP

"Key on wake up" is one way of returning from a power down state caused by the STP or WIT instruction. If any terminal of port P2 has a "L" level applied, after bit 7 (KWESEL) of the System Control Register SYSCON (at address $EC) is set to'1', an interrupt is generated and the microcontroller returns to the normal operating state. As shown in Figure 11.1, a key matrix can be connected to port P2 and the microcontroller can be returned to the normal operating state by pushing any key.

The key-on wake up interrupt is common with the |INT2 interrupt. When KWESEL bit is set to '1', the key-on wake up function is selected. However, key-on wake up can not be used in the normal operating state. When the microcomputer is in the normal operating state, both key-on wake up and |INT2 are invalid. In order to enter the power down mode state generated by the STP or WIT instruction the interrupt flag I must be '0', KWESEL bit must be '1' and all terminals of port P2 must be at "H" level.

Figure 11.1 Key-on Wake up Circuit and Example of External Key Matrix



12.0 INPUT/OUTPUT PORTS

12.1 Port P0

Port P0 is an 8-bit I/O port. CMOS type output is used. It can be accessed as memory at address $E0. Port P0 has a directional register (zero page, address $E1) and individual bits can be programmed for input or output. Programming a directional register bit to "0" sets the corresponding pin as an input pin and programming a directional register bit to "1" sets the corresponding pin as an output pin. If a port is selected as output, any data written to that port will be latched into the port register and sent to the output pin. If a port is read while configured as an output port, the last value written out will be read. If a port is selected as input, the external pin is in a high impedance state.

12.2 Port P1

The port P1 function is the same as that of port P0.

12.3 Port P2

The port P2 function is the same as that of port P0. Port P2 is also used for the key-on wake up function.

12.4 Port P3

The port P3 function is the same as that of port P0, except that P37~P34 are also used as UART pins, P3.2 is also used as the interrupt input pin |INT2 and P31~P30 are also used as the oscillator input pins Xcin and Xcout, respectively.
Since P32 is also used as the interrupt (|INT2) input pin, |INT2 interrupts must be disabled to prevent |INT2 interrupt requests being generated when the level changes while this pin is being used as a normal input port.

12.5 Port P4

Port P4 is an 8-bit input port and can also be used for LCD segment output (SEG31~SEG24). This port is pulled up to VL3 (see section 9.0 LCD CONTROLLER/DRIVER) during a reset and enters the high impedance mode after a reset.

12.6 Segment outputs (SEG0~SEG23)

These are the LCD segment drive output ports. VL3 level is output during a reset.

12.7 Common outputs (COM0~COM3)

These are the LCD common drive output ports. VL3 level is output during a reset.

12.8 LCD power supply input (VL1~VL3)

These pins supply power to the LCD terminals.

12.9 |INT1 Pin

This is an interrupt input pin. Changing the input to this pin from "H" to "L" sets the |INT1 interrupt request bit INT1R (bit 7 of ICON, at address $FE) to "1". The status of the input level is also entered in bit 4 (INT1S) of the Interrupt Source Recognition Register 1 ISOR1 ($EA).

12.10 INT2 Pin (P32/ĪNT2 pin)

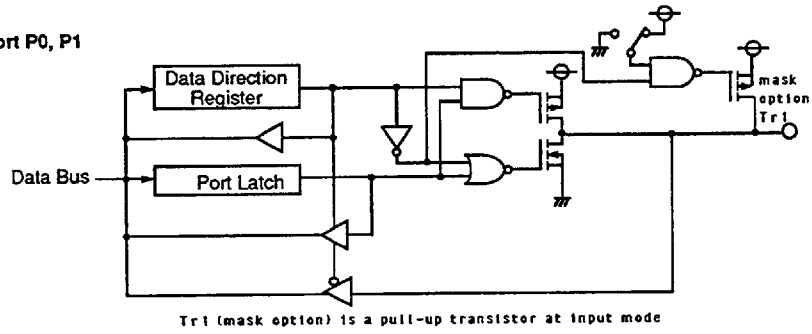
This is an interrupt input pin that is also used as port P32 pin. When used as an interrupt input pin, set the directional register bit for P32 to "0" so that P32 will be in input mode. Changing the input to this pin from "H" to "L" sets the ĪNT2 interrupt request bit INT2R (bit 2 of ISOR1, at address $EA) to "1", and also bit 5 of ICON ($FE) to "1". The status of the input level is also entered in bit 4 (INT2S) of the Interrupt Source Recognition Register 1 ISOR1 ($EA).

12.11 CNTR Pin

The CNTR pin is an I/O pin for timer X. The high impedance mode (input mode) is activated during a reset. The status of the input level is entered in bit 6 (CNTRS) of the Interrupt Source Recognition Register 1 ISOR1 ($EA).

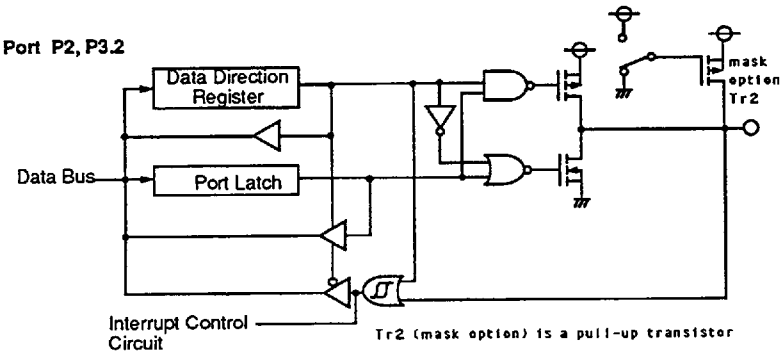
Figure 12.1 Block Diagram of Input/Output Pins

Port P0, P1



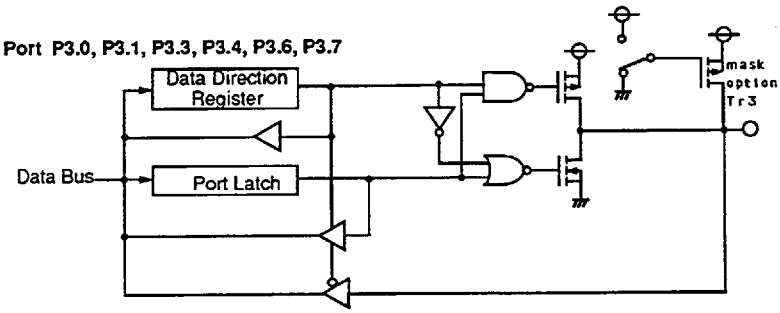
Tr1 (mask option) is a pull-up transistor at input mode

Port P2, P3.2



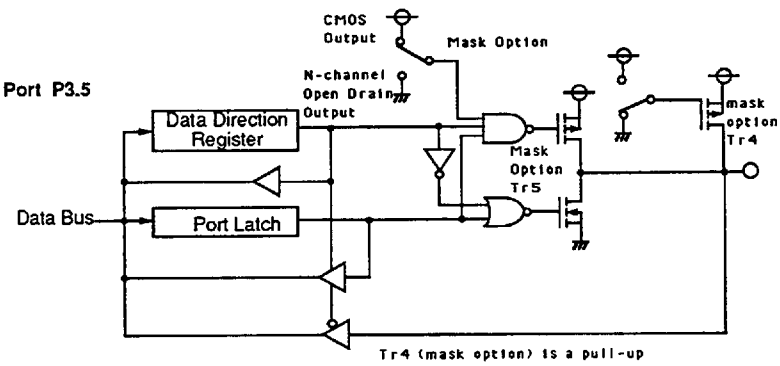
Tr2 (mask option) is a pull-up transistor

Port P3.0, P3.1, P3.3, P3.4, P3.6, P3.7



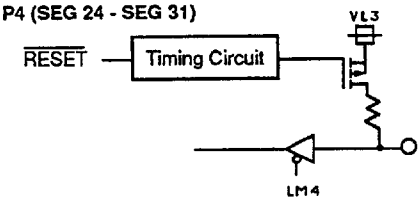
Tr3 (mask option) is a pull-up transistor

Port P3.5

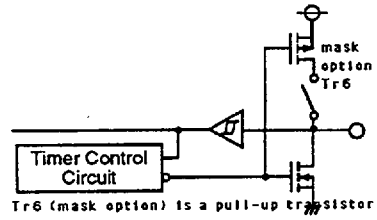


Tr4 (mask option) is a pull-up transistor
Tr5 (mask option) is a P-channel output transistor

Port P4 (SEG 24 - SEG 31)

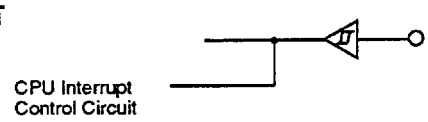


CNTR

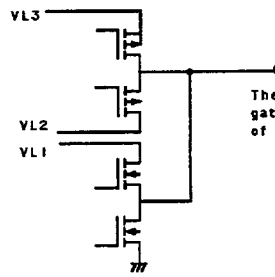


Tr6 (mask option) is a pull-up transistor

INT1

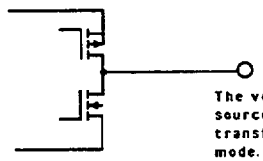


COMMON OUTPUT



The input signals of each trasisto gate are controlled by duty ratio of LCD and its bias mode.

SEGMENT OUTPUT



The voltage that is supplied to source of P-channel and N-channel transistor is controlled by bias mode.

13.0 CLOCK GENERATING CIRCUIT

The M37428 has two built-in oscillation circuits used to generate the clocks required for operation: Xin for the main clock (8MHz max.) and Xcin (32.768kHz) for low speed, low power dissipation time clock function. Normally, the frequency applied to the clock input pin Xin is divided by 4 to create the internal clock Ø (timing output). The frequency at clock pin Xcin can be divided by 2 to obtain the internal clock. This is done by changing bit 0 (SYSCLK) of the System Control Register ($EC).
Figure 13.1 shows a circuit example using a ceramic resonator or crystal oscillator. The manufacturer's recommended values for capacitance and resistance, which depend on the oscillator, should be used. When using an external clock signal, it should be input to Xin (Xcin) and pin Xout (Xcout) should be left unconnected. A circuit example is shown in Figure 13.2.

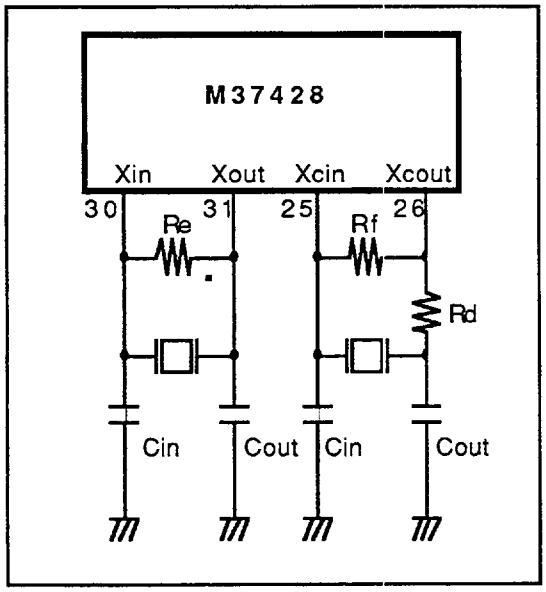


Figure 13.1 Oscillation Circuit Using a Ceramic Resonator or Crystal Oscillator

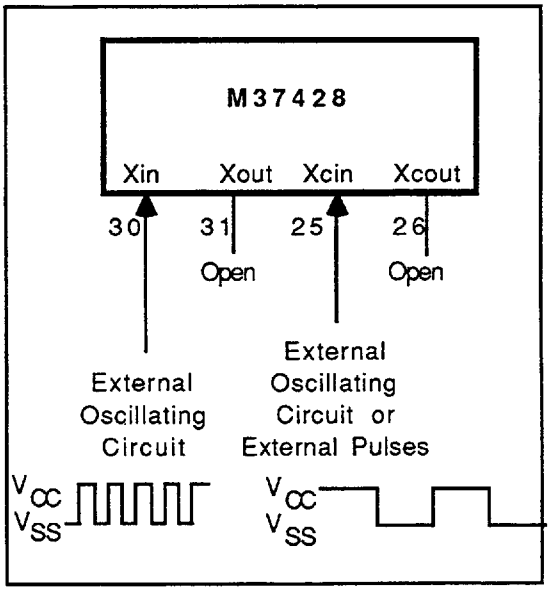


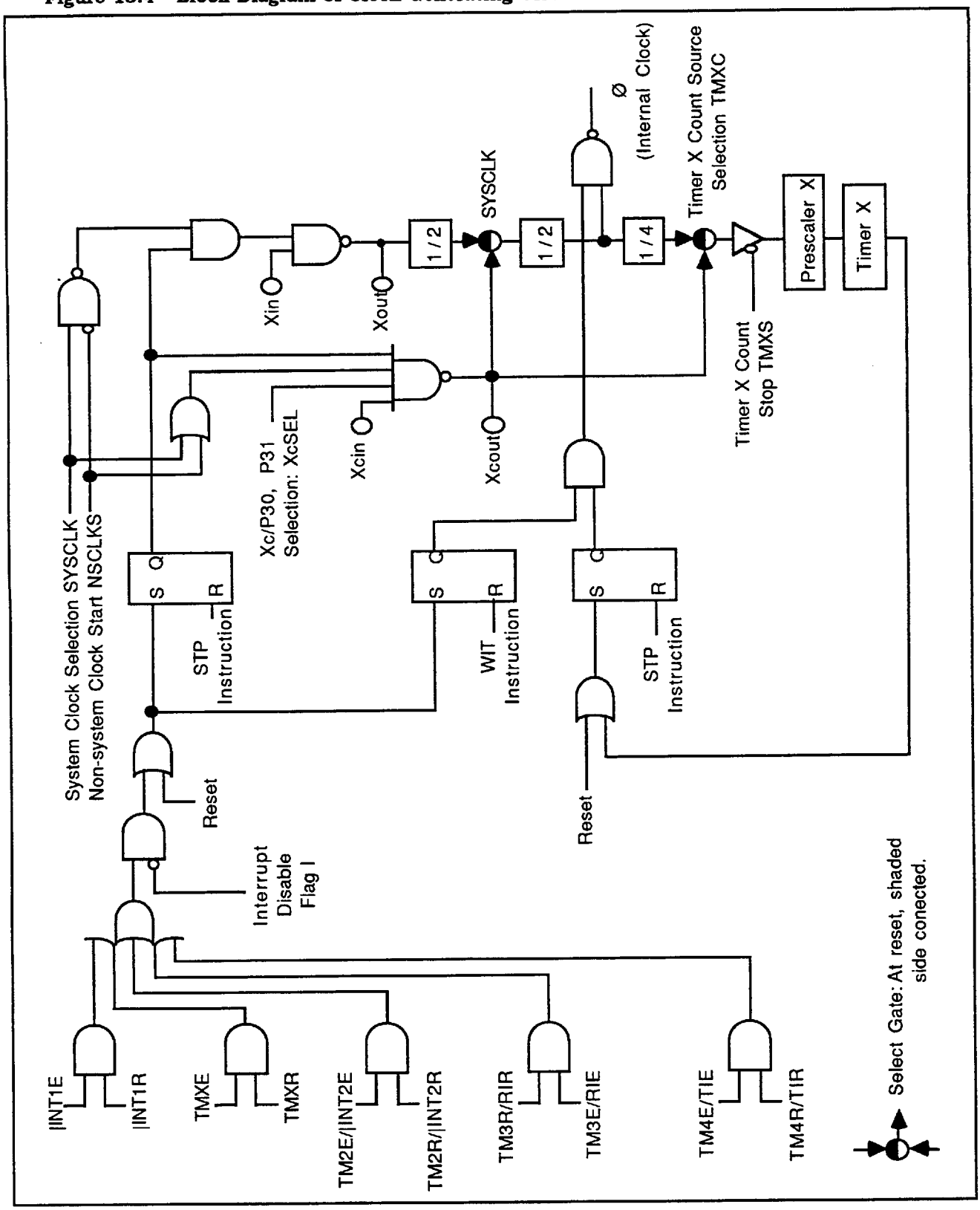
Figure 13.2 Oscillation Circuit Using an External Clock

Figure 13.3 System Control Register ($EC)

	bit 7							bit 0	
SYSCON	KWESEL	NSCLKS	X	XcDR	X	XcSEL	X	SYSCLK	$EC

bit 0: System Clock Selection Bit (0: Xin/4; 1: Xcin/2)
bit 1: X: Not Used
bit 2: Xc/(P30, P31) Selection Bit (0: I/O port; 1: Xcin, Xcout function)
bit 3: X: Not Used
bit 4: Xcout Drivability Selection Bit (0: High; 1: Low)
bit 5: X: Not Used
bit 6: Non-system Clock Start Bit (0: Stop; 1: Start)
bit 7: |INT2/Key-on Wake up Selection Bit (0: |INT2; 1: Key-on Wake up)

Figure 13.4 Block Diagram of Clock Generating Circuit



14.0 CLOCK OSCILLATOR CIRCUIT

Oscillator circuits consist of an "oscillation gate" which operates as an amplifier to provide the gain required for oscillation and an "oscillation control flipflop" for control. Because of that, it is possible to start and stop oscillation as required. For details concerning the starting and stopping of oscillation refer to section LOW POWER CONSUMPTION MODE. Figure 13.4 shows the clock generating circuit block diagram.

The following items must be taken into consideration when programming:

a) System clock switching

System Clock refers to the external clock input (Xin or Xcin) which is selected for CPU operation. Non-system Clock refers to the clock input which is not used for CPU operation.

When switching the system clock, the system clock selection bit 0 SYSCLK (SYSCON register at $EC) must be set after the new system clock oscillation has fully stabilized (Xcin when switching from the normal mode to the low-speed mode; Xin when switching from low speed mode to the normal mode).

Malfunction can occur when switching is performed before clock oscillation has fully stabilized.

b) Xcout drivability selection bit setting (bit 4 of SYSCON)

With the M37428, the Xcout drivability selection bit XcDR (SYSCON register at $EC bit 4) is set to "0" by hardware in either of the following cases to improve the clock function clock oscillation rise characteristics, so "1" cannot be written to this bit (to set low drivability).

1. When the Xc/P30, P31 pins are set for parallel port function (SYSCON's XcSEL bit = "0").
2. When the system clock is in the normal mode (SYSCON's SYSCLK bit = "0") and the non-system clock is stopped (SYSCON's NSCLKS = "0")

The Xcout drivability selection bit is also set to "0" when the STP instruction is executed. Current consumption can be reduced after oscillation stabilizes, or after oscillation is started, by setting the Xcout drivability selection bit to "1".

c) Xc/P30, P31 pin setting

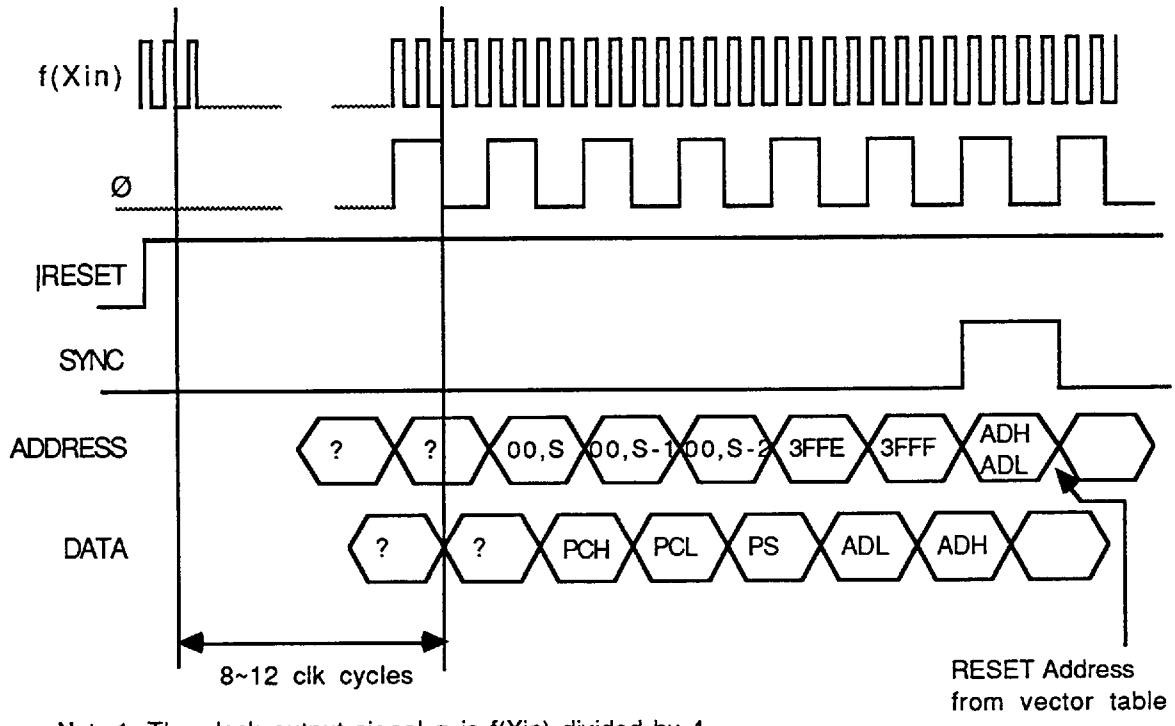
Pins Xc/P30, P31 can not be set for I/O port function when the system clock is Xcin/Xcout. (SYSCLK = "1").

15.0 RESET CIRCUIT

When the power supply voltage is within the recommended range and the RESET pin is returned to "H" level after being held at "L" level for 2~8μs or more, the M37428 is reset according to the sequence shown in Figure 14.1. At RESET the program counter is loaded with the data stored at $3FFF (high byte) and $3FFE (low byte). The status of the special function registers after RESET is as shown in Figure 14.2.

When the power-on RESET is used, the |RESET pin must be held "L" until the Xin ~ Xout oscillation becomes stable.

Figure 15.1 Timing Diagram at RESET



Note 1: The clock output signal ø is f(Xin) divided by 4.
2: The mark "?" indicates an undefined address.

Figure 15.2 Special Function Register status After RESET

Register	Zero Page Address	Contents After Reset
Port 0 Direction Register	$00E1	00000000
Port 1 Direction Register	$00E3	00000000
Port 2 Direction Rgister	$00E5	00000000
Port 3 Direction Register	$00E7	00000000
Interrupt Source Recognition Register1	$00EA	XXXX0000
Interrupt Source Recognition Register2	$00EB	00000000
System Control Register	$00EC	00X0X0X0
LCD Mode Register	$00EF	00X00000
UART Mode Register	$00F4	00000000
UART Control Register	$00F5	X0000000
Timer Control Register 1	$00F6	00000000
Prescaler X	$00FC	11111111
Timer X	$00FD	00000001
Interrupt Control Register	$00FE	00000000
Timer Control Register2	$00FF	00000000

16.0 LOW POWER CONSUMPTION MODE

The M37428M4-XXXFP has two low power consumption modes: "stop" and "wait".

(1) Stop Mode

In the M37428, both the normal clock (XIN) and the clock function clock (XCIN) oscillation can be stopped without changing the internal status of the M37428 (register, I/O ports, internal RAM, etc.) except for the timer X register. Thus, it is possible to restart from the same status after stopping oscillation. This operation greatly reduces power consumption.

Use the STP instruction to stop oscillation in this manner. Executing the STP instruction activates the stop mode. In this mode, the address which fetches the instruction to follow the STP instruction is output to the address bus. Internal clock ø then becomes a "H" level and oscillation stops. At this time, the internal clock ø/4 (XIN/16) is connected to the timer X input.

Oscillation is restarted when either the INT1, UART RxD, UART TxD, INT2 or key on wake up interrupt is received. When an interrupt is received, the interrupt service routine is executed. However, the internal clock ø/4 is not supplied to the CPU until timer X overflows. This is because time is required for stabilization when a ceramic or other resonator is used. Appropriate values will automatically be loaded into timer X prescaler and timer to achieve this delay.

It is also necessary for the timer X count stop bit TMXS to be set to start mode("0"), the timer X interrupt enable bit TMXE be set to disable ("0"), and the timer X interrupt request bit TMXR to be cleared ("0"); these values must be set before executing the STP instruction.

When the internal clock ø/4 is supplied to the CPU, the CPU executes the interrupt service routine. At this time, the first byte of the address of the instruction to follow the STP instruction is saved to the stack as the return destination address. The timer X interrupt request bit is now set, so clear this bit during the interrupt service routine.

To use an interrupt to restart oscillation, the enable bits for the above interrupts must be set before the STP instruction is executed.

(2) Wait Mode

Executing the WIT instruction of the M37428 activates the wait mode. In this mode, the internal clock is stopped and held at "1" but the oscillator does not stop. Because of this, it is possible to restart faster than with the STP instruction. A restart occurs when an interrupt is received, as with the STP instruction. However, in this case, the internal timer is operating so an internal timer interrupt as will as other interrupts can restart the cpu.

17.0 LOW POWER CONSUMPTION CLOCK MODE

The M37428 is provided with a normal clock oscillator circuit Xin-Xout (high-speed 8MHz) and a clock function clock generator circuit Xcin-Xcout (low-speed 32.768kHz). Power consumption can be reduced by operating only Xcin.

These two clocks are controlled by bits 0, 2, 4, and 6 of the System Control Register (SYSCON). Bit 0 (SYSCLK) is the switching bit for the system clock source. Bit 2 (XCSEL) is the switching bit for ports XCIN/P30 and XCOUT/P31. Bit 4 (XCDR) is the Xcout drivability selection bit. Bit 6 (NSCLKS) is the start/stop bit for the nonsystem clock.

Figure 17.1 shows the transition chart for the system clock status. Normal mode (Status A) is activated after reset. Xin/4 is the internal clock in this mode, and Xcin oscillation is stopped. To change from normal mode to the low-speed mode (Status D), it is necessary to enter status B and Status C. This procedure is explained below.

[Shifting from the normal mode to the low-speed mode]

After reset, the settings for the four bits in SYSCON are all "0". This sets up P30 and P31 as normal ports, system clock source as Xin, Xcin oscillation stopped, and Xcout drivability high.

(1) Setting XCSEL to "1" (switching P30 and P31 to XCIN and XCOUT) and setting NSCLKS to "1" causes the clock function clock used as the nonsystem clock to oscillate.
-----(from status A to status B)

(2) After oscillation stabilizes, set XCDR to "1" to set the Xcout drive capacity to "Low". This reduces power consumption .

After that, set SYSCLK to "1" to switch the system clock to Xcin.

-----(from status B to status C)

(3) Set NSCLKS to "0" to stop Xin.

-----(from status C to status D)

[Shifting from the low-speed mode to the clock mode]

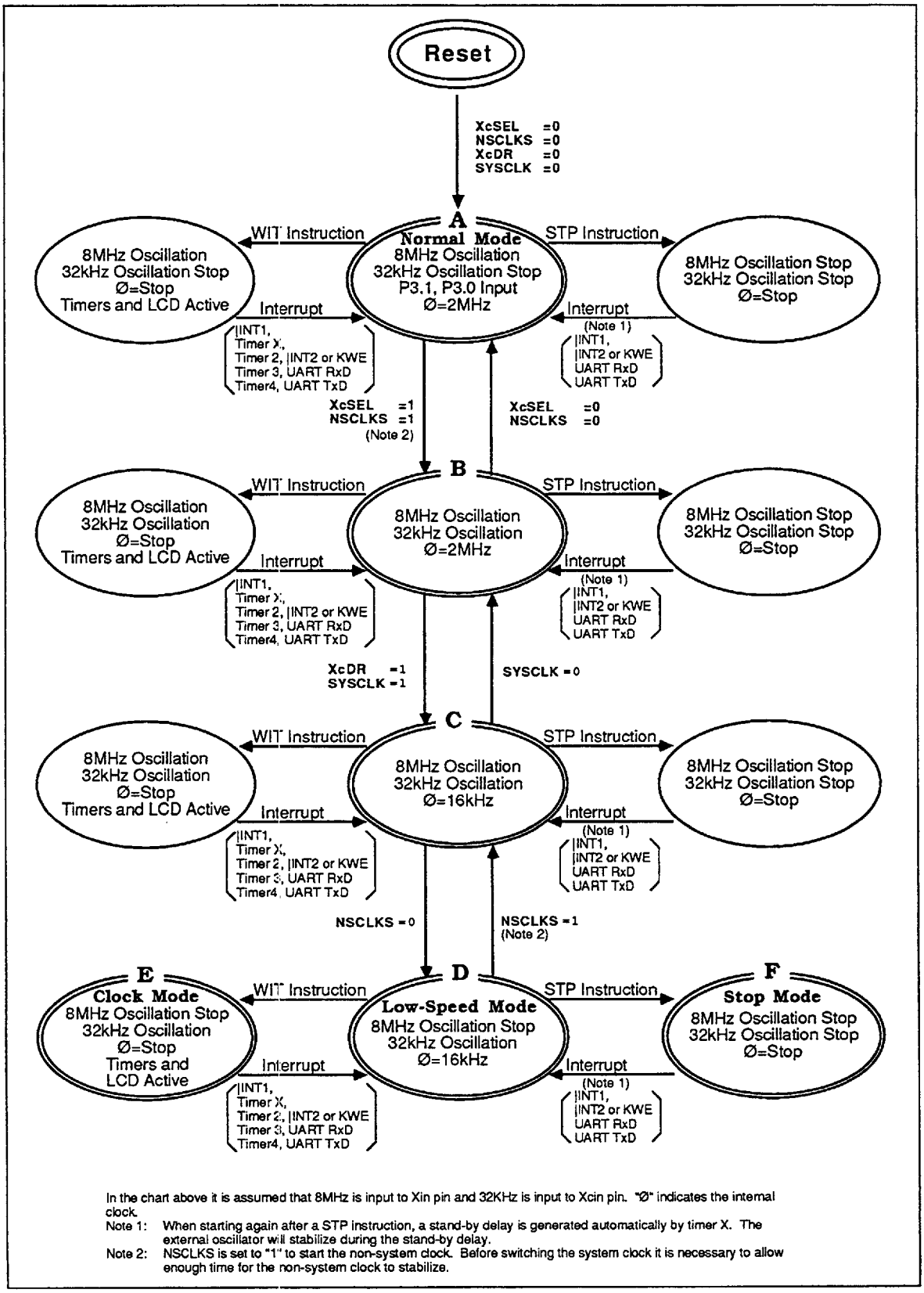
To shift from status D to status E (clock mode), in which only the low-speed clock and LCD functions operate, and for even lower power consumption, execute the WIT instruction to stop the internal clock ø. Any interrupt will reset this status.

[Shifting from any mode to the operation stop mode]

Executing the STP instruction from status A-status C activates the operation stop mode in which only RAM backup is effective.

Interrupts at this time return the cpu to its status previous to execution of the STP instruction.

Figure 17.1 System Clock Status Transition Chart



In the chart above it is assumed that 8MHz is input to Xin pin and 32KHz is input to Xcin pin. "Ø" indicates the internal clock.

Note 1: When starting again after a STP instruction, a stand-by delay is generated automatically by timer X. The external oscillator will stabilize during the stand-by delay.

Note 2: NSCLKS is set to "1" to start the non-system clock. Before switching the system clock it is necessary to allow enough time for the non-system clock to stabilize.

SPECIAL FUNCTION REGISTER BIT STRUCTURE

Interrupt Source Recognition Register 1 ($EA)

	bit 7							bit 0	
ISOR1	X	CNTRS	INT2S	INT1S	TM2R	TM2E	INT2R	INT2E	$EA

bit 0: |INT2 Interrupt Enable (1: Enable)
bit 1: |INT2 Interrupt Request (1: Request)
bit 2: Timer2 Interrupt Enable (1: Enable)
bit 3: Timer2 Interrupt Request (1: Request)
bit 4: |INT1 Status Bit (0: at "L" level; 1: at "H" level)
bit 5: |INT2 Status Bit (0: at "L" level; 1: at "H" level)
bit 6: CNTR Status Bit (0: at "L" level; 1: at "H" level)
bit 7: X: Not Used

Interrupt Source Recognition Register 2 ($EB)

	bit 7							bit 0	
ISOR2	TM4R	TM4E	TIR	TIE	TM3R	TM3E	RIR	RIE	$EB

bit 0: UART Receive Interrupt Enable (1: Enable)
bit 1: UART Receive Interrupt Request (1: Request)
bit 2: Timer3 Interrupt Enable (1: Enable)
bit 3: Timer3 Interrupt Request (1: Request)
bit 4: UART Transmit Interrupt Enable (1: Enable)
bit 5: UART Transmit Interrupt Request (1: Request)
bit 6: Timer4 Interrupt Enable (1: Enable)
bit 7: Timer4 Interrupt Request (1: Request)

System Control Register ($EC)

	bit 7							bit 0	
SYSCON	KWESEL	NSCLKS	X	XcDR	X	XcSEL	X	SYSCLK	$EC

bit 0: System Clock Selection Bit (0: Xin/4; 1: Xcin/2)
bit 1: X: Not Used
bit 2: Xc/(P30, P31) Selection Bit (0: I/O port; 1: Xcin, Xcout function)
bit 3: X: Not Used
bit 4: Xcout Drivability Selection Bit (0: High; 1: Low)
bit 5: X: Not Used
bit 6: Non-system Clock Start Bit (0: Stop; 1: Start)
bit 7: |INT2/Key-on Wake up Selection Bit (0: |INT2; 1: Key-on Wake up)

LCD Mode Register ($EF)

	bit 7							bit 0	
LCDMOD	TM4C	TM4S	X	LM4	LM3	LM2	LM1	LM0	$EF

LM1	LM0	SOURCE
0	1	1/2 Duty
1	0	1/3 Duty
1	1	1/4 Duty

bit 0: Duty Ratio Selection Bit 0 (see table →
bit 1: Duty Ratio Selection Bit 1
bit 2: Bias Selection Bit (0: 1/3 bias; 1: 1/2 bias)
bit 3: LCD Turn on Bit (0: OFF ; 1: ON)
bit 4: P4/LCD Segment Selection Bit (0: Input port P4; 1: SEG24~31)
bit 5: X: Not Used
bit 6: Timer4 Count Stop Bit (0: Start; 1: Stop)
bit 7: Timer4 Count Source Selection Bit (0: Ø/4; 1: Xcin)

UART Status Register ($F3)

	bit 7							bit 0	
USTS	CTSI	X	FE	OE	PE	TEMP	RRDY	TRRDY	$F3

bit 0: Transmitter Buffer Ready ("1" when TXB is empty and ready for another byte)
bit 1: Receiver Ready ("1" when the RXB has finished receiving a byte)
bit 2: Transmitter Register Empty ("1" when the transmitter shift register and TXB are empty)
bit 3: Parity Error ("1" when a parity error is detected in the received data)
bit 4: Overrun Error ("1" when a character is not finished being read from RXB before the next one becomes available)
bit 5: Framing Error ("1" when a valid stop bit is not detected)
bit 6: X : Not Used
bit 7: |CTS Input Status Bit (0: at "L" level; 1: at "H" level)

UART Mode Register ($F4)

	bit 7							bit 0	
UMOD	CTSD	UARTE	EX	BR	ST	CHL	EVN	PEN	$F4

bit 0: Parity Enable Bit (1: Enable)
bit 1: Even/Odd Parity Selection Bit (1: Even, 0: Odd)
bit 2: Character Length Selection (1: 8 bits; 0: 7 bits)
bit 3: Stop Bit Number Selection (1: 2 bits; 0: 1 bit)
bit 4: Baud Rate Oscillation Selection (1: 1/32; 0: 1/2)
bit 5: Baud Rate Clock Source Selection (1: External; 0: Internal)
bit 6: UART Enable (1: Enable; 0: Disable)
bit 7: |CTS Direction Selection (1: output; 0: input)

UART Control Register ($F5)

	bit 7							bit 0	
UCON	ERST	MR	CTSO	CTSE	RIE	RE	UTIE	TE	$F5

bit 0: Transmit Enable (1: Enable)
bit 1: UART Transmit Interrupt Enable (1: Enable)
bit 2: Receive Enable (1: Enable)
bit 3: Receive Interrupt Enable (1:Enable)
bit 4: |CTS Control Enable (1:Enable)
bit 5: |CTS Output Data Register
bit 6: Transmitter Master Reset (1: Enable Operation; 0: Reset)
bit 7: Error Reset (1: Reset Error Flags; 0: Normal State)

Timer Control Register 1 ($F6)

	bit 7							bit 0	
TCON1	TM3S	TM2S	TM1S	TM3C1	TM3C0	TM2C1	TM2C0	TM1C	$F6

bit 0: Timer1 Count Source Selection Bit (0: Ø/4; 1: Xcin)
bit 1: Timer2 Count Source Selection Bit 0 (see table →)
bit 2: Timer2 Count Source Selection Bit 1 (see table →)
bit 3: Timer3 Count Source Selection Bit 0 (see table →)
bit 4: Timer3 Count Source Selection Bit 1 (see table →)
bit 5: Timer1 Count Stop Bit (0: Start; 1: Stop)
bit 6: Timer2 Count Stop Bit (0: Start; 1: Stop)
bit 7: Timer3 Count Stop Bit (0: Start; 1: Stop)

TM2C1	TM2C0	SOURCE
0	0	Ø/4
0	1	Xcin
1	0	TM1 Over-
1	1	flow

TM3C1	TM3C0	SOURCE
0	0	Ø/4
0	1	Xcin
1	0	TM2 Over-
1	1	flow

Interrupt Control Register ($FE)

	bit 7							bit 0	
ICON	INT1R	INT1E	TM2R/INT2R	TM2E/INT2E	TM3R/RIR	TM3E/RIE	TM4R/TIR	TM4E/TIE	$FE

bit 0: Double Function= Timer4 or UART: see ISOR2 $EB (1: Enable)
bit 1: Double Function= Timer4 or UART: see ISOR2 $EB (1: Request)
bit 2: Double Function= Timer3 or UART: see ISOR2 $EB (1: Enable)
bit 3: Double Function= Timer3 or UART: see ISOR2 $EB (1: Request)
bit 4: Double Function= Timer2 or INT2: see ISOR1 $EA (1: Enable)
bit 5: Double Function= Timer2 or INT2: see ISOR1 $EA (1: Request)
bit 6: External Interrupt INT1 Enable (1:Enable)
bit 7: External Interrupt INT1 Request (1:Request)

Timer Control Register 2 ($FF)

TCON2

bit 7							bit 0	
TMXR	TMXE	TMXS	TMXC	TMOD1	TMOD0	PMOD1	PMOD0	$FF

bit 0: Processor Mode Bit 0
bit 1: Processor Mode Bit 1
bit 2: Timer X Mode Bit 0
bit 3: Timer X Mode Bit 1
bit 4: Timer X Count Source Selection Bit (0: Ø/4; 1: Xcin)
bit 5: Timer X Count Stop (0: Start; 1: Stop)
bit 6: Timer X Interrupt Enable (1: Enable)
bit 7: Timer X Interrupt Request (1: Request)

PMOD		Processor Mode
1	0	
0	0	Single-Chip Mode
Note: PMOD0 and PMOD1 must always be equal to "0".		

TMOD		Timer X Function Mode
1	0	
0	0	Timer Mode
0	1	Pulse Output Mode
1	0	Event Counter Mode
1	1	Pulse Width Measurement Mode

ELECTRIC CHARACTERISTICS

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Test conditions	Limits	Unit
V_{CC}	Supply Voltage	Output transistors are "OFF"	-0.3~7	V
V_I	Supply Voltage for LCD, VL1~VL3		-0.3~Vcc+0.3	V
V_I	Input voltage P0~P4,Xin		-0.3~Vcc+0.3	V
V_I	Input voltage |INT1, CNVss		-0.3~7	V
V_I	Input voltage |RESET, CNTR		-0.3~13	V
V_O	Output voltage P0~P3, COM0~COM3 SEG0~SEG31, Xout		-0.3~Vcc+0.3	V
V_O	Output voltage CNTR		-0.3~7	V
P_d	Power dissipation	Ta = 25 °C	300	mW
T_{opr}	Operating temperature		-10~70	°C
T_{stg}	Storage temperature		-40~125	°C

RECOMMENDED OPERATING CONDITIONS (Vcc= 2.8V~5.5V, Ta= -10 ~ 70 °C)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
Vcc	Supply Voltage (Note1)	f(Xin)=8MHz	4.5		5.5	V
		f(Xin)=1.1MHz	2.8		5.5	
Vss	Supply Voltage			0		V
Vih	"H" Input voltage P0, P1, P3.0, P3.1 (Note2) P3.3~P3.7 (Note3), P4, |RESET, Xin, CNVss		0.7*Vcc		Vcc	V
Vih	"H" Input voltage P2, P3.2, P3.4, P3.6, P3.7 (Note4), |INT1, CNTR		0.74*Vcc		Vcc	V
Vil	"L" Input voltage P0, P1, P3.0, P3.1(Note2) P3.3~P3.7(Note3), P4, CNVss		0		0.3*Vcc	V
Vil	"L" Input voltage P2, P3.2, P3.4, P3.6 (Note4), |INT1, CNTR		0		0.26*Vcc	V
Vil	"L" Input voltage |RESET		0		0.12*Vcc	V
Vil	"L" Input voltage Xin		0		0.16*Vcc	V
Ioh	"H" output current P0 ~ P3(Note5), Xout				-2	mA
Iol(peak)	"L" peak output current P0 ~ P3, CNTR, Xout(Note6)				10	mA
Iol(avg)	"L" average output current P0 ~ P3, CNTR, Xout(Note7)				5	mA
f(Xin)	Clock oscillating frequency (Note8)	Vcc=4.5~5.5V	64		8000	kHz
		Vcc=2.8~5.5V	64		1100	
f(Xcin)	Clock oscillating frequency for clock function (Note8)	Vcc=2.8~5.5V	32		50	kHz

Note 1: For RAM retention only, minimum value of Vcc is 2V.
2: When using Port P3.1 as Xcin, 0.85Vcc≤Vih≤Vcc, 0≤Vil≤0.15Vcc for port P3.1.
3: When P3.4, P3.6, and P3.7 operate as input ports.
4: When P3.4, P3.6, and P3.7 operate as RxD, CLK, and CTS input, respectively. Especially when the input oscillation frequency is more than 50 kHz, the following is recommended: 0.8Vcc≤Vih≤Vcc, 0≤Vil≤0.2Vcc
5: The total of Ioh of port P0, P1, P2, P3 and Xout should be 35mA max.
6: The total of Iol(peak) of port P0 ~ P3 should be 55mA max, and for port P3, CNTR, and Xout should be 45mA max.
7: Iol(avg) is the average current in 100ms.
8: When changing the contents of bit 0 of address $EC, f(Xin) needs the following range: f(Xin)>3f(Xcin).

ELECTRICAL CHARACTERISTICS (Vss=0V, Ta=-10~+70°C, unless otherwise noted)

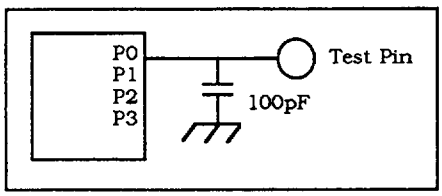
Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
Voh	"H" output voltage P0 ~ P3 (Note9, 10)	Vcc=5V, Ioh=-2mA		3			V
		Vcc=3V, Ioh=-0.7mA		2			
Voh	"H" output voltage Xout	Vcc=5V, Ioh=-1.5mA		3			V
		Vcc=3V, Ioh=-0.3mA		2			
Vol	"L" output voltage P0 ~ P3(Note10), CNTR	Vcc=5V, Iol=10mA				2	V
		Vcc=3V, Iol=0.3mA				1	
Vol	"L" output voltage Xout	Vcc=5V, Iol=1.5mA				2	V
		Vcc=3V, Iol=0.3mA				1	
Vt+~Vt-	Hysteresis IINT1, CNTR	Vcc=5V		0.25		1	V
		Vcc=3V		0.15		0.7	
Vt+~Vt-	Hysteresis P3.4, P3.6, P3.7	When used as RxD, CLK, CTS input	Vcc=5V		0.5		V
			Vcc=3V		0.4		
Vt+~Vt-	Hysteresis P3.1	When used as Xcin input	Vcc=5V		0.7		V
			Vcc=3V		0.5		
Vt+~Vt-	Hysteresis P2, P3.2	Vcc=5V			0.5		V
		Vcc=3V			0.4		
Vt+~Vt-	Hysteresis IRESET	Vcc=5V			0.5	0.7	V
		Vcc=3V			0.35		
Vt+~Vt-	Hysteresis Xin	Vcc=5V			0.5		V
		Vcc=3V			0.35		
Iil	"L" input current P4(RESET= "high") P0~P3, CNTR w/o pull-up tr. IINT1, IRESET, Xin	Vcc=5V, Vi=0V				-5	µA
		Vcc=3V, Vi=0V				-4	
Iil	"L" input current P0~P3, CNTR with pull-up tr.	Vcc=5V, Vi=0V		-30	-70	-140	µA
		Vcc=3V, Vi=0V		-6	-25	-45	
Iil	"L" input current P4 (RESET= "low")	Vcc=5V, VL3=5V, Vi=0V		-30		-140	µA
		Vcc=3V, VL3=3V, Vi=0V		-6		-45	
Iih	"H" input current P4(RESET= "high") {P0~P3, IINT1, IRESET, Xin]	Vcc=5V, Vi=5V				5	µA
		Vcc=3V, Vi=3V				4	
Iih	"H" input current P4 (RESET+ "low")	Vcc=5V,VL3=5V, Vi=5V				5	µA
		Vcc=3V,VL3=3V, Vi=3V				4	
RCOM	Output impedance COM0~COM3	VL1=Vcc/3 VL2=2VL1, VL3=Vcc Other COM,SEG pins are open	Vcc=5V	30	200	2000	Ω
			Vcc=3V	70	500	4000	
RSEG	Output impedance SEG0~SEG31		Vcc=5V		2	8	kΩ
			Vcc=3V		3		
Icc	Output pins are open. IRESET, P0~P3 are connected to Vcc. All other pins are connected to Vss. Xin and Xcin are input frequency signals.	Supply current (in operation)	f(Xin)=8MHz, Vcc=5V		6	12	mA
			f(Xin)=1MHz, Vcc=3V		0.4		
			Ta=25°C, Xin=0V f(Xcin)=32.8kHz at low power mode (XcDR=1) Vcc=5V		45	85	µA
			Ta=25°C, Xin=0V f(Xcin)=32.8kHz at low power mode (XcDR=1) Vcc=3V		18	26	
Icc		Supply current (in WAIT mode)	f(Xin)=8MHz, Vcc=5V		2		mA
			f(Xin)=1MHz, Vcc=3V		0.2		
			Ta=25°C, Xin=0 f(Xcin)=32.8kHz at low power mode (XcDR=1) Vcc=5V		20	60	µA
			Ta=25°C, Xin=0 f(Xcin)=32.8kHz at low power mode (XcDR=1) Vcc=3V		9	25	
Icc		Supply current (in STOP mode)	f(Xin)=0 f(Xcin)=0 Vcc=5V Ta=25°C		0.1	1	µA
			f(Xin)=0 f(Xcin)=0 Vcc=5V Ta=70°C			10	
Vram	RAM retention voltage	f(Xin)=0, f(Xcin)=0		2		5.5	V

Note 9: Except when the output type of P3.5 is N-channel open drain (mask option).
10: If P3.0 is used as Xcout, capability of load driving is lower than the above.

TIMING REQUIREMENTS (Vss=5V±10%, Vss=0V, Ta=-10°C~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
tw1	|INT1, |INT2 external clock input pulse width		1			µs
		Vcc=2.8V	4			µs
twR	|RESET external clock input pulse width (Note 1)		2			µs
		Vcc=2.8V	8			µs
tc	External clock input cycle time (Xin pin)		125			ns
tw	External clock input pulse width (Xin pin)		62			ns
tr	External clock rising edge time (Xin pin)				20	ns
tf	External clock falling edge time (Xin pin).				20	ns
tcc	External clock input cycle time (P31/Xcin pin, Xcin)		20			µs
twc	External clock input pulse width (P31/Xcin pin, Xcin)		5			µs
trc	External clock rising edge time (P31/Xcin pin, Xcin)				6.2	µs
tfc	External clock falling edge time (P31/Xcin pin, Xcin)				6.2	µs

Note 1: Hold RESET pin to "L" level while eight or more pulses are input from Xin.



Port P0, P1, P2, P3 Pins Test Circuit