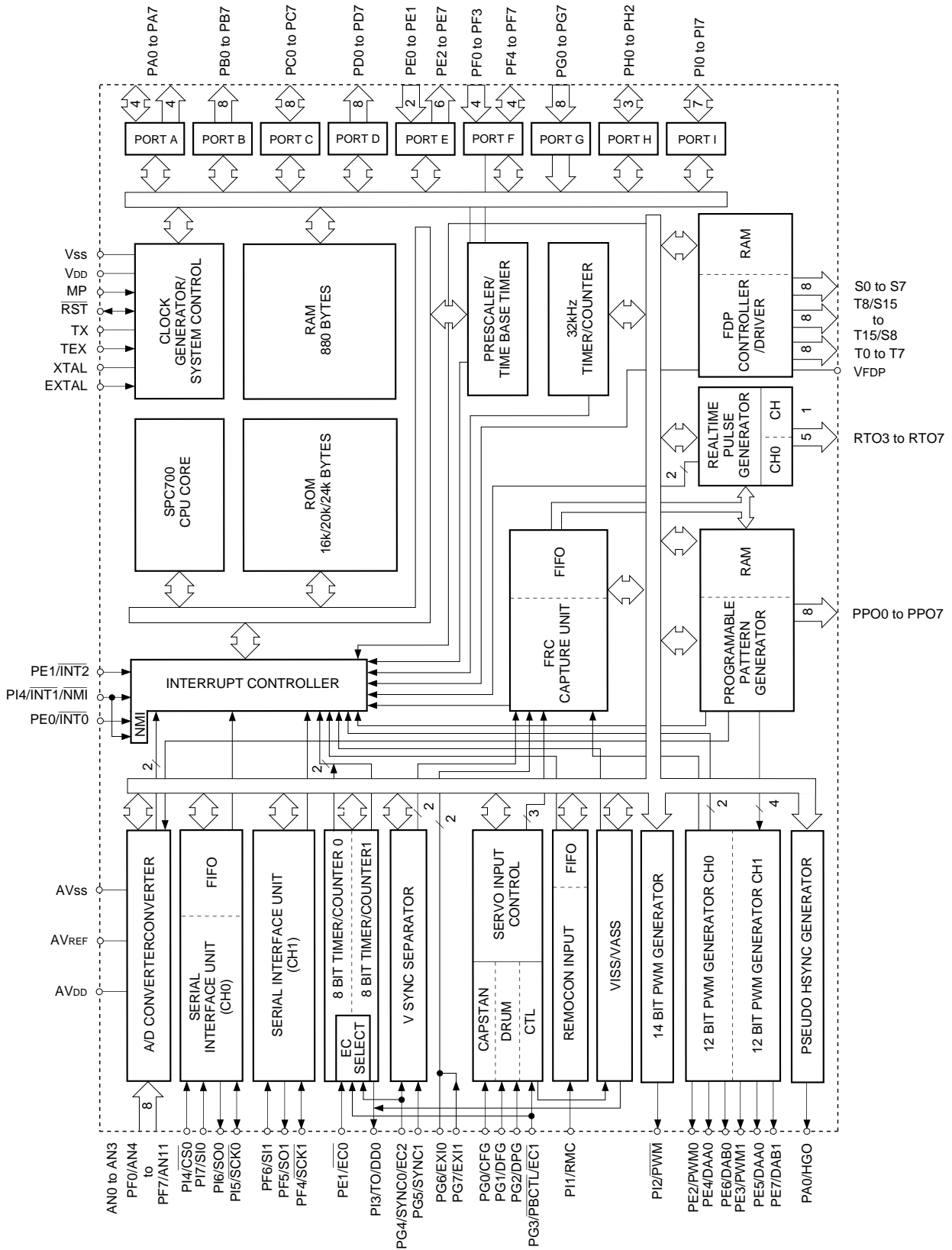
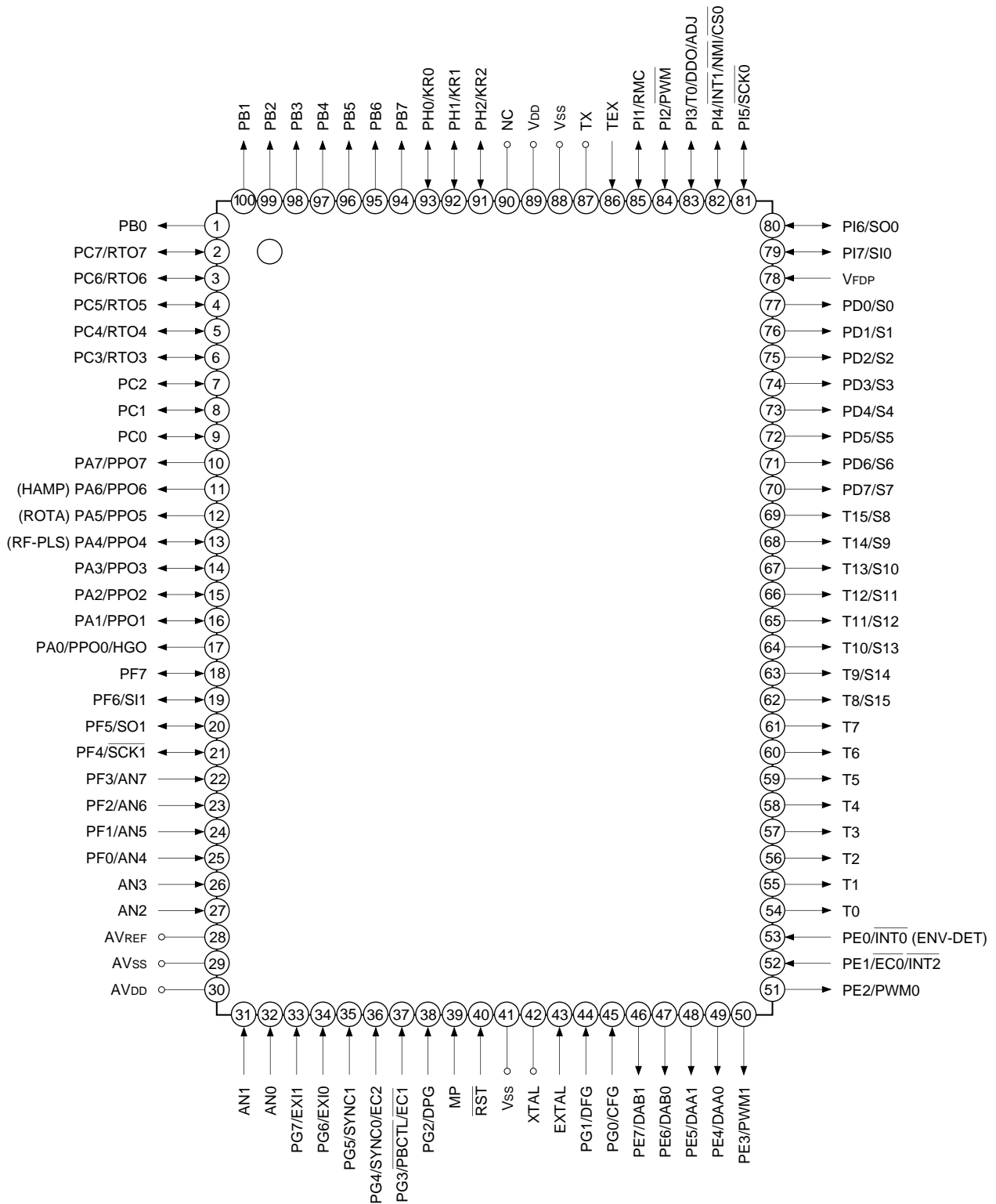


Block Diagram



Pin Configuration (Top View)



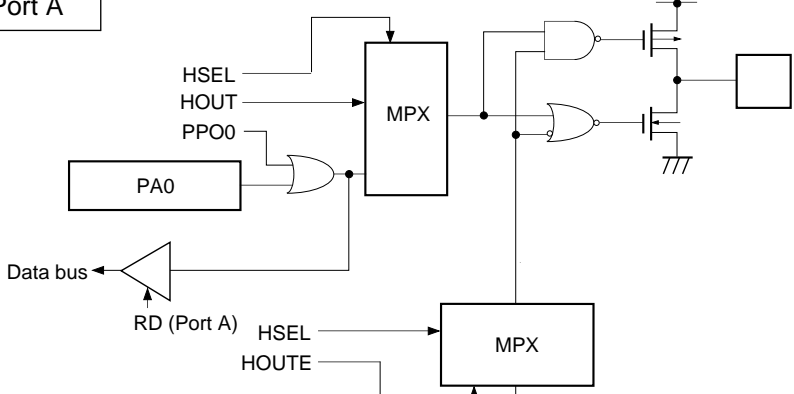
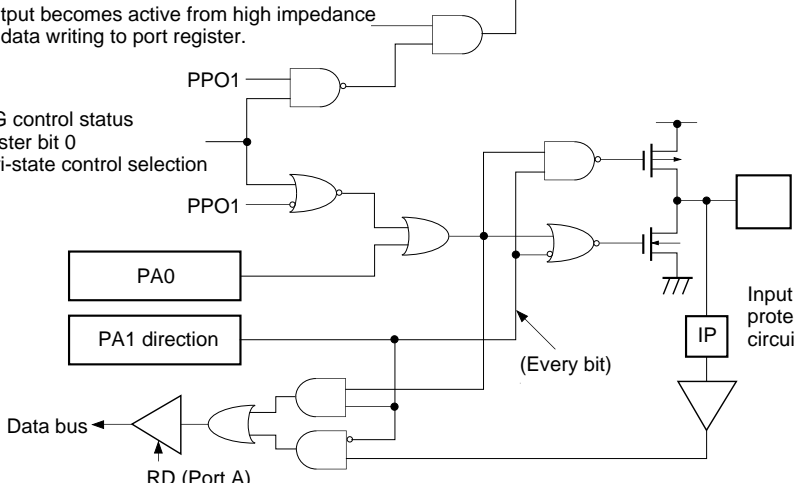
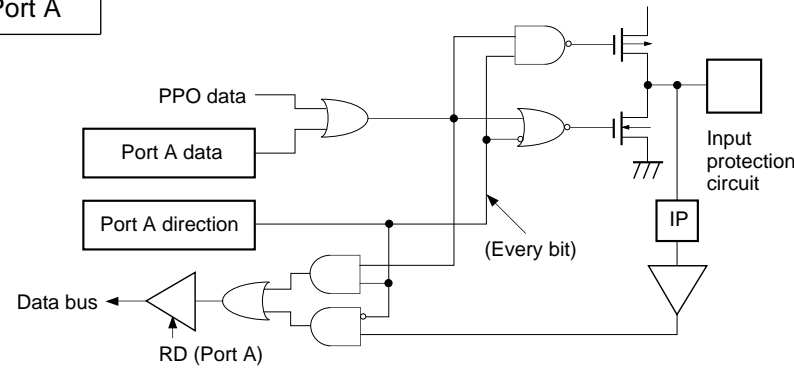
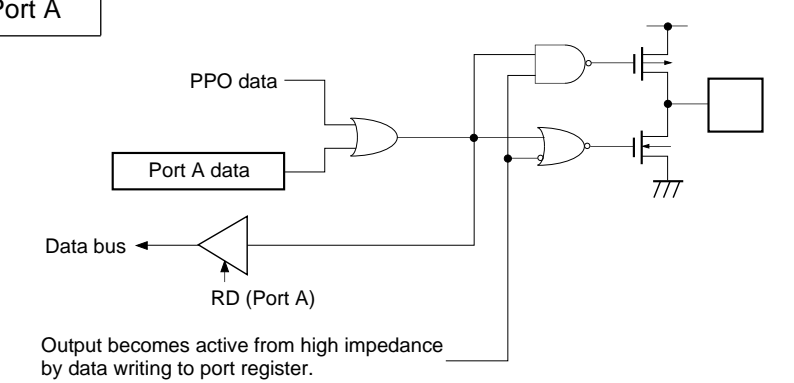
- Note)** 1. NC (Pin 90) is always connected to V_{DD}.
 2. V_{SS} (Pins 41 and 88) are both connected to GND.

Pin Description

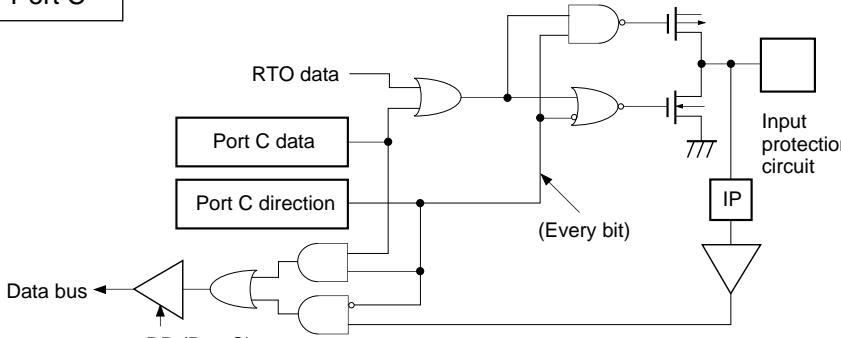
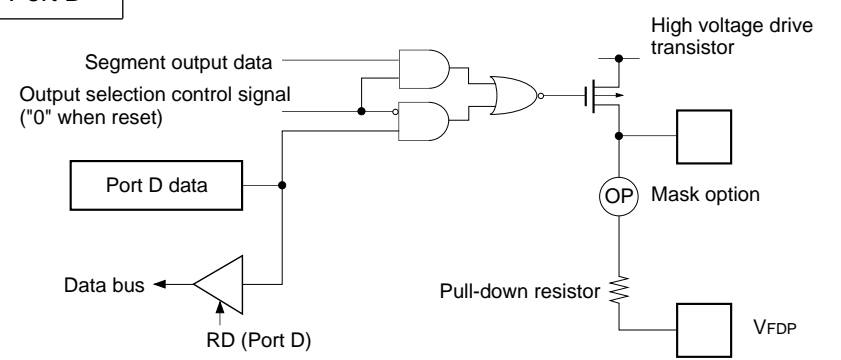
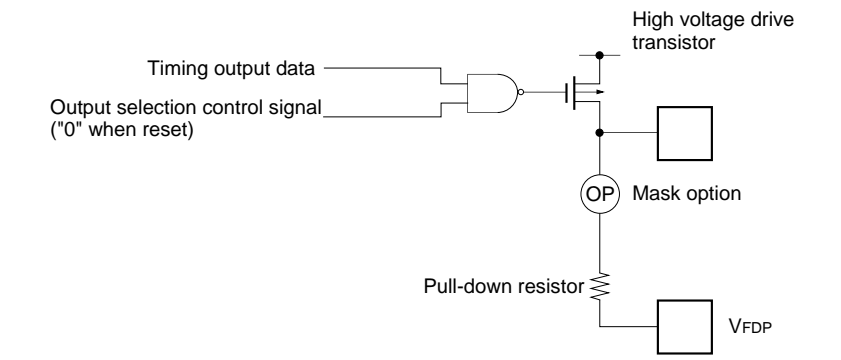
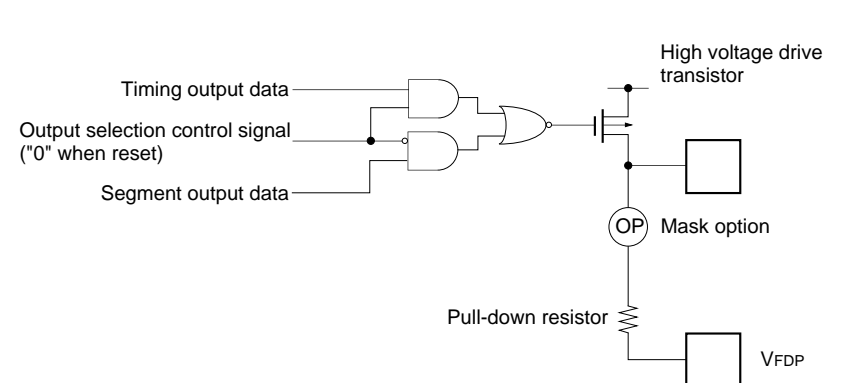
Symbol	I/O	Description		
PA0/PPO0 /HGO	Output/Real time output/Output	(Port A) 8-bit I/O port. Enable to specify I/O by bit unit. Data is gated with PPO content by OR-gate and they are output. (8 pins)	Pseudo HSYNC output pin.	
PA1/PPO1	I/O/ Real time output		Programmable pattern generator (PPG) output. Functions as high precision real-time pulse output port. (8 pins)	
PA2/PPO2				
PA3/PPO3				
PA4/PPO4				
PA5/PPO5	Output/ Real time output		Head switching output pins.	
PA6/PPO6				
PA7/PPO7				
PB0 to PB7	Output	8-bit output port. Tri-state can be controlled. (8 pins)		
PC0 to PC2	Output	(Port C) 8-bit I/O port. Enable to specify I/O by bit unit. Data is gated with RTO content by OR-gate and they are output. (8 pins)	Real-time pulse generator (RTG) output. Functions as high precision real-time pulse output port. (5 pins)	
PC3/PPO3 to PC7/PPO15	Output/ Real time output			
T0 to T7	Output	FDP timing signal output pin.		
T8/S15 to T15/S8	Output/Output	Output pins for FDP timing signal and segment signal.		
PD0/S0 to PD7/S7	Output/Output	(Port D) 8-bit output port. (8 pins)	FDP segment signal output pin.	
PE0/ $\overline{\text{INT0}}$	Input/Input	(Port E) 8-bit port. Lower 2 bits are input pins and upper 6 bits are output pins. (8 pins)	Trigger pulse input pin for head switching output.	Input pin to request external interruption. Active when falling edge.
$\overline{\text{PE1/EC0/INT2}}$	Input/Input/Input		External event input pin for timer/counter.	Input pin to request external interruption. Active when falling edge.
PE2/PWM0	Output/Output		PWM output pins. (2 pins)	
PE3/PWM1	Output/Output			
PE4/DAA0	Output/Output			DA gate pulse output pins. (2 pins)
PE5/DAA1	Output/Output			
PE6/DAB0	Output/Output			
PE7/DAB1	Output/Output			
AN0 to AN3	Input	Analog input pins to A/D converter. (8 pins)		
PF0/AN0 to PF3/AN3	Input/Input	(Port F) 8-bit I/O port. Enable to specify I/O by bit unit. (8 pins)		
PF4/ $\overline{\text{SCK1}}$	I/O/I/O			Serial clock (CH1) I/O pin.
PF5/SO1	I/O/Output			Serial data (CH1) output pin.
PF6/SI1	I/O/Input			Serial data (CH1) input pin.
PF7	I/O			

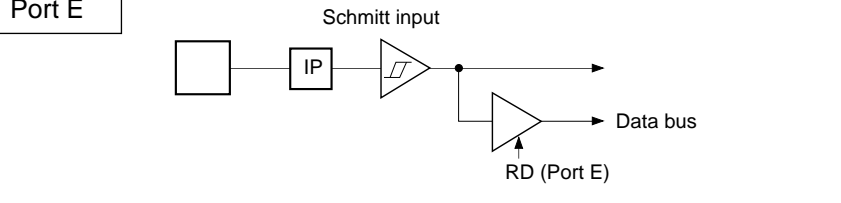
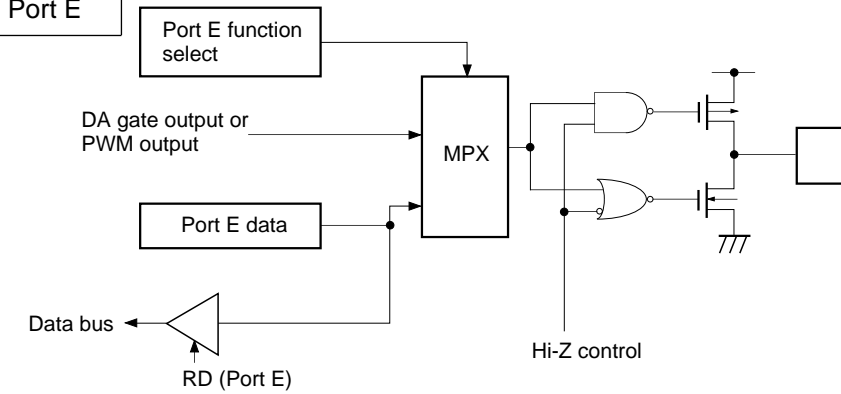
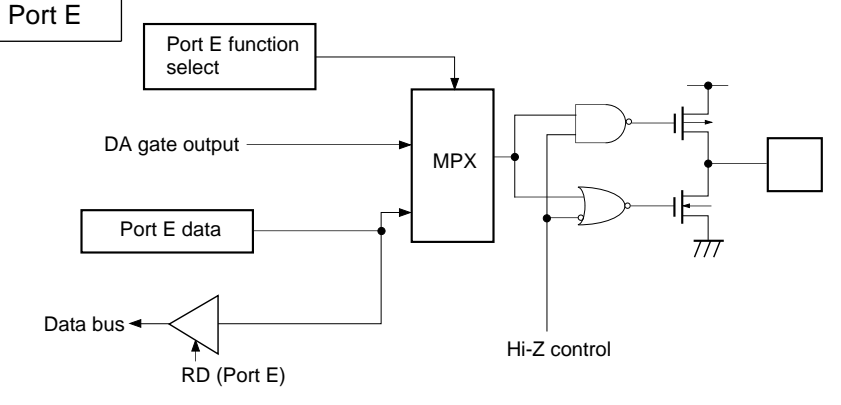
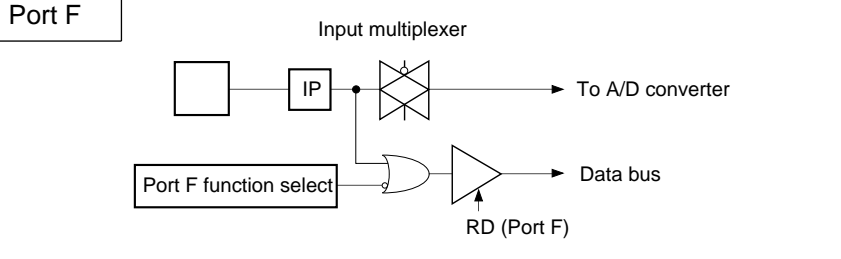
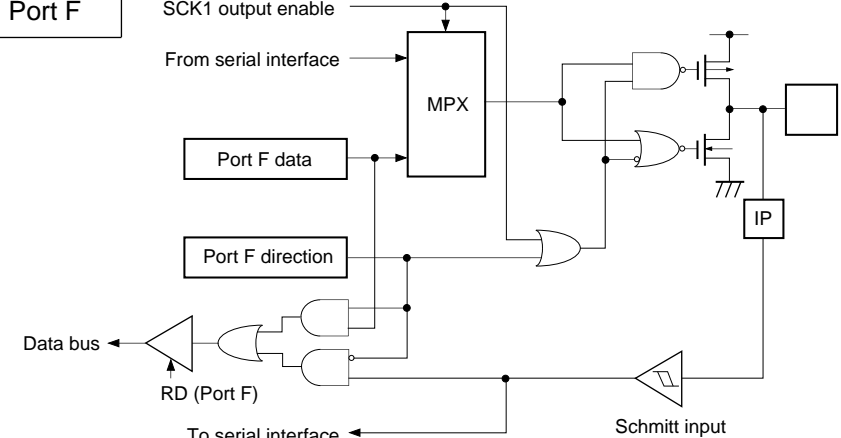
Symbol	I/O	Description		
PG0/CFG	Input/Input	(Port G) 8-bit input port. (8 pins)	Capstan FG input pin.	
PG1/DFG	Input/Input		Drum FG input pin.	
PG2/DPG	Input/Input		Drum PG input pin.	
PG3/ PBCTL/EC1	Input/Input/Input		Playback CTL input pin.	External event input pin for timer/counter.
PG4/ SYNC0/EC2	Input/Input/Input		Composite sync signal input pins.	External event input pin for timer/counter.
PG5/SYNC1	Input/Input		External input pins for FRC capture unit.	
PG6/EXI0	Input/Input			
PG7/EXI1	Input/Input			
PH0/KR0 to PH2/KR2	I/O/Input	(Port H) 3-bit I/O port. (3 pins)	Key return input signal for key scanning at FDP segment signal.	
PI1/RMC	I/O/Input	(Port I) 8-bit I/O port. Enable to specify I/O by bit unit. (8 pins)	Remote control receiving circuit input pin.	
PI2/PWM	I/O/Input		14-bit PWM output pin.	
PI3/TO/ DDO/ADJ	I/O/Output/Output/ Output		Timer/counter, CTL duty detection, 32kHz oscillation adjustment output pin.	
PI4/INT1/ NMI/CS0	I/O/Input/ Input/Input		Input pin to request external interruption, non-maskable interruption and for serial chip select (CH0). Active when falling edge.	
PI5/SCK0	I/O/Input		Serial clock (CH1) I/O pin.	
PI6/SO0	I/O/Output		Serial data (CH1) output pin.	
PI7/SI0	I/O/Input		Serial data (CH1) input pin.	
EXTAL	Input		Connecting pin of crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and input opposite phase clock to XTAL pin.	
XTAL	Output			
TEX	Input	Connecting pin of crystal oscillator for 32kHz timer clock. When used as event counter, input to TEX pin and leave TX pin open. (Feedback resistor is not removed.)		
TX	Output			
RST	Input	System reset pin of active "L" level.		
MP	Input	Microprocessor mode input pin. Always connect to GND.		
V _{FDP}		FDP voltage supply pin when specifying internal resistor by mask option.		
AV _{DD}		Positive power supply pin of A/D converter.		
AV _{REF}	Input	Reference voltage input pin of A/D converter.		
AV _{SS}		GND pin of A/D converter.		
V _{DD}		Positive power supply pin.		
V _{SS}		GND pin. Connect both V _{SS} pins to GND.		

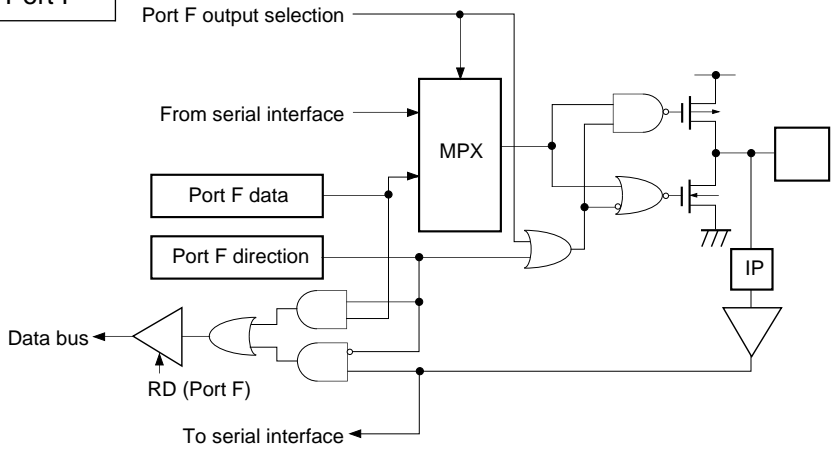
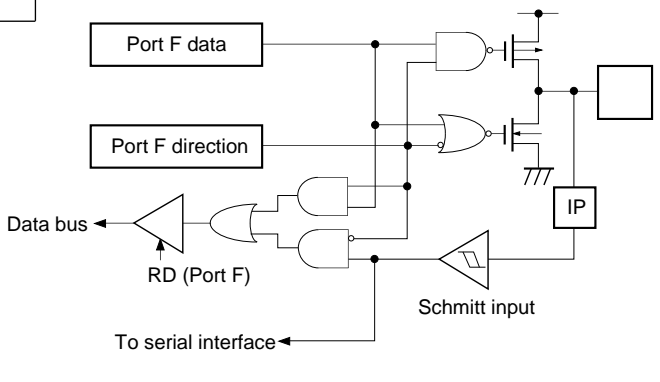
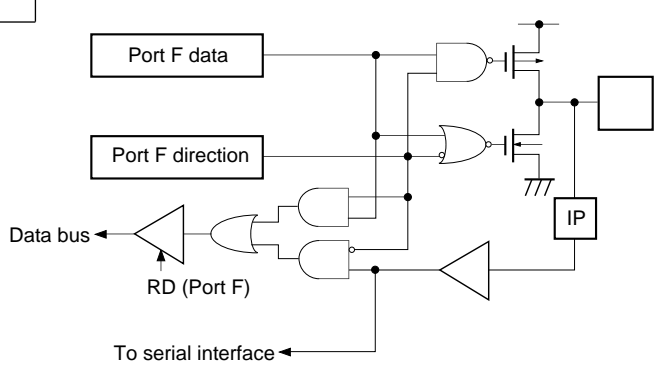
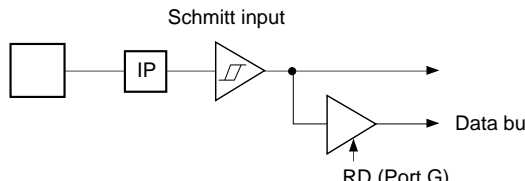
Input/Output Circuit Formats for Pins

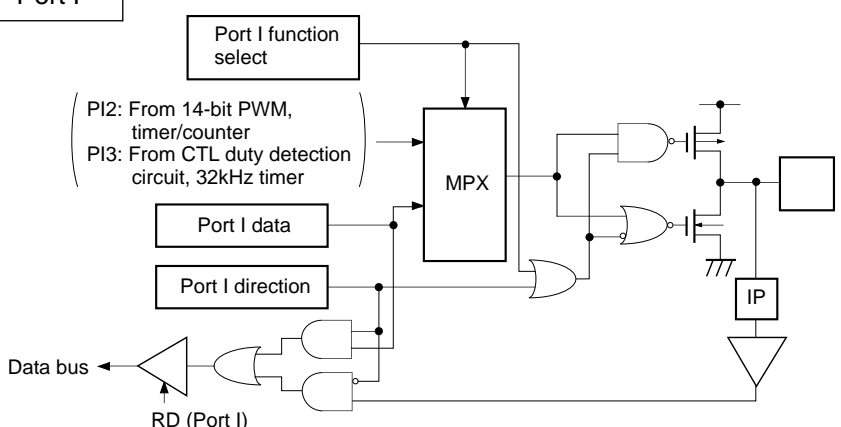
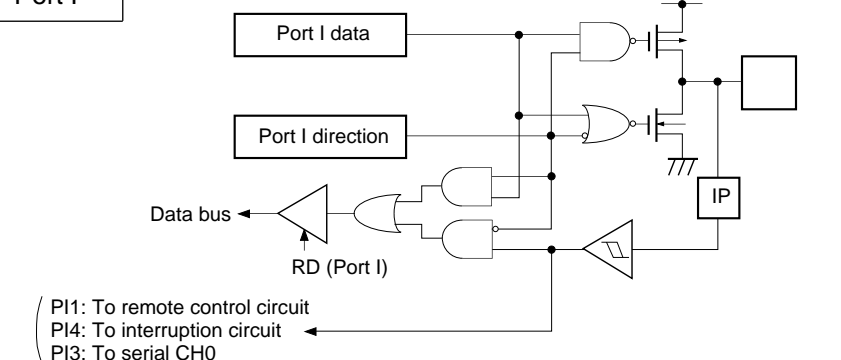
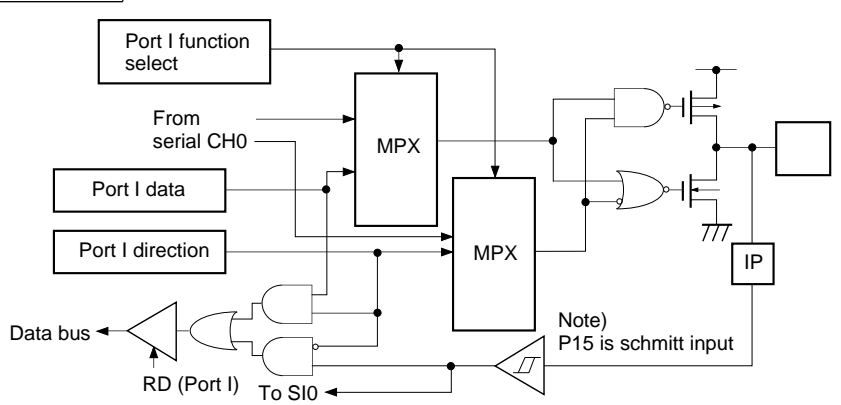
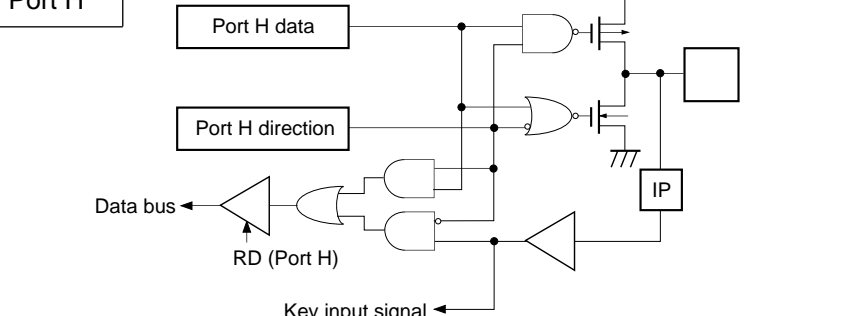
Pin	Circuit format	When reset
<p>PA0/PPO0/HGO</p> <p>1 pin</p>	<p>Port A</p>  <p>Output becomes active from high impedance by data writing to port register.</p>	<p>Hi-Z</p>
<p>PA1/PPO1</p> <p>1 pin</p>	<p>PPG control status register bit 0 Tri-state control selection</p>  <p>(Every bit)</p> <p>Input protection circuit</p>	<p>Hi-Z</p>
<p>PA2/PPO2 to PA4/PPO4</p> <p>3 pins</p>	<p>Port A</p>  <p>(Every bit)</p> <p>Input protection circuit</p>	<p>Hi-Z</p>
<p>PA5/PPO5 to PA7/PPO7</p> <p>3 pins</p>	<p>Port A</p>  <p>Output becomes active from high impedance by data writing to port register.</p>	<p>Hi-Z</p>

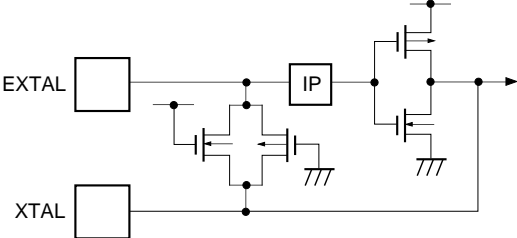
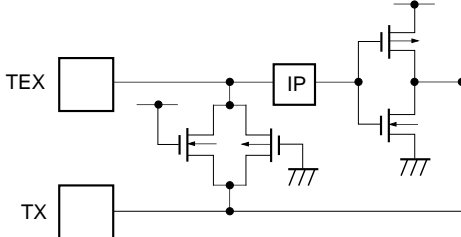
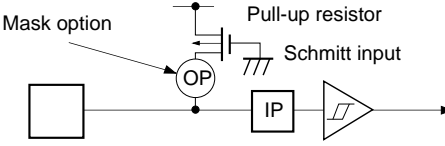
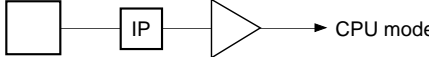
Pin	Circuit format	When reset
PB0 to PB7 8 pins	<p>Port B</p> <p>Port B data</p> <p>Data bus</p> <p>RD (Port B)</p> <p>Port B tri-state control</p>	Hi-Z
PC0 to PC2 3 pins	<p>Port C</p> <p>Port C data</p> <p>Port C direction</p> <p>Data bus</p> <p>RD (Port C)</p> <p>(Every bit)</p> <p>Input protection circuit</p>	Hi-Z
PC3/RTO3 1 pin	<p>Port C</p> <p>RTO3</p> <p>PC3</p> <p>PC3 direction</p> <p>Data bus</p> <p>RD (Port C)</p> <p>(Every bit)</p> <p>Input protection circuit</p>	Hi-Z
PC3/RTO4 1 pin	<p>Port C</p> <p>RTO4</p> <p>RTG interruption control register bit 7 Tri-state control selection</p> <p>PC4</p> <p>PC4 direction</p> <p>Data bus</p> <p>RD (Port C)</p> <p>(Every bit)</p> <p>Input protection circuit</p>	Hi-Z

Pin	Circuit format	When reset
<p>PC5/RTO5 to PC7/RTO7</p> <p>3 pins</p>	<p>Port C</p>  <p>RTO data</p> <p>Port C data</p> <p>Port C direction</p> <p>(Every bit)</p> <p>Input protection circuit</p> <p>IP</p> <p>Data bus</p> <p>RD (Port C)</p>	<p>Hi-Z</p>
<p>PD0/S0 to PD7/S7</p> <p>8 pins</p>	<p>Port D</p>  <p>Segment output data</p> <p>Output selection control signal ("0" when reset)</p> <p>Port D data</p> <p>Data bus</p> <p>RD (Port D)</p> <p>High voltage drive transistor</p> <p>Mask option</p> <p>OP</p> <p>Pull-down resistor</p> <p>VFDP</p>	<p>Hi-Z</p>
<p>T0 to T7</p> <p>8 pins</p>	 <p>Timing output data</p> <p>Output selection control signal ("0" when reset)</p> <p>High voltage drive transistor</p> <p>Mask option</p> <p>OP</p> <p>Pull-down resistor</p> <p>VFDP</p>	<p>Hi-Z</p>
<p>T8/S15 to T15/S8</p> <p>8 pins</p>	 <p>Timing output data</p> <p>Output selection control signal ("0" when reset)</p> <p>Segment output data</p> <p>High voltage drive transistor</p> <p>Mask option</p> <p>OP</p> <p>Pull-down resistor</p> <p>VFDP</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PE0/$\overline{\text{INT0}}$ PE1/$\overline{\text{EC0/INT2}}$</p> <p>2 pins</p>	<p>Port E</p> 	<p>Hi-Z</p>
<p>PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1</p> <p>4 pins</p>	<p>Port E</p> 	<p>Hi-Z</p>
<p>PE6/DAB0 PE7/DAB1</p> <p>2 pins</p>	<p>Port E</p> 	<p>High level</p>
<p>PF0/AN4 to PF3/AN7</p> <p>4 pins</p>	<p>Port F</p> 	<p>Hi-Z</p>
<p>PF4/$\overline{\text{SCK1}}$</p> <p>2 pins</p>	<p>Port F</p> 	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PF5/SO1</p> <p>1 pin</p>	<p>Port F</p>  <p>Port F output selection</p> <p>From serial interface</p> <p>MPX</p> <p>Port F data</p> <p>Port F direction</p> <p>Data bus</p> <p>RD (Port F)</p> <p>To serial interface</p>	<p>Hi-Z</p>
<p>PF6/SI1</p> <p>1 pin</p>	<p>Port F</p>  <p>Port F data</p> <p>Port F direction</p> <p>Data bus</p> <p>RD (Port F)</p> <p>To serial interface</p> <p>Schmitt input</p>	<p>Hi-Z</p>
<p>PF7</p> <p>1 pin</p>	<p>Port F</p>  <p>Port F data</p> <p>Port F direction</p> <p>Data bus</p> <p>RD (Port F)</p> <p>To serial interface</p>	<p>Hi-Z</p>
<p>PG0/CFG PG1/DFG PG2/DPG PG3/PBCTL/ EC1 PG4/SYNC0/ EC2 PG5/SYNC1 PG6/EXI0 PG7/EXI1</p> <p>8 pins</p>	<p>Port G</p>  <p>Schmitt input</p> <p>IP</p> <p>Data bus</p> <p>RD (Port G)</p> <p>Note) For PG4/SYNC and PG5/SYNC1, CMOS schmitt input or TTL schmitt input can be selected with the mask option.</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PI2/$\overline{\text{PWM}}$ PI3/$\overline{\text{TO}}$/ $\overline{\text{DDO/ADJ}}$</p> <p>2 pins</p>	<p>Port I</p>  <p>Port I function select</p> <p>(PI2: From 14-bit PWM, timer/counter PI3: From CTL duty detection circuit, 32kHz timer)</p> <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>IP</p>	<p>Hi-Z</p>
<p>PI1/$\overline{\text{RMC}}$ PI4/$\overline{\text{INT1}}$/ $\overline{\text{NMI/CS0}}$ PI7/$\overline{\text{SI0}}$</p> <p>3 pins</p>	<p>Port I</p>  <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>IP</p> <p>(PI1: To remote control circuit PI4: To interruption circuit PI3: To serial CH0)</p>	<p>Hi-Z</p>
<p>PI5/$\overline{\text{SCK0}}$ PI6/$\overline{\text{SO0}}$</p> <p>2 pins</p>	<p>Port I</p>  <p>Port I function select</p> <p>From serial CH0</p> <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>To SI0</p> <p>Schmitt input</p> <p>Note) P15 is schmitt input</p> <p>IP</p>	<p>Hi-Z</p>
<p>PH0/$\overline{\text{KR0}}$ to PH2/$\overline{\text{KR2}}$</p> <p>3 pins</p>	<p>Port H</p>  <p>Port H data</p> <p>Port H direction</p> <p>Data bus</p> <p>RD (Port H)</p> <p>Key input signal</p> <p>IP</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>EXTAL XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Shows the circuit composition during oscillation. • Feedback resistor is removed during stop. 	<p>Hi-Z</p>
<p>TEX TX</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Shows the circuit composition during oscillation. • Feedback resistor is removed during 32kHz oscillation circuit stop by software. At this time TEX pin outputs "L" level and TX pin outputs "H" level. 	<p>Oscillation</p>
<p>$\overline{\text{RST}}$</p> <p>1 pin</p>	 <p>Mask option</p> <p>Pull-up resistor</p> <p>Schmitt input</p>	<p>Hi-Z or Pull up</p>
<p>MP</p> <p>1 pin</p>	 <p>CPU mode</p>	<p>Hi-Z</p>

Absolute Maximum Ratings

(V_{SS} = 0V)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	-0.3 to +7.0	V	
	AV _{DD}	AV _{SS} to +7.0* ¹	V	
	AV _{SS}	-0.3 to +0.3	V	
Input voltage	V _{IN}	-0.3 to +7.0* ²	V	
Output voltage	V _{OUT}	-0.3 to +7.0* ²	V	
Display output voltage	V _{OD}	V _{DD} - 40 to V _{DD} + 0.3	V	As P-channel transistor is open drain, V _{DD} is reference.
High level output current	I _{OH}	-5	mA	All pins excluding display outputs (value per pin)* ³
	I _{ODH1}	-15	mA	Display outputs S0 to S7 (value per pin)
	I _{ODH2}	-35	mA	Display outputs T0 to T7, and T8/S15 to T15/S8 (value per pin)
High level total output current	∑I _{OH}	-50	mA	Total for all pins excluding display outputs
	∑I _{ODH}	-100	mA	Total for all display outputs
Low level output current	I _{OL}	15	mA	
Low level total output current	∑I _{OL}	130	mA	Total for all outputs
Operating temperature	T _{opr}	-20 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	600	mW	

*1 AV_{DD} and V_{DD} should be set to a same voltage.

*2 V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*3 It specifies output current of general-purpose I/O port.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	4.5	5.5	V	Guaranteed range during high speed mode (1/2 dividing clock) operation
		3.5	5.5		Guaranteed range during low speed mode (1/16 dividing clock) operation
		2.7	5.5		Guaranteed operation range by TEX clock
		2.5	5.5		Guaranteed data hold operation range during STOP
Analog power supply	AV _{DD}	4.5	5.5	V	*1
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*2
	V _{IHS}	0.8V _{DD}	V _{DD}	V	CMOS schmitt input*3
	V _{IHTS}	2.2	V _{DD}	V	TTL schmitt input*4
	V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL pin*5 TEX pin*6
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	*2
	V _{ILS}	0	0.2V _{DD}	V	CMOS schmitt input*3
	V _{ILTS}	0	0.8	V	TTL schmitt input*4
	V _{ILEX}	-0.3	0.4	V	EXTAL pin*5 TEX pin*6
Operating temperature	T _{opr}	-20	+75	°C	

*1 AV_{DD} and V_{DD} should be set to a same voltage.

*2 Normal input port (each pin of PA1 to PA4, PC, PF0 to PF3, PF5, PF7, PH, PI2, PI3 and PI6), MP pin

*3 Each pin of \overline{RST} , PE0/ $\overline{INT0}$, PE1/ $\overline{EC0}$ / $\overline{INT2}$, PF4/ $\overline{SCK1}$, PF6/ $\overline{SI1}$, PI1/ \overline{RMC} , PI4/ $\overline{CS0}$ / \overline{NMI} / $\overline{INT1}$, PI5/ $\overline{SCK0}$, PI7/ $\overline{SI1}$ and PG (For PG4 and PG5, when CMOS schmitt input is selected with mask option)

*4 Each pin of PG4 and PG5 (When TTL schmitt input is selected with mask option)

*5 It specifies only when the external clock is input.

*6 It specifies only when the external event is input.

DC Characteristics

(Ta = -20 to +75°C, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	VOH	PA to PC, PE PF4 to PF7, PH, PI1 to PI7, RST*1	VDD = 4.5V, IOH = -0.5mA	4.0			V
			VDD = 4.5V, IOH = -1.2mA	3.5			V
Low level output voltage	VOL	PI1 to PI7, RST*1 (VOL only)	VDD = 4.5V, IOL = 1.8mA			0.4	V
			VDD = 4.5V, IOL = 3.6mA			0.6	V
Display output current	IOH	S0 to S7		-8			mA
		S8/T15 to S15/T8, T0 to T7	VDD = 4.5V, VOH = VDD - 2.5V	-20			mA
Open drain output leakage current (P-CH Tr OFF in)	ILOL	S0 to S7, S8/T15 to S15/T8, T0 to T7	VDD = 5.5V, VOL = VDD - 35V VFDP = VDD - 35V			-20	μA
Pull-down resistor*3	RL	S0 to S7, S8/T15 to S15/T8, T0 to T7	VDD = 5V, VOD - VFDP = 30V	60	100	270	kΩ
Input current	IIHE	EXTAL	VDD = 5.5V, VIH = 5.5V	0.5		40	μA
			VDD = 5.5V, VIL = 0.4V	-0.5		-40	μA
	IILE	TEX	VDD = 5.5V, VIH = 5.5V	0.1		10	μA
			VDD = 5.5V, VIL = 0.4V	-0.1		-10	μA
II LR	RST*2	VDD = 5.5V, VIL = 0.4V	-1.5		-400	μA	
I/O leakage current	IIZ	PA to PC, PE to PI, AN1 to AN3, MP, RST*2	VDD = 5.5V, VI = 0, 5.5V			±10	μA
Supply current*4	IDD1	VDD, VSS	16MHz crystal oscillation (C1 = C2 = 15pF), VDD = 5V ± 10%*5		23	45	mA
	IDDS1		16MHz crystal oscillation (C1 = C2 = 15pF), VDD = 5V ± 10%, SLEEP mode		1.2	8	mA
	IDD2		32kHz crystal oscillation (C1 = C2 = 47pF), VDD = 3V ± 10%		38	100	μA
	IDDS2		32kHz crystal oscillation (C1 = C2 = 47pF), VDD = 3V ± 10%, SLEEP mode		7	30	μA
	IDDS3		VDD = 5.5V, STOP mode (32kHz, 16MHz oscillation stop)			10	μA
Input capacity	CIN	Other than S0 to S15, T0 to T7, PA0, PA5 to PA7 PE2 to PE7 PB, VDD, VSS AVDD, AVSS	Clock 1MHz 0V other than the measured pins		10	20	pF

- *1 $\overline{\text{RST}}$ pin is specified when evaluation mode is in use.
- *2 $\overline{\text{RST}}$ pin specifies the input current when the pull-up resistor is selected, and specifies leakage current when non-resistor is selected.
- *3 When built-in pull-down resistor is selected with mask option.
- *4 When entire output pins are open.
- *5 When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 0002FEH) to "00" and operating in high speed mode (1/2 dividing clock).

AC Characteristics

(1) Clock timing

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
System clock frequency	f_c	XTAL EXTAL	Fig. 1, Fig. 2	1		16	MHz
System clock input pulse width	t_{XL} , t_{XH}	XTAL EXTAL	Fig. 1, Fig. 2 External clock drive	28			ns
System clock input rise and fall times	t_{CR} , t_{CF}	XTAL EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count clock input pulse width	t_{EH} , t_{EL}	$\overline{\text{EC0}}$, $\overline{\text{EC1}}$, EC2	Fig. 3	$t_{\text{sys}} + 200^*$			ns
Event count clock input rise and fall times	t_{ER} , t_{EF}	$\overline{\text{EC0}}$, $\overline{\text{EC1}}$, EC2	Fig. 3			20	ms
System clock frequency	f_c	TEX TX	$V_{DD} = 2.7$ to 5.5V Fig. 2 (32kHz clock applying condition)		32.768		kHz
Event count clock input pulse width	t_{TL} , t_{TH}	TEX	Fig. 3	10			μs
Event count clock input rise and fall times	t_{TR} , t_{TF}	TEX	Fig. 3			20	ms

* t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

$t_{\text{sys}} [\text{ns}] = 2000/f_c$ (Upper 2 bits = "00"), $4000/f_c$ (Upper 2 bits = "01"), $16000/f_c$ (Upper 2 bits = "11")

Fig. 1. Clock timing

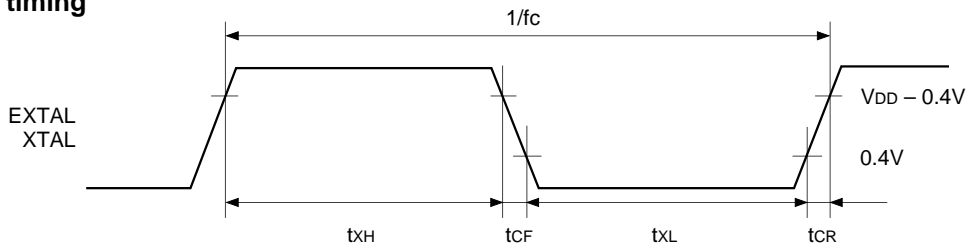


Fig. 2. Clock applying condition

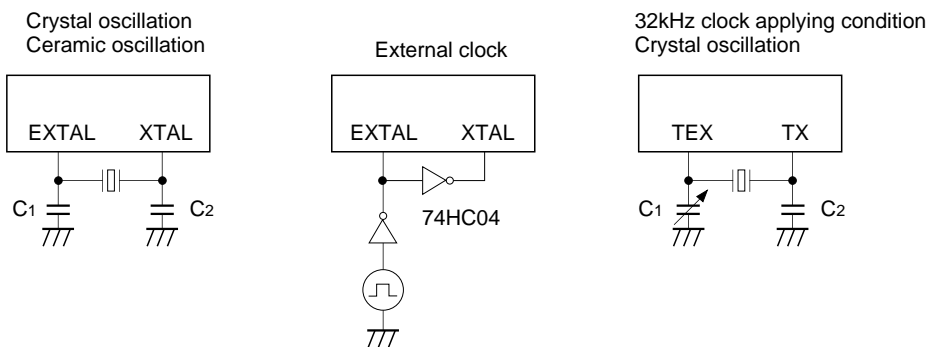
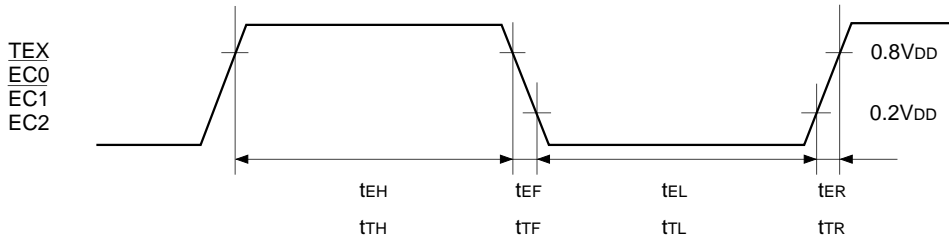


Fig. 3. Event count clock timing



(2) Serial transfer (CH0)

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$)

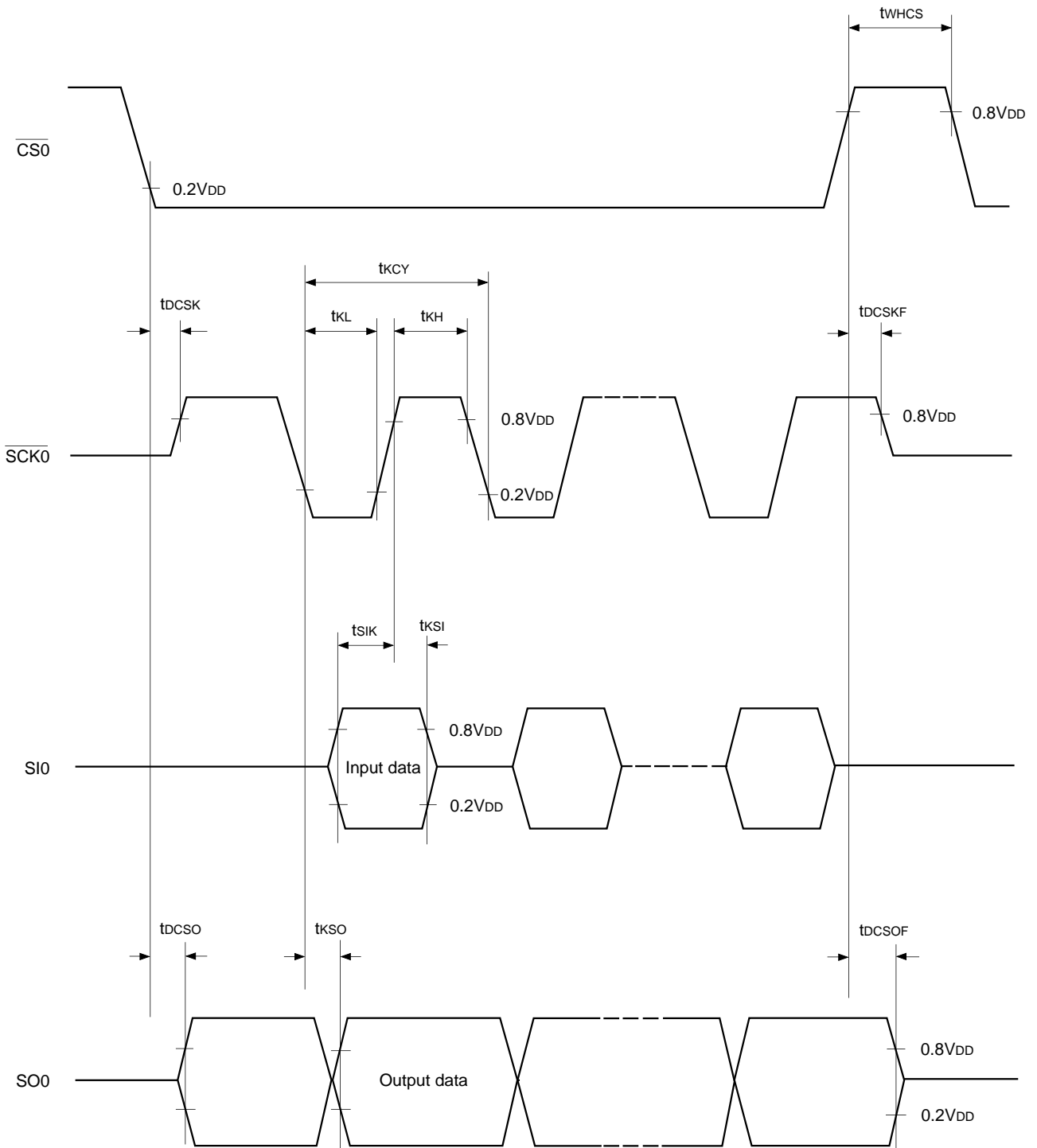
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{CS0}} \downarrow \rightarrow \overline{\text{SCK0}}$ delay time	t_{DCSK}	$\overline{\text{SCK0}}$	Chip select transfer mode ($\overline{\text{SCK0}}$ = output mode)		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS0}} \uparrow \rightarrow \overline{\text{SCK0}}$ floating delay time	t_{DCSKF}	$\overline{\text{SCK0}}$	Chip select transfer mode ($\overline{\text{SCK0}}$ = output mode)		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS0}} \downarrow \rightarrow \text{SO0}$ delay time	t_{DCSO}	SO0	Chip select transfer mode		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS0}} \uparrow \rightarrow \text{SO0}$ floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS0}}$ high level width	t_{WHCS}	$\overline{\text{CS0}}$	Chip select transfer mode	$t_{\text{sys}} + 200$		ns
$\overline{\text{SCK0}}$ cycle time	t_{KCY}	$\overline{\text{SCK0}}$	Input mode	$2t_{\text{sys}} + 200$		ns
			Output mode	$16000/f_c$		ns
$\overline{\text{SCK0}}$ high and low level widths	t_{KH} t_{KL}	$\overline{\text{SCK0}}$	Input mode	$t_{\text{sys}} + 100$		ns
			Output mode	$8000/f_c - 50$		ns
SI0 input set-up time (against $\overline{\text{SCK0}} \uparrow$)	t_{SIK}	SI0	$\overline{\text{SCK0}}$ input mode	100		ns
			$\overline{\text{SCK0}}$ output mode	200		ns
SI0 input hold time (against $\overline{\text{SCK0}} \uparrow$)	t_{KSI}	SI0	$\overline{\text{SCK0}}$ input mode	$t_{\text{sys}} + 200$		ns
			$\overline{\text{SCK0}}$ output mode	100		ns
$\overline{\text{SCK0}} \downarrow \rightarrow \text{SO0}$ delay time	t_{KSO}	SO0	$\overline{\text{SCK0}}$ input mode		$t_{\text{sys}} + 200$	ns
			$\overline{\text{SCK0}}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = $2000/f_c$ (Upper 2 bits = "00"), $4000/f_c$ (Upper 2 bits = "01"), $16000/f_c$ (Upper 2 bits = "11")

Note 2) The load of $\overline{\text{SCK0}}$ output mode and SO0 output delay time is $50\text{pF} + 1\text{TTL}$.

Fig. 4. Serial transfer CH0 timing



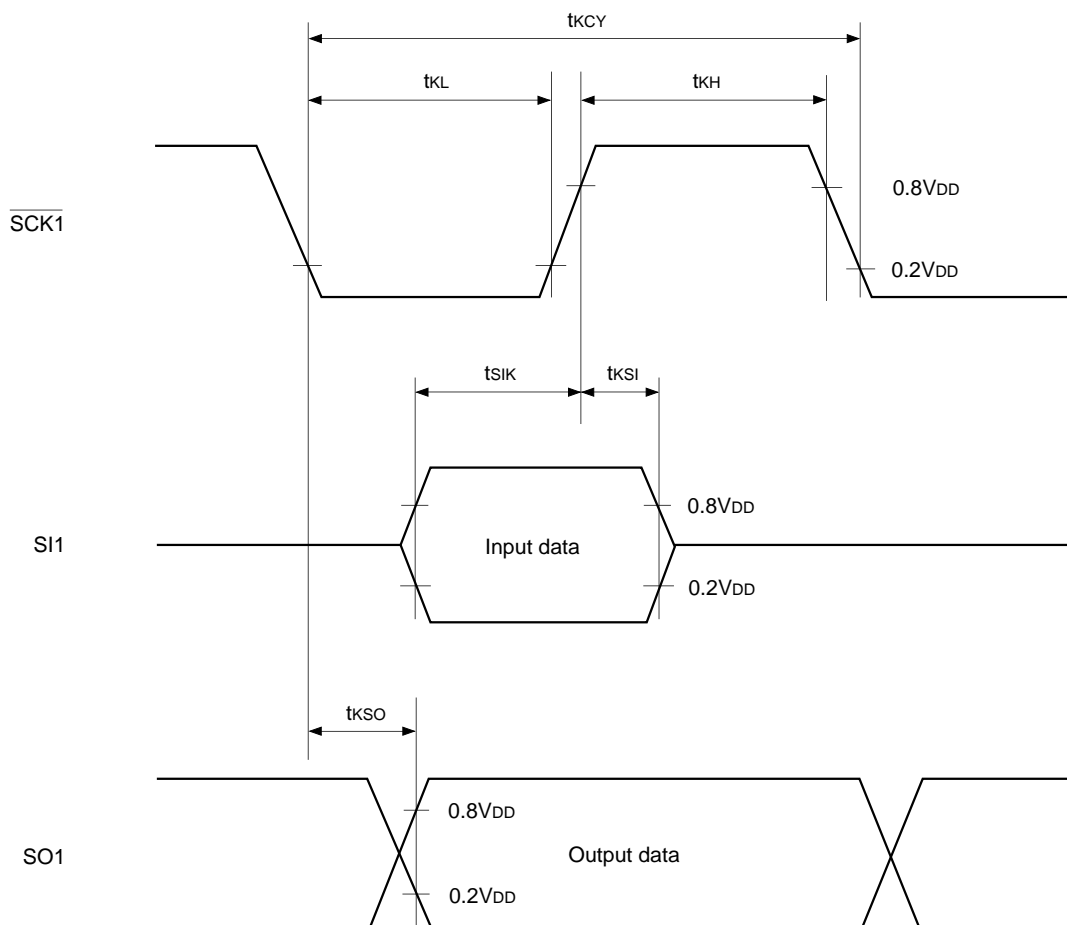
Serial transfer (CH1)

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY}	$\overline{\text{SCK1}}$	Input mode	1000		ns
			Output mode	$16000/f_c$		ns
$\overline{\text{SCK1}}$ high and low level widths	t_{KH} t_{KL}	$\overline{\text{SCK1}}$	Input mode	400		ns
			Output mode	$8000/f_c - 50$		ns
SI1 input set-up time (against $\overline{\text{SCK1}} \uparrow$)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (against $\overline{\text{SCK1}} \uparrow$)	t_{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	200		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}} \downarrow \rightarrow \text{SO1}$ delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		200	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

Note) The load of $\overline{\text{SCK1}}$ output mode and SO1 output delay time is $50\text{pF} + 1\text{TTL}$.

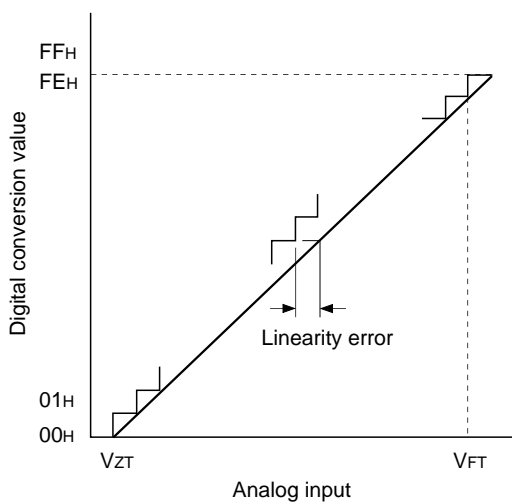
Fig. 5. Serial transfer CH1 timing



(3) A/D converter characteristics (Ta = -20 to +75°C, VDD = AVDD = 4.5 to 5.5V, AVREF = 4.0 to AVDD, VSS = AVSS =

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Only for A/D converter operation Ta = 25°C VDD = AVDD = AVREF = 5.0V			±1	LSB
Absolute error						±2	LSB
Conversion time	t _{CONV}			160/f _{ADC}			µs
Sampling time	t _{SAMP}			12/f _{ADC}			µs
Reference input voltage	V _{REF}	AV _{REF}	V _{DD} = AV _{DD} = 4.5 to 5.5V	AV _{DD} - 0.5		AV _{DD}	V
Analog input voltage	V _{IAN}	AN0 to AN7		0		AV _{REF}	V
AV _{REF} current	I _{REF}	AV _{REF}	Operation mode AV _{REF} = 4.0 to 5.5V		0.6	1.0	mA
			SLEEP mode STOP mode 32kHz operation mode				10

Fig. 6. Definitions of A/D converter terms



* The value of f_{ADC} is as follows by selecting ADC operation clock (MSC: Address 01FEH bit 0).
 When PS2 is selected, f_{ADC} = fc/2
 When PS1 is selected, f_{ADC} = fc

(4) Interruption, reset input (Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t _{IH} t _{IL}	$\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$ $\overline{\text{NMI}}$		1		μs
Reset input low level width	t _{RSL}	$\overline{\text{RST}}$		32/fc		μs

Fig. 7. Interruption input timing

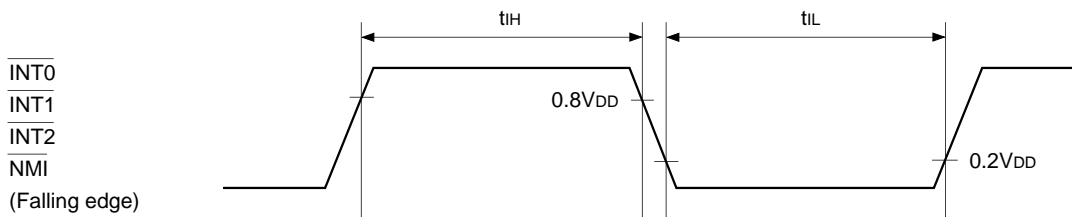
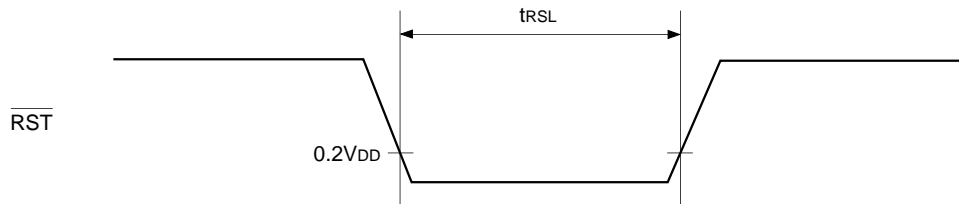


Fig. 8. Reset input timing



(5) Others (Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

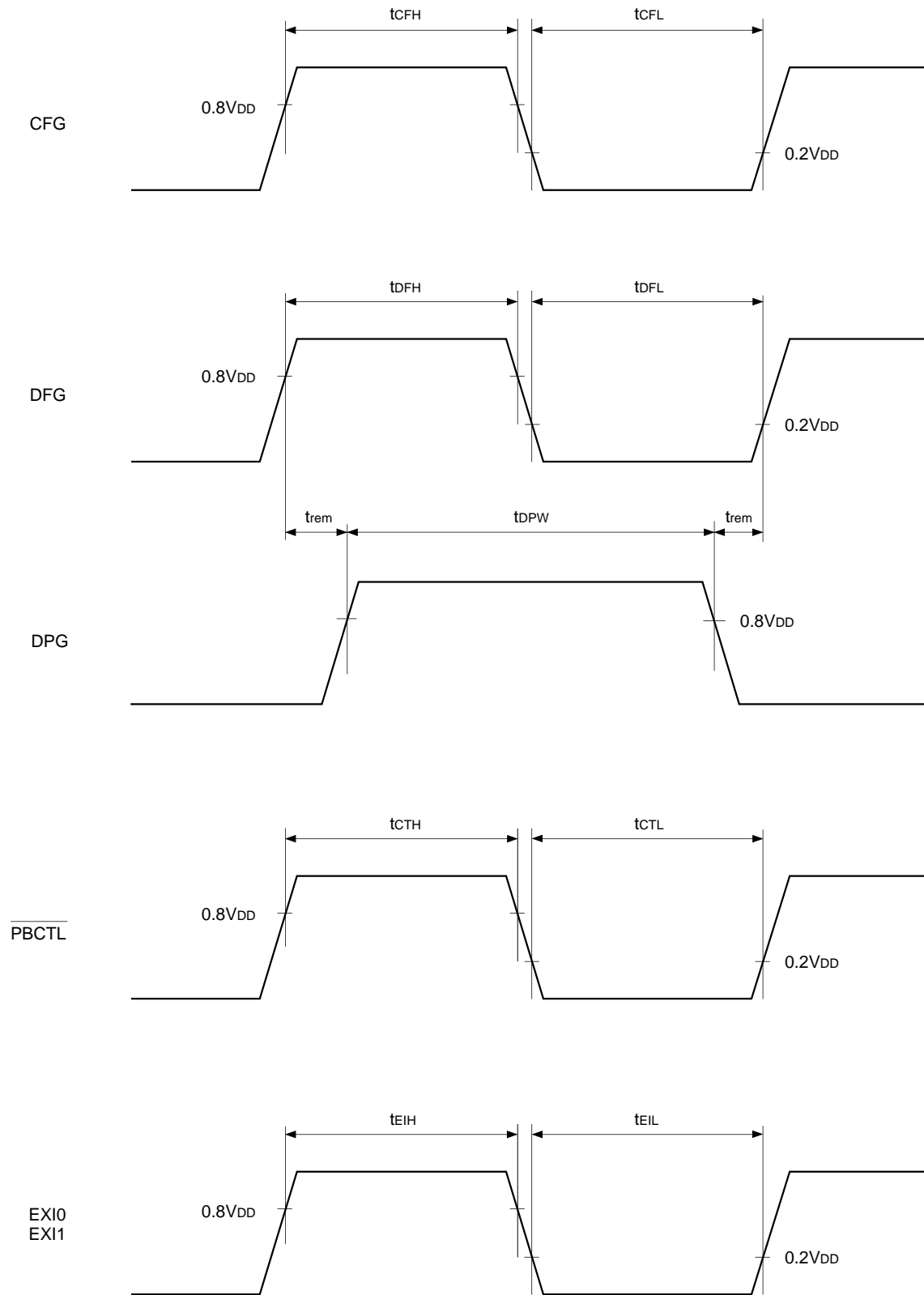
Item	Symbol	Pin	Condition	Min.	Max.	Unit
CFG input high and low level widths	t _{CFH} t _{CFL}	CFG		t _{FRC} × 24 + 200		ns
DFG input high and low level widths	t _{DFH} t _{DFL}	DFG		t _{FRC} × 16 + 200		ns
DPG minimum pulse width	t _{DPW}	DPG		t _{FRC} × 8 + 200		ns
DPG minimum removal time	t _{rem}	DPG		t _{FRC} × 16 + 200		ns
$\overline{\text{PBCTL}}$ input high and low level widths	t _{CTH} t _{CTL}	$\overline{\text{PBCTL}}$	t _{sys} = 2000/fc	t _{FRC} × 8 + t _{sys} + 200		ns
EXI input high and low level widths	t _{EIH} t _{EIL}	EXI0 EXI1	t _{sys} = 2000/fc	t _{FRC} × 8 + t _{sys} + 200		ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) t_{FRC} = 1000/fc (ns)

Fig.9. Other timings



Supplement

Fig.10. Recommended oscillation circuit



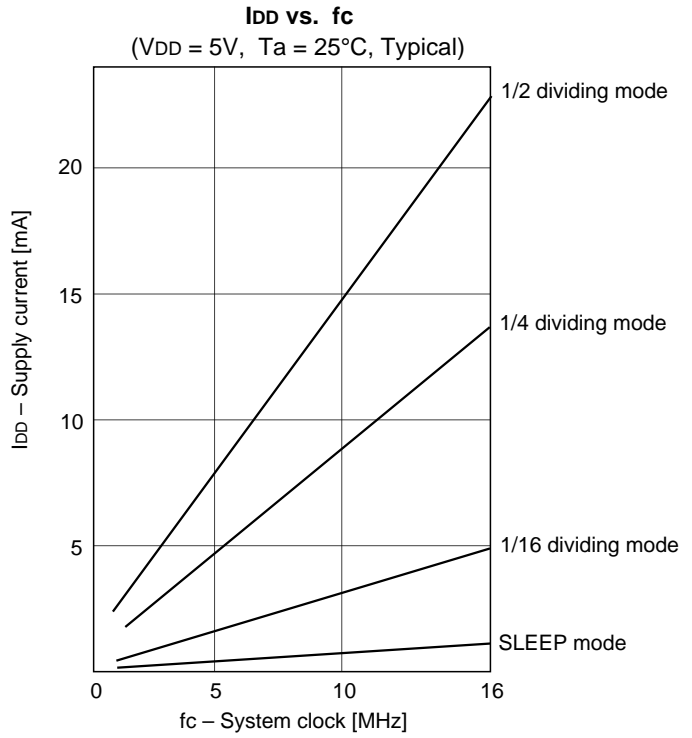
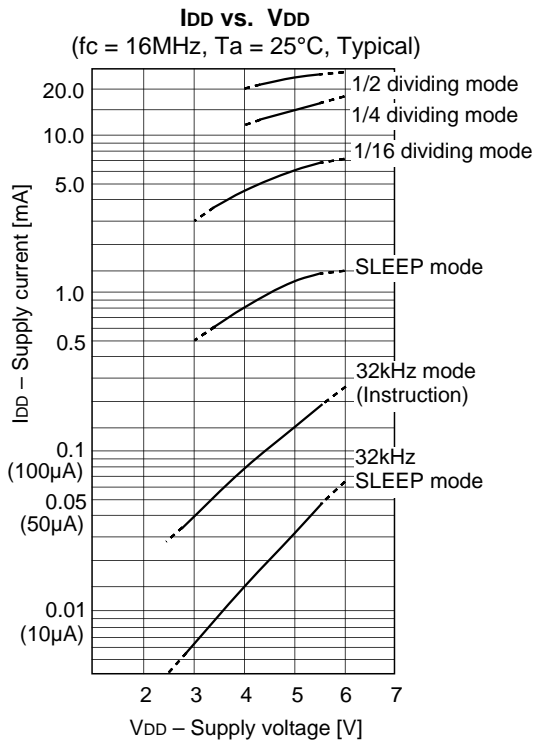
Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00				
		12.00	15	15		
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16 (12)	16 (12)	0	(i)
		10.00	16 (12)	16 (12)		
		12.00	12	12	0	
		16.00	12	12	0	
	P3	32.768kHz	30	18	470k	(ii)

Mask option table

Item	Content	
	Reset pin pull-up resistor	Non-existent
High voltage drive output port pull-down resistor	Non-existent	Existent
Input circuit format*	CMOS schmitt	TTL schmitt

* In PG4/SYNC0/ $\overline{EC}2$ pin and PG5/SYNC1 pin, the input circuit format can be selected every pin.

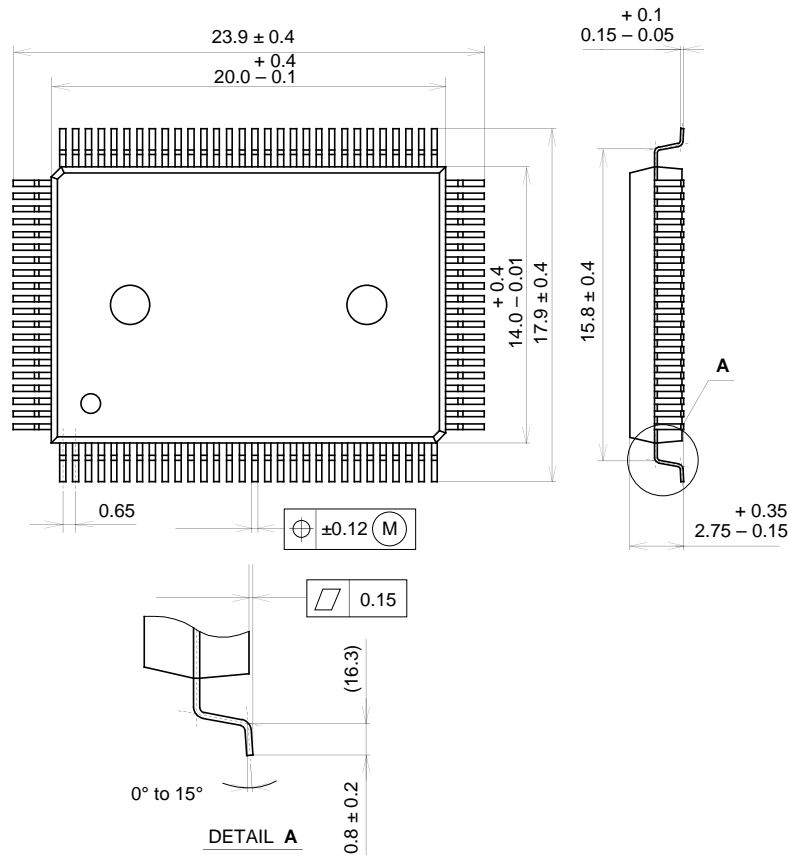
Characteristics Curve



Package Outline

Unit: mm

100PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-100P-L01
EIAJ CODE	*QFP100-P-1420-A
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.4g