CX11656
HomePlug 1.0 PHY

Home Networking Physical Layer Device with Integrated Analog Front End Circuitry

Data Sheet (Preliminary)

Conexant Proprietary Information

Doc. No. 102069A
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CONEXANT™

Revision Notice

Revision	Date	Comments
A	8/19/2002	Initial release.

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Contents

Figures

Tables

1. Introduction

1.1 Overview

The Conexant™ CX11656 device is an integrated physical layer transceiver or PHY (Figure 1-1). It is designed to use existing ac electrical wiring within the home as a networking physical medium. The PHY's robust performance in the electrically noisy power line channel is due to the use of Orthogonal Frequency Division Multiplexing (OFDM). This multi-carrier modulation scheme allows the PHY to dynamically "learn the channel"— data can be shifted from one carrier to another as real time noise and attenuation conditions change. This overcomes the flaw inherent in previous power line networking technologies—as electrical appliances were turned on and off, changing line conditions caused signal quality to become degraded to such an extent that data transmission became impossible. The CX11656's OFDM technology finds the low noise, low attenuation portions of the spectrum available to it and continues data transmission.

The CX11656 is compliant with the *HomePlug Powerline Alliance Industry Specification V1.0*. This ensures interoperability with other HomePlug PHYs. Quality-of-service (QoS) is built into the PHY to ensure low-latency, high reliability channels for streaming audio, streaming video, voice, and gaming, and video.

The PHY utilizes the IEEE 802.3u standard Media Independent Interface (MII). This standard interface can also be configured as a seven-wire General Purpose Serial Interface (GPSI). These standard interfaces allow the CX11656 to be paired almost any embedded media access controller (MAC) for use in a variety of information appliances.

The CX11656 operates on both +1.8 V and +3.3 V supplies and is packaged in a 144-pin Low Quad Flat Pack (LQFP).

The CX11656 ordering information is listed in Table 1-1.

A functional block diagram of the CX11656 is shown in Figure 1-2.

Please contact Conexant marketing for information concerning the AFE.

Figure 1-1. CX11656 HomePlug 1.0 PHY Simplified Hardware Interface

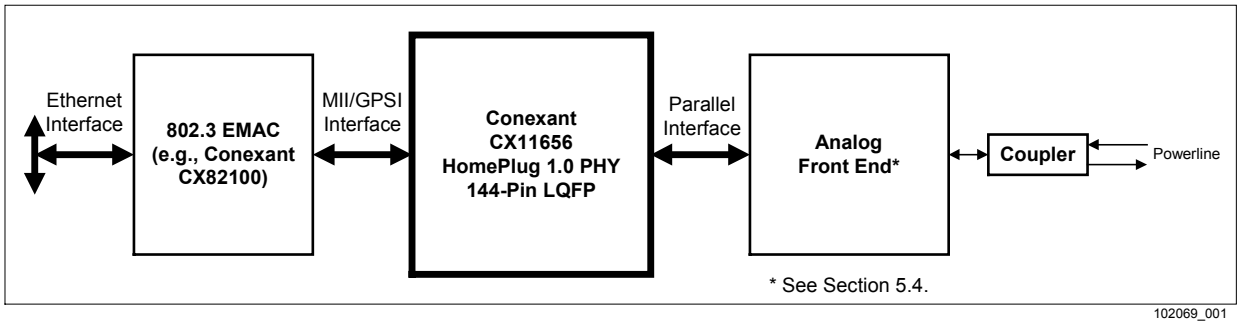
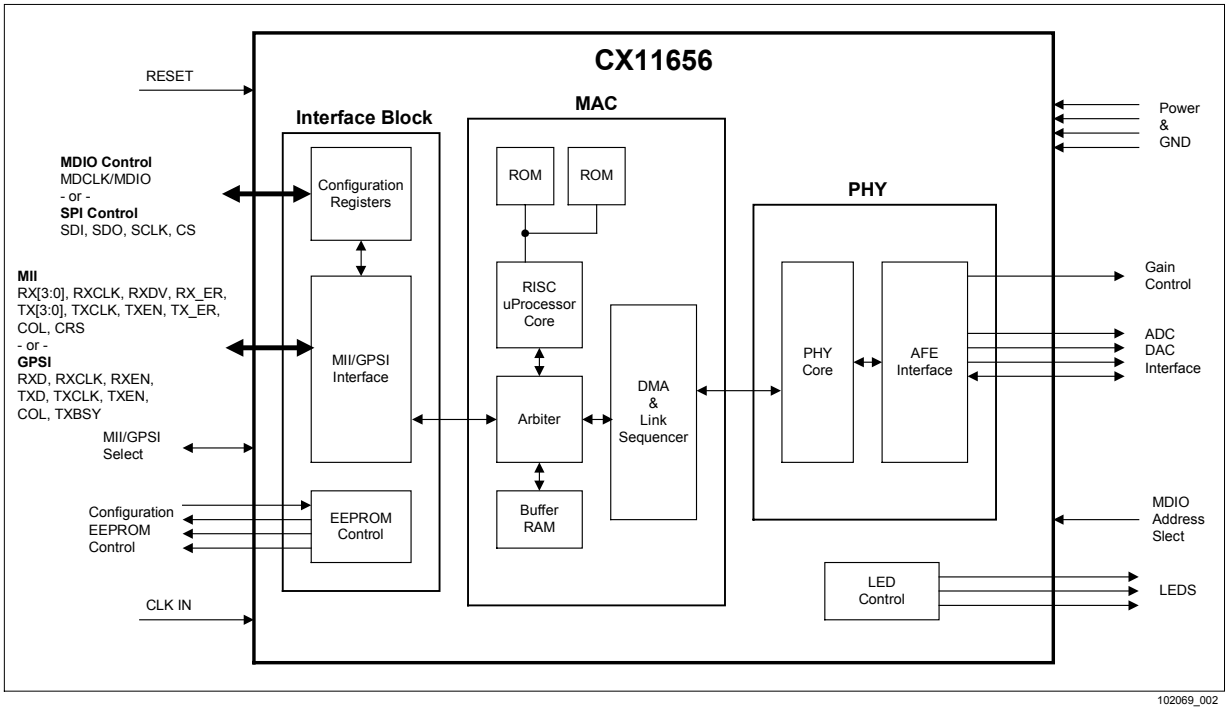


Table 1-1. CX11656 HomePlug 1.0 PHY and CX82100-41 Ordering Information

Marketing Order No.	HomePlug 1.0 PHY [144-Pin LQFP] Part No.	Home Network Processor (HNP) [196-Pin FPBGA] Part No.
DSHP-L100-001	CX11656-11	CX82100-41

Figure 1-2. CX11656 HomePlug 1.0 PHY Functional Block Diagram



1.2 Features

- Single-chip powerline networking controller with IEEE802.3u MII interface
- Implements the *HomePlug Powerline Alliance Industry Specification V1.0*
- General purpose 7-wire serial PHY data interface
- Selectable MDI/SPI PHY management interface
- Up to 14 Mbps data rate on the powerline
- Orthogonal Frequency Division Multiplexing (OFDM) with patented signal processing techniques for high data reliability in noisy media conditions
- Intelligent channel adaptation maximizes throughput under harsh channel conditions
- Integrated quality-of-service (QoS) features such as prioritized random access, contention-free access, and segment bursting
- 56-bit DES Link Encryption with key management for secure powerline communications
- EEPROM interface for fast access to configuration parameters allows system designs to leverage standard Ethernet drivers
- 3.3 V signaling, 5 V tolerant interface
- Support for three status LEDs
- 144-pin LQFP package

1.3 Applications

- Residential gateways and home routers
- Network home or small office PCs
- Enable no wire installation networking for information appliances
- LAN gaming
- Share DSL or cable modem access
- MDU/MTU applications
- Embedded applications

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2. Hardware Interface

2.1 CX11656 PHY Hardware Interface Signals

The CX11656 PHY hardware interface signals are shown in Figure 2-1.

CX11656 PHY pin signals are shown in Figure 2-2 and are listed in Table 2-1.

CX11656 PHY hardware interface signals are defined in Table 2-2.

Figure 2-1. CX11656 PHY Hardware Interface Signals - 144-Pin LQFP

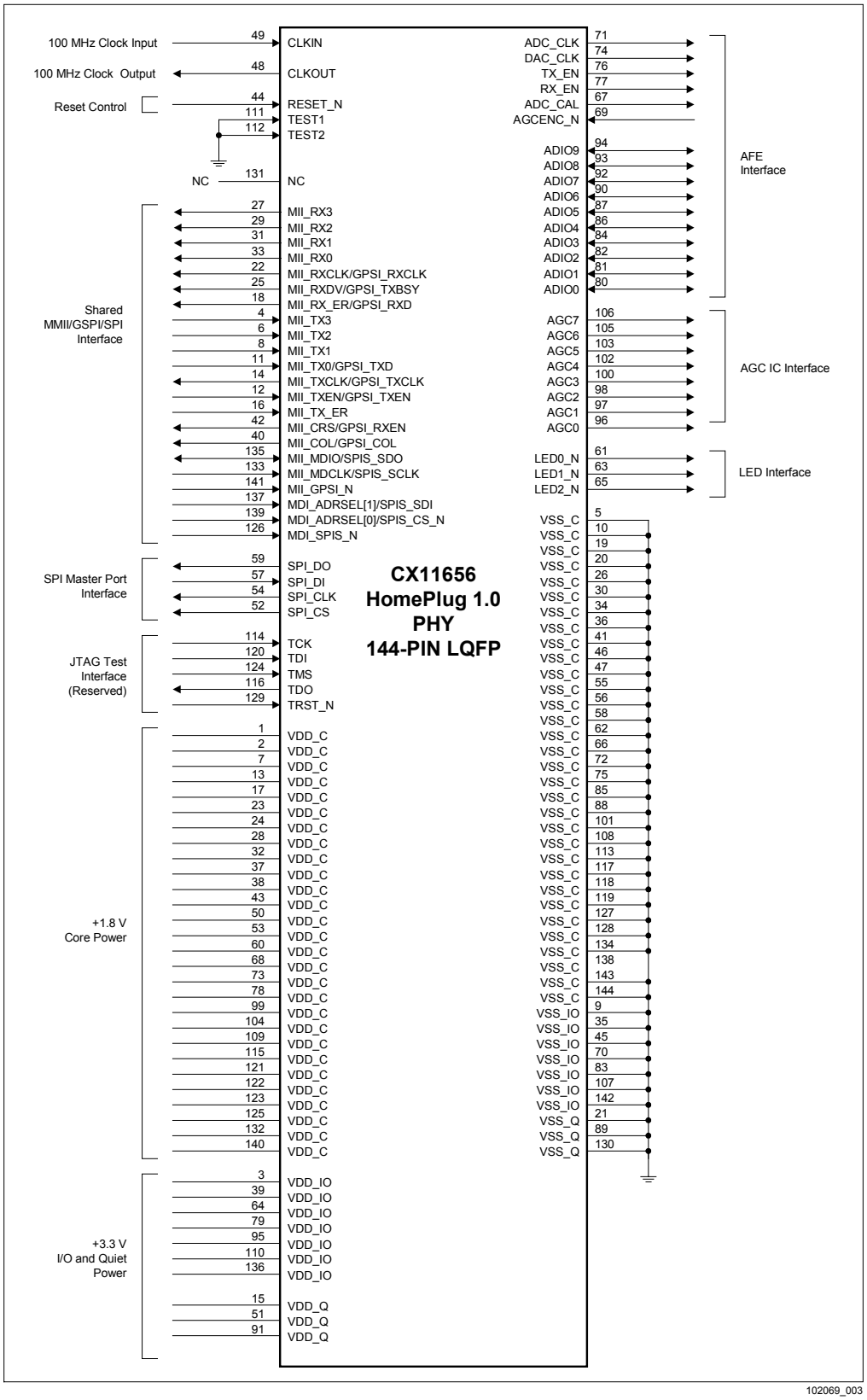

Figure 2-2. CX11656 PHY Pin Signals - 144-Pin LQFP

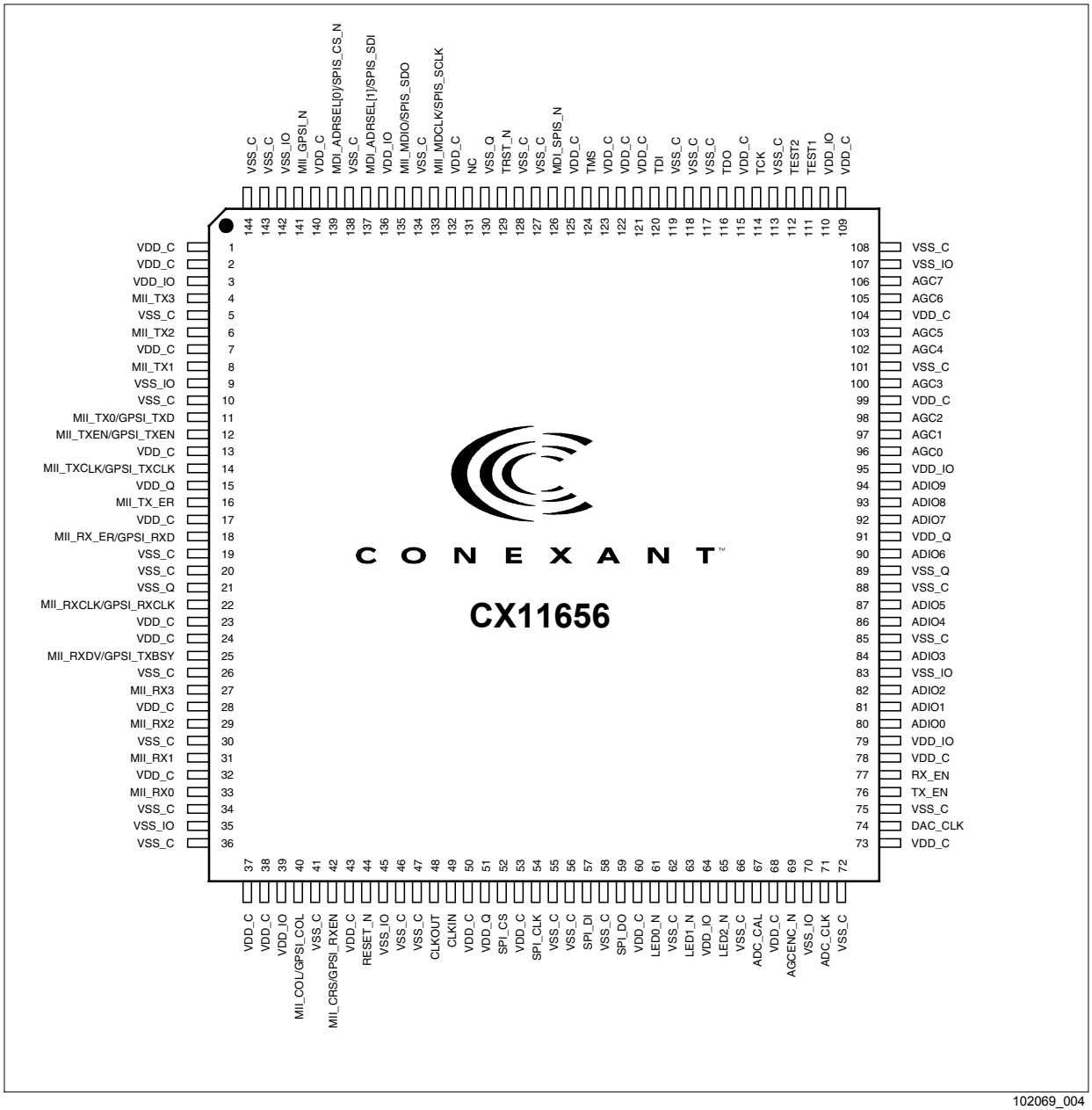

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Table 2-1. CX11656 PHY Pin Signals - 144-Pin LQFP

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	VDD_C	37	VDD_C	73	VDD_C	109	VDD_C
2	VDD_C	38	VDD_C	74	DAC_CLK	110	VDD_IO
3	VDD_IO	39	VDD_IO	75	VSS_C	111	TEST1
4	MII_TX3	40	MII_COL/GPSI_COL	76	TX_EN	112	TEST2
5	VSS_C	41	VSS_C	77	RX_EN	113	VSS_C
6	MII_TX2	42	MII_CRS/GPSI_RXEN	78	VDD_C	114	TCK
7	VDD_C	43	VDD_C	79	VDD_IO	115	VDD_C
8	MII_TX1	44	RESET_N	80	ADIO0	116	TDO
9	VSS_IO	45	VSS_IO	81	ADIO1	117	VSS_C
10	VSS_C	46	VSS_C	82	ADIO2	118	VSS_C
11	MII_TX0/GPSI_TXD	47	VSS_C	83	VSS_IO	119	VSS_C
12	MII_TXEN/GPSI_TXEN	48	CLKOUT	84	ADIO3	120	TDI
13	VDD_C	49	CLKIN	85	VSS_C	121	VDD_C
14	MII_TXCLK/GPSI_TXCLK	50	VDD_C	86	ADIO4	122	VDD_C
15	VDD_Q	51	VDD_Q	87	ADIO5	123	VDD_C
16	MII_TX_ER	52	SPI_CS	88	VSS_C	124	TMS
17	VDD_C	53	VDD_C	89	VSS_Q	125	VDD_C
18	MII_RX_ER/GPSI_RXD	54	SPI_CLK	90	ADIO6	126	MDI_SPIS_N
19	VSS_C	55	VSS_C	91	VDD_Q	127	VSS_C
20	VSS_C	56	VSS_C	92	ADIO7	128	VSS_C
21	VSS_Q	57	SPI_DI	93	ADIO8	129	TRST_N
22	MII_RXCLK/GPSI_RXCLK	58	VSS_C	94	ADIO9	130	VSS_Q
23	VDD_C	59	SPI_DO	95	VDD_IO	131	NC
24	VDD_C	60	VDD_C	96	AGC0	132	VDD_C
25	MII_RXDV/GPSI_TXBSY	61	LED0_N	97	AGC1	133	MII_MDCLK/SPIS_SCLK
26	VSS_C	62	VSS_C	98	AGC2	134	VSS_C
27	MII_RX3	63	LED1_N	99	VDD_C	135	MII_MDIO/SPIS_SDO
28	VDD_C	64	VDD_IO	100	AGC3	136	VDD_IO
29	MII_RX2	65	LED2_N	101	VSS_C	137	MDI_ADRSEL[1]/ SPIS_SDI
30	VSS_C	66	VSS_C	102	AGC4	138	VSS_C
31	MII_RX1	67	ADC_CAL	103	AGC5	139	MDI_ADRSEL[0]/ SPIS_CS_N
32	VDD_C	68	VDD_C	104	VDD_C	140	VDD_C
33	MII_RX0	69	AGCENC_N	105	AGC6	141	MII_GPSI_N
34	VSS_C	70	VSS_IO	106	AGC7	142	VSS_IO
35	VSS_IO	71	ADC_CLK	107	VSS_IO	143	VSS_C
36	VSS_C	72	VSS_C	108	VSS_C	144	VSS_C

Table 2-2. CX11656 PHY Hardware Signal Definitions

Signal Name	Pin	I/O	I/O Type	Signal Name/Description
Media Independent Interface (MII) These pins are multiplexed with the GPSI pins and are selected when MII_GSPI_N signal is at VDD.				
MII_RX[3:0]	27, 29, 31, 33	O	Ot1	**MII Receive Data.** Data is transferred from the CX11656 to the external MAC across these four lines, MII_RX[3:0], one nibble at a time.
MII_RXCLK/ GPSI_RXCLK	22	O	Ot1	**MII Receive Clock.** MII_RXCLK outputs a continuous 25 MHz clock to the external MAC.
MII_RXDV/ GPSI_TXBSY	25	O	Ot1	**MII Receive Data Valid.** When asserted high, MII_RXDV indicates that the incoming data on the MII_RX[3:0] pins are valid.
MII_RX_ER/ GPSI_RXD	18	O	Ot1	**MII Receive Error.** When asserted high, MII_RX_ER indicates to the external MAC that an error has occurred during the frame reception.
MII_TX[3:1] MII_TX0/GPSI_TXD	4, 6, 8 11	I	It	**MII Transmit Data.** Data is transferred to the CX11656 from the external MAC across these four lines (MII_TX[3:0]) one nibble at a time.
MII_TXCLK/ GPSI_TXCLK	14	O	Ot1	**MII Transmit Clock.** MII_TXCLK outputs a continuous 25MHz clock to the external MAC.
MII_TXEN/ GPSI_TXEN	12	I	It	**MII Transmit Enable.** This signal indicates to the CX11656 that valid data is present on the MII_TX[3:0] pins.
MII_TX_ER	16	I	It	**MII Transmit Error.** MII_TX_ER is activated by the external host controller when an error condition is detected during packet transmission. The CX11656 will ignore any MII transmission within which MII_TX_ER is asserted. MII_TX_ER is ignored if MII_TXEN is not asserted.
MII_CRS/ GPSI_RXEN	42	O	Ot1	**MII Carrier Sense.** When asserted high, MII_CRS indicates to the external host that traffic is present on the powerline and the host should wait until the signal goes invalid before sending additional data. This signal is an asynchronous output signal.
MII_COL/ GPSI_COL	40	O	Ot1	**MII Collision Detect.** This signal indicates to the external host that a collision has occurred on the MII interface. This signal is an asynchronous output signal.
MII Management Data Interface (MDI) These pins are multiplexed with the SPIS_SDO and SPIS_SCLK signals and are selected when MDI_SPIS_N is at VDD.				
MII_MDIO/ SPIS_SDO	135	I/O	It/Ot1	**MII Management Data Output.** MII_MDIO is the bidirectional signal that carries the data for the Management Data Interface.
MII_MDCLK/ SPIS_SCLK	133	I	It	**MII Management Data Clock.** MII_MDCLK is the clock reference for the MII_MDIO signal.

Table 2-2. CX11656 PHY Hardware Signal Definitions (Continued)

Signal Name	Pin	I/O	I/O Type	Signal Name/Description
General Purpose Serial Interface (GPSI) These pins are multiplexed with the MII pins and are selected when MII_GSPI_N signal is at VSS.				
MII_RX_ER/ GPSI_RXD	18	O	Ot1	**GPSI Receive Data.** GPSI_RXD carries data received from the powerline and delivers to the external host. Data is driven on the falling edge of the GPSI_RXCLK.
MII_RXCLK/ GPSI_RXCLK	22	O	Ot1	**GPSI Receive Clock.** GPSI_RXCLK is the timing reference for the serial data transfer from the CX11656 to the external host. This clock operates at 10 MHz.
MII_TX0/GPSI_TXD GPSI_TXD	11	I	It	**GPSI Transmit Data.** GPSI_TXD carries data transmitted from the external host to the CX11656 for transmission over the powerline. Data is latched on the falling edge of the GPSI_TXCLK.
MII_TXCLK/ GPSI_TXCLK	14	O	Ot1	**GPSI Transmit Clock.** This signal is the timing reference for the serial data transfer from the external host to the CX11656. This clock operates at 10 MHz.
MII_CRS/ GPSI_RXEN	42	O	Ot1	**GPSI Receive Enable.** When asserted high, GPSI_RXEN indicates valid data is on the GPSI_RXD line.
MII_TXEN/ GPSI_TXEN	12	I	It	**GPSI Transmit Enable.** When asserted high, GPSI_TXEN indicates when the external host is providing valid data on GPSI_TXD.
MII_RXDV/ GPSI_TXBSY	25	O	Ot1	**GPSI Transmit Busy.** GPSI_TXBSY is asserted within 120 GPSI clocks after GPSI_TXEN indicates a TX frame is being sent by the local host. GPSI_TXBSY stays true until the entire TX frame is loaded into an internal buffer AND a new buffer is allocated to the GPSI TX interface. This signal should be monitored by the GPSI TX host. A new GPSI TX frame should not be sent until GPSI_TXBSY returns to false to prevent TX buffer overflows. GPSI_TXBSY is an asynchronous output signal.
MII_COL/ GPSI_COL	40	O	Ot1	**GPSI Collision Detect.** GPSI_COL is driven false in GPSI mode.
SPI Slave Port Selected when MDI_SPIS_N signal is at VSS.				
MII_MDIO/ SPIS_SDO	135	O	Ot1	**SPI Slave Data Out.** SPIS_SDO is the SPI data from the CX11656 to the external host.
MDI_ADRSEL[1]/ SPIS_SDI	137	I	It	**SPI Slave Data In.** SPIS_SDI is the SPI data from the external host to the CX11656. This pin is shared with the MDI_ADRSEL[1].
MII_MDCLK/ SPIS_SCLK	133	I	It	**SPI Slave Clock.** SPIS_SCLK is the timing reference signal for SPI_SDI and SPI_SDO.
MDI_ADRSEL[0]/ SPIS_CS_N	139	I	It	**SPI Slave Chip Select.** When asserted low, SPIS_CS_N enables SPI data transfers on the CX11656. This pin is shared with the MDI_ADRSEL[0].
SPI Master Port (Configuration PROM Interface)				
SPI_DO	59	O	Ot1	**SPI Master Data Out.** SPI_DO is the CX11656 configuration data from the CX11656 to the external E 2 PROM.
SPI_DI	57	I	It	**SPI Master Data In.** SPI_DI is the CX11656 configuration data from the external E 2 PROM to the CX11656.
SPI_CLK	54	O	Ot1	**SPI Master Clock.** SPI_CLK is the timing reference signal for SPI_DI and SPI_DO.
SPI_CS	52	O	Ot1	**SPI Master Chip Select.** When asserted high, SPI_CS enables data transfers on the SPI Master Interface.
LED Control				
LED0_N	61	O	Ot1	**Collision Detection.** LED0_N is asserted low for 9–10 ms upon detection of a collision.
LED1_N	63	O	Ot1	**LED1Activity Detection.** LED1_N is asserted low for 9–10 ms upon the receipt of a properly addressed unicast or broadcast frame or the transmission of a frame.
LED2_N	65	O	Ot1	**Link Detection.** LED2_N is asserted low when initialization is complete successfully and “network” is established.

Table 2-2. CX11656 PHY Hardware Signal Definitions (Continued)

Signal Name	Pin	I/O	I/O Type	Signal Name/Description
Analog Front End Interface				
ADC_CLK	71	O	Ot1	**ADC Clock.** ADC clock output to the Analog Conversion IC.
DAC_CLK	74	O	Ot1	**DAC Clock.** DAC clock output to the Analog Conversion IC.
TX_EN	76	O	Ot1	**Analog Front End Transmit Enable.** Transmit Enable signal
RX_EN	77	O	Ot1	**Analog Front End Receive Enable.** Receive Enable signal
ADIO[9:0]	94, 93, 92, 90, 87, 86, 84, 82, 81, 80	I/O	It/Ot12	**Analog/Digital I/O.** ADC and DAC Data. Multiplexed parallel interface to Analog Conversion IC.
AGC[7:0]	106, 105, 103, 102, 100, 98, 97, 96	O	Ot1	**AGC Gain Select.** Gain control driven by the CX11656 to set the AGC level.
ADC_CAL	67	O	Ot1	**ADC Calibrate.** This pin must remain low during normal operation of the ADC. It is pulsed high to request a calibration cycle. The ADC_CAL minimum pulse width is 4 clock cycles. While this signal is high the ADC calibration registers are cleared and the calibration control circuitry is reset. The ADC_CAL pulse will go high 217 clock cycles (2.6 ms) after power on reset drops, and will remain high for the required 4 clock cycles.
AGCENC_N	69	I	It	**AGC Encode.** An inactive signal (logic 1) applied to this input selects unitary AGC format. An active signal (logic 0) applied to this input selects encoded AGC format.
Test Access Port (Reserved)				
TCK	114	I	It	**Test Clock.** Test Clock for the IEEE 1149.1 JTAG Port.
TDI	120	I	It	**Test Data In.** Data In for the IEEE 1149.1 JTAG Port.
TMS	124	I	It	**Test Mode Select.** Test Mode Select for the IEEE 1149.1 JTAG Port.
TDO	116	O	Ot1	**Test Data Out.** Data Out for the IEEE 1149.1 JTAG Port.
TRST_N	129	I	It	**Test Reset.** This pin will be used to reset the TAP controller. It should be connected to ground when the JTAG port is not in use.
System Control				
RESET_N	44	I	It	**Reset.** Resets logic circuitry, but not clock circuitry. Reset is active low and should be held low for a minimum of 100 ns.
CLKIN	49	I	Ix	**Clock Input.** 100 MHz clock input driven by an external oscillator or AFE. Note: CLKIN connects directly to the +1.8 V core of the IC and does not connect to the +3.3 V I/O ring. Therefore, this pin is not +3.3 or 5 V tolerant.
CLKOUT	48	O	Ox	**Clock Output.** 100 MHz clock output. This pin should be left as NO CONNECT.
MDI_ADRSEL[1]/ SPIS_SDI, MDI_ADRSEL[0]/ SPIS_CS_N	137, 139	I	It	**MDI PHY Address Selection.** MDI_ADRSEL[1:0] is the address select used to compare against the upper two bits of the MDI Address. These pins share function with SPIS_SDI and SPIS_CS_N and should be pulled-up or down with external resistors to set the appropriate value which is read by the CX11656 during power up.
MDI_SPIS_N	126	I	It	**Management Data Interface/Serial Peripheral Interface Slave Select.** When asserted low, MDI_SPIS_N selects which PHY management signals are active.
MII_GPSI_N	141	I	It	**Media Independent Interface/General Purpose Serial Interface Select.** When asserted low, MII_GPSI_N selects which PHY data interface signals are active.
TEST1	111	I	It	**Factory Test Pin 1.** Tie to I/O Ground.
TEST2	112	I	It	**Factory Test Pin 2.** Tie to I/O Ground.
NC	131			**No Connect.**

Table 2-2. CX11656 PHY Hardware Signal Definitions (Continued)

Signal Name	Pin	I/O	I/O Type	Signal Name/Description
Power Supplies				
VDD_C	1, 2, 7, 13, 17, 23, 24, 28, 32, 37, 38, 43, 50, 53, 60, 68, 73, 78, 99, 104, 109, 115, 121, 122, 123, 125, 132, 140	P	PWR	**+1.8 V Digital Power**
VSS_C	5, 10, 19, 20, 26, 30, 34, 36, 41, 46, 47, 55, 56, 58, 62, 66, 72, 75, 85, 88, 101, 108, 113, 117, 118, 119, 127, 128, 134, 138, 143, 144	G	GND	**Digital Ground**
VDD_IO	3, 39, 64, 79, 95, 110, 136	P	PWR	**+3.3 VI/O Power**
VSS_IO	9, 35, 45, 70, 83, 107, 142	G	GND	**I/O Ground**
VDD_Q	15, 51, 91	P	PWR	**+3.3 V Quiet Power.** Connect to +3.3 V I/O Power
VSS_Q	21, 89, 130	G	GND	**Quiet Ground.** Connect to I/O Ground

2.2 CX11656 PHY Electrical and Environmental Specifications

DC electrical characteristics are listed Table 2-3.

Operating conditions are specified in Table 2-4.

Absolute maximum ratings are stated in Table 2-5.

Power consumption is listed in Table 2-6.

Table 2-3. CX11656 PHY DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Voltage High	V_{IH}	2.0	–	–	VDC	
Input Voltage Low	V_{IL}	–	–	0.8	VDC	
Output Voltage High	V_{OH}	2.4	–	–	VDC	I_{OH} = -1 mA
Output Voltage Low	V_{OL}	–	–	0.4	VDC	I_{OH} = 1 mA
Input Current	I_I	-15	–	15	µA	
Supply Current	I_{DD}		370		mA	
Supply Current	I_{CC}	–	25		mA	
Note: Any signal applied to the CX11656 clock pin (CLKIN) should not exceed +1.8 V.						

Table 2-4. CX11656 PHY Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Core Supply Voltage	VDD_C	1.7	1.8	1.9	VDC
I/O Supply Voltage	VDD_IO	3.0	3.3	3.6	VDC
Operating Temperature	T_A	0		+70	°C

Table 2-5. CX11656 PHY Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Core Supply Voltage	VDD_C	-0.35 to +1.95	VDC
I/O Supply Voltage	VDD_IO	-0.35 to +3.65	VDC
Input Voltage	VIN	-0.35 to (VDD +0.35)	VDC
Storage Temperature Range	TSTG	-55 to +125	°C
Analog Inputs	VIN	-0.35 to (VDDA + 0.35)	VDC
Voltage Applied to Outputs in High Impedance (Off) State	VHZ	-0.35 to (VDDA +0.35)	VDC

Table 2-6. CX11656 PHY Power Consumption

Mode	Typ. Current (mA)	Max. Current (mA)	Typ. Power (mW)	Max. Power (mW)
VDD_C	TBD	TBD	TBD	TBD
VDD_IO	TBD	TBD	TBD	TBD
Test conditions: VDD_C = +1.8 VDC for typical values; +1.9 VDC for maximum values. VDD_IO = +3.3 VDC for typical values; +3.465 VDC for maximum values.				

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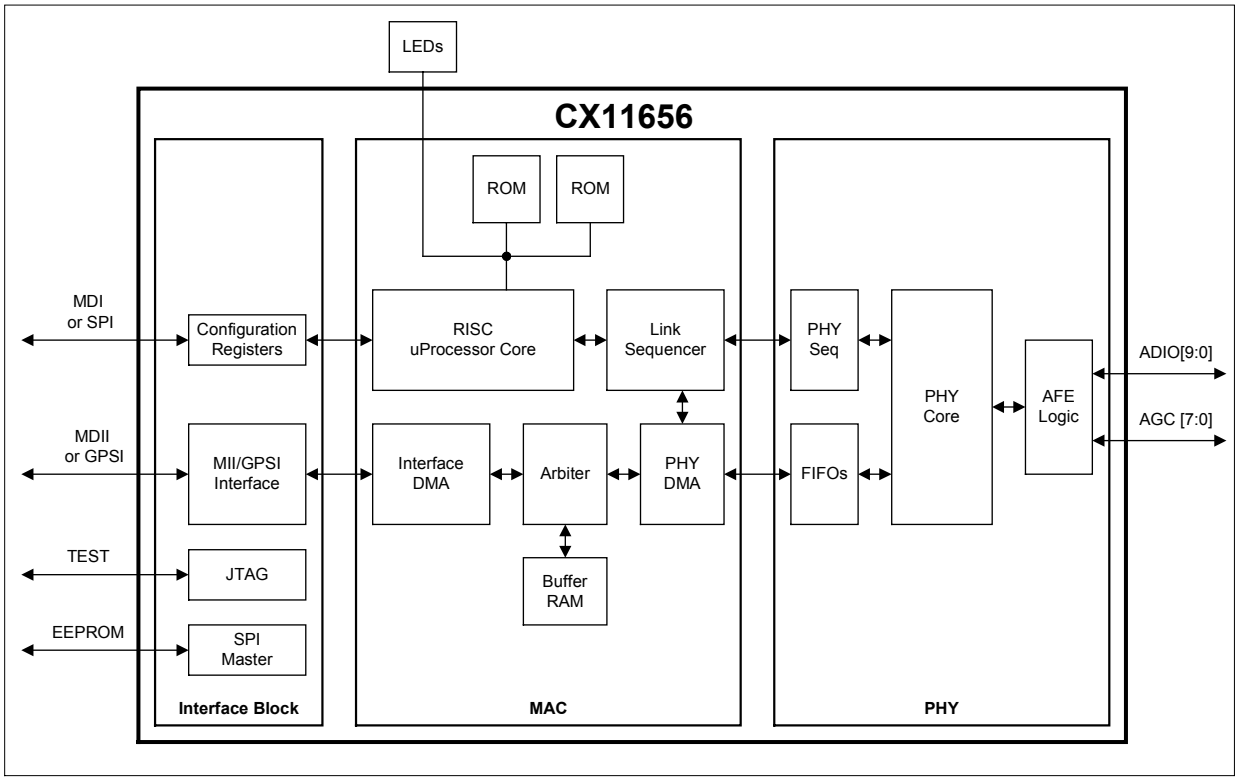
3. CX11656 Functional Description

The interfaces that provide data, status, and control to and from the CX11656 include:

- External host interface provided via the Media Independent Interface (MII) format (described by IEEE 802.3u, Clause 22) or a General Purpose Serial Interface (GPSI)
- Management control provided via the Management Data Interface (MDI) or the Serial Peripheral Interface (SPI)
- Analog Front End interface
- LEDs indicating network status
- Optional EEPROM interface providing a path to initialize the CX11656
- The JTAG port implements the IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture.

A block diagram of the CX11656 PHY is shown in Figure 3-1.

Figure 3-1. CX11656 PHY Block Diagram

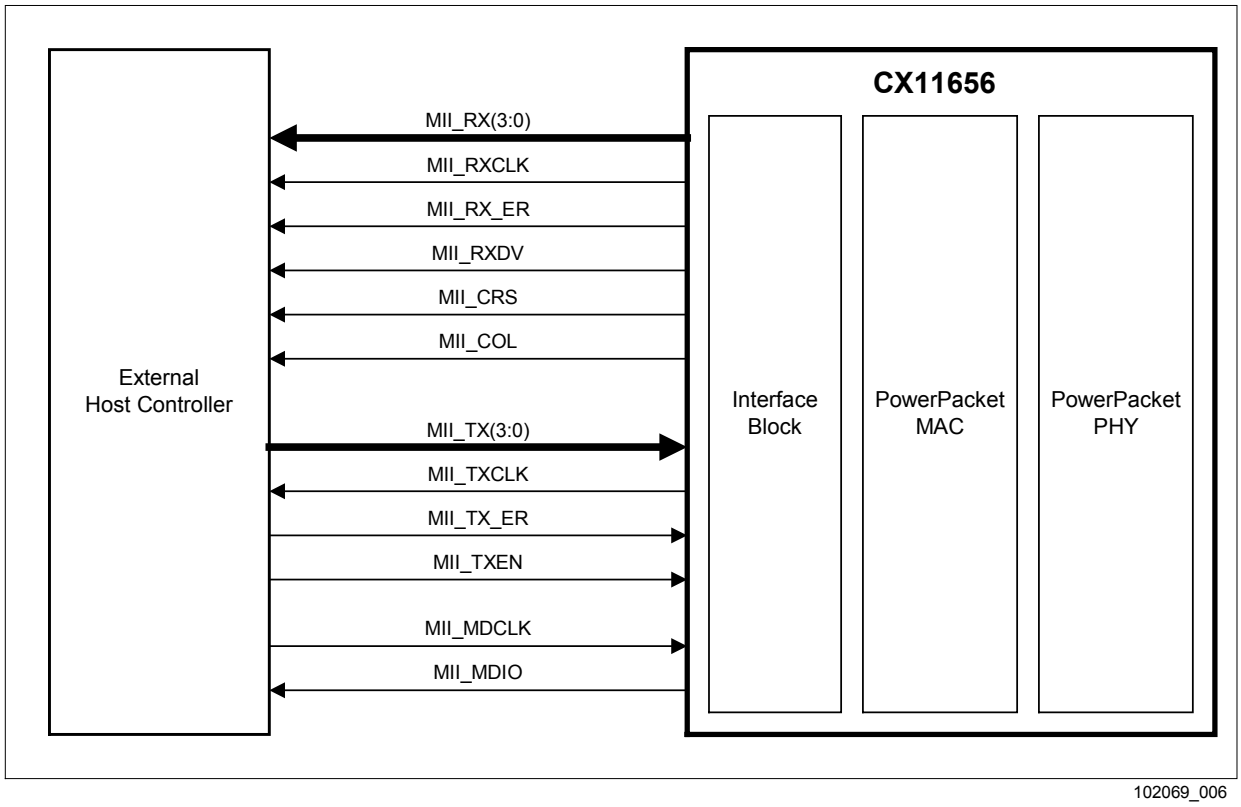


3.1 MII Data Interface with MDI Control

Data communication between the CX11656 and the external host controller is provided via the Media Independent Interface (MII) or a reduced General Purpose Serial Interface (GPSI). The MII_GPSI_N select pin is included on the chip interface to configure the CX11656 in either MII mode or GPSI mode. Access to the CX11656's internal MII status and control registers is via the Management Data Interface or a SPI interface. The MDI_SPIS_N select pin is included on the chip interface to configure the CX11656 in either MDI mode or SPI mode. The information that follows describes the MII communication interface along with the MDI management interface as a typical example.

The MII data interface with MDI control is illustrated in Figure 3-2.

Figure 3-2. MII Data Interface with MDI Control



3.1.1 MII Interface

MII is an industry standard, multi-vendor, interoperable interface between separate MAC and PHY devices. It provides a simple interconnection between the CX11656 and IEEE802.3 Ethernet MAC controllers (commonly referred to as external host controllers in this document) available from a variety of IC suppliers. The MII consists of separate 4-bit data paths for transmit and receive data along with carrier sense and collision detection. Data is transferred between the MAC and PHY over each 4-bit data path synchronous with a clock signal supplied to the host by the CX11656. The MII interface also provides a 2-wire bidirectional serial management data interface (MDI). This interface provides access to the status and control registers in the CX11656.

3.1.1.1 MII Timing Diagram

The transmission behavior of the MII interface is illustrated in Figure 3-3.

The receive behavior of the MII interface is illustrated in Figure 3-4.

An unsuccessful attempt to transmit a packet, resulting in a collision, is illustrated in Figure 3-5.

The MII receive timing is illustrated in Figure 3-6.

The MII transmit timing is illustrated in Figure 3-7.

The MII DC characteristics are listed in Table 3-1.

Note: *MII_CRS is asynchronous to MII_TXCLK.*

Figure 3-3. MII TX Waveform

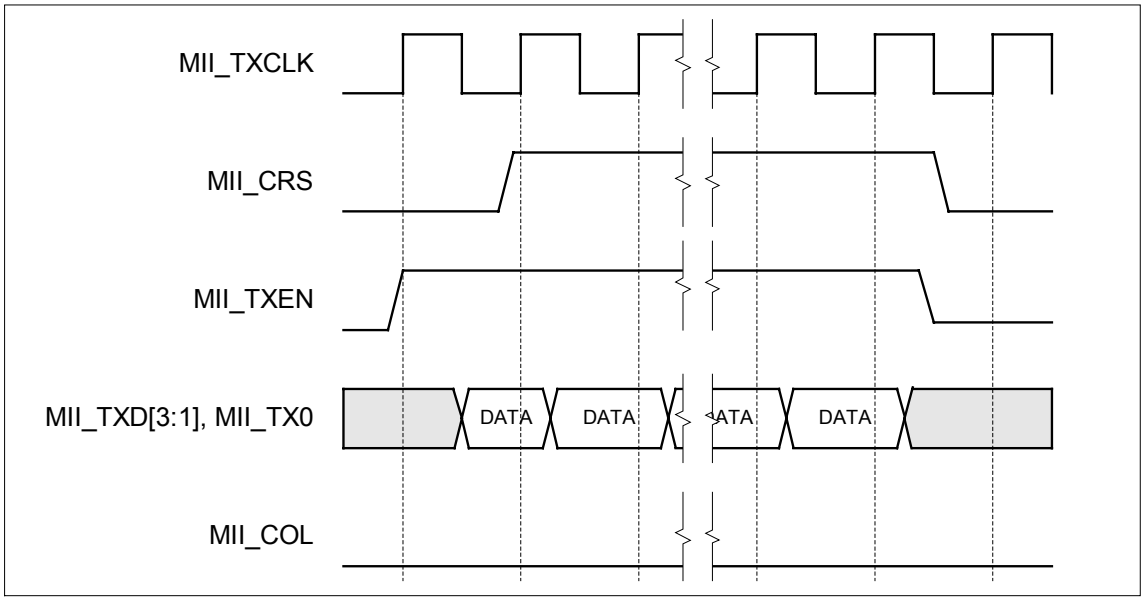


Figure 3-4. MII RX Waveform

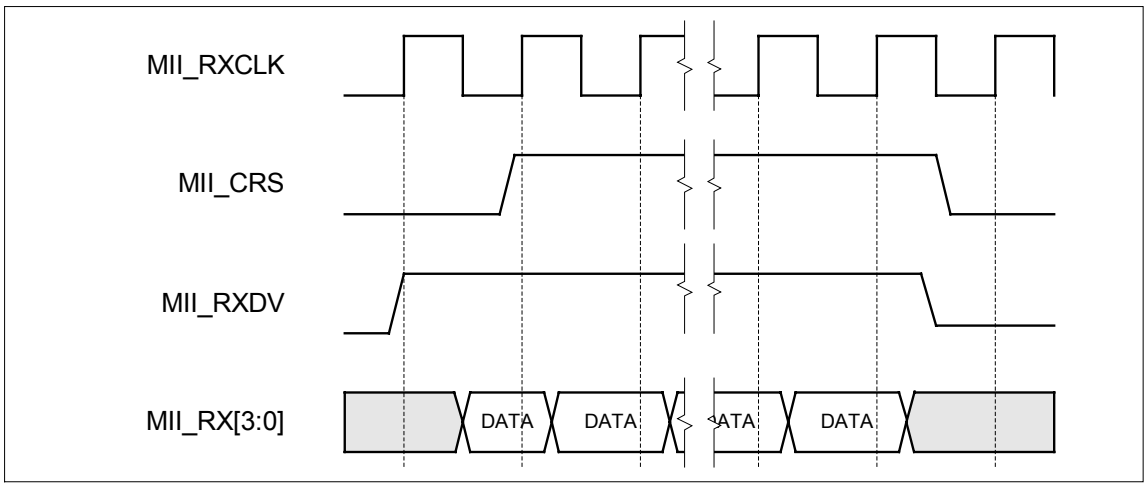


Figure 3-5. MII TX with Collision Based on RX Activity

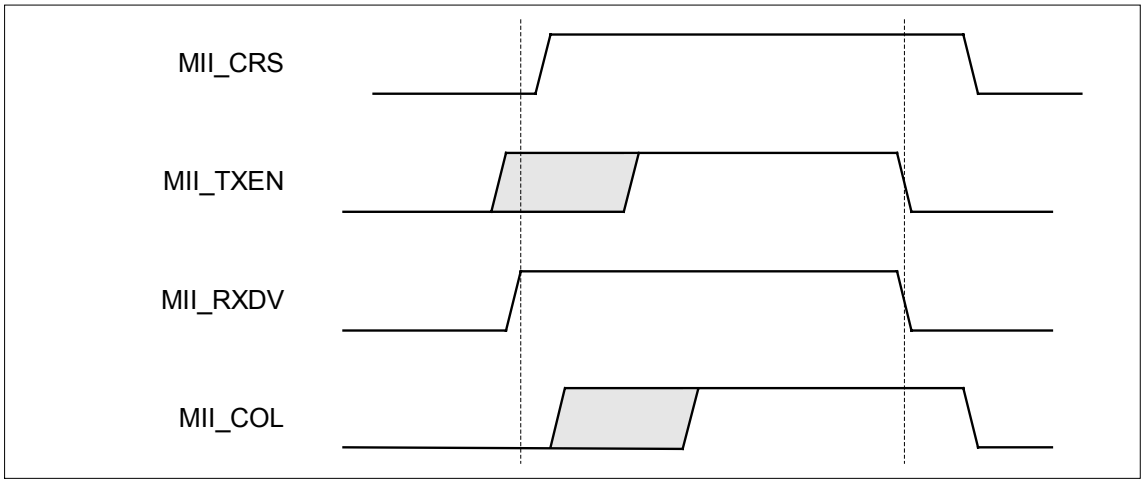
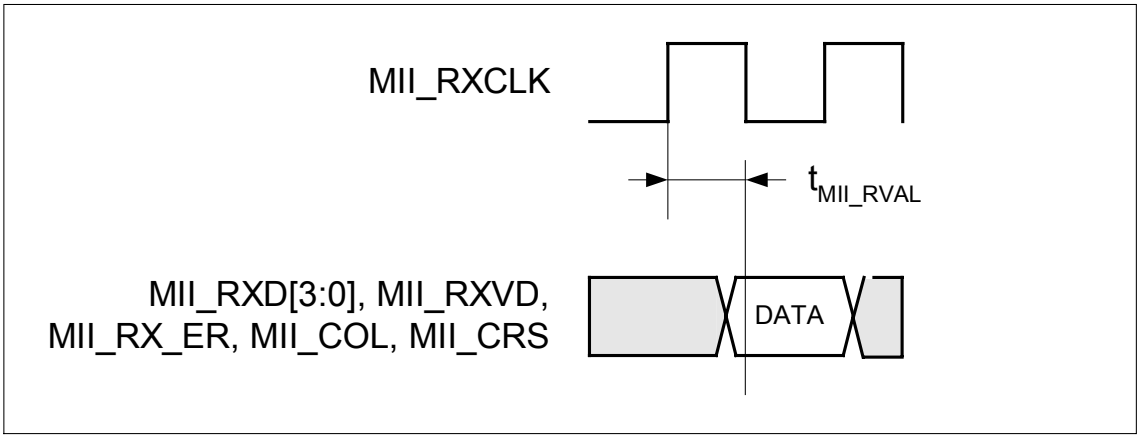
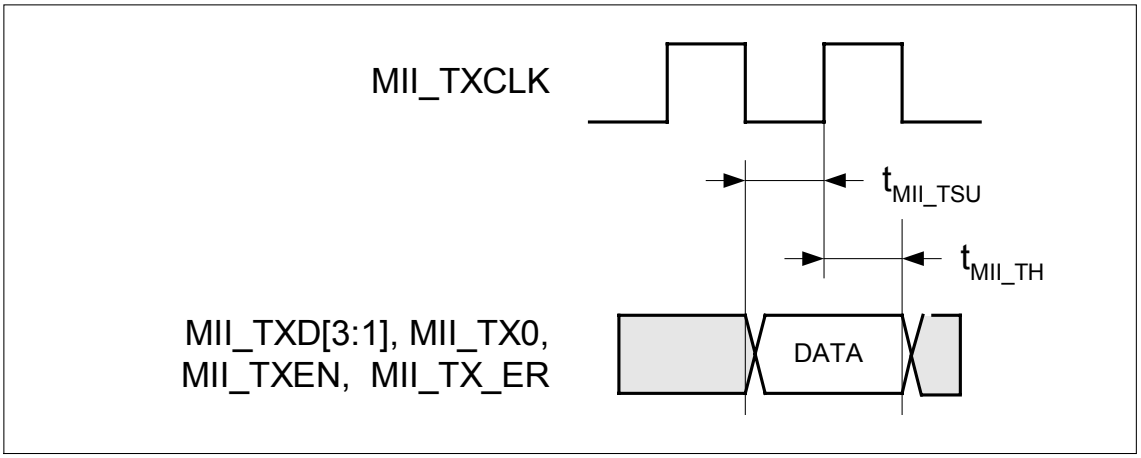


Figure 3-6. MII Receive Timing



102069_010

Figure 3-7. MII Transmit Timing



102069_011

Table 3-1. MII DC Characteristics

Parameter Symbol	Parameter Name	Test Condition	Min.	Max.	Unit
Receive Timing					
t_{MII_RVAL}	MII_RX[3:0], MII_RXDV valid from ↑ MII_RXCLK	Measured from Vilmax = 0.8V or Measured from Vihmin = 2.0V	0	25	ns
Transmit Timing					
t_{MII_TSU}	MII_TXEN, MII_TX0, MII_TX[3:1] setup to ↓ MII_TXCLK	Measured from Vilmax = 0.8V or Measured from Vihmin = 2.0V	8		ns
t_{MII_TH}	MII_TXEN, MII_TX0, MII_TX[3:1] hold to ↑ MII_TXCLK	Measured from Vilmax = 0.8V or Measured from Vihmin = 2.0V	0		ns

3.1.1.2 MII Signal Descriptions

The following description references Clause 22, Media Independent Interface specification, used in the 100 Mbps half-duplex mode. The MII is used as a data channel that transfers data back and forth with flow controlled by the carrier sense signal (MII_CRS).

MII_TXCLK and MII_RXCLK. The CX11656 generates a stable, continuous 25 MHz square wave that is supplied on MII_TXCLK and MII_RXCLK. These clocks provide the timing reference for the transfer of the MII_TXEN and MII_TX signals, as well as MII_RX, MII_RX_ER, and MII_RXDV.

MII_RX_ER. MII_RX_ER is activated when the CX11656 detects an error in the receive stream as a result of decoding.

MII_TX_ER. MII_TX_ER is activated by the external host controller when an error condition is detected during packet transmission. The CX11656 will ignore any MII transmission within which MII_TX_ER is asserted. MII_TX_ER is ignored if MII_TXEN is not asserted.

MII_TXEN. MII_TXEN from the external host provides the framing for the Ethernet packet. An active MII_TXEN indicates to the CX11656 that data on MII_TX[3:0] should be sampled using MII_TXCLK.

MII_TX[3:0]. MII_TX[3:0] contains the data to be transmitted and transitions synchronously with respect to MII_TXCLK. MII_TX[0] is the least significant bit. It is generally assumed that the data will contain a properly formatted Ethernet frame. That is, the first bits on MII_TX[3:0] correspond to the preamble, followed by SFD and the rest of the Ethernet frame (DA, SA, length/type, data, CRC).

MII_RXDV. MII_RXDV is asserted by the CX11656 to indicate that the CX11656 has decoded receive data to present to the external host.

MII_RX[3:0]. MII_RX[3:0] contains the data recovered from the medium by the CX11656 and transitions synchronously with respect to MII_RXCLK. MII_RX[0] is the least-significant bit. The CX11656 formats the frame such that the external MAC will be presented with expected preamble plus SFD.

MII_CRS. MII_CRS is used to tell the external host when the CX11656 is available for sending a packet. MII_CRS is asynchronous to MII_TXCLK. When a packet is being transmitted, CRS is held high. CRS will go low whenever the CX11656 is ready to accept another packet.

On transmit, the CX11656 asserts MII_CRS some time after MII_TXEN becomes active, and drops MII_CRS after MII_TXEN goes inactive AND when the CX11656 is ready to receive another packet from the external host for transmission. When MII_CRS has been negated for at least 900ns, the external MAC may assert MII_TXEN again if there is another packet to send. This differs from nominal behavior of MII_CRS in that MII_CRS can extend past the end of the packet by an arbitrary amount of time, while the CX11656 is gaining access to the channel and transmitting the packet. MII_CRS does not affect the receive side of the channel. Once packets start arriving from the powerline medium and begin transmission to the external host controller over the MII interface, the external host **must** be ready to receive or the packet can be lost. Note that external MACs programmed to run in 100 Mbps mode do not use a jabber timeout, so there is no timing restriction on how long MII_CRS can be asserted.

Figure 3-8. MII Flow Control Overview, Part 1

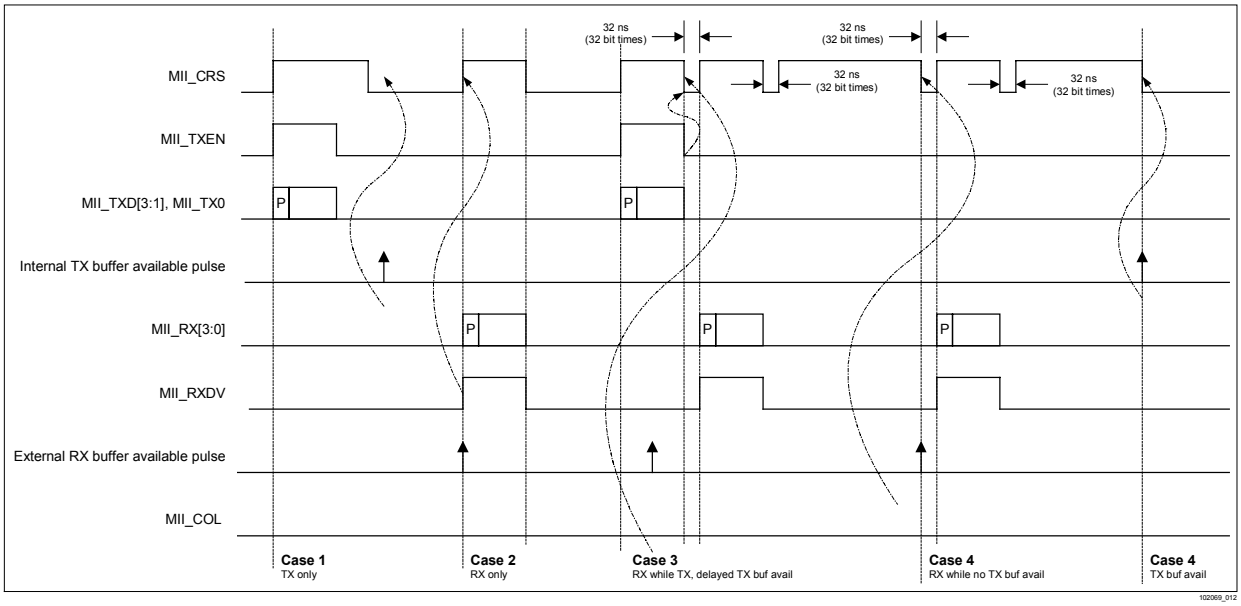
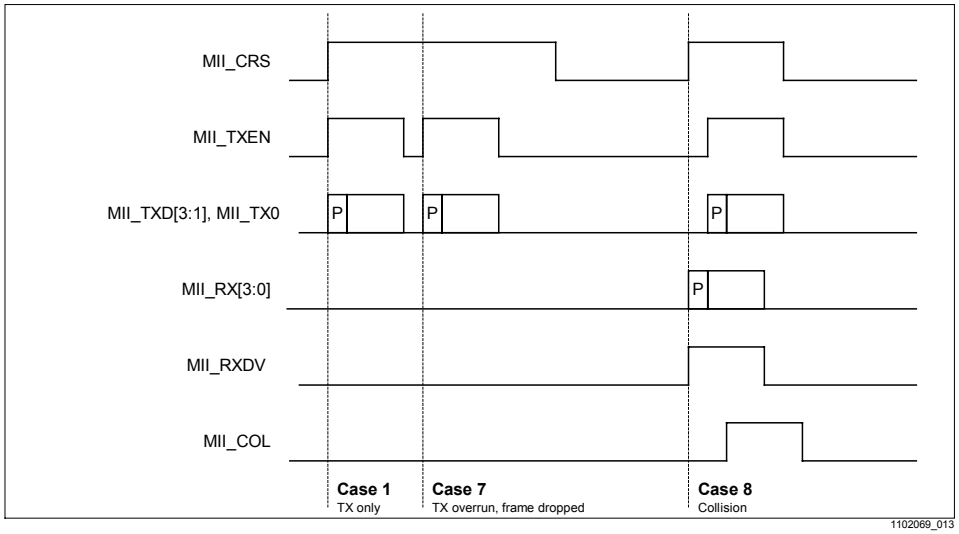


Figure 3-9. MII Flow Control Overview, Part 2



3.1.1.3 MII Frame Structure

The frame structure transmitted on the MII or GPSI interface is the following sequence of fields:

Interframe Gap	Preamble	Start Frame	Delimiter Data

Interframe Gap

A period on the MII interface during which no data activity occurs on the MII.

Preamble

Begins a frame transmission that consists of 7 octets with the following bit values:

10101010 10101010 10101010 10101010 10101010 10101010 10101010

The preamble is stripped by the CX11656 when transmitting (the preamble is not transmitted on the PLC medium) and pre-pended by the CX11656 when receiving.

Start Frame Delimiter

Indicates the start of a frame and follows the preamble. The SFD bit sequence is 10101011.

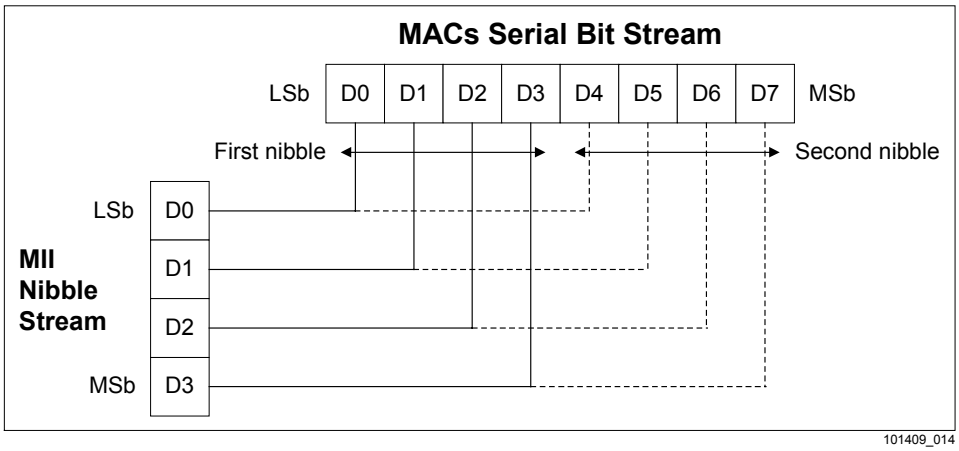
The start frame delimiter is stripped by the CX11656 when transmitting (the SFD is not transmitted on the PLC medium) and pre-pended by the CX11656 when receiving

Data

Data sent over the MII interface consists of N bytes of data transmitted as 2N nibbles.

The de-assertion of the MII_TXEN signals the End Of Frame (EOF) for data transmitted on the MII_TX[3:0] pins. Likewise, the de-assertion of the MII_RXDV signals the EOF for data transmitted on MII_RX[3:0].

Figure 3-10. Partition of Serial Bit Stream to Nibble Stream



3.1.2 MDI Control Interface

The Management Data Interface connects the external host to the CX11656 for purposes of controlling the CX11656 and gathering status. A specific frame format and protocol definition exists for exchanging management frames over this interface. A register definition exists as well that specifies a basic register set with an extension mechanism. The CX11656 implements the basic register set only.

The MDI receive timing is illustrated in Figure 3-11.

The MDI transmit timing is illustrated in Figure 3-12.

The MDI DC characteristics are listed in Table 3-2.

Figure 3-11. MDI Receive Timing

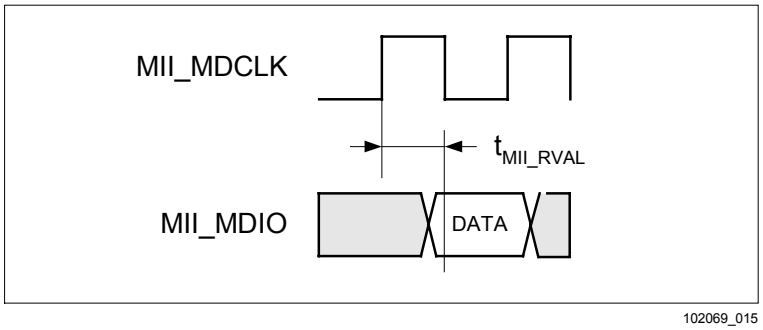


Figure 3-12. MDI Transmit Timing

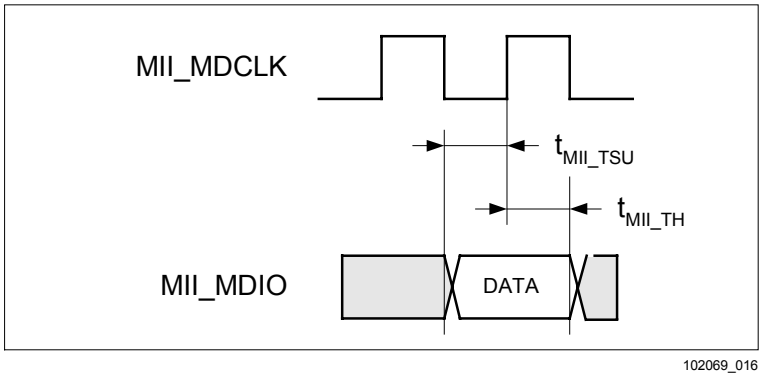


Table 3-2. MI DC Characteristics

Parameter Symbol	Parameter Name	Test Condition	Min.	Max.	Unit
Receive Timing					
t_{MI_RVAL}	MII_MDIO valid from ↑ MII_MDCLK	Measured from Vilmax = 0.8V or Measured from Vihmin = 2.0V	0	300	ns
Transmit Timing					
t_{MI_TSU}	MII_MDIO setup to ↑ MII_MDCLK	Measured from Vilmax = 0.8V or Measured from Vihmin = 2.0V	10		ns
t_{MI_TH}	MII_MDIO hold to ↑ MII_MDCLK	Measured from Vilmax = 0.8V or Measured from Vihmin = 2.0V	10		ns

3.1.2.1 MDI Signal Descriptions

Management Data Input/Output

MII_MDIO is a bi-directional signal that is used to transfer status and control information between the CX11656 and the external host. Control information is driven by the external host synchronously with respect to MII_MDCLK and is sampled synchronously by the CX11656. Status information is transferred from the CX11656 to the external host in the same manner.

Management Data Clock

MII_MDCLK is sourced by the external host as the timing reference for transfer of information on the MII_MDIO signal.

3.1.3 MII Management Register Set

The IEEE 802.3u mandated management data registers for control and status are accessible via the Management Data Interface (MDI). These registers are also accessible via the industry supported serial peripheral interface. The MDI Port will only respond to addresses 0xbXX000 when the XX field (MSbits of the MDI address) match the state of the MDI_ADRSEL[1:0] input signals. These registers can also be accessed from the SPI Slave port when the MDI_SPIS_N select line has been tied low to select the SPI Slave port.

Table 3-3 summarizes the Power Line Control and Status Register.

The MDI Frame Structure is shown in Figure 3-13.

Table 3-3. Powerline Control and Status Register (PLCSR) Summary

PLCSR	Register Name	MII Mandated
0	Control Register	X
1	Status Register	X

Figure 3-13. MDI Frame Structure

	PRE	ST	OP	PHYAD	RAGAD	TA	Data	Idle
READ	1...1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
WRITE	1...1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

3.1.3.1 PRE (Preamble)

At the beginning of each MDI transaction, the external host shall send a sequence of 32 contiguous logic “1” bits on the MDIO signal so the CX11656 can establish synchronization. The CX11656 needs to observe this 32 bit sequence on the MII_MDIO signal before it responds to any transaction.

3.1.3.2 ST (Start of Frame)

Indicated by a “01” pattern.

3.1.3.3 OP (Operation Code)

READ is indicated by “10”. WRITE is indicated by “01”.

3.1.3.4 PHYAD (PHY Address)

The PHY Address is 5 bits, allowing up the 32 unique PHY addresses. The CX11656 will respond to PHY addresses indicated by 0bXX000. The “XX” bits of the PHY address are controlled by the CX11656 interface pins MDI_ADRSEL(0:1). This allows the designer to assign the CX11656 to one of 4 unique PHY addresses.

3.1.3.5 REGAD (Register Address)

The Register Address is 5 bits and is used to index the maximum of 32 individual registers in the MDI address space. The CX11656 only implements the two mandated MII registers. 0b00000 will index the MII Control Register and 0b00001 will index the MII Status Register.

3.1.3.6 TA (Turnaround)

The turnaround time is a 2-bit time spacing between the Register Address field and the Data field to avoid contention during a read transaction.

For reads, both the external host and the CX11656 remain three-stated for the first bit time. The CX11656 will drive a “0” during the second bit time.

For writes, the external host drives a “1” for the first bit time and a “0” bit for the second bit time.

3.1.3.7 Data

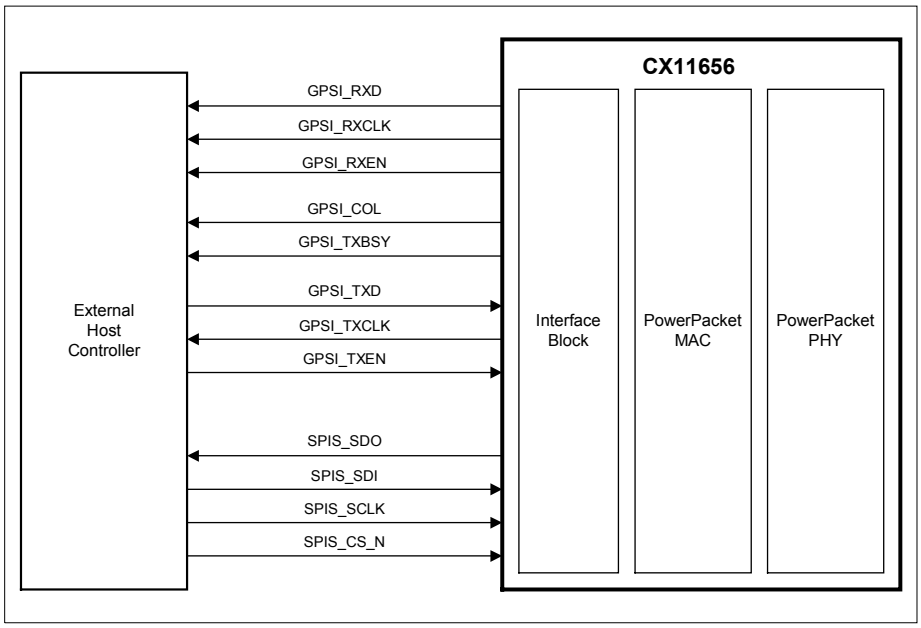
The data field is 16 bits. The first data bit transmitted and received is bit 15 of the register being addressed.

3.2 GPSI Interface with SPI Control

The General Purpose Serial Interface (GPSI) is a flexible, bi-directional serial interface that can be utilized in place of the MII. It provides a straightforward interface to a communications controller through a synchronous serial data stream for transmit and receive data. When using the GPSI interface, the management interface can either be MDI or SPI, selected by the MDI_SPIS_N pin. The information that follows describes the GPSI communication interface along with the SPI management interface as a typical example.

The GPSI interface signals are shown in Figure 3-14.

Figure 3-14. GPSI Data Interface with SPI Control



3.2.1 GSPI Interface

GPSI is an interoperable interface providing a simple interconnection between the CX11656 and embedded microcontrollers. Data is transferred between the host controller and the CX11656 over separate 1-bit transmit and receive data paths synchronous with clock signals supplied to the host by the CX11656.

3.2.1.1 GPSI Timing Diagrams

The figures below show the transmission and reception of packets and the corresponding behavior of the GPSI interface. A packet is transferred from the host when GPSI_TXEN goes high. An unsuccessful attempt is made to transmit a packet in Case 5. The received packet is passed to the host when GPSI_RXEN is high.

The GSPI flow control is illustrated in Figure 3-15.

The GSPI transmit and receive timing are illustrated in Figure 3-16 and Figure 3-17, respectively.

Figure 3-15. GPSI Flow Control

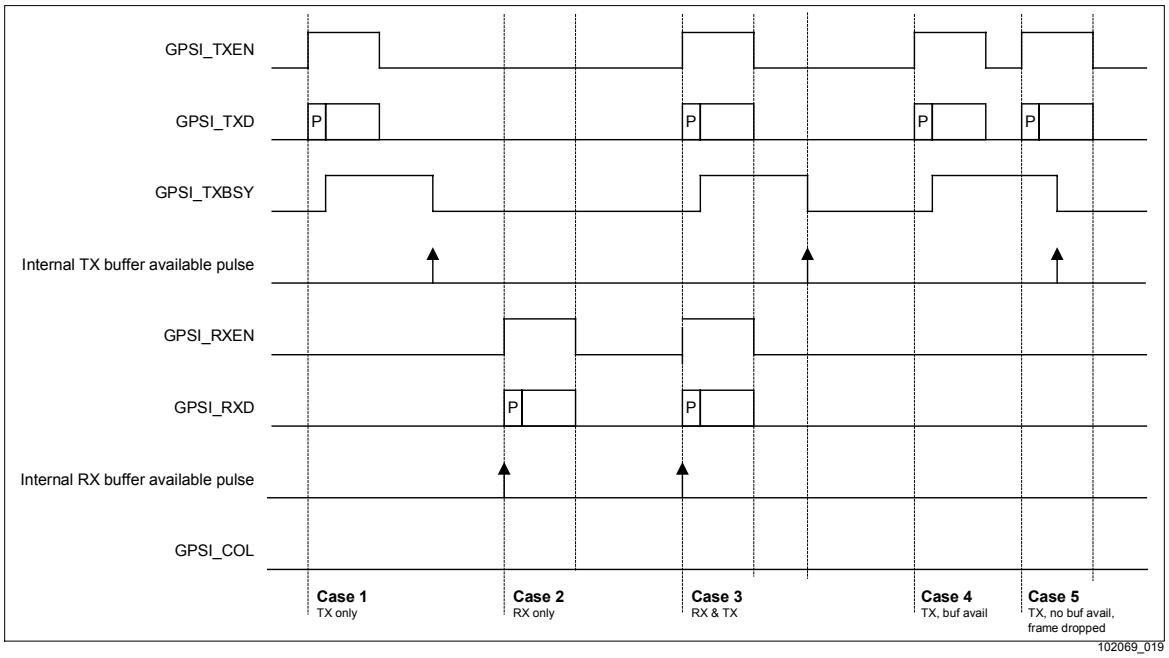


Figure 3-16. GPSI Transmit Timing

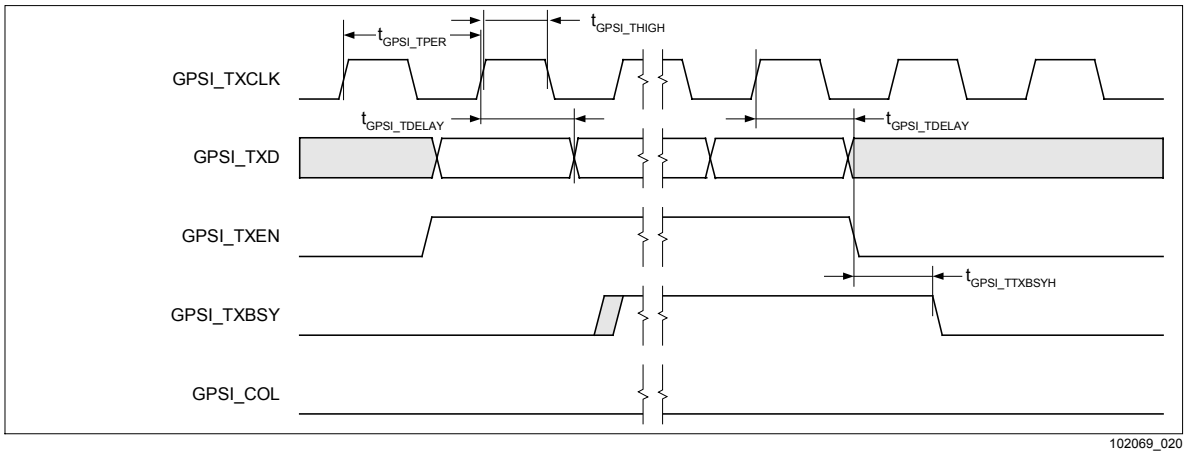
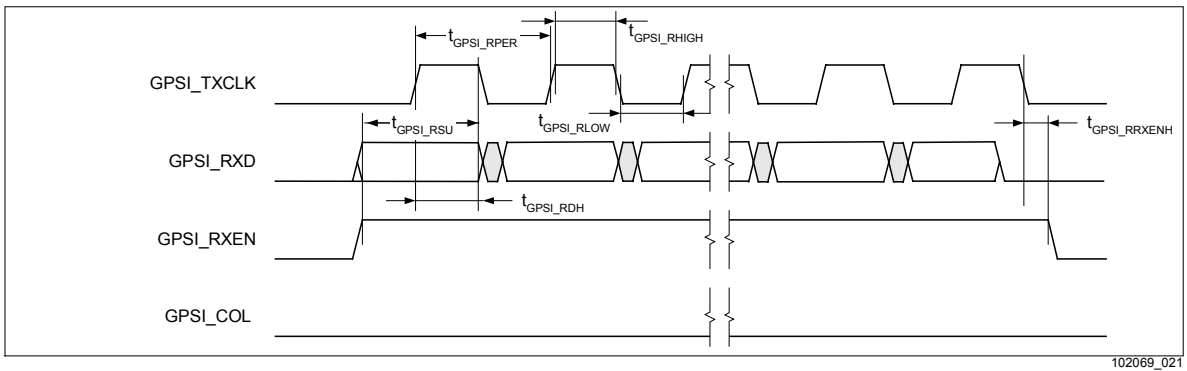


Figure 3-17. GPSI Receive Timing



3.2.1.2 GPSI DC Characteristics

The GSPI DC characteristics are listed in Table 3-4.

Table 3-4. GPSI DC Characteristics

Parameter Symbol	Parameter Name	Test Condition	Min	Max	Unit
Receive Timing					
t_{GPSI_RPER}	GPSI RXCLK Period	@ 1.5 V	99.99	100.01	ns
t_{GPSI_RHIGH}	GPSI RXCLK High Time	@ 1.5 V	40	60	ns
t_{GPSI_RLOW}	GPSI RXCLK Low Time	@ 1.5 V	40	60	ns
t_{GPSI_RSU}	GPSI_RXD and GPSI_RXEN Setup to ↑ GPSI_RXCLK	@ 1.5 V	15		ns
t_{GPSI_RDH}	GPSI_RXD Hold after ↑ GPSI_RXCLK	@ 1.5 V	15		ns
t_{GPSI_RRXENH}	GPSI_RXEN Hold after ↓ GPSI_RXCLK	@ 1.5 V	0		ns
Transmit Timing					
t_{GPSI_TPER}	GPSI TXCLK Period	@ 1.5 V	99.99	100.01	ns
t_{GPSI_THIGH}	GPSI TXCLK High Time	@ 1.5 V	40	60	ns
t_{GPSI_TDELAY}	GPSI_TXD and GPSI_TXEN Delay from ↑ GPSI_TXCLK	@ 1.5 V	0	70	ns
t_{GPSI_TRXENH}	GPSI_RXEN Hold after ↓ GPSI_TXEN	@ 1.5 V	0		ns

3.2.1.3 GPSI Signal Descriptions

GPSI_TXCLK and GPSI_RXCLK: The CX11656 generates a stable, continuous 10 MHz square wave that is supplied on GPSI_TXCLK and GPSI_RXCLK. These clocks provide the timing reference for the transfer of the GPSI_TXEN and GPSI_TXD signal, as well as GPSI_RXEN and GPSI_RXD.

GPSI_RXD: GPSI_RXD contains the data recovered from the medium by the CX11656 and transitions synchronously with respect to GPSI_RXCLK. The CX11656 properly formats the frame such that the external host controller will be presented with the expected preamble plus SFD.

GPSI_RXEN: GPSI_RXEN is asserted by the CX11656 to indicate that the CX11656 has decoded receive data to present to the external host controller.

GPSI_TXBSY: GPSI_TXBSY is an optionally used signal to tell the external host controller when the CX11656 is available for sending packets. When a packet is being transmitted, GPSI_TXBSY is held high. GPSI_TXBSY will go low whenever the CX11656 is ready to send another packet. If this signal is not used, the transmitting logic must pace the packet transmissions to ensure that no packets are lost due to buffer overflow.

On transmit, the CX11656 asserts GPSI_TXBSY sometime after GPSI_TXEN becomes active, and drops GPSI_TXBSY after GPSI_TXEN goes inactive AND when the CX11656 is ready to accept another packet for transmission. When GPSI_TXBSY falls, the external host controller may assert GPSI_TXEN again if there is another packet to send.

GPSI_TXBSY does not affect nor reflect the receive side of the channel. Once packets start arriving off of the powerline medium and begin transmission to the external host controller over the GPSI interface, the external host controller MUST be ready to receive or the packet can be lost.

GPSI_TXEN: GPSI_TXEN from the external host provides the framing for the Ethernet packet. An active GPSI_TXEN indicates to the CX11656 that data on GPSI_TXD should be sampled using GPSI_TXCLK.

GPSI_TXD: GPSI_TXD contains the data to be transmitted and transitions synchronously with respect to GPSI_TXCLK. It is generally assumed that the data will contain a properly formatted Ethernet frame (see MII Frame Structure above). That is, the first bits on GPSI_TXD correspond to the preamble, followed by Start Frame Delimiter (SFD) and the rest of the Ethernet frame (DA, SA, length/type, data, CRC).

3.2.2 SPI Slave Port Interface

The CX11656 implements a SPI Slave port that when connected to an external host controller containing a SPI Master, can be used to control access to the two configuration registers. The SPI Slave port uses a 16- bit control field (MSb first) consisting of a 6-bit command field, a 5-bit reserved field, and a 5-bit address field to control access to the two configuration registers detailed above (Table 3-5). Following the control field, the 16-bit register contents are written or read based on the command field.

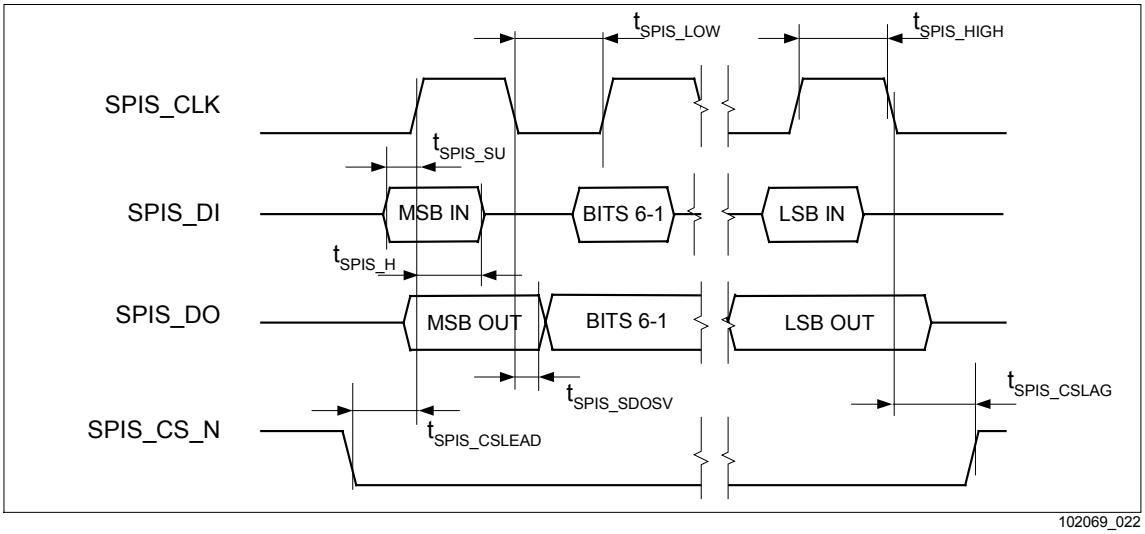
Table 3-5. SPI Slave Command Summary

Register function	Control Field															
	15	14	13	12	11	10	9	87	6	5	4	3	2	1	0	
	Command Field						Reserved Field				Address Field					
	5	4	3	2	1	0	4	3	2	1	0	4	3	2	1	0
Write PLCSR0 (Control Register)	L	L	L	L	**H**	**L**	H	L	L	L	L	L	L	L	L	**L**
Read PLCSR0 (Control Register)	L	L	L	L	**H**	**H**	H	L	L	L	L	L	L	L	L	**L**
Write PLCSR1 (Status Register)	L	L	L	L	**H**	**L**	H	L	L	L	L	L	L	L	L	**H**
Read PLCSR1 (Status Register)	L	L	L	L	**H**	**H**	H	L	L	L	L	L	L	L	L	**H**

3.2.2.1 SPI Slave Port Signal Timing

SPI Slave Port timing is illustrated in Figure 3-18.

Figure 3-18. SPI Slave Port Timing



3.2.2.2 SPI Slave Port DC Characteristics

The SPI Slave Port DC characteristics are listed in Table 3-6.

Table 3-6. SPI Slave Port DC Characteristics

Parameter Symbol	Parameter Name	Test Condition	Min	Max	Unit
t_{SPIS_F}	SPIS_SCLK Frequency			2.1	MHz
t_{SPIS_HIGH}	SPIS_SCLK High Time	@ 1.5 V	400		ns
t_{SPIS_LOW}	SPIS_SCLK Low Time	@ 1.5 V	400		ns
t_{SPIS_SDOVD}	SPIS_SDO Valid Output Delay from SPIS_SCLK	@ 1.5 V	0	500	ns
t_{SPIS_CSLEAD}	SPIS_CS Lead to SPIS_SCLK	@ 1.5 V	500		ns
t_{SPIS_CSLAG}	SPIS_CS Lag from SPIS_SCLK	@ 1.5 V	1500		ns
t_{SPIS_SU}	SPIS_SDI Setup Time to SPIS_SCLK	@ 1.5 V	200		ns
t_{SPIS_H}	SPIS_SDI Hold Time to SPIS_SCLK	@ 1.5 V	200		ns

3.3 Clocks

The CX11656 runs from a single 100 MHz oscillator input and generates a 50 MHz clock to feed the ADC, a 50 MHz clock to feed the DAC, the 25 MHz MII clock, and the 10 MHz GPSI clock. The 100 MHz clock input directly feeds the clock distribution network that clocks up to 60% of the digital logic.

Note: *Both CLKIN and CLKOUT connect directly to the +1.8 V core of the IC and do not connect to the +3.3 V I/O ring. Therefore these pins are not +3.3 V or +5 V tolerant.*

The oscillator must have ± 25 PPM RMS maximum tolerance including initial accuracy, temperature/voltage range and 5 years of aging. This oscillator must have a symmetry no worse than 40/60, jitter of 75 ps and 4 ns rise and fall time. The oscillator must be rated over the desired temperature range and ± 10% voltage range. The CX11656 uses a crystal input cell to receive the clock input.

3.4 AFE Interface

The CX11656 provides a simple parallel interface to the analog front end (AFE). The analog data is clocked into or out of the CX11656 on a 10-bit bi-directional parallel data bus under control of transmit or receive enable signals and sample clock references provided to the AFE from the CX11656. The CX11656 also provides a parallel byte-wide automatic gain control interface.

3.4.1 ADC/DAC Interface

The CX11656 outputs a sequential stream of digital time samples of the OFDM waveforms for transmission. The digital transmit signal is passed on to the A/D Converter. The ADC digitizes the analog OFDM receive signal for input to the CX11656. The DAC converts digital samples into analog waveforms.

3.4.1.1 ADC/DAC Timing Diagrams

AFE TX and RX activity is illustrated in Figure 3-19.

AFE clock waveforms are illustrated in Figure 3-20.

AFE transmit and receive timing is illustrated in Figure 3-21 and Figure 3-22, respectively.

Figure 3-19. AFE TX and RX Activity

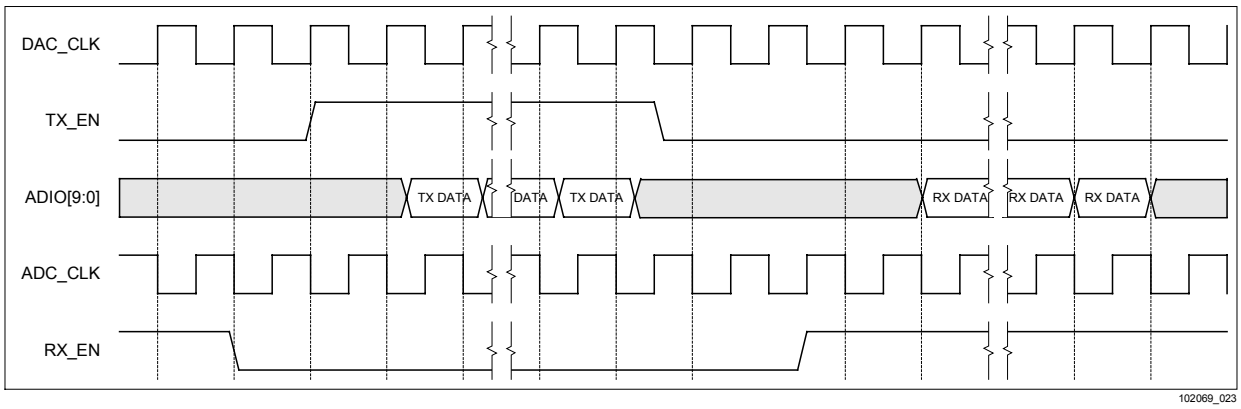


Figure 3-20. AFE Clock Waveforms

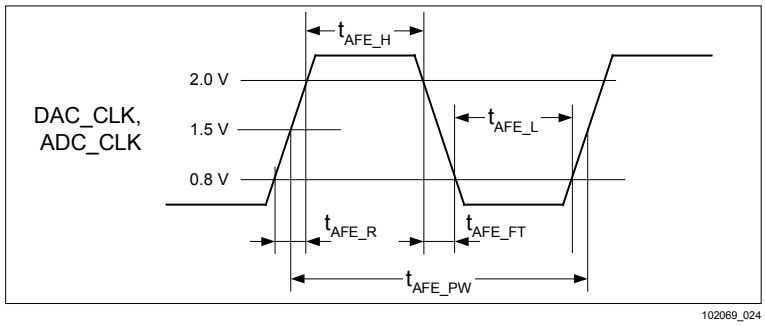


Figure 3-21. AFE Transmit Timing Diagram

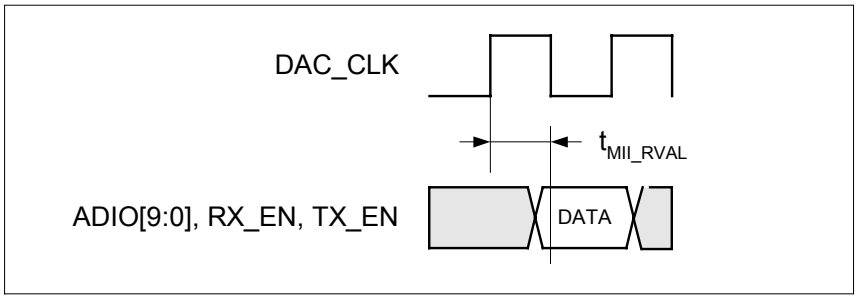
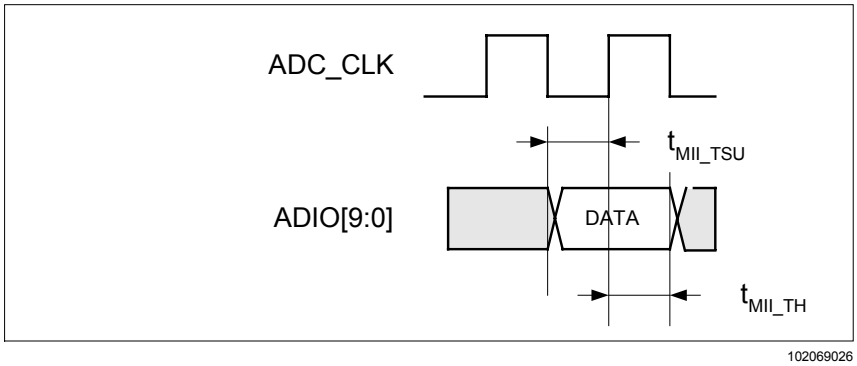


Figure 3-22. AFE Receive Timing Diagram



3.4.1.2 DAC DC Characteristics

The DAC DC characteristics are listed in Table 3-7.

Table 3-7. DAC DC Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	Number of Bits			10		bits
	Data Format			Straight Binary		
	Sample Rate		50			MSPS
DAC Data Output						
V_{OH}	High level output voltage	1, 2	2.4			V
V_{OL}	Low level output voltage	1, 3			0.4	V
t_{AFE_RVAL}	Propagation Delay Time	1	5.0	8.2	15.0	ns
DAC Clock Output						
t_{AFE_PW}	DAC Clock Pulse Width	1	10		15	ns
t_{AFE_R}	DAC Clock Rise Time	1			2	ns
t_{AFE_FT}	DAC Clock Fall Time	1			2	ns
t_J	DAC Clock Jitter	1			75	ps rms
Conditions: 1. V_{DD} = 3.3 V, CL = 15 pF, RL = 1K Ω 2. I_{OH} = -1 mA 3. I_{OL} = 1mA						

3.4.1.3 ADC DC Characteristics

The ADC DC characteristics are listed in Table 3-8.

Table 3-8. ADC DC Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	Number of Bits			10		bits
	Data Format			Straight Binary		
	Sample Rate		50			MSPS
ADC Data Input						
V_{IH}	High level input voltage	1	2.0			V
V_{IL}	Low level input voltage	1			0.8	V
t_A	Aperture Delay Time	1		2.7		ns
t_{AFE_TSU}	Data Setup Time	1	3			ns
t_{AFE_TH}	Data Hold Time	1	3			ns
ADC Clock Output						
V_{OH}	High level output voltage	1	2.1		V	
V_{OL}	Low level output voltage	1			0.9	V
t_{AFE_H}	ADC/DAC Clock Pulse Width High	1	10		15	ns
t_{AFE_L}	ADC/DAC Clock Pulse Width Low	1	10		15	ns
t_{AFE_R}	ADC/DAC Clock Rise Time	1			2	ns
t_{AFE_FT}	ADC/DAC Clock Fall Time	1			2	ns
$t_{J\ ADC/DAC}$	Clock Jitter	1			75	ps rms
Conditions: VDD = 3.3 V, CL = 15 pF, RL = 1K Ω						

3.4.2 AGC Circuitry

The CX11656 receives 10-bit digitized samples from the D/A Converter and uses them to adjust the Switched Gain Amplifier (SGA) gain to maintain optimum signal level at the input of the ADC. The AGC[7:0] control bus is used to pass a Gain Control Value (GCV) to the SGA. If the AGCENC_N input pin is low, the GCV is encoded on pins [3:0] of the AGC[7:0] control bus. If the AGCENC_N input pin is high, the GCV is decoded on pins [7:0] of the AGC[7:0] control bus with pins [7:4] selecting the gain switch setting for the first stage amplifier and pins [3:0] selecting the gain switch setting for the second stage amplifier.

RX gain control values are listed in Table 3-9.

Table 3-9. RX Gain Control Values

GCV (AGCENC_N = 0)	GCV (AGCENC_N = 1)		Front End Gain (dB)	Notes
AGC[3:0]	AGC[7:4]	AGC[3:0]		
0 0 0 0	0 0 0	0 0 0	OFF	Mute RX during TX mode
0 0 0 1	1 0 0 0	1 0 0 0	0	
0 0 1 0	0 1 0 0	1 0 0 0	8	
0 0 1 1	0 0 1 0	1 0 0 0	16	
0 1 0 0	0 0 0 1	1 0 0 0	24	
0 1 0 1	0 0 0 1	0 1 0 0	32	
0 1 1 0	0 0 0 1	0 0 1 0	40	
0 1 1 1	0 0 0 1	0 0 0 1	48	

3.4.2.1 AGC DC Characteristics

AGC DC characteristics are listed in Table 3-10.

Table 3-10. AGC DC Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VOH	High level output voltage	1	2.1			V
VOL	Low level output voltage	1			0.9	V
tR	Rise time	1		5		ns
tF	Fall time	1		5		ns
Conditions: VDD = 3.3 V, CL = 15 pF, RL = 1K Ω						

3.5 SPI Master Interface

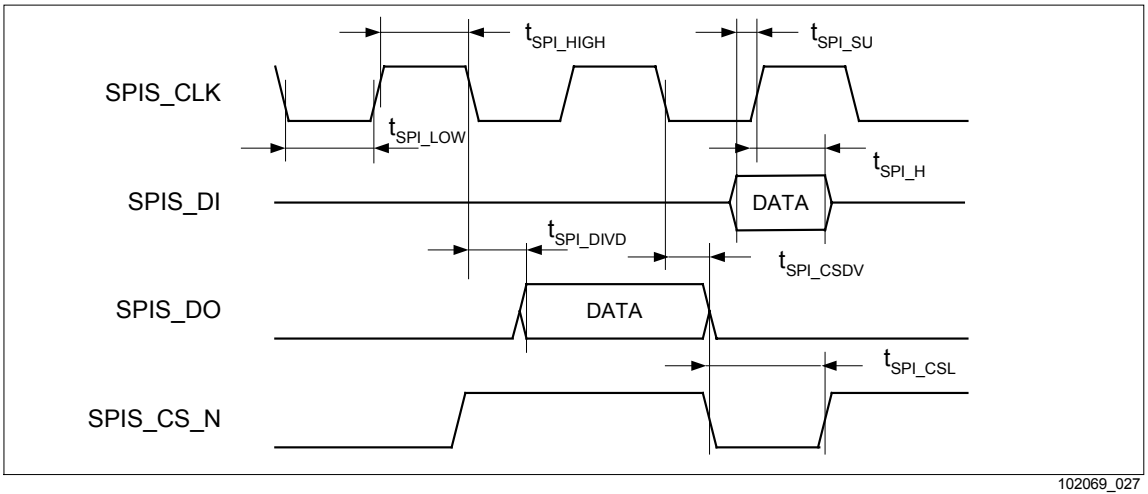
The SPI Master interface gives the system designer the option of providing the CX11656 with the necessary configuration information from a simple, SPI-controlled EEPROM as opposed to supplying this information via MAC management frames (transmitted over the MII interface). The information stored in the EEPROM is intended to initialize the CX11656 with specific information that will not be changed throughout its normal course of operation. For specific features that require real-time control, this information must be provided via the MAC management frames and not from the EEPROM.

The EEPROM must be an Atmel AT93C46, or equivalent, programmed in 8-bit mode.

3.5.1 SPI Master Interface Timing

The SPI Master interface signal timing is illustrated in Figure 3-23.

Figure 3-23. SPI Master Interface Signal Timing Diagram



3.5.2 SPI Master Interface DC Characteristics

The SPI Master interface DC characteristics are listed in Table 3-11.

Table 3-11. SPI Master Interface DC Characteristics

Parameter Symbol	Parameter Name	Test Condition	Min	Max	Unit
t_{SPI_F}	SPI_SCLK Frequency			6.125	MHz
t_{SPI_HIGH}	SPI_SCLK High Time	@ 1.5 V	70	90	ns
t_{SPI_LOW}	SPI_SCLK Low Time	@ 1.5 V	70	90	ns
t_{SPI_DIVD}	SPI_DI Valid Output Delay from SPI_SCLK	@ 1.5 V	0	15	ns
t_{SPI_CSVD}	SPI_CS Valid Output Delay from SPI_SCLK	@ 1.5 V	0	15	ns
t_{SPI_CSL}	SPI_CS Low Time	@ 1.5 V	1000		ns
t_{SPI_SU}	SPI_DO Setup Time to SPI_SCLK	@ 1.5 V	50		ns
t_{SPI_H}	SPI_DO Hold Time to SPI_SCLK	@ 1.5 V	0		ns

3.6 LED Interface

LED interface signals are described in Table 3-12.

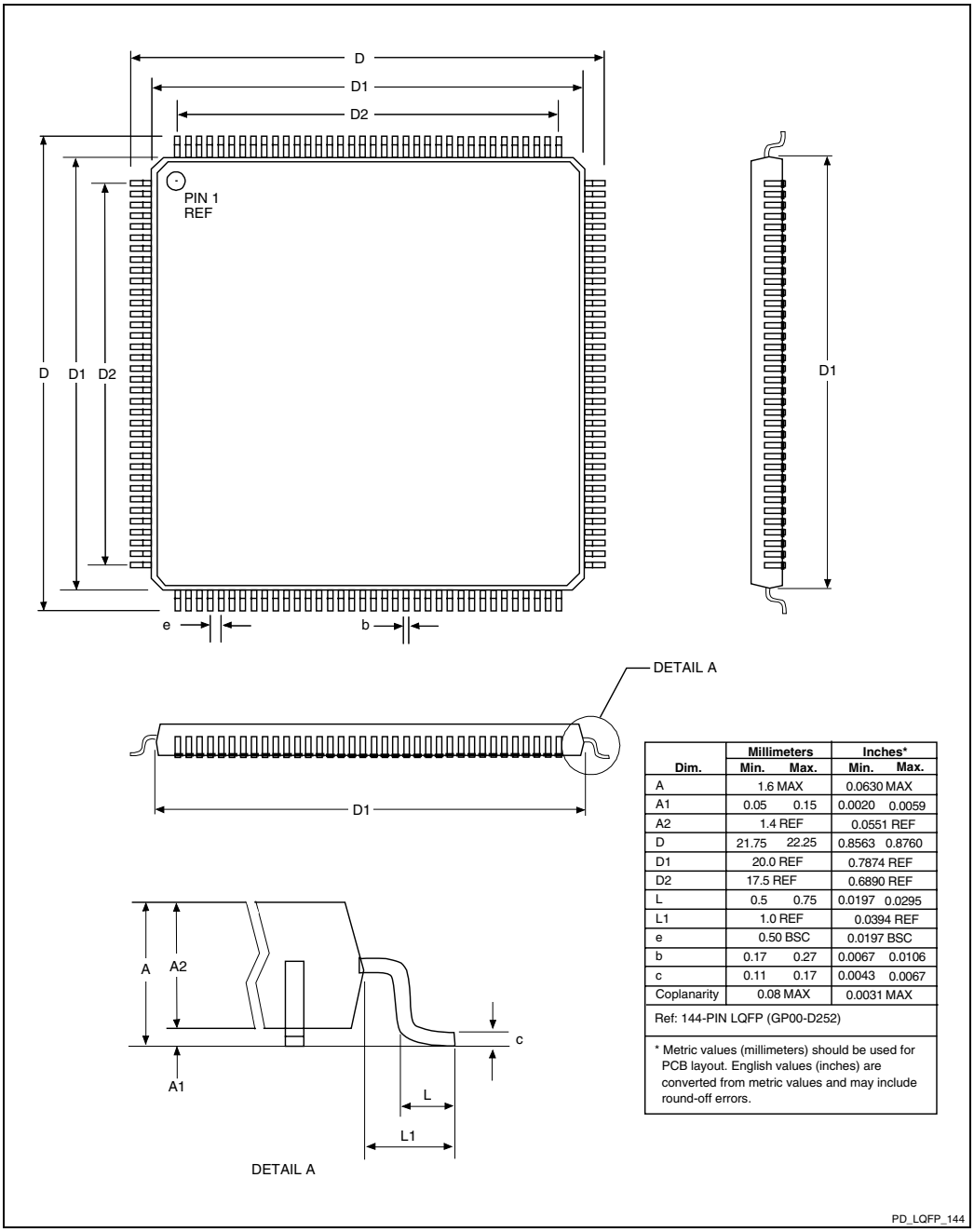
Table 3-12. LED Interface Signal Description

Signal	Status	Description
LED0_N	Collision	**LED0_N: Collision Detection.** Activates for a duration of 9–10 ms upon detection of a collision.
LED1_N	Activity	**LED1_N: Activity Detection.** Activates for a duration of 9–10 ms upon the receipt of a properly addressed unicast or broadcast frame or the transmission of a frame.
LED2_N	Link	**LED2_N: Link Detection.** Turns on when initialization is completed successfully and “network” is established.

4. Package Dimensions

Package dimensions for the 144-pin LQFP are shown in Figure 4-1.

Figure 4-1. Package Dimensions - 144-Pin LQFP



Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A		1.6 MAX		0.0630 MAX
A1	0.05	0.15	0.0020	0.0059
A2		1.4 REF		0.0551 REF
D	21.75	22.25	0.8563	0.8760
D1		20.0 REF		0.7874 REF
D2		17.5 REF		0.6890 REF
L	0.5	0.75	0.0197	0.0295
L1		1.0 REF		0.0394 REF
e		0.50 BSC		0.0197 BSC
b	0.17	0.27	0.0067	0.0106
c	0.11	0.17	0.0043	0.0067
Coplanarity		0.08 MAX		0.0031 MAX

Ref: 144-PIN LQFP (GP00-D252)

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

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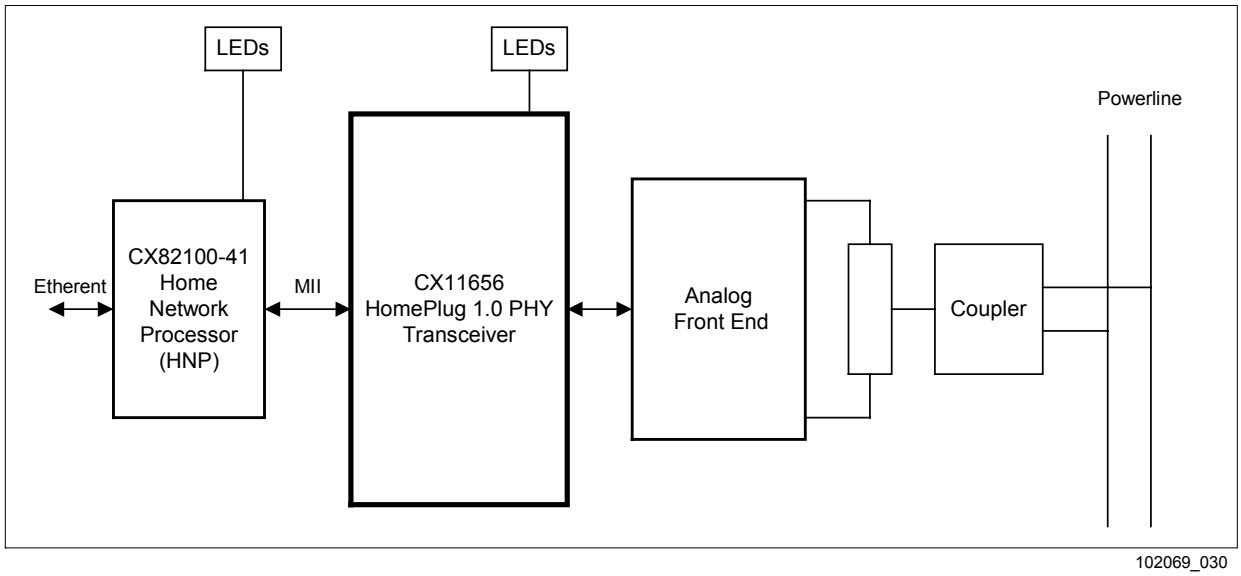
5. Application Designs

5.1 Ethernet Router Application

An Ethernet Router application design is illustrated in Figure 5-1.

Refer to CX82100 Home Network Processor (HNP) Data Sheet (Doc. No. 101306) for CX82100-41 information.

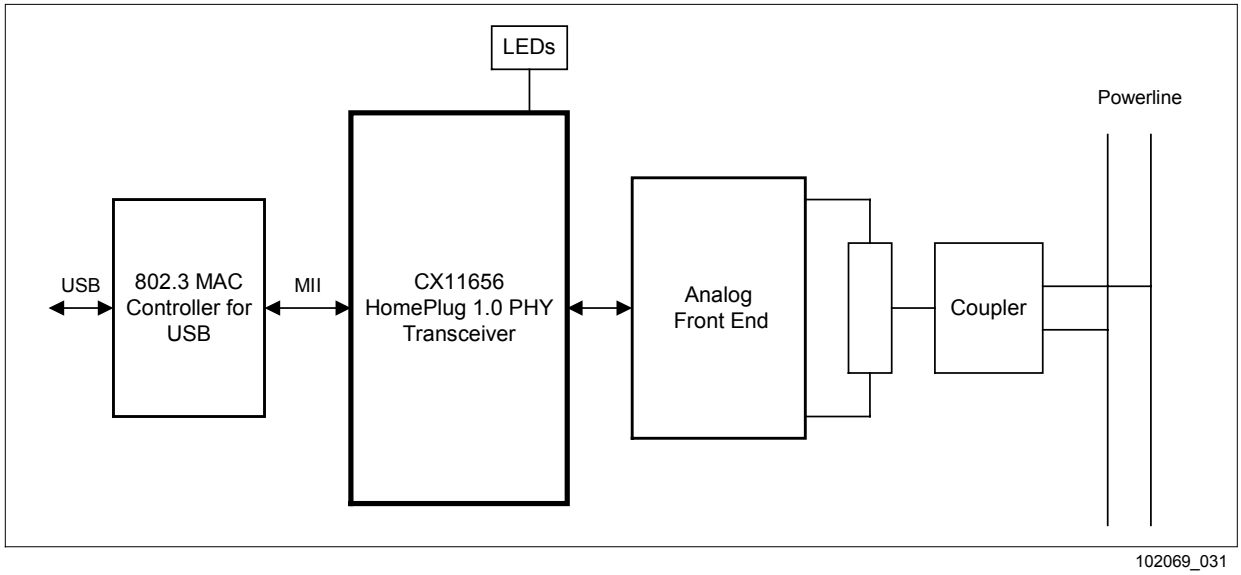
Figure 5-1. Ethernet Router Application Block Diagram



5.2 USB Application

A USB application design is illustrated in Figure 5-2.

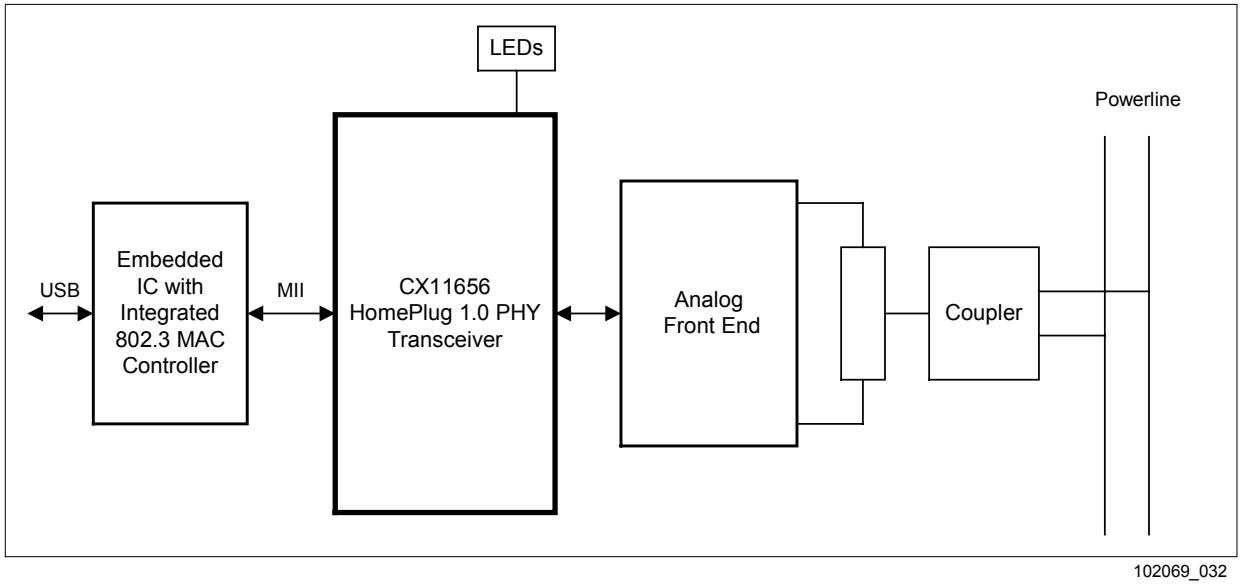
Figure 5-2. USB Application Block Diagram



5.3 Embedded Application

An embedded application design is illustrated in Figure 5-3.

Figure 5-3. Embedded Application Block Diagram



5.4 ADI-Related Components

For further information regarding the ADI components used in the Analog Front End, please refer to the following ADI data sheets:

AD8007/AD8008 - Low Distortion High Speed Amp

AD6417 - LC^{2}MOS Precision Mini-DIP Analog Switch

AD8016 – Low Power, High Output Current xDSL Line Driver

AD9975 – Broadband Modem Mixed-Signal Front End

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NOTES

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