

Dual N-Channel 100-V (D-S) MOSFET

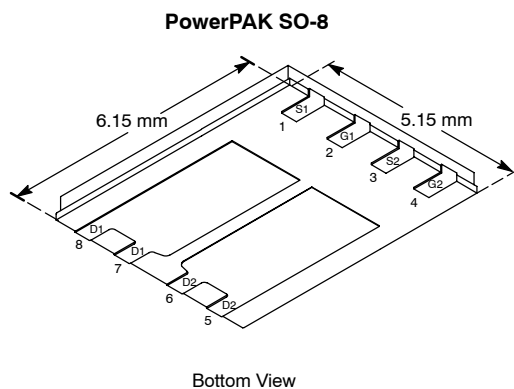
PRODUCT SUMMARY		
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
100	0.049 @ V _{GS} = 10 V	5.9
	0.060 @ V _{GS} = 6 V	5.5

FEATURES

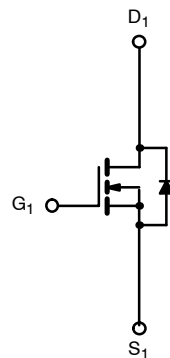
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package
- Dual MOSFET for Space Savings

APPLICATIONS

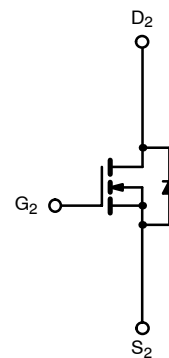
- Synchronous Buck Shoot-Through Resistant
- Optimized for Primary Side Switch



Ordering Information: Si7942DP-T1



N-Channel MOSFET



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V _{DS}	100		V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	5.9	3.8	A
	T _A = 70°C		4.7	3.0	
Pulsed Drain Current		I _{DM}	20		
Continuous Source Current (Diode Conduction) ^a		I _S	2.9	1.2	
Single Avalanche Current	L = 0.1 mH	I _{AS}	20		
Single Avalanche Energy		E _{AS}	20		mJ
Maximum Power Dissipation ^a	T _A = 25°C	P _D	3.5	1.4	W
	T _A = 70°C		2.2	0.9	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	t ≤ 10 sec	R _{thJA}	26	35	°C/W
	Steady State		60	85	
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	2.2	2.7	

Notes

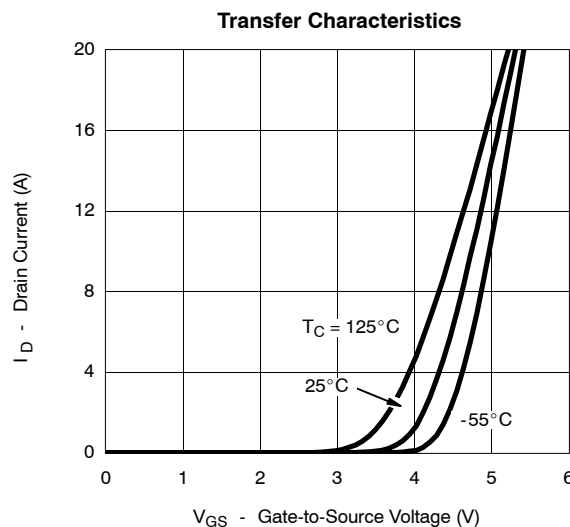
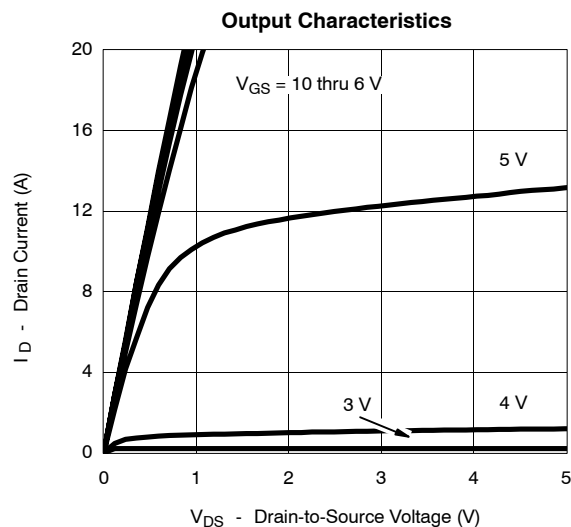
a. Surface Mounted on 1" x 1" FR4 Board.

SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2		4.0	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80 V, V _{GS} = 0 V			1	μA
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 55 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	20			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 5.9 A		0.041	0.049	Ω
		V _{GS} = 6 V, I _D = 5.5 A		0.048	0.060	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 5.9 A		14		S
Diode Forward Voltage ^a	V _{SD}	I _S = 2.9 A, V _{GS} = 0 V		0.77	1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 5.9 A		16	24	nC
Gate-Source Charge	Q _{gs}			3.8		
Gate-Drain Charge	Q _{gd}			5.5		
Gate Resostance	R _g			2.2		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, R _L = 50 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω		15	25	ns
Rise Time	t _r			15	25	
Turn-Off Delay Time	t _{d(off)}			35	55	
Fall Time	t _f			20	30	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.9 A, di/dt = 100 A/μs		50	75	

Notes

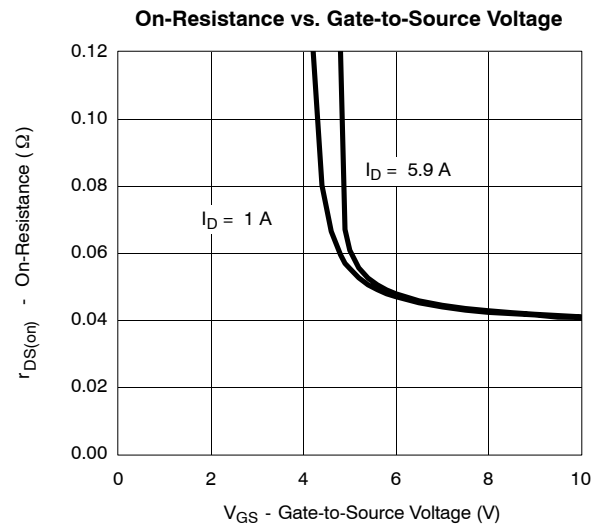
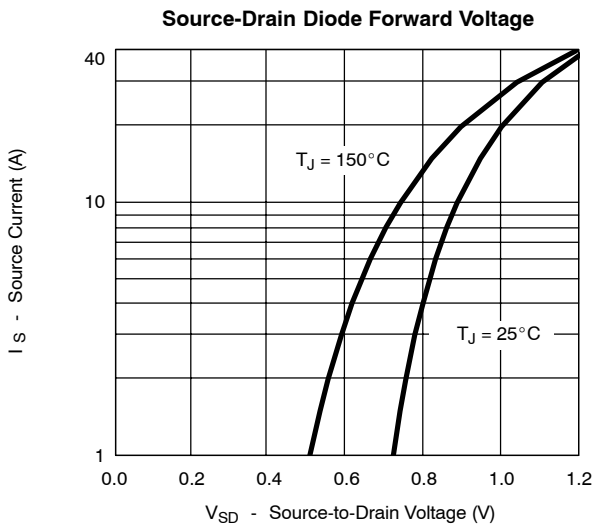
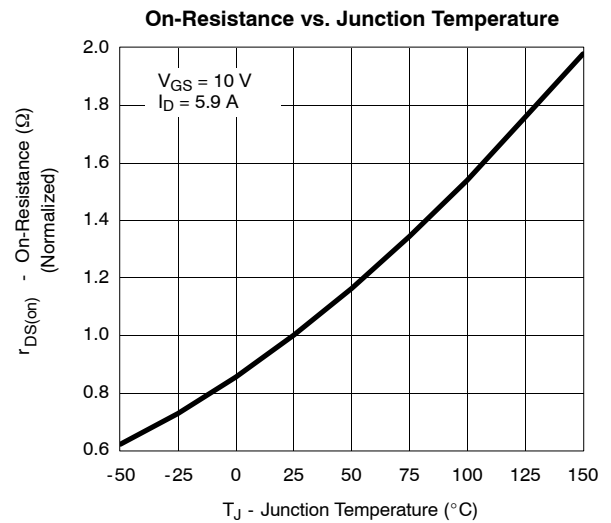
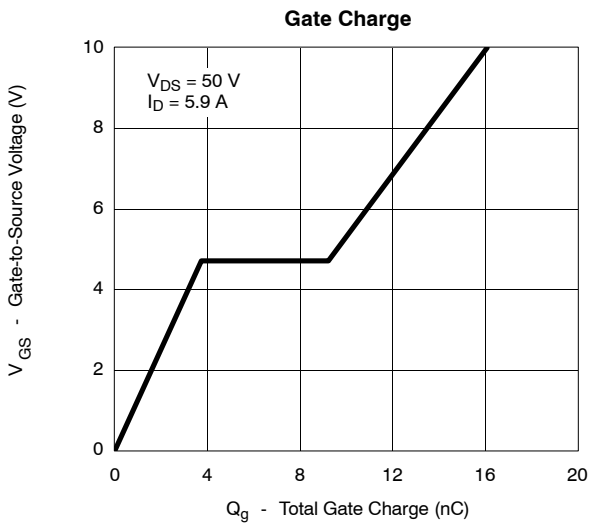
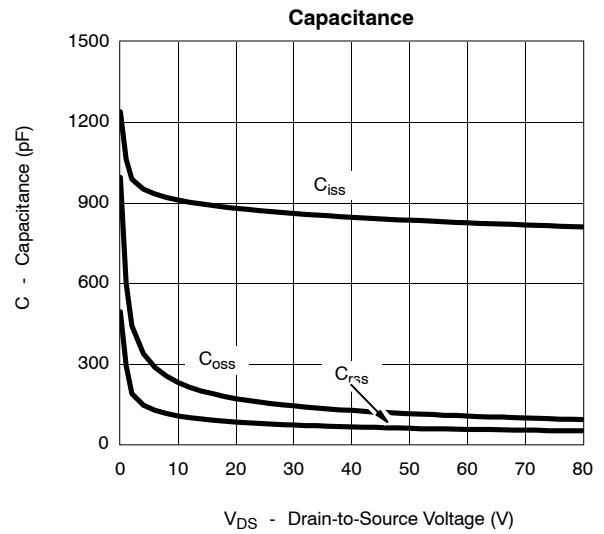
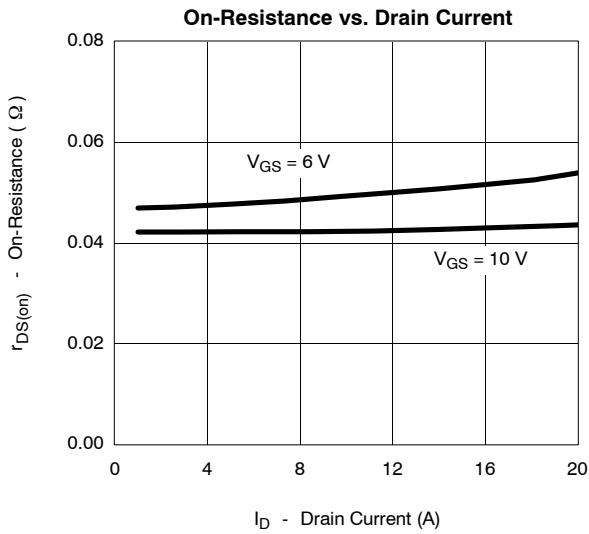
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



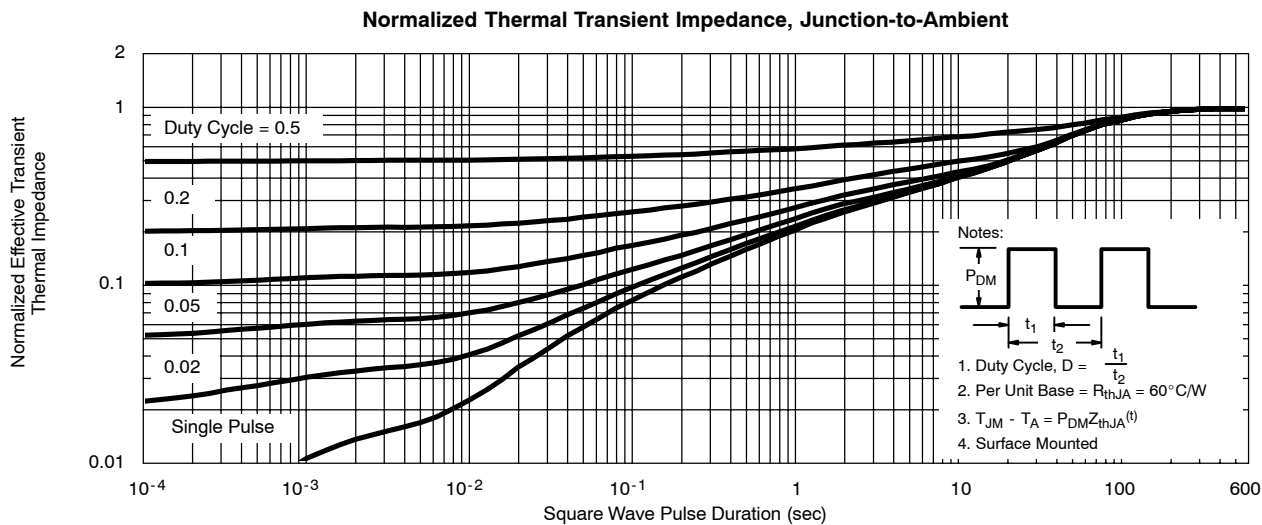
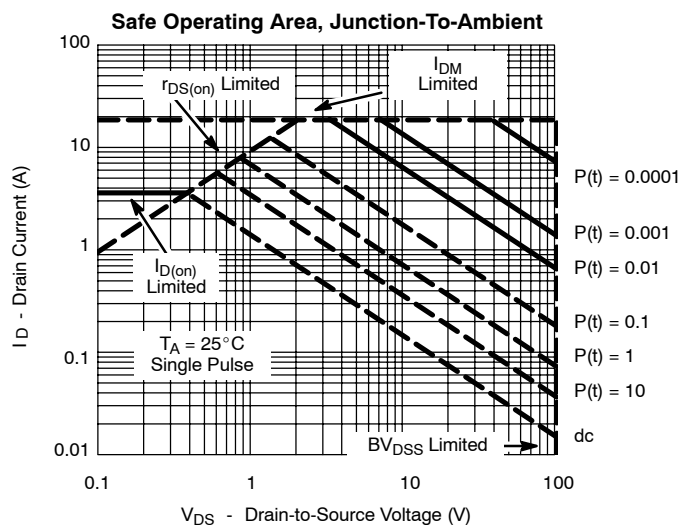
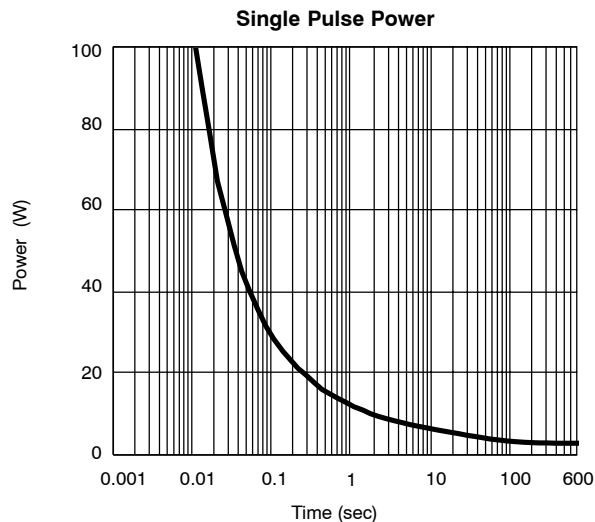
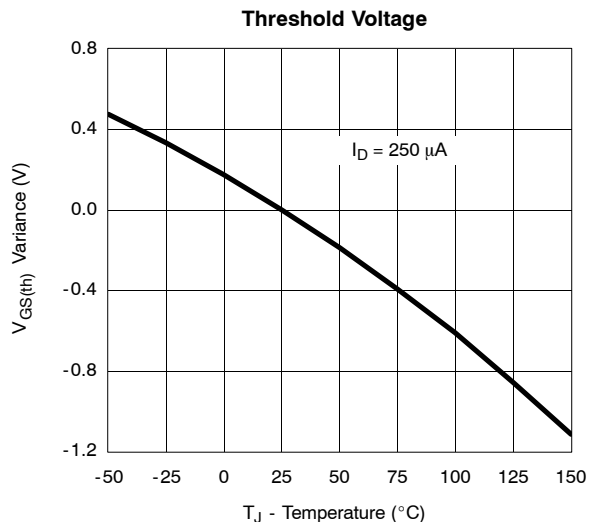


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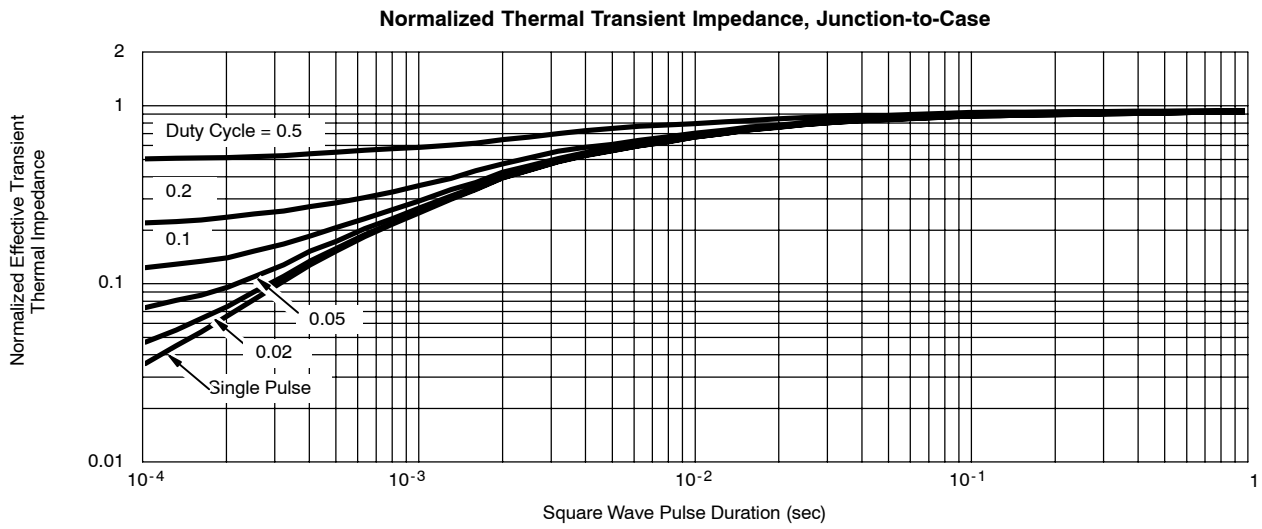


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