



MOTOROLA

MCM14552

256-BIT STATIC RANDOM ACCESS MEMORY

The MCM14552 is a static random access memory (RAM) organized in a 64 x 4 bit pattern. The three chip enable inputs can be used as extensions of the six address inputs, creating 9-bit address scheme. Eight MCM14552 devices may be used to comprise a 2048-bit memory (512 x 4) without additional address decoding.

The mode control (M) is used to change the control logic characteristic of the circuit. For example, with M high, the 3-state input (T) fully controls the 3-state characteristic of the output. With M low, the output 3-state characteristic is controlled by chip enable inputs (CE), write enable input (WE) and T.

The memory is designed so that dc signals may operate the memory, with no maximum pulse width restrictions.

Medium speed, micropower operation, and control flexibility make the device useful in scratch pad or buffer applications where battery operation or high noise immunity are required.

- Quiescent Current = 50 μ A/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- 3-state Output Capability for Memory Expansion
- Output Data Latch Eliminates Need for Storage Buffer
- Access Time = 700 ns typical @ V_{DD} = 10 Vdc
- Fully Decoded and Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

NOTE: Pin 20(LE) must be connected to V_{SS}

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V _{in}	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device	T _A	-55 to +125	°C
CL/CP Device		-40 to +85	
Storage Temperature Range	T _{stg}	-65 to +150	°C

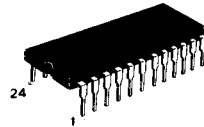
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

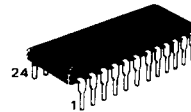
CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

256-BIT (64 x 4) STATIC RANDOM ACCESS MEMORY

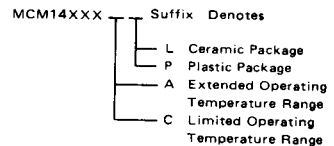


L SUFFIX
CERAMIC PACKAGE
CASE 623

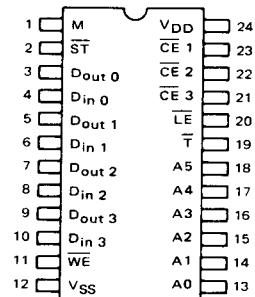


P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION



PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	VDD Vdc	T _{low} *		25°C			T _{high} *		Unit	
			Min	Max	Min	Typ	Max	Min	Max		
Output Voltage "0" Level V _{in} V _{DD} or 0	V _{OL}	5.0	-	0.05	-	0	0.05	-	0.05	Vdc	
		10	-	0.05	-	0	0.05	-	0.05		
		15	-	0.05	-	0	0.05	-	0.05		
	"1" Level V _{in} 0 or V _{DD}	V _{OH}	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
			10	9.95	-	9.95	10	-	9.95	-	
			15	14.95	-	14.95	15	-	14.95	-	
Input Voltage** "0" Level (V _O 4.5 or 0.5 Vdc) (V _O 9.0 or 1.0 Vdc) (V _O 13.5 or 1.5 Vdc)	V _{IL}	5.0	-	1.5	-	2.25	1.5	-	1.5	Vdc	
		10	-	3.0	-	4.50	3.0	-	3.0		
		15	-	4.0	-	6.75	4.0	-	4.0		
	"1" Level (V _O - 0.5 or 4.5 Vdc) (V _O 1.0 or 9.0 Vdc) (V _O 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	-	3.5	2.75	-	3.5	-	Vdc
			10	7.0	-	7.0	5.50	-	7.0	-	
			15	11.0	-	11.0	8.25	-	11.0	-	
Output Drive Current (AL Device) (V _{OH} - 2.5 Vdc) Source (V _{OH} - 4.6 Vdc) (V _{OH} - 9.5 Vdc) (V _{OH} - 13.5 Vdc)	I _{OH}	5.0	-1.2	-	-1.0	-1.7	-	-0.7	-	mAdc	
		5.0	-0.25	-	-0.2	-0.36	-	-0.14	-		
		10	-0.62	-	-0.5	-0.9	-	-0.35	-		
	Sink (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	I _{OL}	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdc
			10	1.6	-	1.3	2.25	-	0.9	-	
			15	4.2	-	3.4	8.8	-	2.4	-	
Output Drive Current (CL/CP Device) (V _{OH} - 2.5 Vdc) Source (V _{OH} - 4.6 Vdc) (V _{OH} - 9.5 Vdc) (V _{OH} - 13.5 Vdc)	I _{OH}	5.0	-1.0	-	-0.8	-1.7	-	-0.6	-	mAdc	
		5.0	-0.2	-	-0.16	-0.36	-	-0.12	-		
		10	-0.5	-	-0.4	-0.9	-	-0.3	-		
	Sink (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	I _{OL}	5.0	0.52	-	0.44	0.88	-	0.36	-	mAdc
			10	1.3	-	1.1	2.25	-	0.9	-	
			15	3.6	-	3.0	8.8	-	2.4	-	
Input Current (AL Device)	I _{in}	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	μAdc	
Input Current (CL/CP Device)	I _{in}	15	-	±1.0	-	±0.00001	±1.0	-	±14.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	-	-	-	-	5.0	7.5	-	-	pF	
Quiescent Current (AL Device) (Per Package)	I _{DD}	5.0	-	5.0	-	0.050	5.0	-	150	μAdc	
		10	-	10	-	0.100	10	-	300		
		15	-	20	-	0.150	20	-	600		
Quiescent Current (CL/CP Device) (Per Package)	I _{DD}	5.0	-	50	-	0.050	50	-	375	μAdc	
		10	-	100	-	0.100	100	-	750		
		15	-	200	-	0.150	200	-	1500		
Total Supply Current** I _T (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.98 μA/kHz) f + I _{DD}							μAdc	
		10	I _T = (3.96 μA/kHz) f + I _{DD}								
		15	I _T = (5.86 μA/kHz) f + I _{DD}								
Three-State Leakage Current (AL Device)	I _{TL}	15	-	±0.1	-	±0.00001	±0.1	-	±3.0	μAdc	
Three-State Leakage Current (CL/CP Device)	I _{TL}	15	-	±1.0	-	±0.00001	±1.0	-	±7.5	μAdc	

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.

T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

=Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc

2.0 Vdc min @ V_{DD} = 10 Vdc

2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.



SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Figure	Symbol	V _{DD}	Min	Typ	Max	Unit
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	1	t_{TLH}	5.0 10 15	— — —	180 90 65	360 180 130	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	1	t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Read Cycle Time	1, 2	$t_{cyc}(R)$	5.0 10 15	— — —	2000 750 500	6000 2200 1650	ns
Write Cycle Time	3, 4	$t_{cyc}(W)$	5.0 10 15	— — —	1200 750 500	3600 2200 1650	ns
Address to Strobe Setup Time	1, 3	$t_{su}(A-\overline{ST})$	5.0 10 15	1500 450 350	500 150 120	— — —	ns
Strobe to Address Hold Time	1, 3	$t_h(\overline{ST}-A)$	5.0 10 15	150 100 75	50 0 0	— — —	ns
Address to Chip Enable Setup Time	2, 4	$t_{su}(A-\overline{CE})$	5.0 10 15	1800 600 450	600 200 150	— — —	ns
Chip Enable to Address Hold Time	2, 4	$t_h(\overline{CE}-A)$	5.0 10 15	450 300 225	150 100 75	— — —	ns
Strobe or Chip Enable Pulse Width When Reading	1, 2	$t_{WL}(R)$	5.0 10 15	1800 450 350	450 150 100	— — —	ns
Strobe or Chip Enable Pulse Width When Writing	3, 4	$t_{WL}(W)$	5.0 10 15	3600 1800 1350	1200 600 400	— — —	ns
Read Setup Time	1	$t_{su}(R)$	5.0 10 15	0 0 0	-100 -40 -30	— — —	ns
Read Hold Time	1	$t_h(R)$	5.0 10 15	540 240 180	180 60 45	— — —	ns
Data Setup Time	3, 4	$t_{su}(D)$	5.0 10 15	1800 600 450	600 200 150	— — —	ns
Data Hold Time	3, 4	$t_h(D)$	5.0 10 15	600 150 120	200 50 30	— — —	ns

*The formula given is for the typical characteristics only.

(continued)

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C) (continued)

Characteristic	Figure	Symbol	V _{DD}	Min	Typ	Max	Unit
Write Enable Setup Time	3, 4	t _{SU} (WE)	5.0	720	240	—	ns
			10	240	80	—	
			15	180	55	—	
Write Enable Hold Time	3, 4	t _H (WE)	5.0	150	50	—	ns
			10	60	20	—	
			15	45	15	—	
Read Access Time from Strobe	1, 3	t _{ACC} (R-ST)	5.0	—	2000	6000	ns
			10	—	700	2100	
			15	—	350	1600	
Read Access Time from Chip Enable	2	t _{ACC} (R-CE)	5.0	—	2100	6300	ns
			10	—	750	2250	
			15	—	400	1700	
Output Enable/Disable Delay from Chip Enable or Write Enable	2, 4	t _R (CE), t _R (WE)	5.0	—	400	1200	ns
			10	—	200	600	
			15	—	150	450	
Three-State Enable/Disable Output Delay	2	t(T)	5.0	—	400	1200	ns
			10	—	160	480	
			15	—	120	360	
Latch to Output Propagation Delay	1	t _{LE}	5.0	—	500	1500	ns
			10	—	200	600	
			15	—	150	450	

*The formula given is for the typical characteristics only.

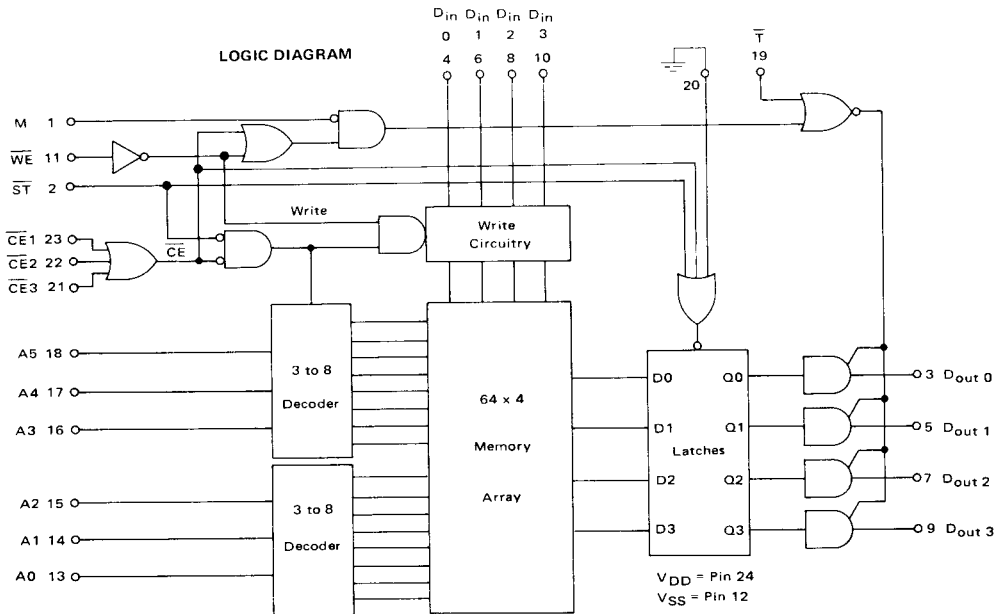
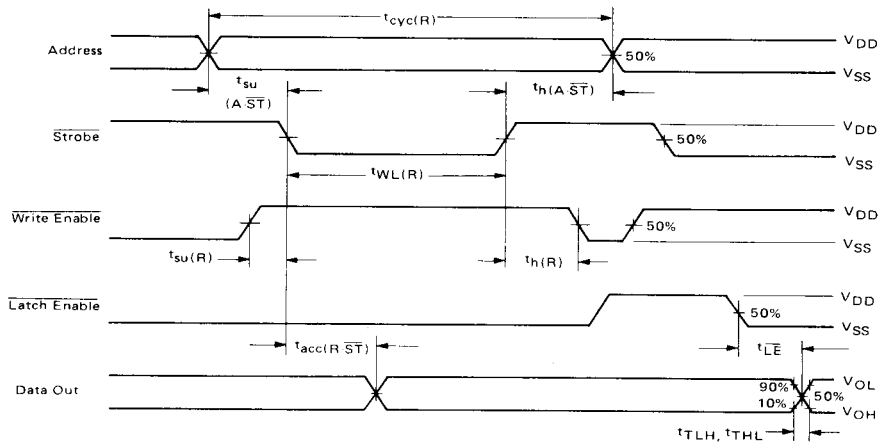
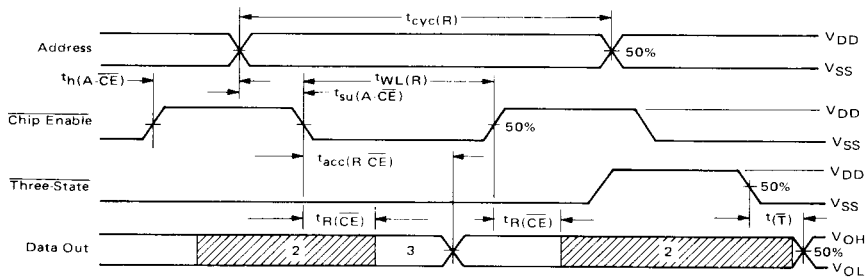


FIGURE 1 – READ CYCLE WAVEFORMS UTILIZING STROBE TO ACCESS MEMORY



- Notes:
- 1 $\overline{CE}1, \overline{CE}2, \overline{CE}3$ and \overline{T} are low, M is high.
 - 2 \overline{WE} may be held high during the complete read cycle.

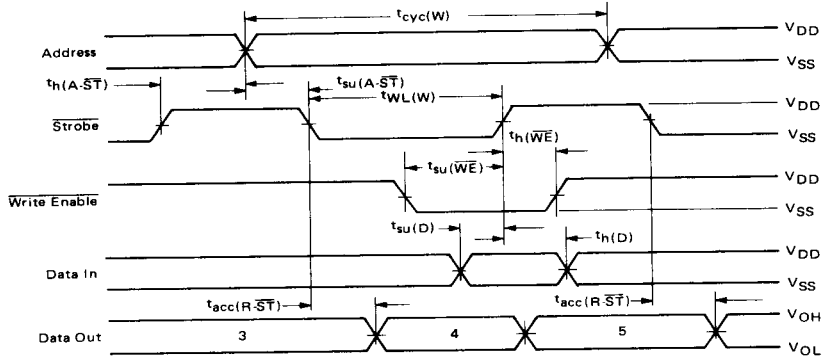
FIGURE 2 – READ CYCLE WAVEFORMS UTILIZING CHIP ENABLE TO ACCESS MEMORY



- Notes:
- 1 - Unused $\overline{CE}, \overline{ST}, M$ and \overline{T} are low and \overline{WE} is high.
 - 2 - High impedance output state occurs when any \overline{CE} is high and M is low, or when \overline{T} is high.
 - 3 - The output displays data from the previous state.
 - 4 - $t_{WL}(R) \geq t_{acc}(R \overline{CE})_{max}$.

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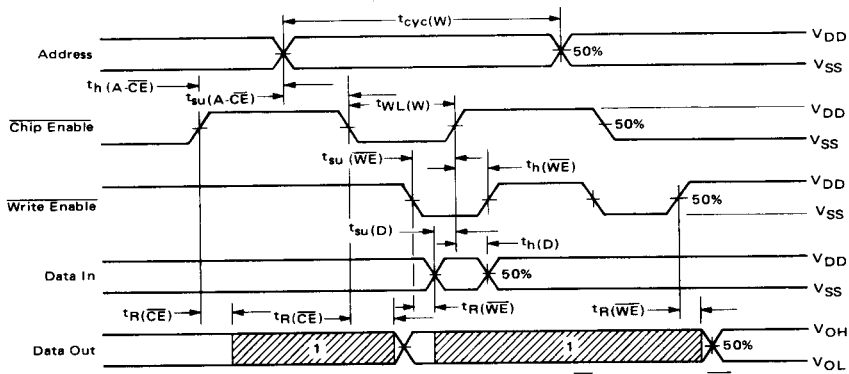
FIGURE 3 – WRITE CYCLE WAVEFORMS UTILIZING STROBE



- Notes:
- 1 – $\overline{CE}1$, $\overline{CE}2$, $\overline{CE}3$ and \overline{T} are maintained at the logical "0" level.
 - 2 – M is maintained at the logical "1" level.
 - 3 – The output displays the contents of the previous state.
 - 4 – The output displays the contents of the presently addressed location as in a read modify write cycle.
 - 5 – The output displays the data that was written into addressed location.

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FIGURE 4 – WRITE CYCLE WAVEFORM UTILIZING CHIP ENABLE



- Notes:
- 1 – High impedance output state occurs when \overline{CE} is high or when \overline{WE} is low, for M and \overline{T} maintained in the low state.
 - 2 – Unused \overline{CE} 's, ST, M and \overline{T} are maintained at the logical "0" level.

TRUTH TABLE

Function	CE 1	CE 2	CE 3	T	LE	M	ST	WE	D _{in}	D _{out}	Comments
Address Changing Valid	X	X	X	X	X	X	1	X	X	R/A	D _{out} will be active if all CE = 0, T = 0 and WE = 1 or if M = 1 and T = 0
Address Changing Not Valid	0	0	0	X	X	X	0	X	X	R/A	D _{out} will be active if T = 0 and WE = 1 or if M = 1 and T = 0
D _{out} Disabled (in high resistance state)	X	X	1	X	X	0	X	X	X	R	Disables write circuitry
D _{out} Enabled (in active state)	0	0	0	0	X	X	X	1	X	A	Read operation, D _{out} active
Read Address Memory Location Into Output Latch	X	X	X	0	X	1	X	X	X	A	Read or write, D _{out} active
Disable Reading From Memory	X	X	1	X	X	X	X	X	X	R/A	If WE = 0, D _{in} = D _{out}
Write Into Memory	0	0	0	X	X	X	0	0	A	R/A	
Write Disabled	X	X	1	X	X	X	X	X	X	R/A	
Output Latch Enabled	0	0	0	X	0	X	0	X	X	R/A	
Output Latch Disabled	X	X	1	X	X	X	X	X	X	R/A	

R - High resistance state at D_{out} X - Don't care condition (must be in the "1" or "0" state)
 A - An active level of either V_{DD} or V_{SS} 1 - A high level at V_{DD}
 R/A - An R or A condition depending on the don't care condition 0 - A low level at V_{SS}

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FIGURE 5 - 512 WORD x 16 BIT MEMORY BOARD Data Inputs

