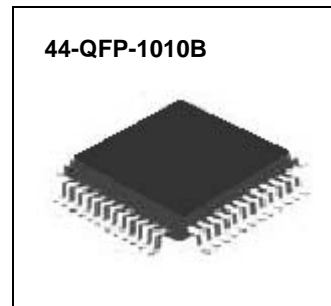# FAN8038C
4-Channel Motor Drive IC

Features

- 4-CH H-Bridge driver
- Built-in DC-DC converter controller
- Built-in Power-on reset (POR) circuit
- Built-in battery charging circuit
- Built-in battery voltage monitoring circuit
- Built-in thermal shutdown (TSD) circuit
- Built-in general OP-Amplifier
- Low power consumption
- Built-in power controller circuit

Description

FAN8038C is monolithic IC for portable CD player, and suitable for a 4-CH motor driver which drives focus acutator, tracking actuator, sled motor and spindle motor of portable CD player system. And it also provides DC-DC converter, reset, recharge, and short circuit protection.
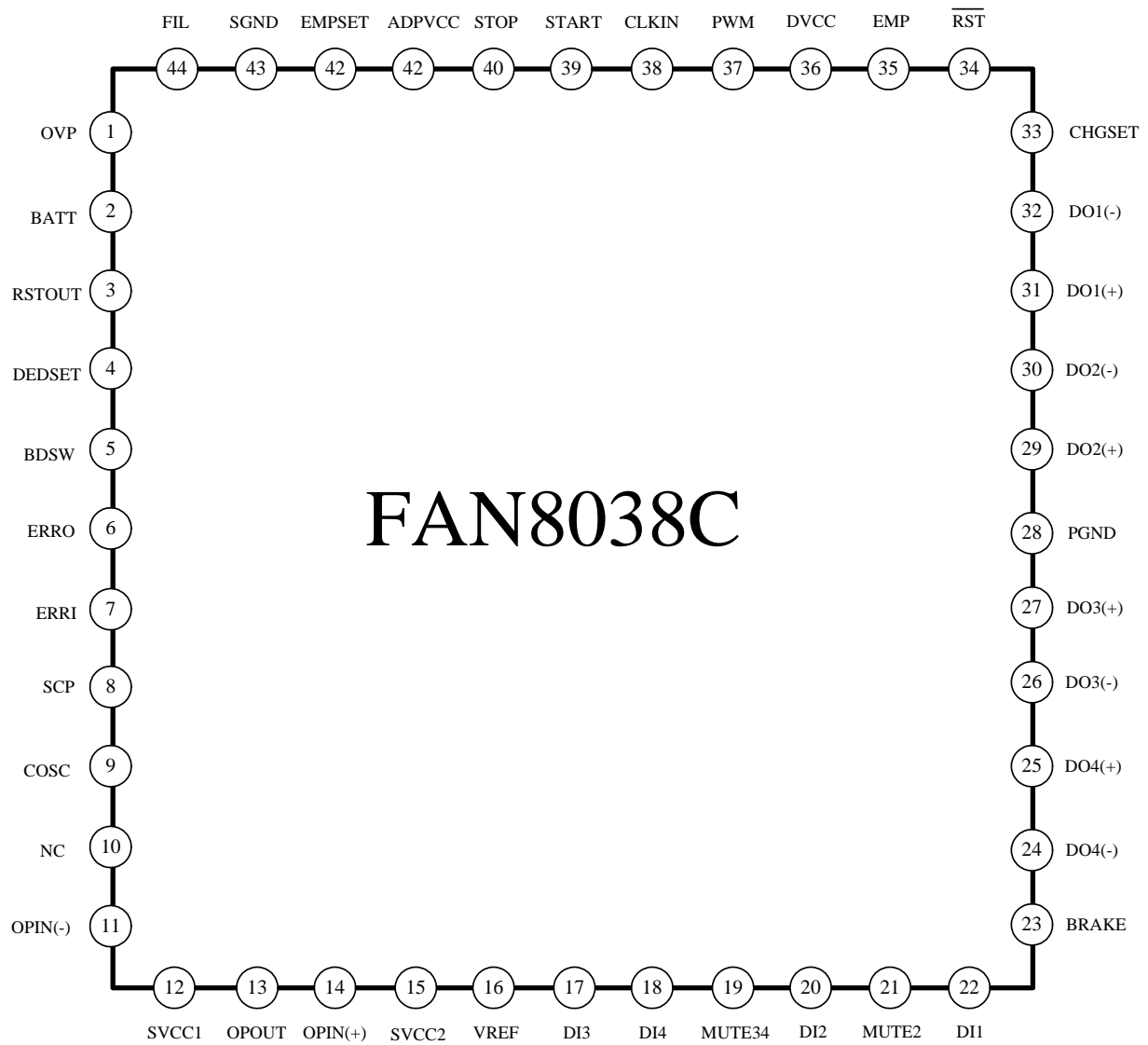
44-QFP-1010B

Typical application

- Portable Compact Disk Player (CDP)
- Portable Mini Disk Player (MD)
- Disc-Man
- Other Potable Compact Disk Media

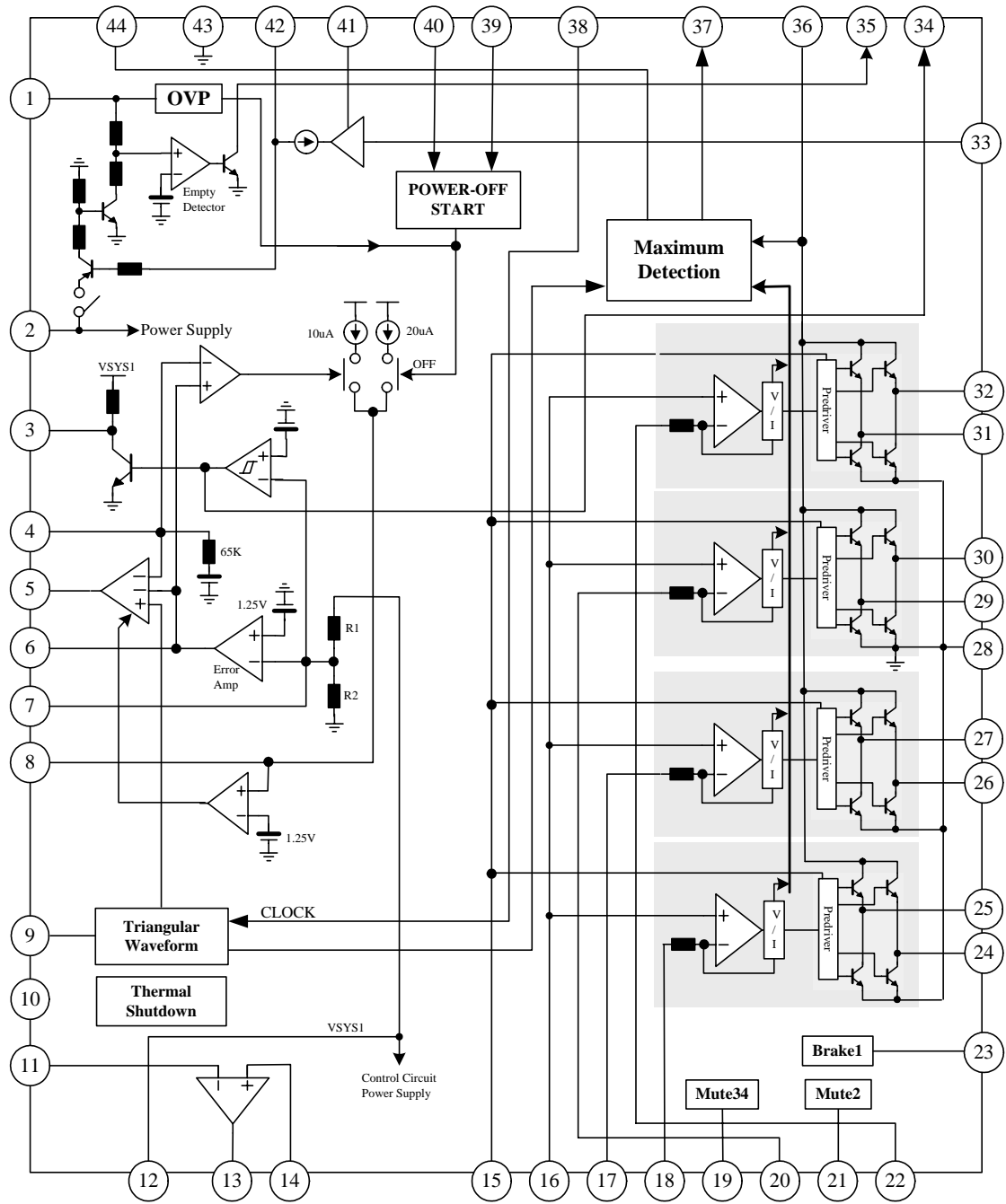## Ordering Information

Device	Package	Operating Temp.
FAN8038C	44-QFP-1010B	-35°C ~ +85°C

Rev. 1.0.0

Pin Assignments

FIL — 44
SGND — 43
EMPSET — 42
ADPVCC — 42
STOP — 40
START — 39
CLKIN — 38
PWM — 37
DVCC — 36
EMP — 35
$\overline{RST}$ — 34

OVP — 1
BATT — 2
RSTOUT — 3
DEDSET — 4
BDSW — 5
ERRO — 6
ERRI — 7
SCP — 8
COSC — 9
NC — 10
OPIN(-) — 11

FAN8038C

33 — CHGSET
32 — DO1(-)
31 — DO1(+)
30 — DO2(-)
29 — DO2(+)
28 — PGND
27 — DO3(+)
26 — DO3(-)
25 — DO4(+)
24 — DO4(-)
23 — BRAKE

12 — SVCC1
13 — OPOUT
14 — OPIN(+)
15 — SVCC2
16 — VREF
17 — DI3
18 — DI4
19 — MUTE34
20 — DI2
21 — MUTE2
22 — DI1

Pin Definitions

Pin Number	Pin Name	I/O	Pin Function Description
1	OVP	I	Battery voltage motor
2	BATT	-	Battery power supply input
3	RSTOUT	O	Power-on reset output
4	DEDSET	I	Dead time setting capacitor
5	BDSW	O	Transistor drive for voltage step-up
6	ERRO	O	Error amplifier output
7	ERRI	I	Error amplifier Input
8	SCP	I	Short circuit protection time setting capacitor
9	COSC	O	Triangular waveform output
10	N.C	-	No connection
11	OPIN(-)	I	OP-amplifier negative input
12	SVCC1	-	Control circuit power supply
13	OPOUT	O	OP-amplifier output
14	OPIN(+)	I	OP-amplifier positiveinput
15	SVCC2	-	Pre-driver power supply
16	VREF	I	Reference voltage input
17	DI3	I	Channel 3 control signal Input
18	DI4	I	Channel 4 control signal Input
19	MUTE34	I	Channel 3 and 4 mute signal input
20	DI2	I	Channel 2 control signal Input
21	MUTE2	I	Channel 2 mute signal inpu
22	DI1	I	Channel 1 control signal Input
23	BRAKE	I	Channel 1 brake signal input
24	DO4(-)	O	Channel 4 negative output
25	DO4(+)	O	Channel 4 positive output
26	DO3(-)	O	Channel 3 negative output
27	DO3(+)	O	Channel 3 positive output
28	PGND	-	Power block power Ground
29	DO2(+)	O	Channel 2 positive output
30	DO2(-)	O	Channel 2 negative output
31	DO1(+)	O	Channel 1 positive output
32	DO1(-)	O	Channel 1 negative output
33	CHGSET	I	Charge current setting resistance
34	RST	O	Power-on reset inverting output
35	EMP	O	Battery voltage detection output (Empty detection)
36	DVCC	-	H-Bridge block power supply
37	PWM	O	PWM transistor drive output
38	CLKIN	I	External clock input
39	START	I	DC-DC converter start control input
40	STOP	I	DC-DC converter off control input
41	ADPVCC	-	Charging circuit power supply
42	EMPSET		Empty dection level switch
43	SGND	-	Signal ground
44	FIL	I	PWM phase compensation

Internal Block Diagram

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Value	Unit
Maximum supply voltage	V_{CC}	13.2	V
Maximum output current	I_O	500	mA
Power dissipation	P_D	1.0	W
Operating temperature	T_{OPR}	-35 ~ +85	°C
Stroage temperature	T_{STG}	-55 ~ +150	°C

Recommended Operating Conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Charging circuit power supply voltage	ADPVCC	3.0	4.5	8.0	V
Power supply voltage	BATT	1.5	2.4	8.0	V
Control circuit power supply voltage	SVCC1	2.7	3.2	5.5	V
Pre-driver power supply voltage	SVCC2	2.7	3.2	5.5	V
H-Bridge power supply voltage	DVCC	-	PWM	BATT	V
Operating Temperature	Ta	-10	25	70	°C

Electrical characteristics

(Ta=25°C, BATT=2.4V, SVCC1=SVCC2=3.2V, V_{REF}=1.6V, ADPVCC=0V, f_{CLKIN}=88.2KHz, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
COMMON SECTION						
BATT Stand-by Current	I_{ST}	BATT=10.5V, SVCC1=SVCC2=VREF=0V	-	-	5	μA
BATT Supply Current (No Load)	I_{BATT}	DVCC=0.45V, MUTE34=3.2V	-	2.5	3.5	mA
SVCC Supply Current (No Load)	I_{SVCC1}	DVCC=0.45V, MUTE34=3.2V, ERRI=0V	-	3.0	3.5	mA
SVCC2 Supply Current (No Load)	I_{SVCC2}	DVCC=0.45V, MUTE34=3.2V	-	3.5	5.0	mA
ADPVCC Supply Current (No Load)	I_{ADPVCC}	ADPVCC=4.5V, ROUT=OPEN	-	0.2	1.0	mA
H-BRIDGE DRIVER PART						
Voltage Gain CH1, 3, 4	$G_{VC}134$	-	12	14	16	dB
Voltage Gain CH2	$G_{VC}2$		21.5	23.5	24.5	dB
Gain Error By Polarity	ΔG_{VC}	-	-2	0	2	dB
Input pin Resistance CH1, 3, 4	$R_{DI}134$	IN=1.7 and 1.8V	9	11	13	KΩ
Input pin Resistance CH2	$R_{DI}2$	IN=1.7 and 1.8V	6	7.5	9	KΩ
Maximum Output Voltage	V_{OUT}	RL=8Ω, DVCC=BATT=4V, IN=0 ~ 3.2V	1.9	2.1	-	V
Saturation Voltage (Lower)	$V_{SAT}1$	IO= -300mA, IN=0 and 3.2V	-	240	400	mV
Saturation Voltage (Upper)	$V_{SAT}2$	IO=300mA, IN=0 and 3.2V	-	240	400	mV
Input offset Voltage	V_{IO}	-	-8	0	8	mV
Output Offset Voltage CH1, 3, 4	$V_{OO}134$	VREF=IN=1.6V	-70	0	70	mV
Output Offset Voltage CH2	$V_{OO}2$	VREF=IN=1.6V	-130	0	130	mV
DEAD Zone	V_{DB}	-	-20	0	20	mV
Brake1 On Voltage	V_{M1ON}	DI1=1.8V	2.0	-	-	V
Brake1 Off Voltage	V_{M1OFF}	DI1=1.8V	-	-	0.8	V
MUTE2 On Voltage	V_{M2ON}	DI2=1.8V	2.0	-	-	V
MUTE2 Off Voltage	V_{M2OFF}	DI2=1.8V	-	-	0.8	V
MUTE34 On Voltage	V_{M34ON}	DI3=DI4=1.8V	-	-	0.8	V
MUTE34 Off Voltage	V_{M34OFF}	DI3=DI4=1.8V	2.0	-	-	V
VREF On Voltage	V_{REFON}	IN1=IN2=IN3=IN4=1.8V	1.2	-	-	V
VREF Off Voltage	V_{REFOFF}	IN1=IN2=IN3=IN4=1.8V	-	-	0.8	V
BRAKE1 Brake Current	I_{BRAKE}	Brake Current	4	7	10	mA

*Granteed Design Value

Electrical Characteristics

(Ta=25°C, BATT=2.4V, SVCC1=SVCC2=3.2V, V$_{REF}$=1.6V, ADPVCC=0V, f$_{CLKIN}$=88.2KHz, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
PWM POWER SUPPLY DRIVING						
PWM Sink Current	I$_{PWM}$	DI1=2.1V	10	13	17	mA
*DVCC Level Shift Voltage	V$_{SHIF}$	DI1=1.8V, DVCC-OUT1F	0.35	0.45	0.55	V
DVCC Leak Current	I$_{DLK}$	DVCC=9V, SVCC1,2=BATT=0V	-	0	5	μA
*PWM Amp Transfer Gain	G$_{PWM}$	DI1=1.8V, DVCC=1.2V ~ 1.4V	1/60	1/50	1/40	1/KΩ
DC-DC CONVERTER						
ERROR AMP						
SVCC1 Pin Threshold Voltage	V$_{S1TH}$	-	3.05	3.20	3.35	V
ERRO Pin Output Voltage H	V$_{EOH}$	ERRI=0.7V, IO = -100μA	1.4	1.6	-	V
ERRO Pin Output Voltage L	V$_{EOL}$	ERRI=1.3V, IO = 100μA	-	-	0.3	V
SHORT CIRCUIT PROTECTION						
SCP Pin Voltage	V$_{SCP}$	ERRI=1.3V	-	0	0.1	V
SCP Pin Current 1	I$_{SCP1}$	ERRI=0.7V	6	10	16	μA
SCP Pin Current 2	I$_{SCP2}$	ERRI=1.3V, OFF=0V	12	20	32	μA
SCP Pin Current 3	I$_{SCP3}$	ERRI=1.3V, BATT=9.5V	12	20	32	μA
*SCP Pin Impedance	R$_{SCP}$	-	175	220	265	KΩ
SCP Pin Threshold Voltage	V$_{SCPTH}$	ERRI=0.7V, COSC=470PF	1.10	1.20	1.30	V
Over Voltage Protection Detect	V$_{OVP}$	OVP Voltage	9.5	10	10.5	V
TRANSISTOR DRIVING						
BDSW Pin Output Voltage 1H	V$_{SW1H}$	BATT=COSC=1.5V =SVCC2=0V, 10mA	0.78	0.98	1.13	V
BDSW Pin Output Voltage 2H	V$_{SW2H}$	COSC=0V, I$_O$ = -10mA, ERRI=0.7V SCP=0V	1.0	1.5	-	V
BDSW Pin Output Voltage 2L	V$_{SW2L}$	CT=2V, IO=1-mA	-	0.3	0.45	V
BDSW Pin Oscillating Reequency1	f$_{SW1}$	COSC=470pF, =SVCC2=0V	65	80	95	KHz
SW Pin Oscillating Reequency 2	f$_{SW2}$	COSC=470pF, CLKIN=0V	60	70	82	KHz
BDSW Pin Oscillating Reequency 3	f$_{SW3}$	COSC=470pF	-	88.2	-	KHz
*BDSW Pin Minimum Pulse Width	T$_{SWMIN}$	COSC=470pF, ERRO=0.5 → 0.7V	0.01	-	0.6	μs
Pulse Duty Start	D$_{SW1}$	COSC=470PF, SVSS1,SVCC2=0V	40	50	60	%
MAX. Pulse Duty at Self-Running	D$_{SW2}$	COSC=470pF, ERR0=0.8V, CLKIN=0V	50	60	70	%
MAX. Pulse Duty at CLKIN Synchronization	D$_{SW3}$	ERR0=0.8V, COSC=470pF	45	55	65	%

*Granteed Design Value

Electrical Characteristics

(Ta=25°C, BATT=2.4V, SVCC1=SVCC2=3.2V, V_{REF}=1.6V, ADPVCC=0V, f_{CLKIN}=88.2KHz, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
DEAD TIME						
*DEDSET Pin Impedance	R_{DEDSET}	-	52	65	78	KΩ
DEDSET Pin Output Voltage	V_{DEDSET}	-	0.78	0.88	0.98	V
INTERFACE						
STOP Pin Threshold Voltage	V_{STOPTH}	ERRI=1.3V	2.0	-	-	V
STOP Pin Bias Current	I_{STOP}	OFF=0V	75	95	115	µA
START Pin On Threshold Voltage	V_{STATH1}	SVCC1,SVCC2=0V, COSC=2V	1.3	-	-	V
START Pin Off Threshold Voltage	V_{STATH2}	SVCC1,SVCC2=0V, COSC=2V	-	-	2.1	V
START Pin Bias Current	I_{START}	START=0V	13	16	19	µA
CLKIN Pin Threshold Voltage H	$V_{CLKINTHH}$	-	2.0	-	-	V
CLKIN Pin Threshold Voltage L	$V_{CLKINTHL}$	-	-	-	0.8	V
CLKIN Pin Bias Current	I_{CLKIN}	CLKIN=3.2V	-	-	10	µA
START CURCUIT						
Starter Switching Voltage	V_{SSV}	SVCC1,SVCC2=0V → 3.2V START=0V	2.3	2.5	2.7	V
Starter Switching Hysteresis Width	V_{SSHS}	START=0V	130	200	300	mV
Discharge Release Voltage	V_{DIS}	-	1.63	1.83	2.03	V
RESET CIRCUIT						
*SVCC1 RESET Threshold Voltage Ratio	R_{RSTOTH}	-	85	90	95	%
RESET Detection Hysteresis Width	V_{RSTHS}	-	25	50	100	mV
RSTOUT Pin Output Voltage	V_{RSTO}	IO=1mA, SVCC1,SVCC2=2.8V	-	-	0.5	V
RSTOUT Pin Pull Up Resistance	R_{RSTO}	-	72	90	108	KΩ
RST Pin Output Voltage 1	V_{RST1}	IO= -1mA, SVCC1,SVCC2=2.8V	2.0	-	2.4	V
RST Pin Output Voltage 2	V_{RST2}	IO= -1mA, SVCC1,SVCC2=0V	2.0	-	2.4	V
*RST Pin Pull Up Resistance	R_{RST}	-	77	95	113	KΩ

*Granteed Design Value

Electrical Characteristics

(Ta=25°C, BATT=2.4V, SVCC1=SVCC2=3.2V, V_{REF}=1.6V, ADPVCC=0V, f_{CLKIN}=88.2KHz, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
OP-AMP						
Input Bias Current	I_{BIAS}	IN(+)=1.6V	-	-	300	nA
Input Offset Voltage	V_{OFOP}	IN(+)=1.6V	-5.5	0	5.5	mV
High Level Output Voltage	V_{OHOP}	RL=OPEN	2.8	-	-	V
Low Level Output Voltage	V_{OLOP}	RL=OPEN	-	-	0.2	V
Output Drive Current (Source)	V_{SOURCE}	50Ω GND	-	-6.5	-3.0	mA
Output Drive Current (Sink)	V_{SINK}	50Ω SVCC	0.4	0.7	-	mA
*Open Loop Voltage Gain	GVO	VIN= -75dB, F=1kHz	-	70	-	dB
*Slew Rate	SR	-	-	0.5	-	V/µs
BATTERY CHARGING CURCUIT						
CHGSET Pin Bias Voltage	V_{CHGSET}	ADPVCC=4.5V, CHGSET=1.8kΩ	0.71	0.81	0.91	V
*CHGSET Pin Output Resistance	R_{CHGSET}	ADPVCC=4.5V	0.75	0.95	1.20	KΩ
EMPSET Pin Leak Current 1	I_{EMPSET}	ADPVCC=4.5V, CHGSET=OPEN	-	-	1.0	µA
EMPSET Pin Leak Current 2	I_{EMPSET}	ADPVCC = 0.6V, CHGSET = 1.8kΩ	-	-	1.0	µA
EMPSET Pin Saturation Voltage	V_{EMPSET}	ADPVCC = 4.5V, I_O = 300mA, CHGSET = 0Ω	-	0.45	1.0	V
EMPTY DETECTION						
EMP Detection Voltge 1	V_{EMPT1}	V_{EMPSET} = 0V	2.1	2.2	2.3	V
EMP Detection Voltge 2	V_{EMPT2}	I_{EMPSET} = -2µA	1.7	1.8	1.9	V
EMP Detection Hysteresis Voltage 1	V_{EMHS1}	V_{EMPSET} = 0V	25	50	100	mV
EMP Detection Hysteresis Voltage 2	V_{EMHS2}	I_{EMPSET} = -2µA	25	50	100	mV
EMP Pin Output Voltage	V_{EMP}	I_O = 1mA, OVP = 1V	-	-	0.5	V
EMP Pin Output Leak Current	I_{EMPLK}	OVP = 2.4V	-	-	1.0	µA
*OVP Pin Input Resistance	R_{OVP}	V_{EMPSET} = 0V	17	23	27	KΩ
OVP Pin Leak Current	I_{OVPLK}	SVCC1 = SVCC2 = 0V, OVP = 4.5V	-	-	1.0	V
EMP_SET Pin Detection Voltage	V_{EMPSET}	V_{EMPSET} = BATT-EMPSET, OVP = 2V	1.5	-	-	V
EMP_SET Pin Detection Current	I_{EMPSET}	EMPSET	-2	-	-	µA

*Granteed Design Value

Application Information

1. BAKE AND MUTE FUNCTION

- Of the four channel drivers, channel 1 has a brake function, and the other channels have a mute function.
- When the BRAKE (pin23) is set to high level, both channel 1 outputs go low level. (Brake mode).
- When the MUTE2 (pin21) is set to high level, the channel 2 output is muted.
- When the MUTE34 (pin19) is set to high level, the channel 3 and 4 outputs are muted.
-

2. REFERENCE VOLTAGE(VREF) DROP MUTE

- When the voltage applied to VREF (pin16) is 1.0V or less (typical), the H-bridge driver outputs are set to high impedance.

3. THERMAL SHUTDOWN (TSD)

- If the chip temperature reaches 150°C (typical), the H-bridge driver output current is cut-off and the thermal shut down circuit has a hysteresis temperature of 25°C.

4. H-BRIDGE DRIVER (4-CHANNELS)

- The driver input resistance is 11KΩ(typical) for channels 1, 3 , and 4, and 7.5KΩ for channel 2. Set the gain according to the following formula.
-

Channel	Gain	Unit
CH1 CH3 CH4	$Gv = 20\log\left\|\dfrac{55K}{11K + R_{EXT}}\right\|$	dB
CH2	$Gv = 20\log\left\|\dfrac{110K}{7.5K + R_{EXT}}\right\|$	dB

where, R_{EXT} is externally connected input resistance.

5. SWITCHING REGULATED POWER SUPPLY DRIVE

- The power supply of H-bridge driver consists of DVCC(pin36) for output stage power supply and VSYS2 (pin15) for predriver power supply.

Figure 1. Switching Regulated Power Supply

6. DC-DC CONVERTER CONTROL CIRCUIT

6-1. Set to output voltage

• The DC-DC converter output voltage, SVCC1, is set by internal resistors R3 and R4 and the voltage, SVCC1, is defined as follows.

$$SVCC1 = (1 + \frac{R3}{R4})1.267 = 2.5[V]$$

• This voltage, SVCC1, can be varied with the addition of an external resistors R1 and R2 as shown Figure.2 and the voltage is defined as follows.

$$SVCC1 = \left(\frac{\dfrac{R1 \cdot R3}{R1 + R3} + \dfrac{R2 \cdot R4}{R2 + R4}}{\dfrac{R2 \cdot R4}{R2 + R4}} \right) \times 1.267[V]$$

• Where, R1 and R2 are exteranl resistors, and R3 and R4 are internal resistors.

Figure 2. Schematic of DC-DC Converter

6-2. Power-on Reset function

• If the output voltage of DC-DC conver, SVCC1,is over than 90%, the RSTOUT(pin3) goes from low level to high level, and RST (pin34) goes to high level to low level. The reset voltage has 50mV of hysteresis to prevent output chattering.

6-3. Delayed Short Circuit Protection

• When the error amplifier output (pin6) become high level state during the abnormal conditions such as over load or short ciruit, the exteral capacitor, C_{SCP}, is charged, and when the SCP (pin8) voltage reaches 1.25V(typ.), the PWM comparator output, BDSW(pin5), is shwitch-off.

- The time until switching-off is set by the capacitor, C$_{SCP}$, and the equation is as follows:

$$t_{SCP} = \frac{C_{SCP} \times V_{SCP}}{i_{SCP}} [sec]$$

$$where, V_{SCP} = 1.25[V], i_{SCP} = 10[uA]$$

6-4. Soft Start Function

- The soft start function operates when a capacitor is connected between DEDSET(pin4) and GND. Also, the maximum duty cab be varied by connecting a resistor to pin4.

$$t_{SOFT} = C_{DEDSET} \times R$$

$$Where, R = 65[K\Omega]$$

7. POWER OFF FUNCTION

- When low level is applied to STOP (pin40), SCP (pin8) is charged, and when the voltage reaches 1.25V (typical), the PWM comparator output, BDSW(pin5), is shwitch-off.
- The time until switching-off is set by the capacitor, C$_{SCP}$, and the equation is as follows:

$$t_{OFF} = \frac{C_{SCP} \times V_{TH}}{i_{OFF}} [sec]$$

$$Where, V_{TH} = 1.25[V], i_{OFF} = 20[uA]$$

-

8. BATTERY CHARGER AND MONITORING FUNCTION

8-1. Set to Battey Charging Current

- The power supply for the charging circuit is ADPVCC (pin41), and battery charger circuit is separated from any other block. The resistance between CHGSET (pin33) and GND sets the charging current, i$_{CHG}$.
- This current, i$_{CHG}$, is drawn from EMPSET (pin42).
- The thermal shutdown circuit is provided, and when the chip temperature rise up to about 150°C the charging current, i$_{CHG}$, is cut-off and it has the temperature hysteresis of about 30°C.

8-2. Over Voltage Protection

- When the voltage applied to the OVP (pin1) reaches 9.7V, SCP (pin8) is charged, and when the voltage reaches 1.25V (typical), the PWM comparator output, BDSW(pin5), is shwitch-off.
- The time until switching-off is set by the capacitor, C$_{SCP}$, and the equation is as follows:
-

$$t_{OVP} = \frac{C_{SCP} \times V_{TH}}{i_{OVP}} [sec]$$
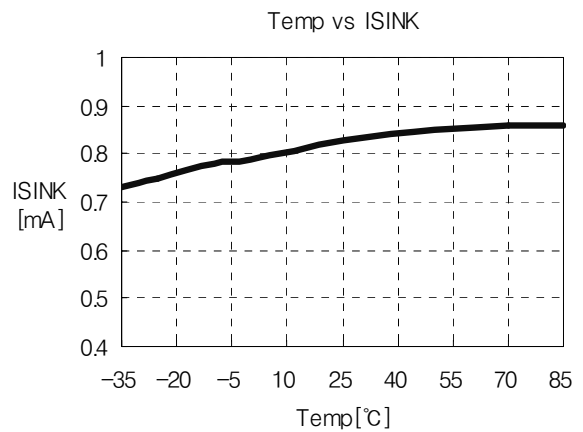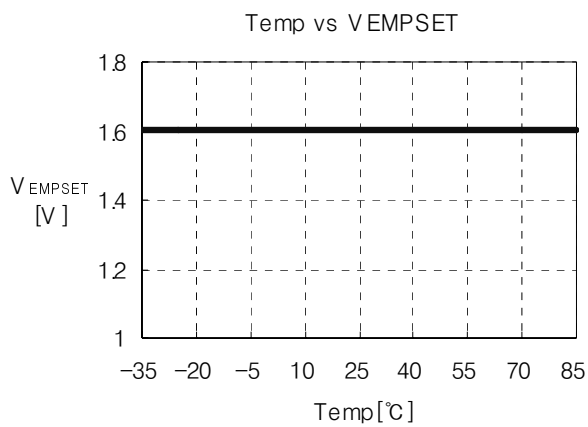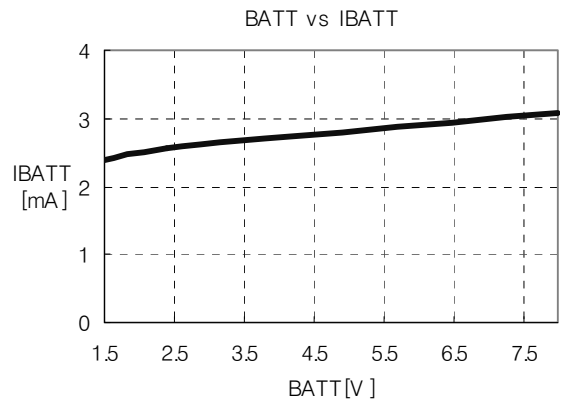
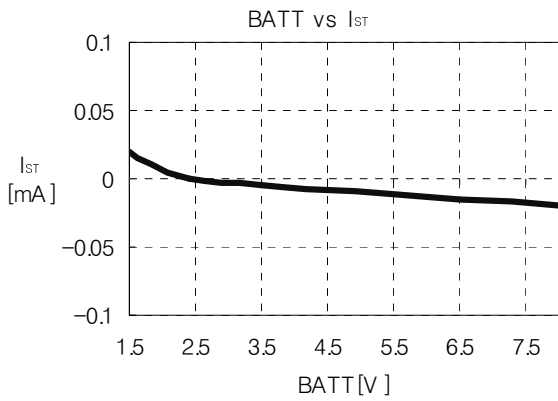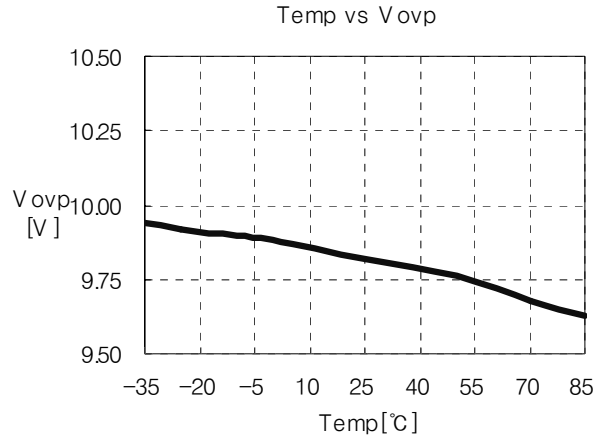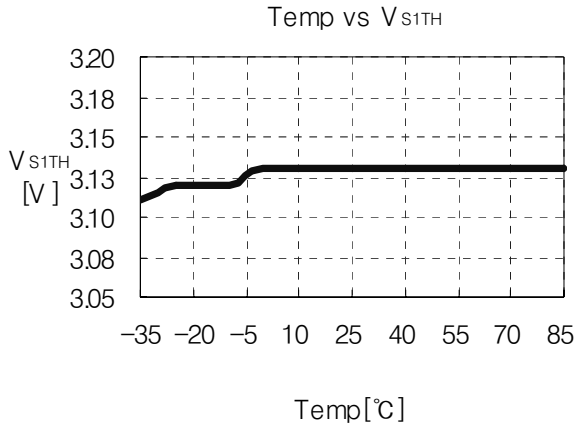$$Where, V_{TH} = 1.25[V], i_{OVP} = 20[uA]$$

-

8-3. Empty Detecting Circuit

- when the voltage applied to the OVP (pin1) falls below the detector voltage, EMP (pin35) goes from high level to low level (open collector output). The detector voltage has 50mV of hysteresis to prevent output chattering.
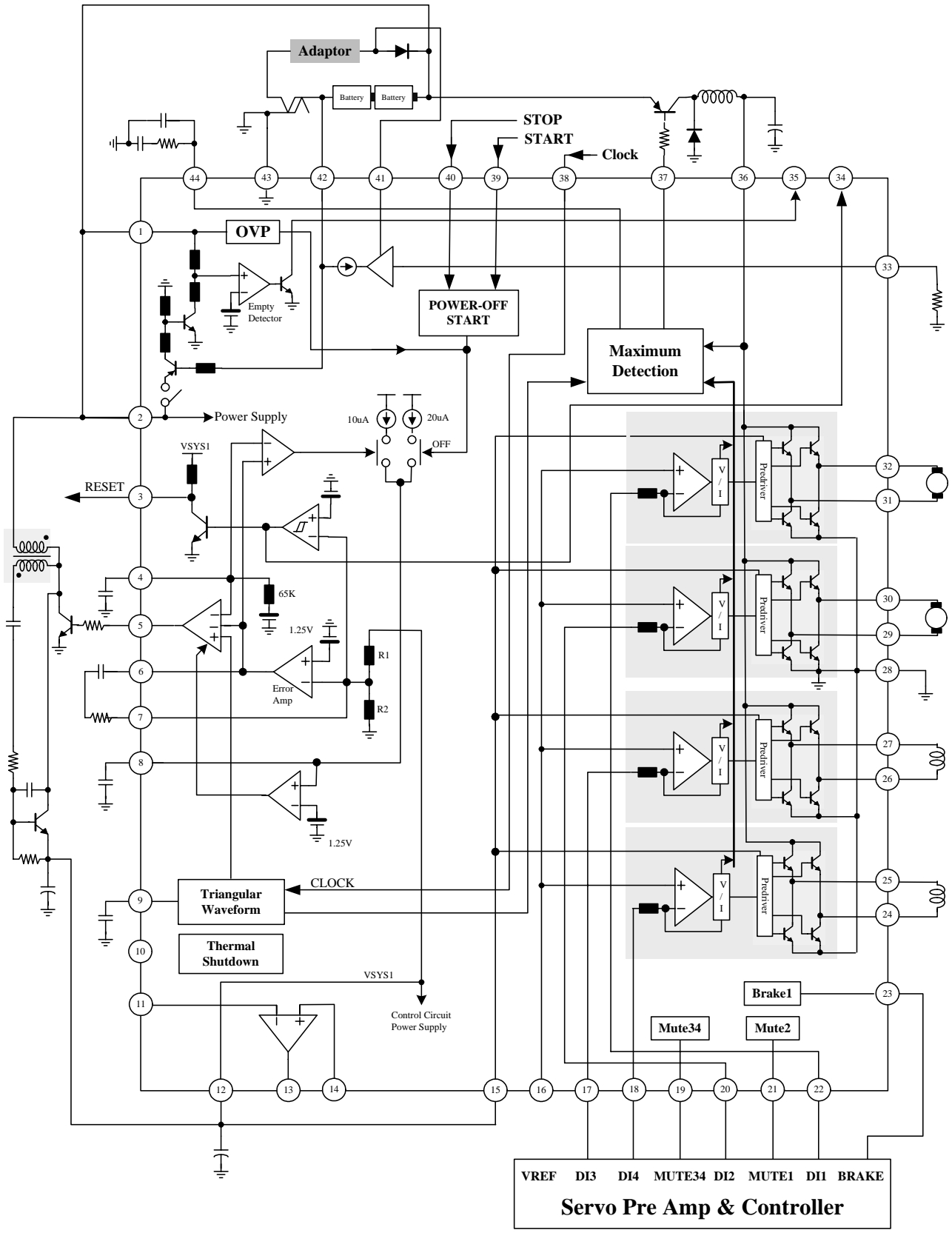- EMPSEL (pin42) to switch the detection voltage as shown below.
-

EMPSET	Detect Voltage	Hysteresis	Mode
LOW	2.2V	50mV	Battery Mode
HIGH-Z	1.8V	50mV	Adapter Mode

Typical Performance Characteristics

Temp vs V_{S1TH}

Temp vs V_{ovp}

BATT vs I_{ST}

BATT vs IBATT

Temp vs V_{EMPSET}

Temp vs ISINK

Application Circuits

Adaptor

STOP
START
Clock

OVP

Empty Detector

POWER-OFF START

Maximum Detection

Power Supply

VSYS1

RESET

65K

1.25V

Error Amp

R1
R2

1.25V

Triangular Waveform

CLOCK

Thermal Shutdown

VSYS1

Control Circuit Power Supply

10uA   20uA   OFF

Brake1

Mute34   Mute2

VREF   DI3   DI4   MUTE34   DI2   MUTE1   DI1   BRAKE

Servo Pre Amp & Controller

Package Dimension

44-QFP-1010B

Dimension : Millimeters

DISCLAIMER

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.