

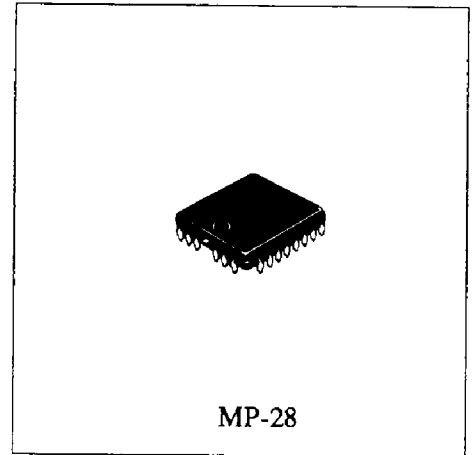
# HD61945MP

## PLL Synthesizer IC

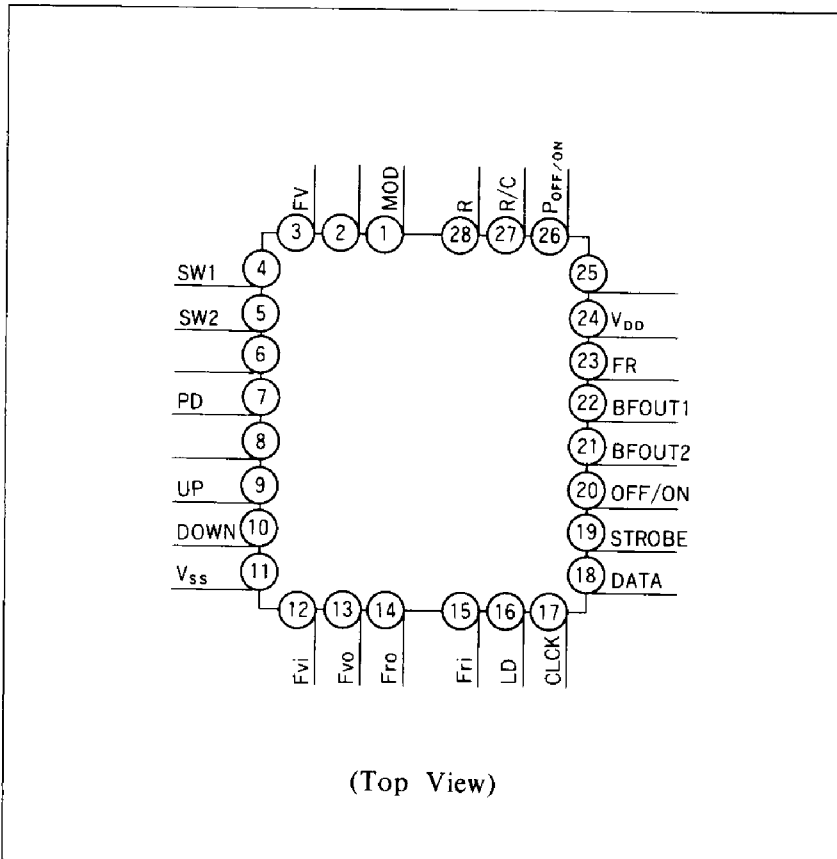
The HD61945MP for PLL synthesizer IC has been developed for cellular radio applications.

### Features

- Incorporates an 11-bit counter for standard frequency, a 10-bit main counter for the comparative frequency and a 7-bit swallow counter.
- Low power dissipation in intermittent operation mode.



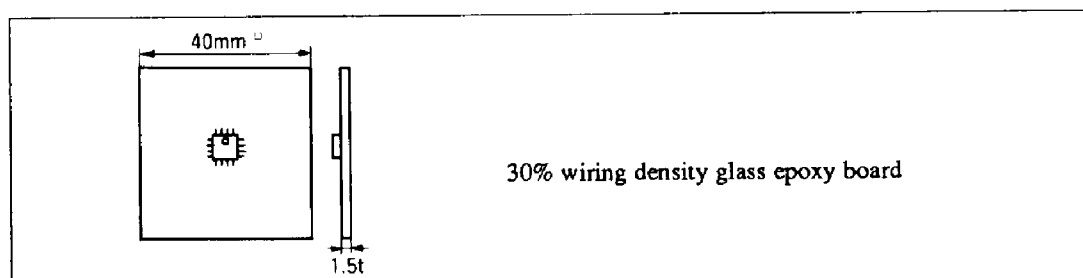
### Pin Arrangement



**Absolute Maximum Ratings (Published specifications) ( $T_a = 25^\circ\text{C}$ ,  $V_{ss} = 0\text{ V}$ )**

Item	Symbols	HD61945MP	Unit	Notes
Supply voltage	$V_{DD\text{ max}}$	7.0	V	*2
Input terminal voltage range	$V_{IN}$	-0.3 to $V_{DD} + 0.3$	V	
Power dissipation	$P_d$	500	mW	*1
Operating ambient temperature range	$T_{opr}$	-30 to +75	$^\circ\text{C}$	
Storage temperature range	$T_{stg}$	-55 to +125	$^\circ\text{C}$	

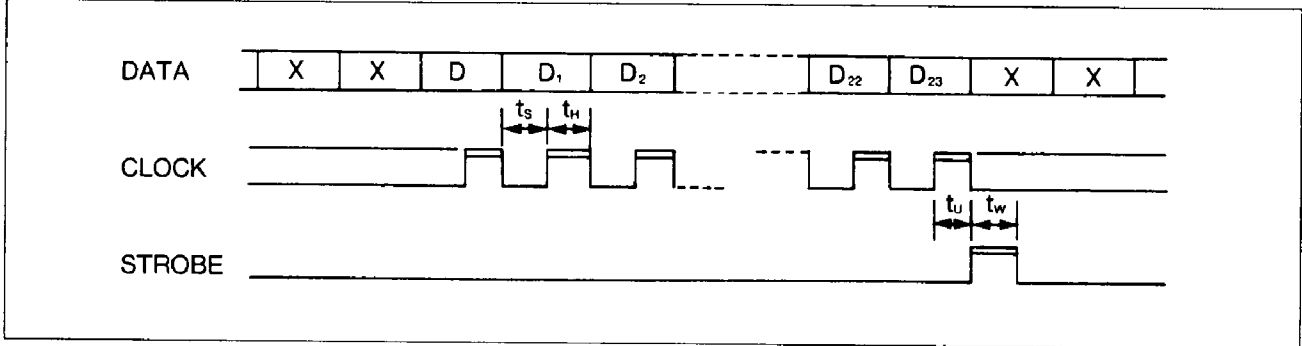
Notes: \*1. For  $T_a = 75^\circ\text{C}$  when mounted on a glass epoxy board.



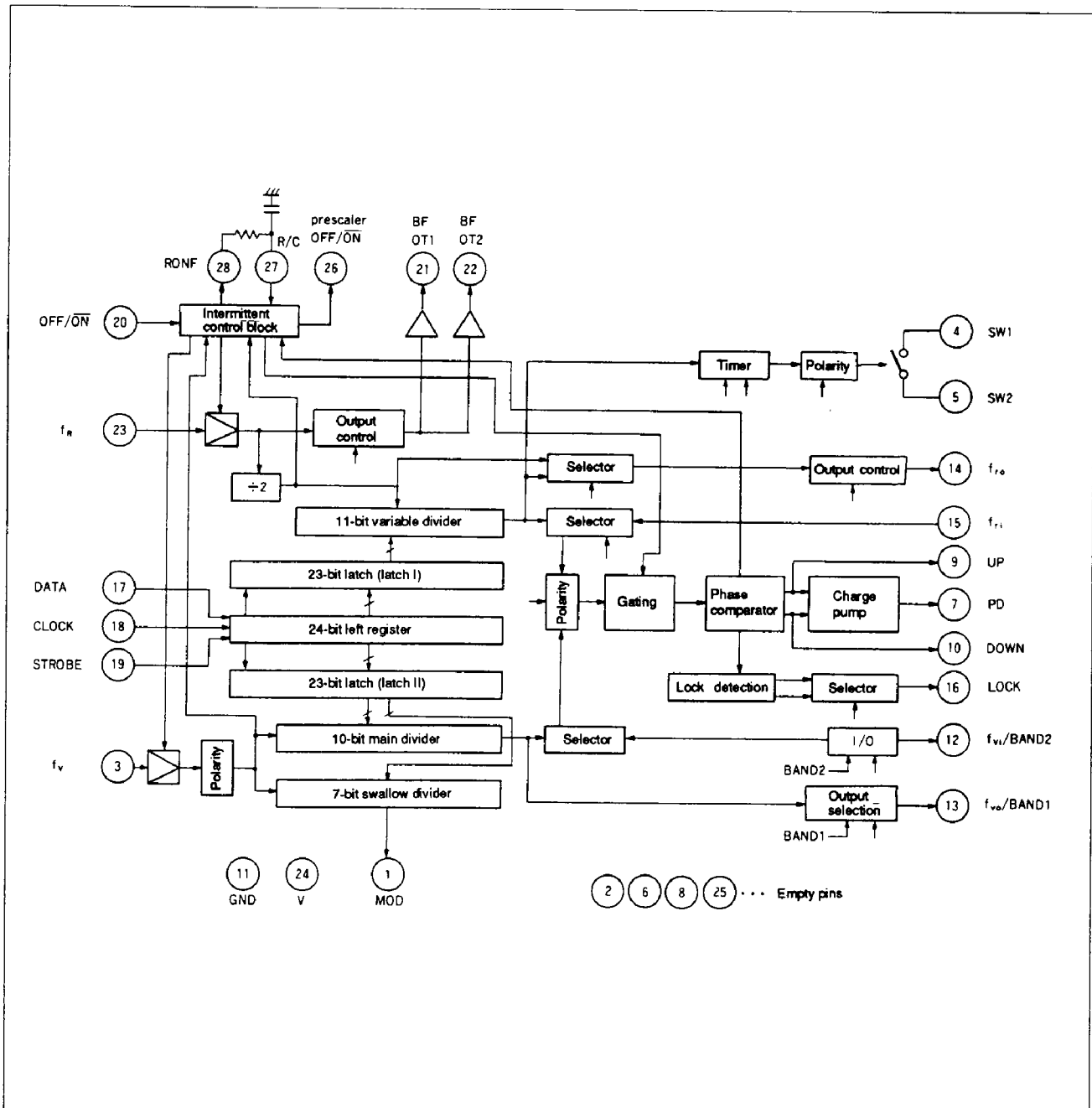
\*2. Standard operating voltage should be  $5.0 \pm 0.25\text{ V}$ .

### Data, Clock, Strobe Timing Chart

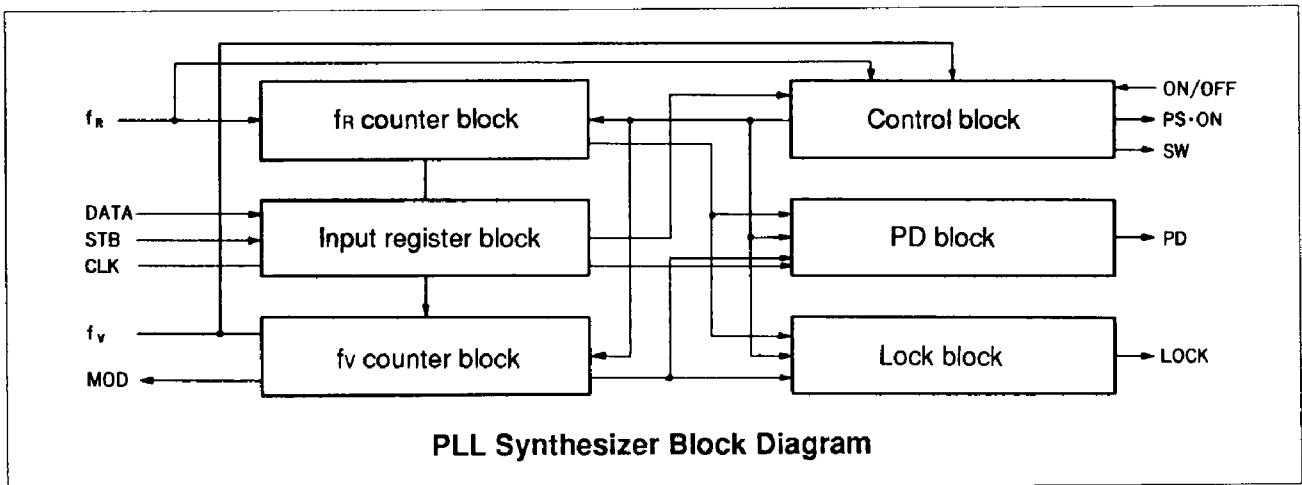
( $t_s, t_H \cong 500 \text{ ns}$  or  $> 400 \text{ ns}$ ,  $t_w \cong 500 \text{ ns}$  or  $> 400 \text{ ns}$ ,  $t_v \cong 500 \text{ ns}$  or  $> 0 \text{ ns}$ )



### Block Diagram



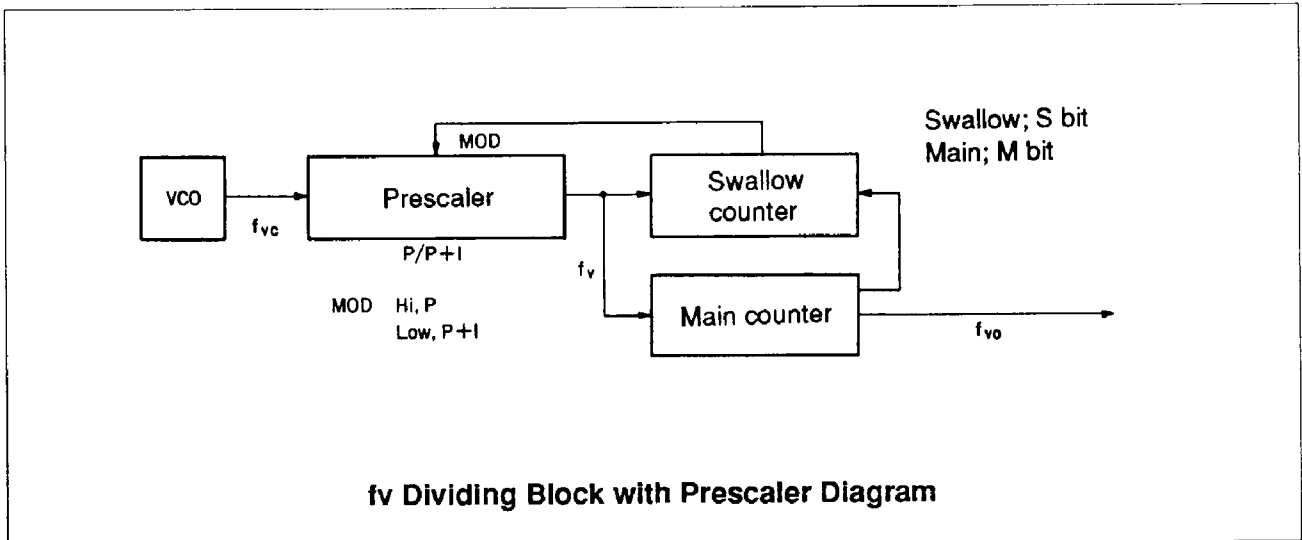
**Block Functions**



**PLL Synthesizer Block Diagram**

**f<sub>R</sub> counter block:** The  $f_R$  consists of an 11-bit counter and a half divider. Reference frequency  $f_R$  is divided by the dividend at the input register pins.

**f<sub>V</sub> counter block:** The  $f_V$  counter block consists of a 10-bit main counter 7-bit swallow counter. It determines the dividend with an external prescaler.



**f<sub>V</sub> Dividing Block with Prescaler Diagram**

**Input register block:** The input register block has two 24-bit registers and determines block setting values. It converts serial input signals to parallel format for input register.

**PD block:** The PD block sends acceleration or deceleration signals to VCO with a phase detector. It can reverse external inputs and signals, depending on values set at the input register.

**Lock block:** The lock block detects PLL lock status.

**Control block:** The control block controls block timing operations.

## Pin Functions

Pin No.	Pin Name	I/O	Description	Remarks																							
1	MOD	O	Control signal output pin for the dual-modulus prescaler connected externally.	Set to "L" when pin 20 is "H."																							
2	NC	—																									
3	FV	I	Input pin for the comparison divider. To connect to the prescaler, ac connection should be used because the amplifier incorporates a bias circuit.																								
4	SW1	—	An analog switch is incorporated between pins 4 and 5. It switches on or off according to the strobe signals (pin 19) for the serial-data latch or the synchronous signals from the intermittent control block. Polarity is determined by D20 of the control register II. Switching time can be set to four modes by D21 and D22. Therefore, the switches can be used to change the VCOLPF characteristic.	Refer to Control register I and II.																							
5	SW2	—																									
6	NC	—																									
7	PD	O	Built-in charge pump output pin. Output polarity is set by D21 of control register I. PD output determined by the relation between reference divider output phase $\phi_r$ and comparison divider output phase $\phi$ is shown in the chart below.	Refer to Control register I.																							
<table border="1"> <thead> <tr> <th>D21 set value</th> <th><math>\phi_r &gt; \phi_v</math></th> <th><math>\phi_r = \phi_v</math></th> <th><math>\phi_r &lt; \phi_v</math></th> </tr> </thead> <tbody> <tr> <td>"0"</td> <td>"H"</td> <td>HiZ</td> <td>"L"</td> </tr> <tr> <td>"1"</td> <td>"L"</td> <td>HiZ</td> <td>"H"</td> </tr> </tbody> </table>					D21 set value	$\phi_r > \phi_v$	$\phi_r = \phi_v$	$\phi_r < \phi_v$	"0"	"H"	HiZ	"L"	"1"	"L"	HiZ	"H"											
D21 set value	$\phi_r > \phi_v$	$\phi_r = \phi_v$	$\phi_r < \phi_v$																								
"0"	"H"	HiZ	"L"																								
"1"	"L"	HiZ	"H"																								
8	NC	—																									
9	UP	O	External charge pump output pin. Output polarity can be changed by D21 of control register I. Output determined by the relation between reference divider output phase $\phi_r$ and comparison divider output phase $\phi_v$ is shown in the chart below.	Refer to Control register I.																							
10	DOWN	O	<table border="1"> <thead> <tr> <th>Pin Name</th> <th>D21 set value</th> <th><math>\phi_r &gt; \phi_v</math></th> <th><math>\phi_r = \phi_v</math></th> <th><math>\phi_r &lt; \phi_v</math></th> </tr> </thead> <tbody> <tr> <td rowspan="2">UP</td> <td>"0"</td> <td>"L"</td> <td>"H"</td> <td>"H"</td> </tr> <tr> <td>"1"</td> <td>"H"</td> <td>"H"</td> <td>"L"</td> </tr> <tr> <td rowspan="2">DOWN</td> <td>"0"</td> <td>"H"</td> <td>"H"</td> <td>"L"</td> </tr> <tr> <td>"1"</td> <td>"H"</td> <td>"H"</td> <td>"H"</td> </tr> </tbody> </table>	Pin Name	D21 set value	$\phi_r > \phi_v$	$\phi_r = \phi_v$	$\phi_r < \phi_v$	UP	"0"	"L"	"H"	"H"	"1"	"H"	"H"	"L"	DOWN	"0"	"H"	"H"	"L"	"1"	"H"	"H"	"H"	
Pin Name	D21 set value	$\phi_r > \phi_v$	$\phi_r = \phi_v$	$\phi_r < \phi_v$																							
UP	"0"	"L"	"H"	"H"																							
	"1"	"H"	"H"	"L"																							
DOWN	"0"	"H"	"H"	"L"																							
	"1"	"H"	"H"	"H"																							
11	Vss	—																									
12	Fvi/BAND2	I/O	When D18 of control register I is "0," pin 12 is in output mode and outputs the state of D19 of control register II to switch VCO band over. When D18 is "1," pin 12 is in input mode and external fv can be input to the phase comparator instead of the internal fv from the comparison divider.	Refer to Control register I and II.																							
13	Fvo/BAND1	O	When D19 of the control register is "0," pin 13 outputs the state of the control register II to switch VCO band over. When D19 is "1," the output from the comparison divider can be output from this pin.	Refer to Control register I and II.																							
14	FR0	O	When D0 of the control register is "0," fr from the reference divider is output from pin 14. When D0 is "1," the reference frequency input from pin 23 is reduced by half and is output from pin 14.	Refer to Control register I.																							

## Pin Functions (continued)

Pin No.	Pin Name	I/O	Description	Remarks
15	FR1	I	External fr input pin. When D20 of control register I is "1," input signals from this pin are input to the phase comparator instead of the fr output signals from the reference divider.	Refer to Control register I.
16	LOCK	O	phase comparator lock detection pin. Outputs "H" when synchronizing. For output mode, either level output or pulse output can be chosen by D22 of control register I.	Refer to Control register I.
17	CLOCK	I	Reference clock input pin for serial data input to control registers I and II.	Pull down
18	DATA	I	Input pin for serial data to be input to control registers I and II. The last data D23 determines whether the data is latched into control register I or II.	Refer to Control register I and II. Pull down
19	STROB	I	Strobe signal input pin to latch the data into the control register. (Data is fetched when "H" signal is input.)	Pull down
20	OFF/ON	I	Phase synchronous dividing control signal input pin. When "L" is input, phase synchronous dividing is started and the state becomes operation mode. When "H" is input, the state becomes receive waiting mode.	Pull down
21	BFOUT2	O	Pin 23 fR inputs are output through the buffer. When D12 = "1," output is prohibited ("L" is fixed). When D12 = "0," signals are output through the buffer.	Refer to Control register I and II.
22	BFOUT1	O		
23	FR	I	Reference signal(12 MHz) input pin. AC connection should be done with TCXO because the amplifier incorporates a bias circuit.	
24	V <sub>DD</sub>	—		
25	NC	—		
26	D OFF/ON	O	Prescaler power on/off signal input pin. Input P off/on = "L" signal	
27	R/C	I	to turn on the prescaler power.	
28	RONF	O	Connect a resistor between pins 27 and 28 and ground a capacitor at pin 27. Then, set operation timing between the prescaler and this IC with a constant.	

HD61945 How to Use Latch

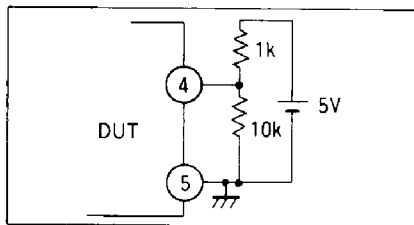
Bit	Latch I (Standard divider: fr → fr0)		Latch I (Variable divider: fv → fv0)		Remarks
	Name	Latch input data	Name	Latch input data	
D1	2N/+2	Output fr = fr + 2N	Output fr = fr + 2	"0"	
D2	LSB	Ntr = 2 × N	When 2N/+2 = "1" and frEXT = "1," D1 to D11 are disregarded.	"0"	Total dividing frequency Ntr is specified as a binary number when the latch is combined with the prescaler 128/129.
D3		N is specified as a binary number.			(Ntr max = 2 <sup>17</sup> - 1)
D4		When 2N/+2 = "0," Ntr can be specified as binary number.			
D5					
D6					
D7					
D8					
D9					
D10					
D11	MSB				
D12	fr Buffer OUT	Output fr to outside	Not output fr to outside		fr: Output buffer
D13	for				
D14	testing	○	Prohibited		
D15					
D16	for	Falling clock	Rising clock		
	POLARITY				In combination with prescaler
D17	fv	Not output fv to outside	Output fv to outside		fv0 outputting (Reserve)
D18	fv	Internal fv	External fv		
	EXTERNAL				fv PD input selection BAND1
D19	fr	Not output fr to outside	Output fr to outside		
	EXTERNAL				fr 0 outputting BAND 2
D20	fr	Internal fr	External fr		
	EXTERNAL				fr PD input selection SWITCH
D21	PD	φr ≥ φv: "H"	φr > φv: "L"		POLA Switch is "ON" when timer is on. Switch is "OFF" when timer is on. Analog switch
	POLARITY				LSB
D22	LOCK	Level output	Pulse output		
	DETECT				Timer "0": T = 16 τ "1": T = 32 τ "2": T = 64 τ "3": T = 128 τ τ = 1/fr
D23	LATCH SELECT	○	○		LATCH SELECT Latch I selection Latch II selection

**Electrical Characteristics** (Ta = 25°C, VDD = 5.0 V, VSS = 0 V)

Item	Symbol	Test Conditions	Min	Typ	Max	Unit	Applicable pins	Notes
Supply voltage	V <sub>DD</sub>		4.75	5.00	5.25	V	24	
Input voltage (1)	V <sub>IH1</sub>		0.7 × V <sub>DD</sub>	—	—	V	3, 15, 17, 18,	
Input voltage (2)	V <sub>IL1</sub>		—	—	0.3 × V <sub>DD</sub>	V	19, 20, 23	
Output voltage (1)	V <sub>OH</sub>	-I <sub>OH</sub> = 0.4 mA	V <sub>DD</sub> - 0.4	—	—	V	1, 7, 9, 10, 12,	
Output voltage (2)	V <sub>OL</sub>	I <sub>OL</sub> = 0.4 mA	—	—	0.4	V	13, 14, 16, 21, 22, 26, 28	
Input leakage current (1)	I <sub>IH(1)</sub>	V <sub>IN</sub> = 5.0 V	—	—	1	μA	4, 5, 12	
Input leakage current (2)	I <sub>IL(2)</sub>	V <sub>IN</sub> = 0 V	-1	—	—	μA	4, 5, 12, 15, 17, 18, 19, 20, 27	
Operating current	I <sub>CC</sub>	V <sub>DD</sub> = 5.0 V	—	7.5	12.0	μA	30	*1
Three-state leakage current (1)	I <sub>ZH</sub>	V <sub>7</sub> = 5.0 V	—	—	1	μA	7	
Three-state leakage current (2)	I <sub>ZL</sub>	V <sub>7</sub> = 0 V	-1	—	—	μA	7	
Switch-on voltage	I <sub>4ON</sub>		—	—	1	V	4	*2
Switch-off voltage	I <sub>4OFF</sub>		4.2	4.5	—	V	4	*2
Input voltage (3)	V <sub>IH2</sub>		4.1	—	—	V	12	
Input voltage (4)	V <sub>IL2</sub>		—	—	0.8	V	12	

Notes: \*1. Value when CH1 is locked (Rx = 915.03 MHz)

\*2. Test with the measurement circuit in figure 1.



**Figure 1**



Pin No.	Signal Names		
	Clock Power Source	Input	Output
1			MOD
2		(N.C)	
3		FV	
4			SW1
5			SW2
6		(N.C)	
7			PD
8		(N.C)	
9			UP
10			DOWN
11	V <sub>SS</sub>		
12		F <sub>vi</sub>	BAND2
13			F <sub>vo</sub>
14			F <sub>ro</sub>
15		F <sub>ri</sub>	
16			LD
17	Clock	CLOCK	
18		DATA	
19		STROBE	
20		OFF/ON	
21			BF OUT2
22			BF OUT1
23		FR	
24	V <sub>DD</sub>		
25		(N.C)	
26			P OFF/ON
27		R/C	
28			R

Notes on denotation: Terminals are denoted by tij, and non-used terminals are denoted by NC.

### System Block Diagram

