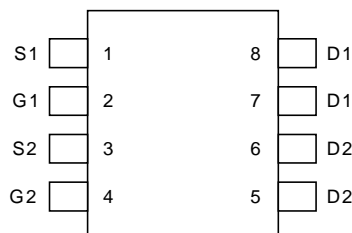


P-Channel Enhancement Mode MOSFET

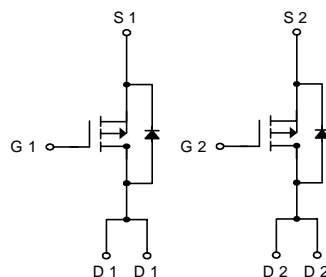
Features

- -30V/-6.1A, $R_{DS(ON)} = 24m\Omega(\text{typ.}) @ V_{GS} = -10V$
 $R_{DS(ON)} = 30m\Omega(\text{typ.}) @ V_{GS} = -4.5V$
- Super High Density Cell Design
- Reliable and Rugged
- SO-8 Package

Pin Description



SO - 8



P-Channel MOSFET

Applications

- Power Management in Notebook Computer, Portable Equipment and Battery Powered Systems

Ordering and Marking Information

<p>APM4925 □□-□□</p> <p style="margin-left: 20px;"> □□ Handling Code □□ Temp. Range □□ Package Code </p>	<p>Package Code K : SO-8</p> <p>Operation Junction Temp. Range C : -55 to 150°C</p> <p>Handling Code TU : Tube TR : Tape & Reel</p>
<p>APM4925 APM4925 XXXXXX</p>	<p style="text-align: center;">XXXXXX - Date Code</p>

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Unit
V_{DSS}	Drain-Source Voltage	-30	V
V_{GSS}	Gate-Source Voltage	± 25	
I_D^*	Maximum Drain Current – Continuous	$T_A = 25^\circ\text{C}$ -6.1	A
I_{DM}	Maximum Drain Current – Pulsed	-40	

*Surface Mounted on FR4 Board, $t \leq 10$ sec.

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Unit
P_D	Maximum Power Dissipation	$T_A = 25^\circ\text{C}$	2.5
		$T_A = 100^\circ\text{C}$	1
T_J	Maximum Junction Temperature	150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	
$R_{\theta\text{JA}}$	Thermal Resistance - Junction to Ambient	50	$^\circ\text{C/W}$

Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	APM4925			Unit
			Min.	Typ ^a	Max.	
Static						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_D = -250\mu\text{A}$	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{DS}} = -24\text{V}, V_{\text{GS}}=0\text{V}$			-1	μA
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}, I_D = -250\mu\text{A}$	-1	-1.5	-2	V
I_{GSS}	Gate Leakage Current	$V_{\text{GS}} = \pm 25\text{V}, V_{\text{DS}}=0\text{V}$			± 100	nA
$R_{\text{DS(ON)}}^b$	Drain-Source On-state Resistance	$V_{\text{GS}} = -10\text{V}, I_D = -6.1\text{A}$		24	27	m Ω
		$V_{\text{GS}} = -4.5\text{V}, I_D = -5.1\text{A}$		30	35	
V_{SD}^b	Diode Forward Voltage	$I_{\text{SD}} = -1.7\text{A}, V_{\text{GS}}=0\text{V}$		-0.7	-1.3	V
Dynamic^a						
Q_g	Total Gate Charge	$V_{\text{DS}} = -15\text{V}, V_{\text{GS}} = -10\text{V}, I_D = -4.6\text{A}$		48	58	nC
Q_{gs}	Gate-Source Charge			10		
Q_{gd}	Gate-Drain Charge			9		
$t_{\text{d(ON)}}$	Turn-on Delay Time	$V_{\text{DD}} = -25\text{V}, R_L = 12.5\Omega, I_D = -2\text{A}, V_{\text{GEN}} = -10\text{V}, R_G = 6\Omega,$		17	33	ns
t_r	Turn-on Rise Time			18	35	
$t_{\text{d(OFF)}}$	Turn-off Delay Time			70	128	
t_f	Turn-off Fall Time			30	56	
C_{iss}	Input Capacitance	$V_{\text{GS}}=0\text{V}, V_{\text{DS}} = -25\text{V}$ Frequency = 1.0MHZ		3200		pF
C_{oss}	Output Capacitance			560		
C_{rss}	Reverse Capacitance			250		

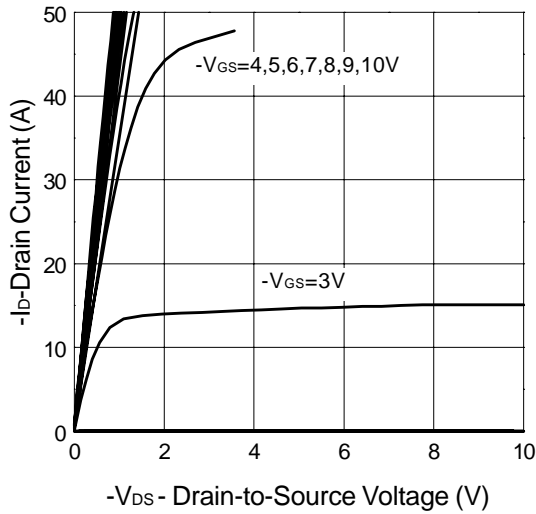
Notes

^a : Guaranteed by design, not subject to production testing

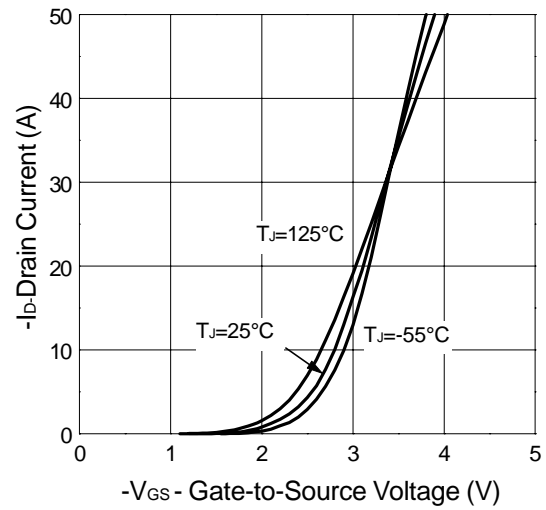
^b : Pulse test ; pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$

Typical Characteristics

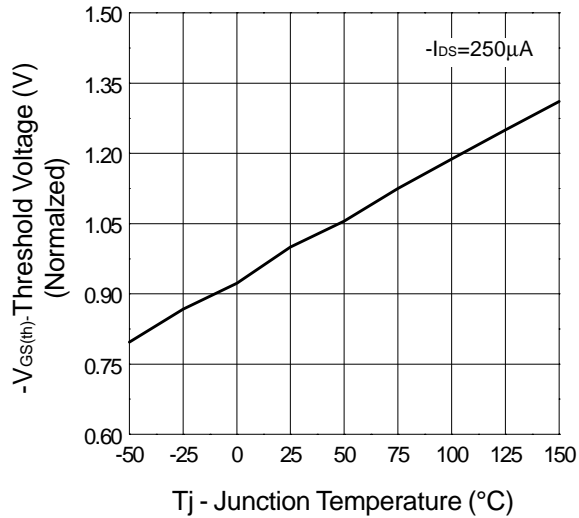
Output Characteristics



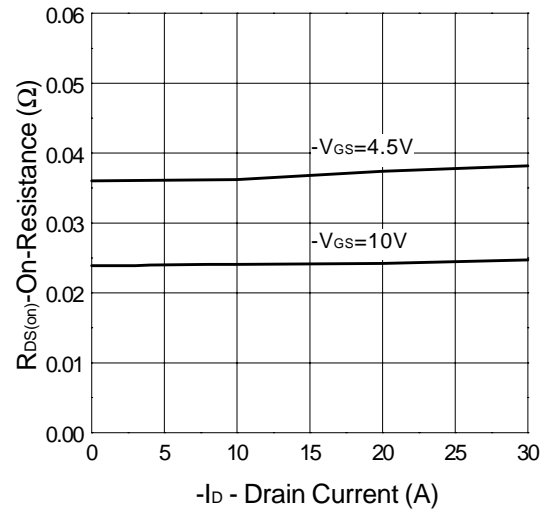
Transfer Characteristics



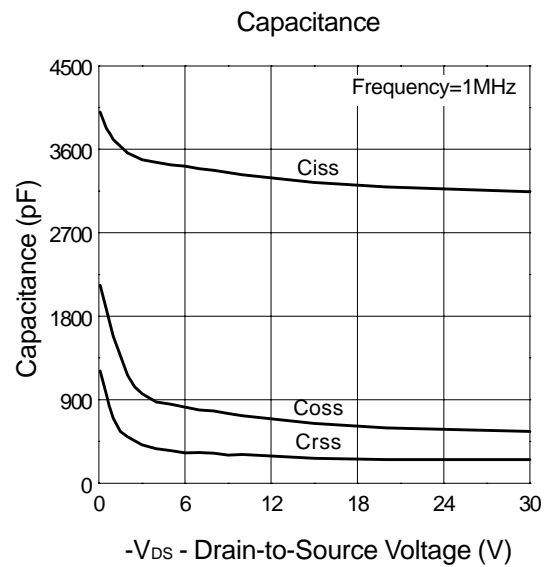
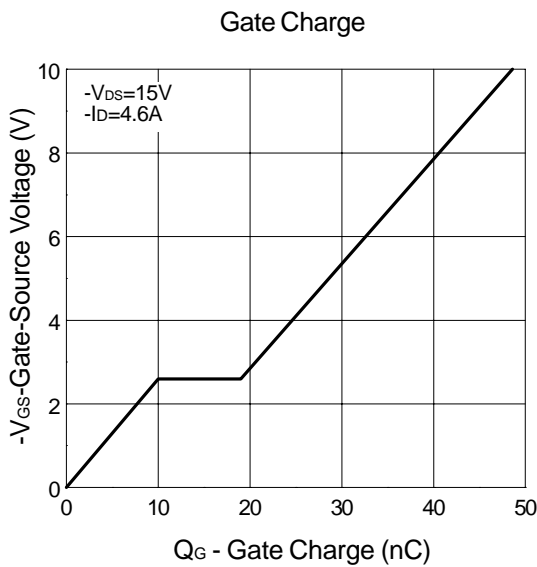
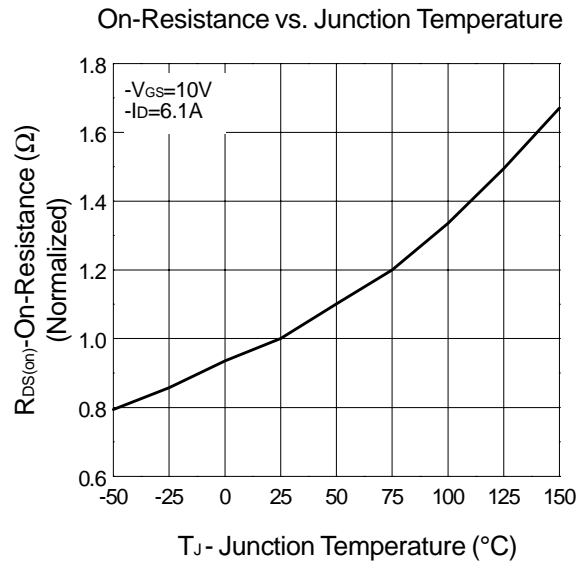
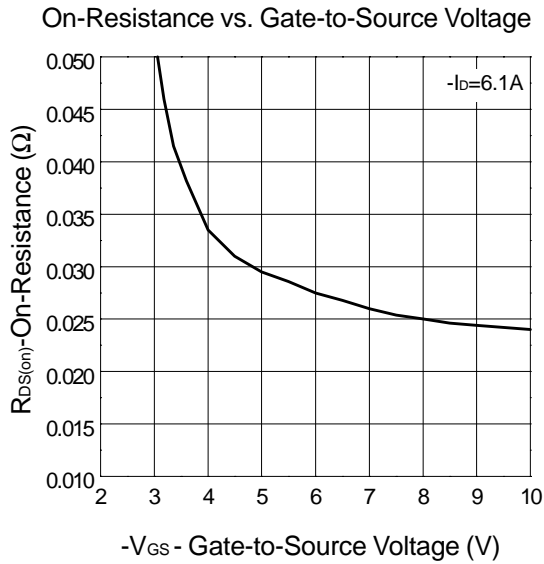
Threshold Voltage vs. Junction Temperature



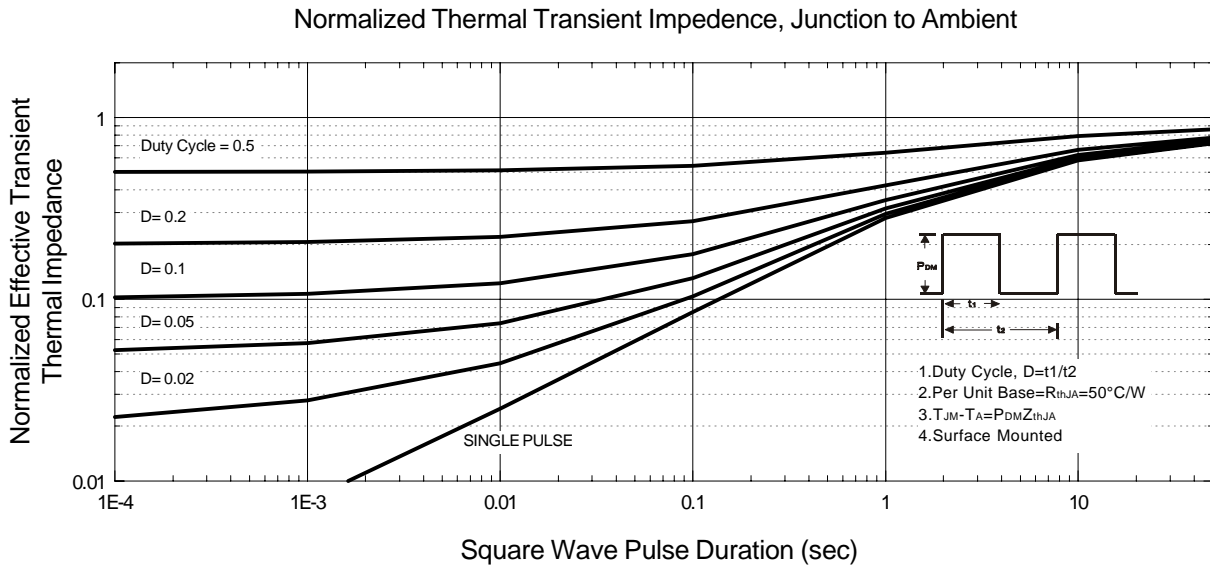
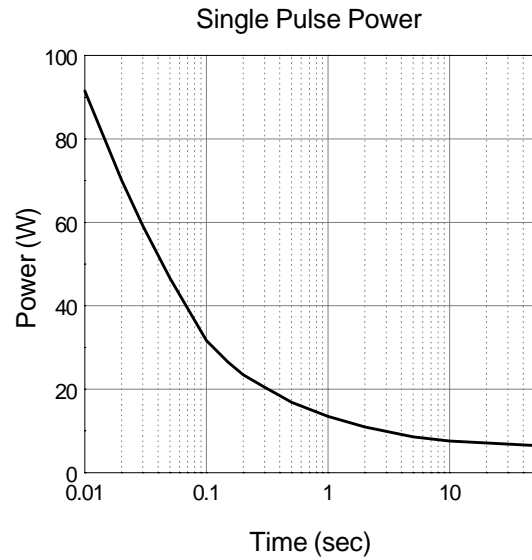
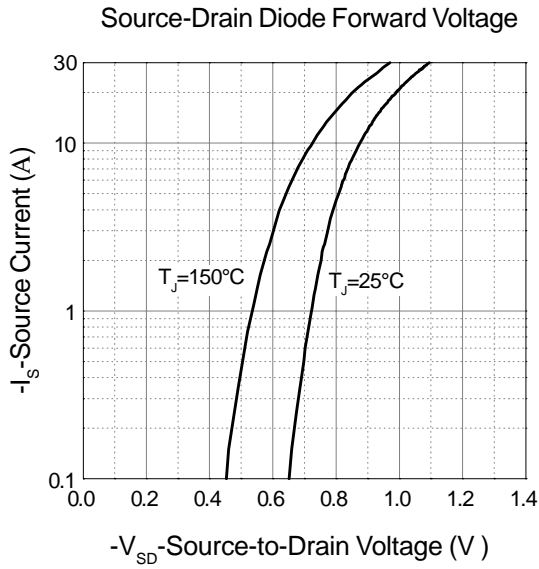
On-Resistance vs. Drain Current



Typical Characteristics

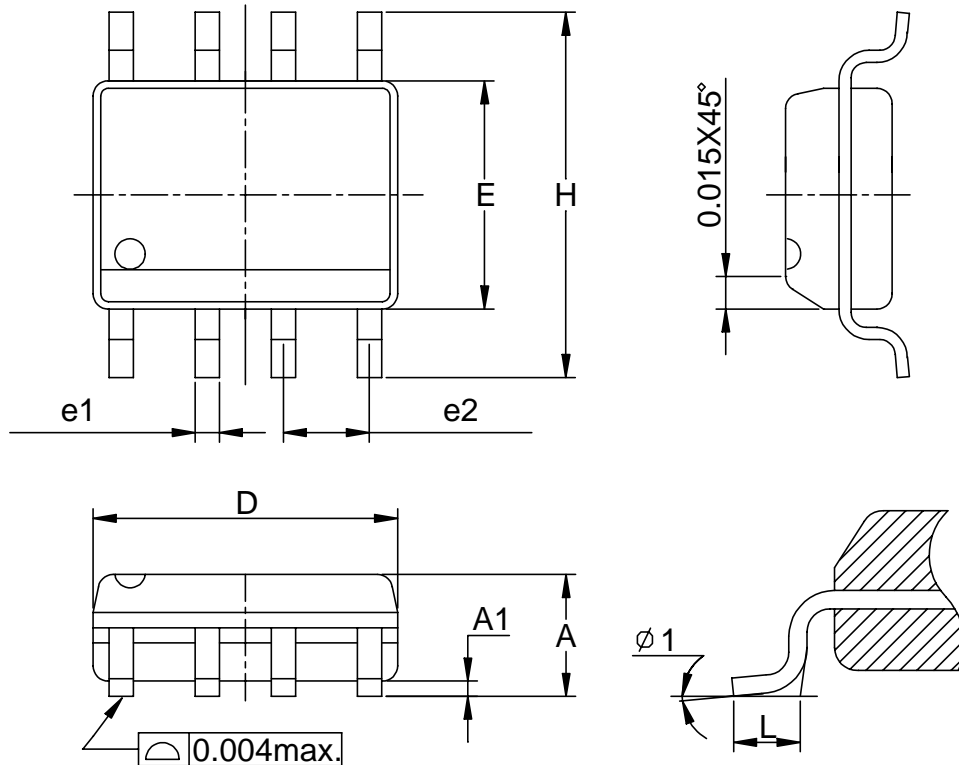


Typical Characteristics



Package Information

SOP-8 pin (Reference JEDEC Registration MS-012)



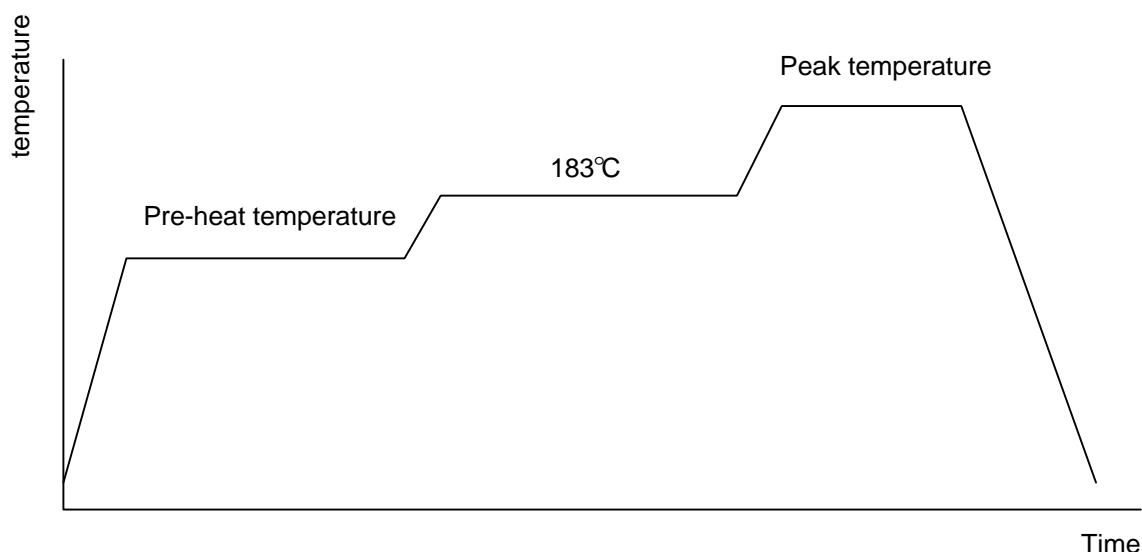
Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.00	0.150	0.157
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
e1	0.33	0.51	0.013	0.020
e2	1.27BSC		0.50BSC	
φ 1	8°		8°	

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb)
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.
Packaging	2500 devices per reel for SOP-8

Reflow Condition (IR/Convection or VPR Reflow)

Reference JEDEC Standard J-STD-020A APRIL 1999



Classification Reflow Profiles

	Convection or IR/ Convection	VPR
Average ramp-up rate(183°C to Peak)	3°C/second max.	10 °C /second max.
Preheat temperature 125 ± 25°C)	120 seconds max.	
Temperature maintained above 183°C	60 ~ 150 seconds	
Time within 5°C of actual peak temperature	10 ~ 20 seconds	60 seconds
Peak temperature range	220 +5/-0°C or 235 +5/-0°C	215~ 219°C or 235 +5/-0°C
Ramp-down rate	6 °C /second max.	10 °C /second max.
Time 25°C to peak temperature	6 minutes max.	

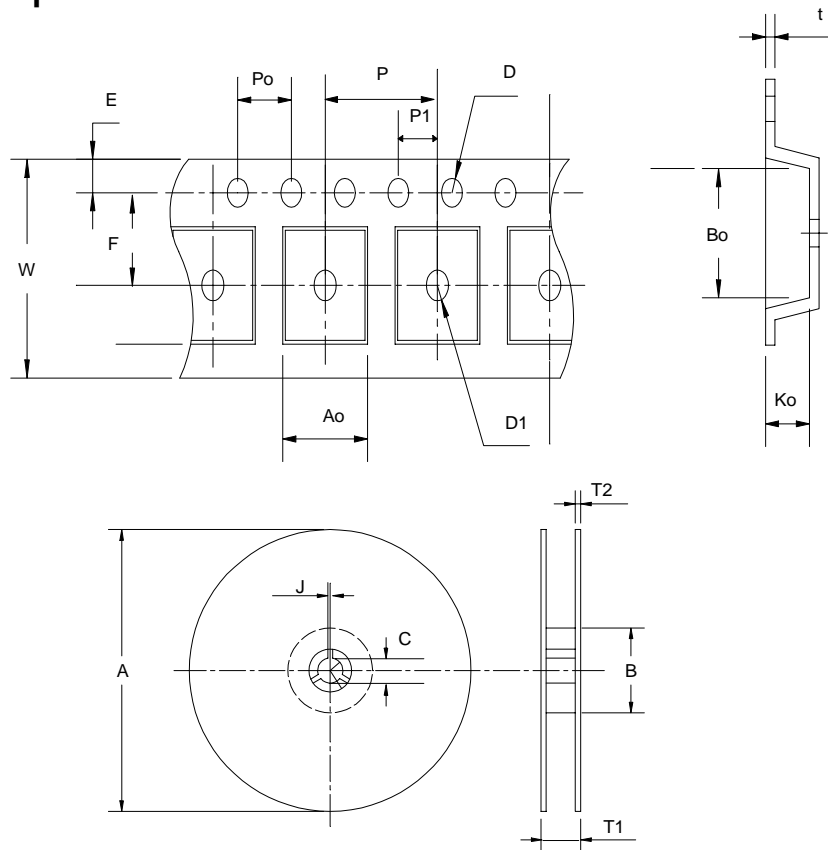
Package Reflow Conditions

pkg. thickness ≥ 2.5mm and all bags	pkg. thickness < 2.5mm and pkg. volume ≥ 350 mm³	pkg. thickness < 2.5mm and pkg. volume < 350mm³
Convection 220 +5/-0 °C		Convection 235 +5/-0 °C
VPR 215-219 °C		VPR 235 +5/-0 °C
IR/Convection 220 +5/-0 °C		IR/Convection 235 +5/-0 °C

Reliability test program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C , 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @ 125 °C
PCT	JESD-22-B, A102	168 Hrs, 100 % RH , 121°C
TST	MIL-STD-883D-1011.9	-65°C ~ 150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms , I _{tr} > 100mA

Carrier Tape



Application	A	B	C	J	T1	T2	W	P	E
SOP- 8	330 ± 1	$62 +1.5$	$12.75+0.15$	2 ± 0.5	12.4 ± 0.2	2 ± 0.2	12 ± 0.3	8 ± 0.1	1.75 ± 0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	5.5 ± 1	$1.55 +0.1$	$1.55+ 0.25$	4.0 ± 0.1	2.0 ± 0.1	6.4 ± 0.1	5.2 ± 0.1	2.1 ± 0.1	0.3 ± 0.013
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	11.5 ± 0.1	$1.5 +0.1$	$1.5+ 0.25$	4.0 ± 0.1	2.0 ± 0.1	8.2 ± 0.1	13 ± 0.1	2.5 ± 0.1	0.35 ± 0.013

Cover Tape Dimensions

Carrier Width	12
Cover Tape Width	9.3

(mm)

Customer Service

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