TDA2590

TV HORIZONTAL OSCILLATOR COMBINATION

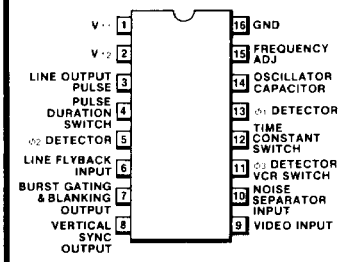
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The TDA2590 is a monolithic integrated circuit designed as a horizontal oscillator combination for TV receivers and monitors. It is constructed using the Fairchild Planar* process.

- **LINE OSCILLATOR USING THE THRESHOLD SWITCHING PRINCIPLE**
- **PHASE COMPARISON BETWEEN SYNC PULSE AND OSCILLATOR VOLTAGE (ϕ_1)**
- **PHASE COMPARISON BETWEEN LINE FLYBACK PULSE AND OSCILLATOR VOLTAGE (ϕ_2)**
- **SWITCH FOR CHANGING THE FILTER CHARACTERISTIC AND THE GATE CIRCUIT (WHEN USED FOR VCR)**
- **COINCIDENCE DETECTOR (ϕ_3)**
- **SYNC SEPARATOR**
- **NOISE SEPARATOR**
- **VERTICAL SYNC SEPARATOR AND OUTPUT STAGE**
- **COLOR BURST KEYING AND LINE FLYBACK BLANKING PULSE GENERATOR**
- **PHASE SHIFTER FOR THE OUTPUT PULSE**
- **OUTPUT PULSE DURATION SWITCHING**
- **OUTPUT STAGE FOR DIRECT DRIVE OF THYRISTOR DEFLECTION CIRCUITS**
- **SYNC GATING PULSE GENERATOR**
- **LOW SUPPLY VOLTAGE PROTECTION**

*Planar is a patented Fairchild process.

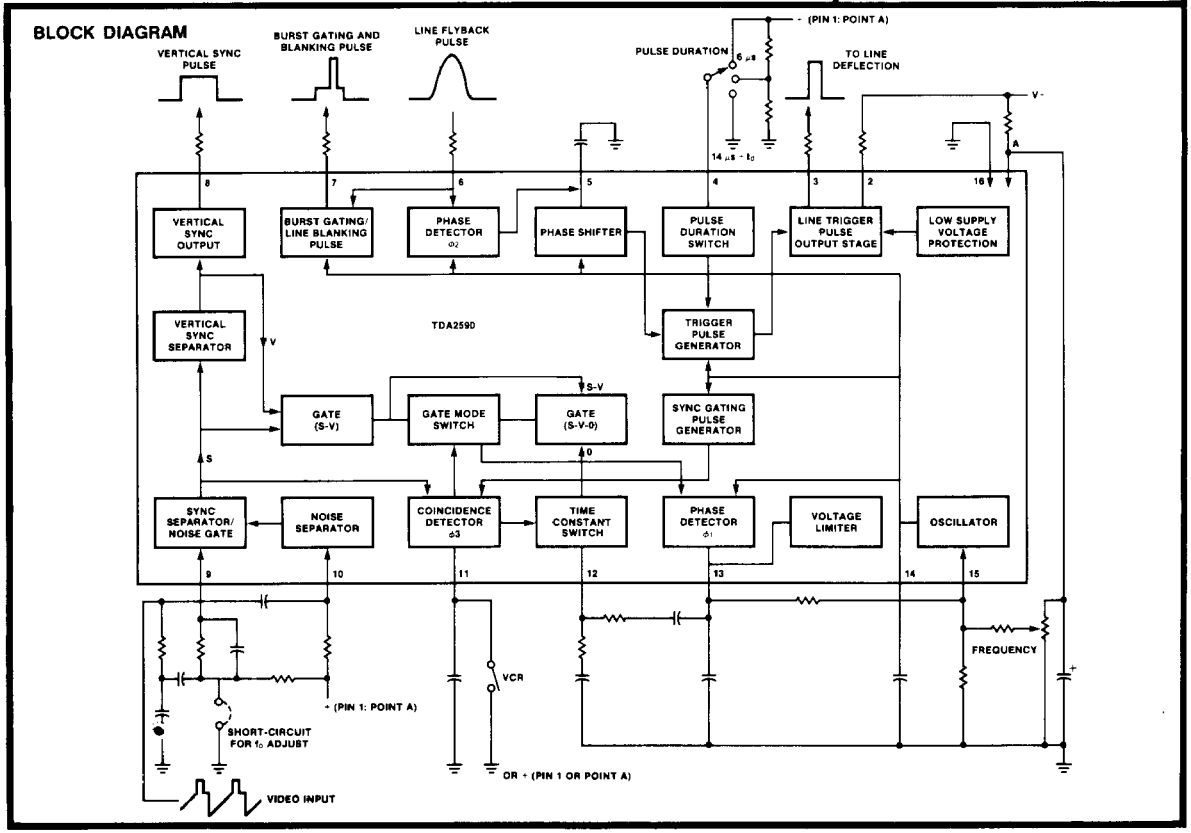
CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9B



ORDER INFORMATION

TYPE	PART NO.
2590	TDA2590

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage at Pin 1 (When Supplied by the IC)	13.2 V
Supply Voltage at Pin 2	18 V
Power Dissipation	800 mW
Storage Temperature	-25°C to +125°C
Operating Temperature	-20°C to +60°C
Pin Temperature (Soldering, 10 s)	260°C

VOLTAGES

V_4, V_{11}	0 to 13.2 V
V_9, V_{10}	-6 to +6 V

CURRENTS

I_2 (peak)	400 mA
I_3 (peak)	-400 mA
I_4	1 mA
I_6	±10 mA
I_7	-10 mA
I_{11}	2 mA

ELECTRICAL CHARACTERISTICS: T_A = 25°C; V_1 = 12 V, See test circuit unless otherwise noted.

CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_1			30		mA
SYNC SEPARATOR (PIN 9)						
Input Switching Voltage	V_9			0.8		V
Input Keying Current	I_9			5	100	μA
Input Blocking Current	I_9	V_9 = -5 V			1	μA
Input Switching Current	I_9				5	μA
Input Voltage ($_{pk-pk}$)	V_9	Sync Positive Video Signal	1	3	7	V_{pk-pk}
NOISE SEPARATOR (PIN 10)						
Input Switching Voltage	V_{10}			1.4		V
Input Keying Current	I_{10}			5	100	μA
Input Switching Current	I_{10}			150		μA
Input Blocking Current	I_{10}	V_{10} = -5 V			1	μA
Input Voltage (pk-pk)	V_{10}	Sync Positive Video Signal	1	3	7	V_{pk-pk}
Superimposed Noise Voltage ($_{pk-pk}$)	V_n				7	V_{pk-pk}
LINE FLYBACK PULSE (PIN 6)						
Input Current	I_6		10			μA
Input Switching Voltage	V_6			1.4		V
Input Limiting Voltage	V_6			-0.7 to +1.4		V
Input Resistance	R_6			400		Ω
PULSE DURATION SWITCH (PIN 4)						
Input Voltage	V_4	t = 0 μs, V_3 = 0 (Note 1)		5.4 to 6.5		V
		t = 6 μs		9.4 to V_1		V
		t = 14 μs + td (Note 6)		0 to 4		V
Input Current	I_4	t = 0 μs, V_3 = 0		0		μA
		t = 6 μs	200			μA
		t = 14 μs + td (Note 6)			-200	μA

ELECTRICAL CHARACTERISTICS: T_A = 25°C; V_1 = 12 V, See test circuit unless otherwise noted. (Cont'd)

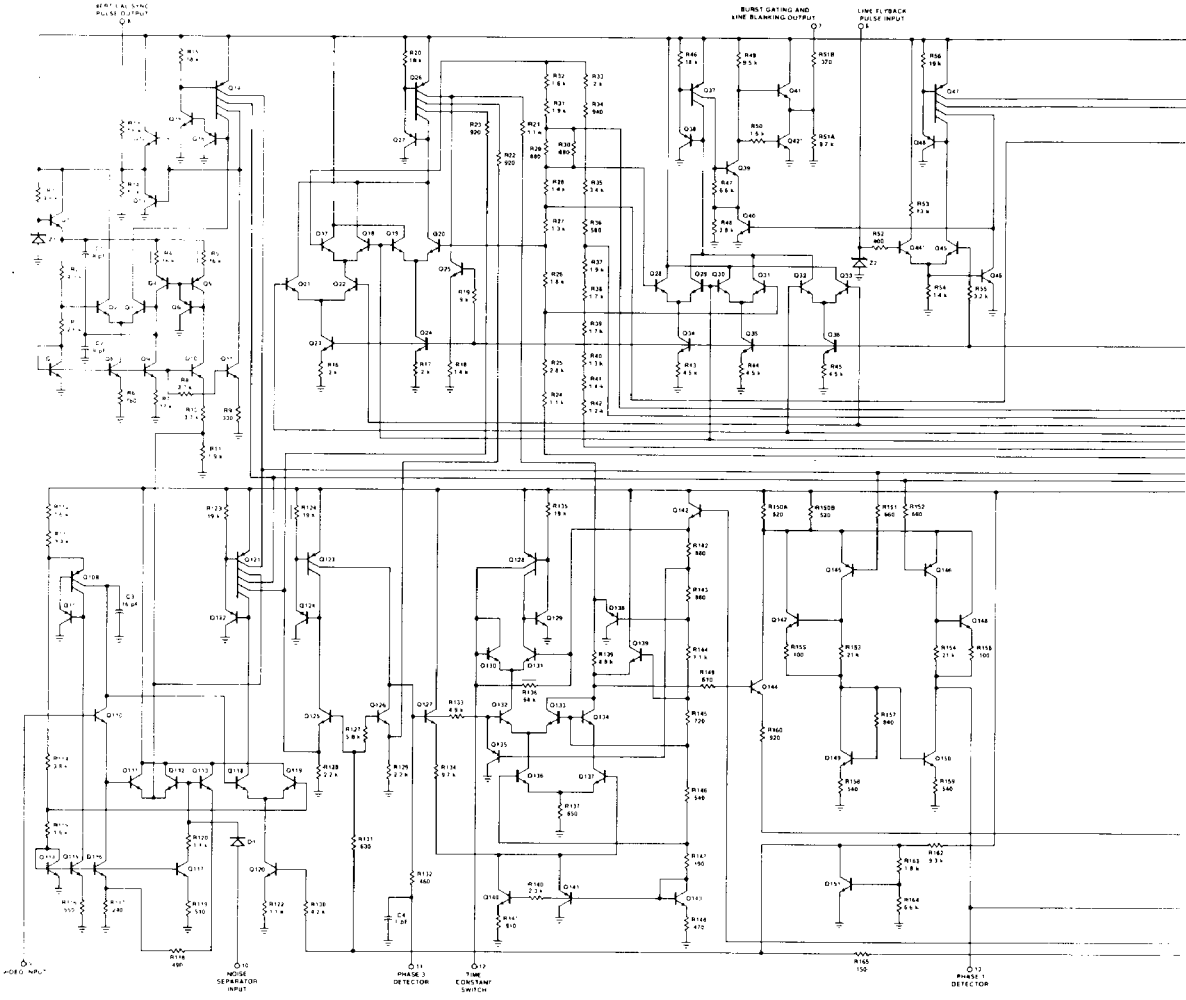
CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR (PIN 14 and PIN 15)						
Low Level Threshold Voltage	V_{14}			4.4		V
High Level Threshold Voltage	V_{14}			7.6		V
Discharge Current	I_{14}			±.47		mA
Free Running Frequency	f_o	C_{14} = 4.7 nF, R_{15} = 12 kΩ		15625		Hz
Spread of Frequency	$\Delta f_o/f_o$	Note 4	-5		+5	%
Frequency Control Sensitivity	$\Delta f_o/\Delta I_{15}$			31		Hz/μA
Adjustment Range	$\Delta f_o/f_o$			±10		%
Frequency Change With Supply Voltage	$\frac{\Delta f_o/f_o}{\Delta V/V_{nom}}$	V_1 = 12 V, Note 4	-.05		+.05	
Frequency Change With Supply Voltage	Δf_o	V_1 = 12 to 5 V, Note 4	10		+10	%
Temperature Coefficient of Oscillator Frequency per °C		Note 4	-10^{-4}		$+10^{-4}$	
COINCIDENCE DETECTOR (ϕ_3) and SWITCHING ON VCR (PIN 11)						
Input Voltage	V_{11}	Note 2		0 to 1.5		V
Input Current	I_{11}	Note 2			-200	μA
Input Voltage	V_{11}			9 to V_1		V
Input Current	I_{11}			1 to 2		mA
Output Voltage	V_{11}			0.5 to 6		V
Peak Output Current	I_{11}	Without Coincidence		0.1		mA
Peak Output Current	I_{11}	With Coincidence		-0.5		mA
VERTICAL SYNC PULSE (PIN 8)		Positive Going				
Output Voltage	V_8		10	11		V_{pk-pk}
Output Resistance	R_8			2		kΩ
Turn-ON Delay	t_{on}	Delay between leading edge of input & output signal		12		μs
Turn-OFF Delay	t_{off}	Delay between trailing edge of input & output signal	t_{on}			μs
BLANKING AND BURST GATING PULSE (PIN 7)		Positive Going				
Burst Gating Pulse Output Voltage	V_7		10	11		V_{pk-pk}
Output Resistance	R_7			400		Ω
Phase Relationship to Leading Edge	t	Note 3 V_7 = 7 V		1.9 typ 1.0 to 2.8		μs
Phase Relationship to Trailing Edge	t	Note 3 V_7 = 7 V		6.6 typ 5.8 to 7.4		μs
Blanking Pulse Output Voltage	V_7			2.5 to 3.5		V
LINE DRIVE PULSE (PIN 3)		Positive Going				
Output Voltage	V_3			10.5		V_{pk-pk}
Output Current (Average Value)	I_3			-100		mA
Output Resistance	R_3	For leading edge of Line Pulse		2.5		Ω
Output Resistance	R_3	For trailing edge of Line Pulse		20		Ω
Output Pulse Duration	t_p	V_4 > 9.4 V		6 typ 4.5-7.5		μs
Output Pulse Duration	t_p	V_4 < 4 V, Note 6		14 + td		μs
Supply Voltage for Switching off the Output Pulse	V_1			4		V

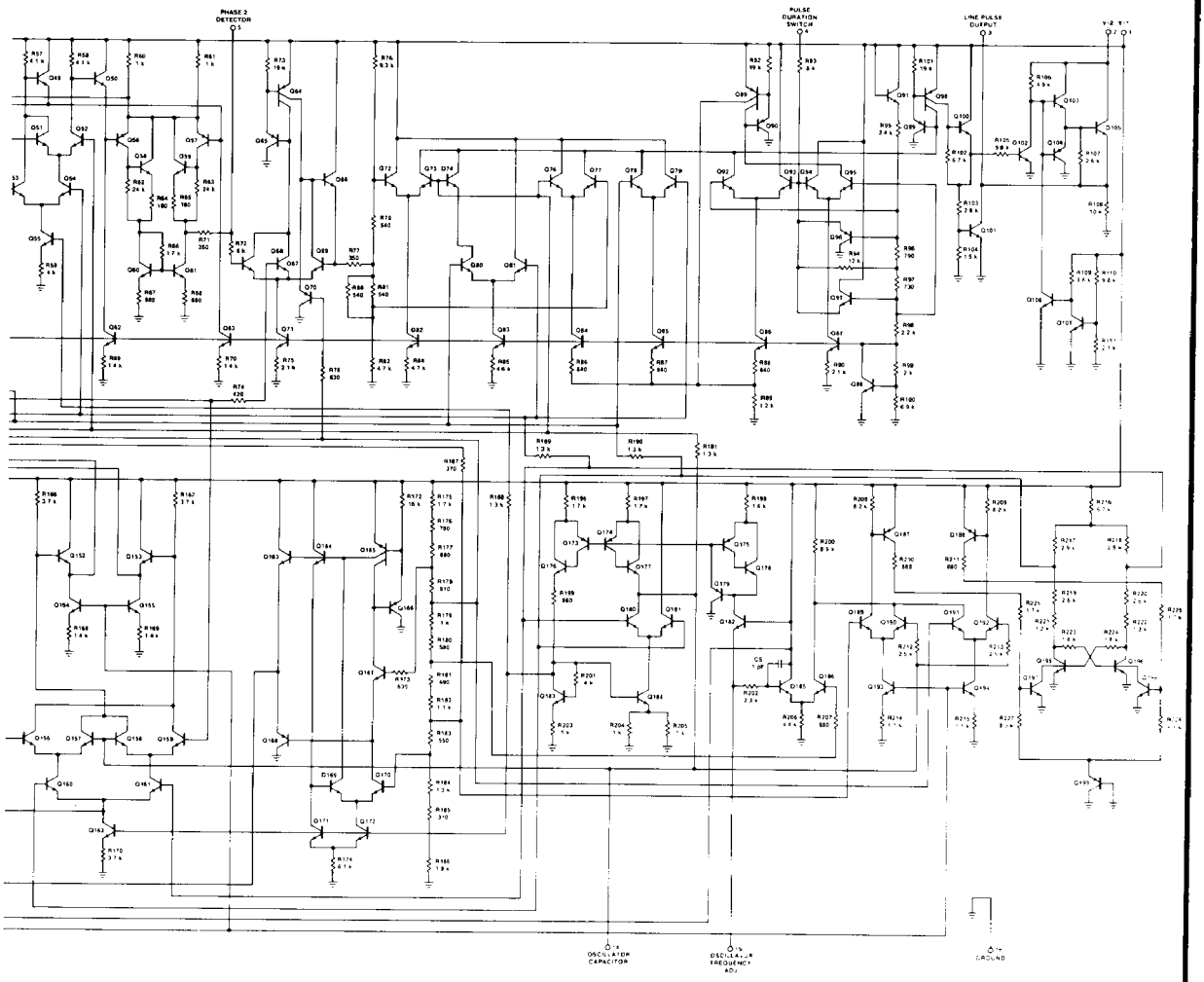
ELECTRICAL CHARACTERISTICS: T_A = 25°C; V_1 = 12 V, See test circuit unless otherwise noted. (Cont'd)

CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
PHASE COMPARISON (ϕ_1) (PIN 13)		Sync Pulse/Oscillator				
Control Voltage Range	V_{13}			3.8 to 8.2		V
Peak Control Current	I_{13}			±2.1 typ ±1.9-2.3		mA
Output Blocking Current	I_{13}	V_{13} = 4 to 8 V			1	μA
Output Resistance	R_{13}	Current Source V_{13} = 4 to 8 V		High		ohmic
Output Resistance	R_{13}	Emitter Follower V_{13} < 3.8 or > 8.2 V		Low		ohmic
Control Sensitivity				2		kHz/μs
Capture & Holding Range	Δf	82 kΩ between Pins 13 & 15		±780		Hz
Spread of Capture & Holding Range	$\Delta(\Delta f)$	Note 4		±10		%
PHASE COMPARISON (ϕ_2) (PIN 5)		Oscillator/Line Flyback Pulse				
Control Voltage Range	V_5			5.4 to 7.6		V
Peak Control Current	I_5			±1		mA
Input Current at Blocked Phase Detector	I_5	V_5 = 5.4 to 7.6 V			5	μA
Output Resistance	R_5	Current Source V_5 = 5.4 to 7.6 V		High		ohmic
Output Resistance	R_5	V_5 = < 5.4 or > 7.6 V		8		kΩ
Allowable Delay between Leading Edge of Output Pulse and Leading Edge of Flyback Pulse (t_{fp} = 12 μs)	t_d			0-15		μs
Static Control Error	$\Delta t/\Delta td$				0.2	%
OVERALL PHASE RELATION		Note 5				
Phase Relation Between Middle of Sync Pulse and the Middle of the Flyback Pulse	t			2.6		μs
Tolerance of Phase Relationship	Δt		-0.7		+0.7	μs
TIME CONSTANT SWITCH (PIN 12)						
Output Voltage	V_{12}			6		V
Output Current	I_{12}		-1		+1	mA
Output Resistance	R_{12}	V_{11} = 2.5 to 7 V		100		Ω
Output Resistance	R_{12}	V_{11} = < 1.5 V or > 9 V		60		kΩ
INTERNAL GATING PULSE						
Pulse Duration	t_p			7.5		μs

NOTES:
1. Can also be left unconnected.
2. When supplied by the IC.
3. Phase relationship between the middle of the sync pulse at the input and leading or trailing edge of the burst gating pulse.
4. Excluding the affect of variations in external components tolerances.
5. The adjustment of the overall phase relation and consequently the leading edge of the output pulse occurs automatically by phase control ϕ_2. If additional adjustment is used, the following values apply:
   ADJUSTMENT SENSITIVITY
   caused by: adjustment voltage $\Delta V_5/\Delta t$ typ 0.1 V/μs
   adjustment current $\Delta I_5/\Delta t$ typ 30 μA/μs
6. td = switch-OFF delay of the line output stage.

EQUIVALENT CIRCUIT




PHASE 2 DETECTOR
PULSE DURATION SWITCH
LINE PULSE OUTPUT
Y-2 Y-1
OSCILLATOR CAPACITOR
OSCILLATOR FREQUENCY ADJ
GROUND

TEST AND APPLICATIONS CIRCUIT