IF Digitizing Subsystem

AD9874*

FEATURES

10 MHz–300 MHz Input Frequency
6.8 kHz–270 kHz Output Signal Bandwidth
8.1 dB SSB NF
0 dBm IIP3
AGC Free Range up to –34 dBm
12 dB Continuous AGC Range
16 dB Front End Attenuator
Baseband I/Q 16-bit (or 24-bit) Serial Digital Output
LO and Sampling Clock Synthesizers
Programmable Decimation Factor, Output Format, AGC, and Synthesizer Settings
370 Ω Input Impedance
2.7 V–3.6 V Supply Voltage
Low Current Consumption: 20 mA
48–Lead LQFP Package (1.4 mm Thick)

APPLICATIONS

Multimode Narrowband Radio Products
Analog/Digital UHF/VHF FDMA Receivers
TETRA, APCO25, GSM/EDGE
Portable and Mobile Radio Products
Base Station Applications

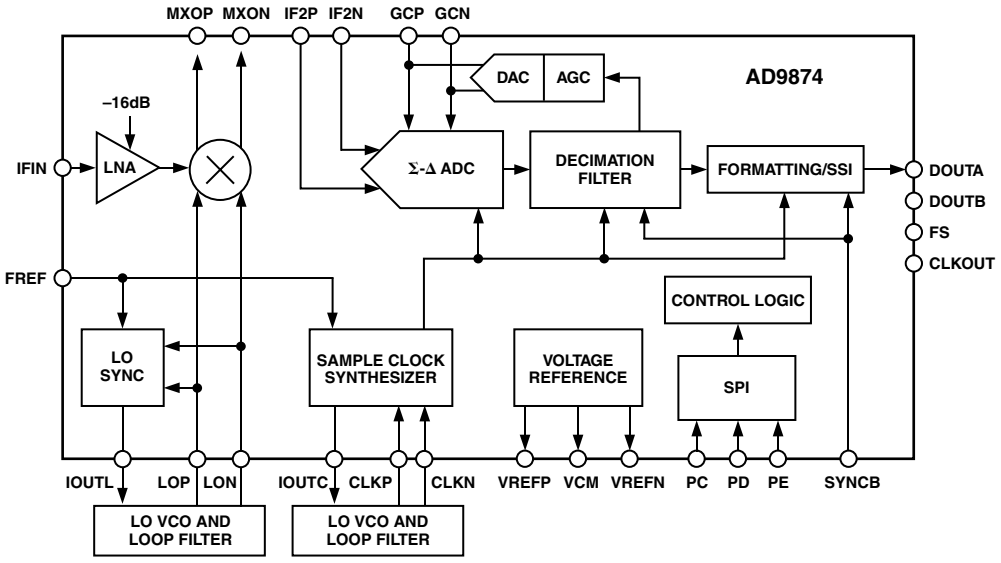
GENERAL DESCRIPTION

The AD9874 is a general-purpose IF subsystem that digitizes a low level 10 MHz–300 MHz IF input with a signal bandwidth ranging from 6.8 kHz to 270 kHz. The signal chain of the AD9874 consists of a low noise amplifier, a mixer, a band-pass sigma-delta analog-to-digital converter, and a decimation filter with programmable decimation factor. An automatic gain control (AGC) circuit gives the AD9874 12 dB of continuous gain adjustment. Auxiliary blocks include both clock and LO synthesizers.

The AD9874's high dynamic range and inherent antialiasing provided by the band-pass sigma-delta converter allow the AD9874 to cope with blocking signals up to 95 dB stronger than the desired signal. This attribute can often reduce the cost of a radio by reducing its IF filtering requirements. Also, it enables multimode radios of varying channel bandwidths, allowing the IF filter to be specified for the largest channel bandwidth.

The SPI port programs numerous parameters of the AD9874, thus allowing the device to be optimized for any given application. Programmable parameters include the following: synthesizer divide ratios; AGC attenuation and attack/decay time; the received signal strength level; decimation factor; the output data format; 16 dB attenuator; and the selected bias currents. The bias currents of the LNA and mixer can be further reduced at the expense of the degraded performance for battery-powered applications.

FUNCTIONAL BLOCK DIAGRAM



*Protected by U.S. Patent No. 5,969,657; other patents pending.

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703

AD9874–SPECIFICATIONS (VDDI = VDDF = VDDA = VDDC = VDDL = VDDD = VDDH = 2.7 to 3.6 V, VDDQ = VDDP = 2.7 V to 5.5 V, f_{CLK} = 18 MSPS, f_{IF} = 109.65 MHz, f_{LO} = 107.4 MHz, f_{REF} = 16.8 MHz, unless otherwise noted.)[1]

Parameter	Temp	Test Level	Min	Typ	Max	Unit
SYSTEM DYNAMIC PERFORMANCE[2]						
SSB Noise Figure @ Min VGA Attenuation[3, 4]	Full	IV		8.1	9.5	dB
@ Max VGA Attenuation[3, 4]	Full	IV		13		dB
Dynamic Range with AGC Enabled[3, 4]	Full	IV	91	95		dB
IF Input Clip Point @ Max VGA Attenuation[3]	Full	IV	–20	–19		dBm
@ Min VGA Attenuation[3]	Full	IV	–32	–31		dBm
Input Third Order Intercept (IIP3)	Full	IV	–5	0		dBm
Gain Variation over Temperature	Full	IV		0.7	2	dB
LNA + MIXER						
Maximum RF and LO Frequency Range	Full	IV	300	500		MHz
LNA Input Impedance	25°C	V		370//1.4		Ω//pF
Mixer LO Input Resistance	25°C	V		1		kΩ
LO SYNTHESIZER						
LO Input Frequency	Full	IV	7.75		300	MHz
LO Input Amplitude	Full	IV	0.3		2.0	V p-p
FREF (Reference) Frequency	Full	IV	0.1		25	MHz
FREF Input Amplitude	Full	IV	0.3		3	V p-p
Minimum Charge Pump Current @ 5 V[5]	Full	VI	0.48	0.67	0.78	mA
Maximum Charge Pump Current @ 5 V[5]	Full	VI	3.87	5.3	6.2	mA
Charge Pump Output Compliance[6]	Full	VI	0.4		VDDP – 0.4	V
Synthesizer Resolution	Full	IV	6.25			kHz
CLOCK SYNTHESIZER						
CLK Input Frequency	Full	IV	13		26	MHz
CLK Input Amplitude	Full	IV	0.3		V_{DDC}	V p-p
Minimum Charge Pump Output Current[5]	Full	VI	0.48	0.67	0.78	mA
Maximum Charge Pump Output Current[5]	Full	VI	3.87	5.3	6.2	mA
Charge Pump Output Compliance[6]	Full	VI	0.4		VDDQ – 0.4	V
Synthesizer Resolution	Full	IV	2.2			kHz
SIGMA-DELTA ADC						
Resolution	Full	IV	16		24	Bits
Clock Frequency (f_{CLK})	Full	IV	13		26	MHz
Center Frequency	Full	V		$f_{CLK}/8$		MHz
Pass-Band Gain Variation	Full	IV			1.0	dB
Alias Attenuation	Full	IV	80			dB
GAIN CONTROL						
Programmable Gain Step	Full	V		16		dB
AGC Gain Range (Continuous)	Full	V		12		dB
OVERALL						
Analog Supply Voltage (VDDA, VDDF, VDDI)	Full	VI	2.7	3.0	3.6	V
Digital Supply Voltage (VDDD, VDDC, VDDL)	Full	VI	2.7	3.0	3.6	V
Interface Supply Voltage[7] (VDDH)	Full	VI	1.8		3.6	V
Charge Pump Supply Voltage (VDDP, VDDQ)	Full	VI	2.7	5.0	5.5	V
Total Current						
High Performance Setting[8]	Full	VI		20	26.5	mA
Low Power Mode[8]	Full	VI		17	22	mA
Standby	Full	VI		0.01	0.1	mA
OPERATING TEMPERATURE RANGE			–40		+85	°C

NOTES

[1] Standard operating mode: LNA/Mixer @ high bias setting, VGA @ Min ATTEN setting, synthesizers in normal (not fast acquire) mode, f_{CLK} = 18 MHz, decimation factor = 900, 16-bit digital output, and 10 pF load on SSI output pins.

[2] This includes 0.9 dB loss of matching network.

[3] AGC with DVGA enabled.

[4] Measured in 10 kHz bandwidth.

[5] Programmable in 0.67 mA steps.

[6] Voltage span in which LO (or CLK) charge pump output current is maintained within 5% of nominal value of VDDP/2 (or VDDQ/2).

[7] VDDH must be less than VDDD + 0.5 V.

[8] Clock VCO off, add additional 0.7 mA with VGA @ Max ATTEN setting.

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (VDDI = VDDF = VDDA = VDDC = VDDL = VDDD = VDDH = 2.7 to 3.6 V, VDDQ = VDDP = 2.7 V to 5.5 V, f_{CLK} = 18 MSPS, f_{IF} = 109.65 MHz, f_{LO} = 107.4 MHz, f_{REF} = 16.8 MHz, unless otherwise noted.)[1]

Parameter	Temp	Test Level	Min	Typ	Max	Unit
DECIMATOR						
Decimation Factor[2]	Full	IV	48		960	
Pass-Band Width	Full	V		50%		f_{CLKOUT}
Pass-Band Gain Variation	Full	IV			1.2	dB
Alias Attenuation	Full	IV	88			dB
SPI-READ OPERATION (See Figure 1a)						
PC Clock Frequency	Full	IV			10	MHz
PC Clock Period (t_{CLK})	Full	IV	100			ns
PC Clock HI (t_{HI})	Full	IV	45			ns
PC Clock LOW (t_{LOW})	Full	IV	45			ns
PC to PD Setup Time (t_{DS})	Full	IV	2			ns
PC to PD Hold Time (t_{DH})	Full	IV	2			ns
$\overline{PE}$ to PC Setup Time (t_S)	Full	IV	5			ns
PC to $\overline{PE}$ Hold Time (t_H)	Full	IV	5			ns
SPI-WRITE OPERATION[3] (See Figure 1b)						
PC Clock Frequency	Full	IV			10	MHz
PC Clock Period (t_{CLK})	Full	IV	100			ns
PC Clock HI (t_{HI})	Full	IV	45			ns
PC Clock LOW (t_{LOW})	Full	IV	45			ns
PC to PD Setup Time (t_{DS})	Full	IV	2			ns
PC to PD Hold Time (t_{DH})	Full	IV	2			ns
PC to PD (or DOUBT) Data Valid Time (t_{DV})	Full	IV	3			ns
$\overline{PE}$ to PD Output Valid to Hi-Z (t_{EZ})	Full	IV		8		ns
SSI[3] (see Figure 2b)						
CLKOUT Frequency	Full	IV	0.867		26	MHz
CLKOUT Period (t_{CLK})	Full	IV	38.4		1153	ns
CLKOUT Duty Cycle (t_{HI}, t_{LOW})	Full	IV	33	50	67	ns
CLKOUT to FS Valid Time (t_V)	Full	IV	–1		1	ns
CLKOUT to DOUT Data Valid Time (t_{DV})	Full	IV	–1		1	ns
CMOS LOGIC INPUTS[4]						
Logic "1" Voltage (V_{IH})	Full	IV	VDDH–0.2			V
Logic "0" Voltage (V_{IL})	Full	IV			0.5	V
Logic "1" Current (V_{IH})	Full	IV		10		mA
Logic "0" Current (V_{IL})	Full	IV		10		mA
Input Capacitance	Full	IV		3		pF
CMOS LOGIC OUTPUTS[3,4,5]						
Logic "1" Voltage (V_{IH})	Full	IV		VDDH–0.2		V
Logic "0" Voltage (V_{IL})	Full	IV			0.2	V

NOTES

[1]Standard operating mode: high IIP3 setting, synthesizers in normal (not fast acquire) mode, f_{CLK} = 18 MHz, decimation factor = 300, 10 pF load on SSI output pins: VDDx = 3.0 V.

[2]Programmable in steps of 48 or 60.

[3]CMOS output mode with C_{LOAD} = 10 pF and Drive Strength = 7.

[4]Absolute Max and Min input/output levels are VDDH +0.3 V and –0.3 V.

[5]I_{OL} = 1 mA; specification is also dependent on Drive Strength setting.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Unit
VDDF, VDDA, VDDC, VDDD, VDDH, VDDL, VDDI	GNDF, GNDA, GNDC, GNDD, GNDH, GNDL, GNDI, GNDS	–0.3	+4.0	V
VDDF, VDDA, VDDC, VDDD, VDDH, VDDL, VDDI	VDDR, VDDA, VDDC, VDDD, VDDH, VDDL, VDDI	–4.0	+4.0	V
VDDP, VDDQ	GNDP, GNDQ	–0.3	+6.0	V
GNDF, GNDA, GNDC, GNDD, GNDH, GNDL, GNDI, GNDQ, GNDP, GNDS	GNDF, GNDA, GNDC, GNDD, GNDH, GNDL, GNDI, GNDQ, GNDP, GNDS	–0.3	+0.3	V
MXOP, MXON, LOP, LON, IFIN, CXIF, CXVL, CXVM	GNDI	–0.3	VDDI + 0.3	V
PC, PD, PE, CLKOUT, DOUTA, DOUTB, FS, SYNCB	GNDH	–0.3	VDDH + 0.3	V
IF2N, IF2P, GCP, GCN	GNDF	–0.3	VDDF + 0.3	V
VREFP, VREFN, RREF	GNDA	–0.3	VDDA + 0.3	V
IOUTC	GNDQ	–0.3	VDDQ + 0.3	V
IOUTL	GNDP	–0.3	VDDP + 0.3	V
CLKP, CLKN	GNDC	–0.3	VDDC + 0.3	V
FREF	GNDL	–0.3	VDDL + 0.3	V
Junction Temperature			150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Thermal Resistance

48-Lead LQFP

θ_{JA} = 76.2°C/W

θ_{JC} = 17°C/W

EXPLANATION OF TEST LEVELS

TEST LEVEL

I. 100% production tested.

II. 100% production tested at 25°C and sample tested at specified temperatures. AC testing done on sample basis.

III. Sample tested only.

IV. Parameter is guaranteed by design and/or characterization testing.

V. Parameter is a typical value only.

VI. All devices are 100% production tested at 25°C; min. and max. guaranteed by design and characterization for industrial temperature range.

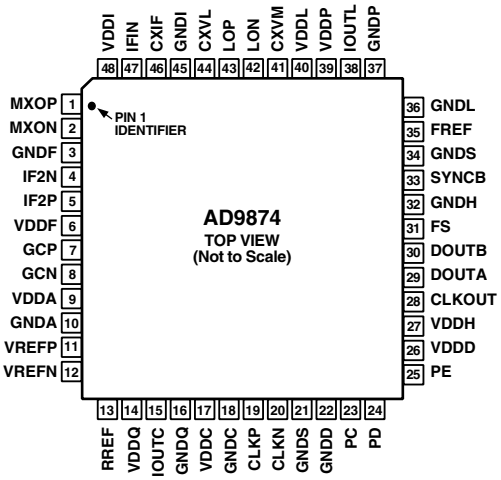
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9874BST	–40°C to +85°C	48-Lead Thin Plastic Quad Flatpack (LQFP)	ST-48
AD9874EB		Evaluation Board	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9874 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Description
1	MXOP	Mixer Output, Positive
2	MXON	Mixer Output, Negative
3	GNDF	Ground for Front End of ADC
4	IF2N	Second IF Input (to ADC), Negative
5	IF2P	Second IF Input (to ADC), Positive
6	VDDF	Positive Power Supply for Front End of ADC
7	GCP	Filter Capacitor for ADC Full-Scale Control
8	GCN	Full-Scale Control Ground
9	VDDA	Positive Power Supply for ADC Back End
10	GNDA	Ground for ADC Back End
11	VREFP	Voltage Reference, Positive
12	VREFN	Voltage Reference, Negative
13	RREF	Reference Resistor: Requires 100 kΩ to GNDA
14	VDDQ	Positive Power Supply for Clock Synthesizer
15	IOUTC	Clock Synthesizer Charge Pump Output Current
16	GNDQ	Ground for Clock Synthesizer Charge Pump
17	VDDC	Positive Power Supply for Clock Synthesizer
18	GNDC	Ground for Clock Synthesizer
19	CLKP	Sampling Clock Input/Clock VCO Tank, Positive
20	CLKN	Sampling Clock Input/Clock VCO Tank, Negative
21	GNDS	Substrate Ground
22	GNDD	Ground for Digital Functions
23	PC	Clock Input for SPI Port
24	PD	Data I/O for SPI Port
25	PE	Enable Input for SPI Port
26	VDDD	Positive Power Supply for Internal Digital Functions

Pin	Mnemonic	Description
27	VDDH	Positive Power Supply for Digital Interface
28	CLKOUT	Clock Output for SSI Port
29	DOUTA	Data Output for SSI Port
30	DOUTB	Data Output for SSI Port (Inverted) or SPI Port
31	FS	Frame Sync for SSI Port
32	GNDH	Ground for Digital Interface
33	SYNCB	Resets SSI and Decimator Counters; Active Low
34	GNDS	Substrate Ground
35	FREF	Reference Frequency Input for Both Synthesizers
36	GNDL	Ground for LO Synthesizer
37	GNDP	Ground for LO Synthesizer Charge Pump
38	IOUTL	LO Synthesizer Charge Pump Output Current Charge Pump
39	VDDP	Positive Power Supply for LO Synthesizer Charge Pump
40	VDDL	Positive Power Supply for LO Synthesizer
41	CXVM	External Filter Capacitor; DC Output of LNA
42	LON	LO Input to Mixer and LO Synthesizer, Negative
43	LOP	LO Input to Mixer and LO Synthesizer, Positive
44	CXVL	External Bypass Capacitor for LNA Power Supply
45	GNDI	Ground for Mixer and LNA
46	CXIF	External Capacitor for Mixer V-I Converter Bias
47	IFIN	First IF Input (to LNA)
48	VDDI	Positive Power Supply for LNA and Mixer

DEFINITION OF SPECIFICATIONS/TEST METHODS

Single-Sideband Noise Figure (SSB NF)

Noise figure (NF) is defined as the degradation in SNR performance (in dB) of an IF input signal after it passes through a component or system. It can be expressed with the following equation:

$$Noise\ Figure = 10 \times LOG(SNR_{IN} / SNR_{OUT})$$

The term SSB is applicable for heterodyne systems containing a mixer. It indicates that the desired signal spectrum resides on only one side of the LO frequency (i.e. single sideband); thus a "noiseless" mixer has a noise figure of 3 dB.

The AD9874's *SSB* noise figure is determined by the following equation:

$$SSB\ NF = P_{IN} - \{10 \times LOG(BW)\} - 174\ dBm/Hz - SNR$$

where P_{IN} is the input power of an unmodulated carrier, BW is the noise measurement bandwidth, –174 *dBm/Hz* is the thermal noise floor at 293°K, and *SNR* is the measured signal-to-noise ratio in dB of the AD9874.

Note, P_{IN} is set to –85 dBm to minimize any degradation in measured SNR due to phase noise from the RF and LO signal generators. The IF frequency, CLK frequency, and decimation factors are selected to minimize any "spurious" components falling within the measurement bandwidth. Note, a bandwidth of 10 kHz is used for the data sheet specification on Page 2. Refer to Figures 22a and 22b for an indication of how NF varies with BW. Also, refer to the TPCs to see how NF is affected by different operating conditions. All references to noise figures within this data sheet imply single-sideband noise figure.

Input Third Order Intercept (IIP3)

IIP3 is a figure of merit to determine a component's or system's susceptibility to intermodulation distortion (IMD) from its third order nonlinearities. Two unmodulated carriers' at a specified frequency relationship (f_1 and f_2) are injected into a nonlinear system exhibiting third order nonlinearities producing IMD components at $2f_1 - f_2$ and $2f_2 - f_1$. IIP3 graphically represents the extrapolated intersection of the carrier's input power with the third order IMD component when plotted in dB. The difference in power (D in dBc) between the two carriers and the resulting third order IMD components can be determined from the following equation:

$$D = 2 \times (IIP3 - P_{IN})$$

Dynamic Range (DR)

Dynamic range is the measure of a small target input signal (P_{TARGET}) in the presence of a large unwanted interferer signal (P_{INTER}). Typically, the large signal will cause some unwanted characteristic of the component or system to degrade, thus making it unable to detect the smaller target signal correctly. In the case of the AD9874, it is often a degradation in Noise Figure at increased VGA attenuation settings that limits its dynamic range (refer to TPC 15a, 15b, and 15c).

The test method for the AD9874 is as follows. The small target signal (an unmodulated carrier) is input at the center of the IF frequency and its power level (P_{TARGET}) is adjusted to achieve an SNR_{TARGET} of 6 dB. The power of the signal is then increased by 3 dB prior to injecting the interferer signal. The offset frequency of the interferer signal is selected so that aliases produced by the decimation filter's response as well as phase noise from the LO (due to reciprocal mixing) do not fall back within the measurement bandwidth. For this reason, an offset of 110 kHz was selected. The interferer signal (also an unmodulated carrier) is then injected into the input and its power level is increased to the point (P_{INTER}) where the target signal SNR is reduced to 6 dB. The dynamic range is determined from the following equation:

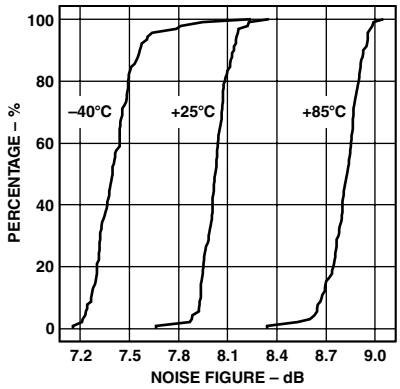
$$DR = P_{INTER} - P_{TARGET} + SNR_{TARGET}$$

Note, the AD9874's AGC is enabled for this test.

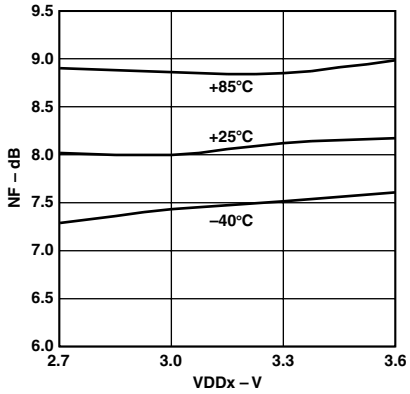
IF Input Clip Point

The IF input clip point is defined to be 2 dB *below* the input power level (P_{IN}), resulting in the "clipping" of the AD9874's ADC. Unlike other linear components that typically exhibit a "soft" compression (characterized by its 1 dB compression point), an ADC exhibits a "hard" compression once its input signal exceeds its rated maximum input signal range. In the case of the AD9874, which contains a Σ-Δ ADC, "hard" compression should be avoided since it causes severe SNR degradation.

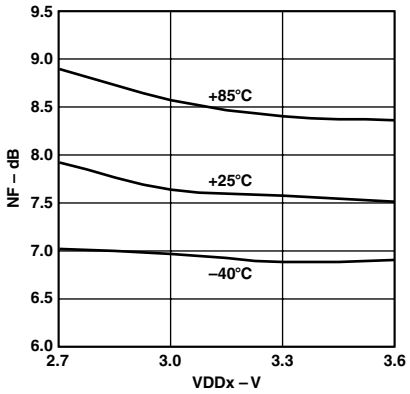
(VDDI = VDDF = VDDA = VDDC = VDDL = VDDD = VDDH = VDDx, VDDQ = VDDP = 5.0 V, f_{CLK} = 18 MSPS, f_{IF} = 109.56 MHz, f_{LO} = 107.4 MHz, T_A = 25°C, LO = –5 dBm, LO and CLK Synthesizer Disabled, 16-Bit Data with AGC and DVGA enabled, unless otherwise noted.)[1]



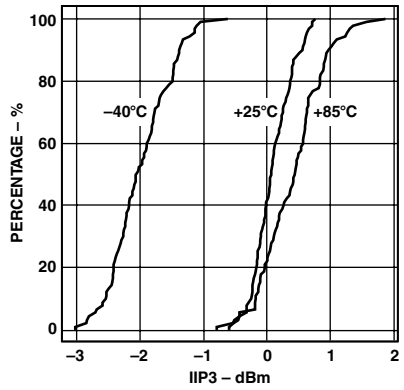
TPC 1a. CDF of SSB Noise Figure (VDDx = 3.0 V, High Bias[2])



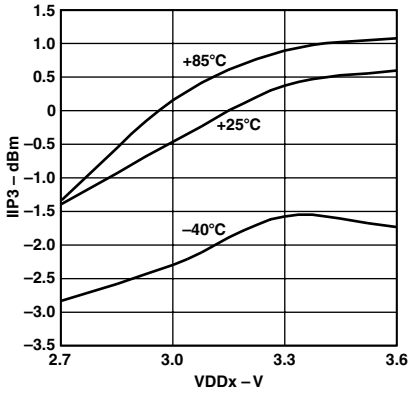
TPC 1b. SSB Noise Figure vs. Supply (High Bias[2])



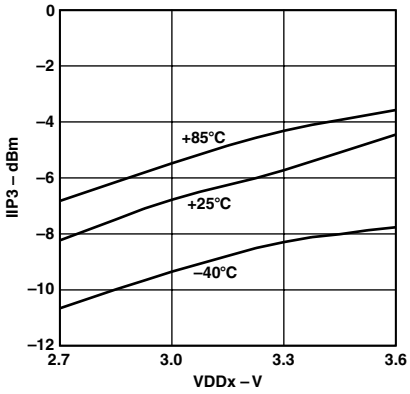
TPC 1c. SSB Noise Figure vs. Supply (Low Bias[3])



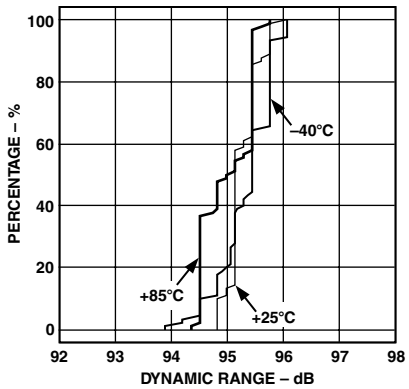
TPC 2a. CDF of IIP3 (VDDx = 3.0 V, High Bias[2])



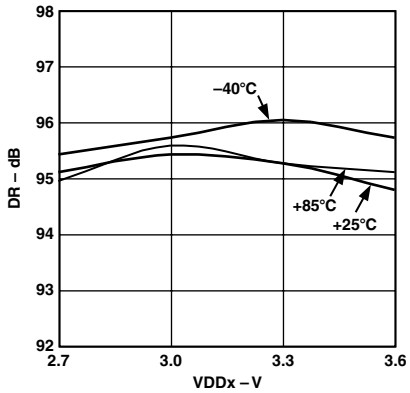
TPC 2b. IIP3 vs. Supply (High Bias[2])



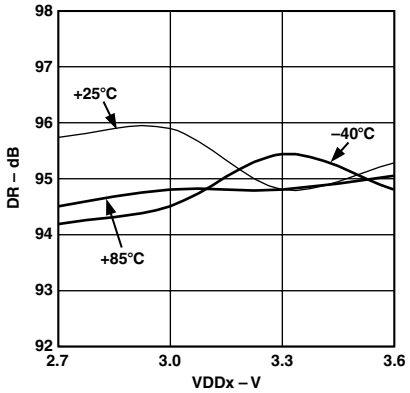
TPC 2c. IIIP3 vs. Supply (Low Bias[3])



TPC 3a. CDF of Dynamic Range (VDDx = 3.0 V, High Bias[2])



TPC 3b. Dynamic Range vs. Supply (High Bias[2])



TPC 3c. Dynamic Range vs. Supply (Low Bias[3])

[1]Data taken with Toko FSLM series 10 µH inductors
[2]High Bias corresponds to LNA_Mixer Setting of 33 in SPI Register 0x01
[3]Low Bias corresponds to LNA_Mixer Setting of 12 in SPI Register 0x01

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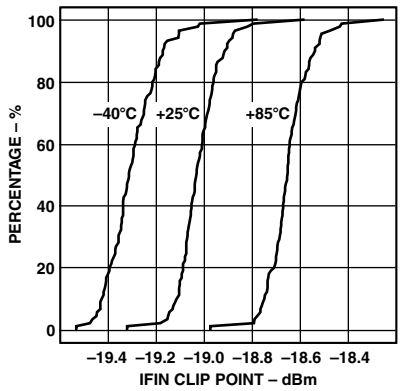
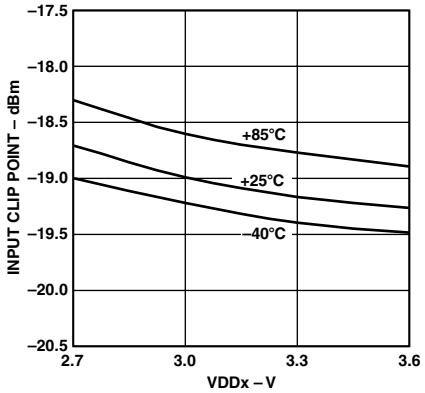
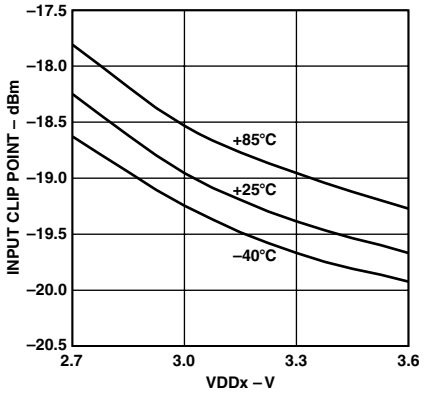


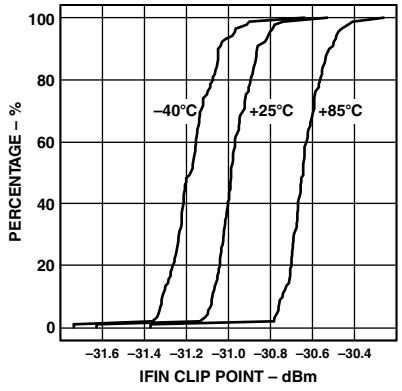
TPC 4a. CDF of Maximum VGA Attenuation "Clip Point" (VDDx = 3.0 V, High Bias[2])



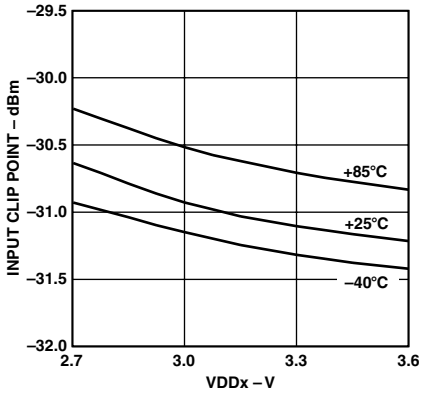
TPC 4b. Maximum VGA Attenuation "Clip Point" vs. Supply (High Bias[2])



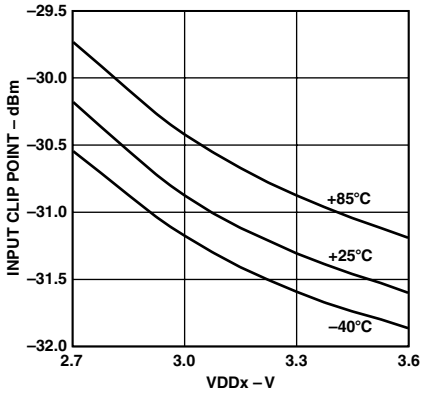
TPC 4c. Maximum VGA Attenuation "Clip Point" vs. Supply (Low Bias[3])



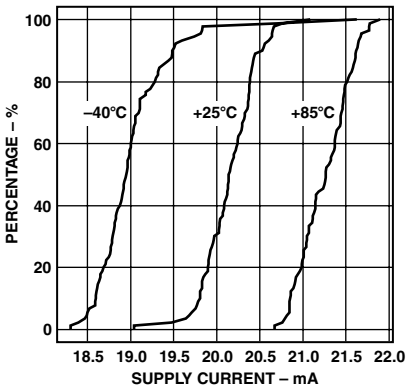
TPC 5a. CDF of Minimum VGA Attenuation "Clip Point" (VDDx = 3.0 V, High Bias[2])



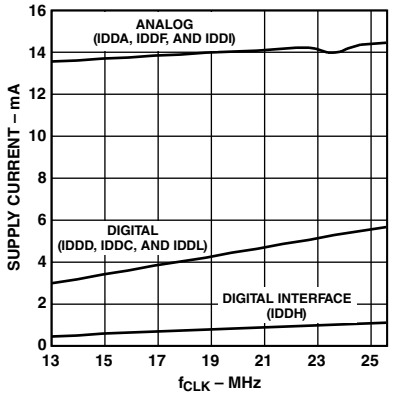
TPC 5b. Minimium VGA Attenuation "Clip Point" vs. Supply (High Bias[2])



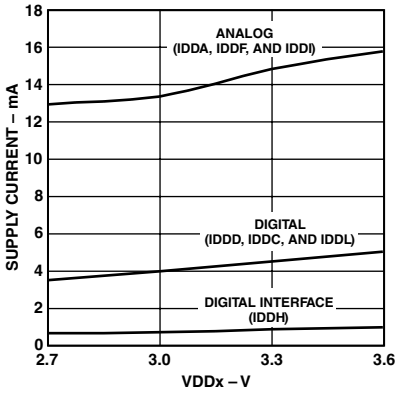
TPC 5c. Minimium VGA Attenuation "Clip Point" vs. Supply (Low Bias[3])



TPC 6a. CDF of Supply Current (VDDx = 3.0 V, High Bias[2])



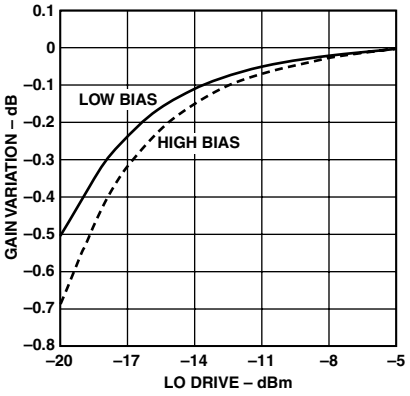
TPC 6b. Supply Current vs. f_{CLK} (VDDx = 3.0 V, High Bias[2])



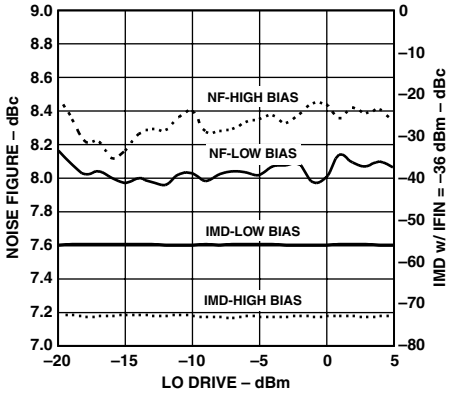
TPC 6c. Supply Current vs. Supply (High Bias[2])

[1]Data taken with Toko FSLM series 10 µH inductors
[2]High Bias corresponds to LNA_Mixer Setting of 33 in SPI Register 0x01
[3]Low Bias corresponds to LNA_Mixer Setting of 12 in SPI Register 0x01

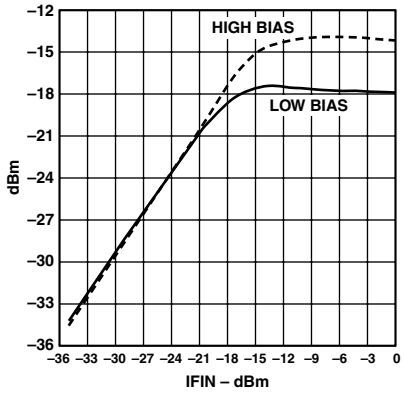
(VDDI = VDDF = VDDA = VDDC = VDDL = VDDD = VDDH = VDDx, VDDQ = VDDP = 5.0 V, f_{CLK} = 18 MSPS, f_{IF} = 109.56 MHz, f_{LO} = 107.4 MHz, T_A = 25°C, LO = –5 dBm, LO and CLK Synthesizer Disabled, 16-Bit Data with AGC and DVGA enabled, unless otherwise noted.)[1]



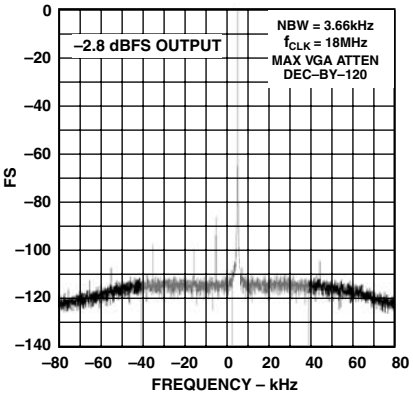
TPC 7a. Normalized Gain Variation vs. LO Drive (VDDx = 3.0 V)



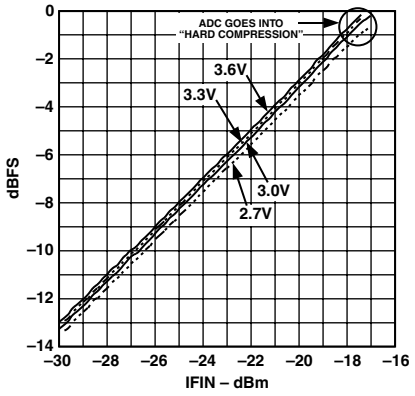
TPC 7b. Noise Figure and IMD vs. LO Drive (VDDx = 3.0 V)



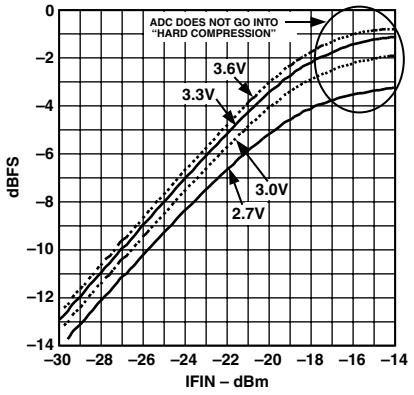
TPC 7c. Gain Compression vs. IFIN with 16 dB LNA Attenuator Enabled



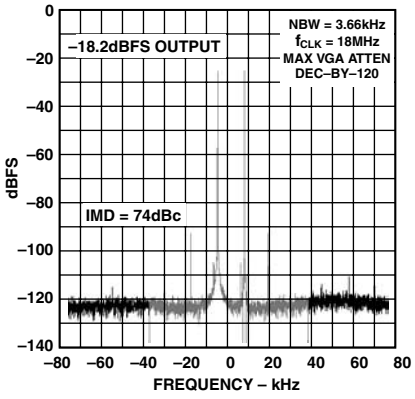
TPC 8a. Complex FFT of Baseband I/Q for Single-Tone (High Bias)



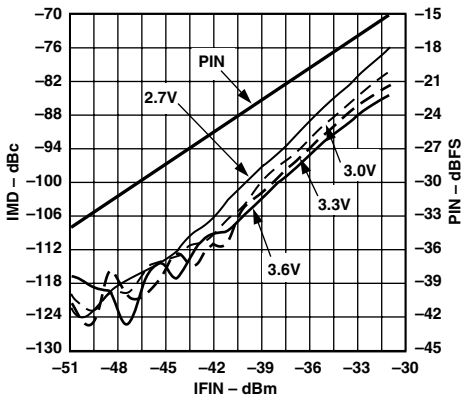
TPC 8b. Gain Compression vs. IFIN (High Bias[2])



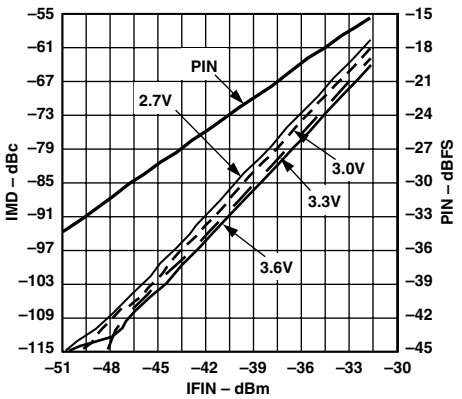
TPC 8c. Gain Compression vs. IFIN (Low Bias[3])



TPC 9a. Complex FFT of Baseband I/Q for Dual Tone IMD (High Bias with each IFIN Tone @ –35 dBm)



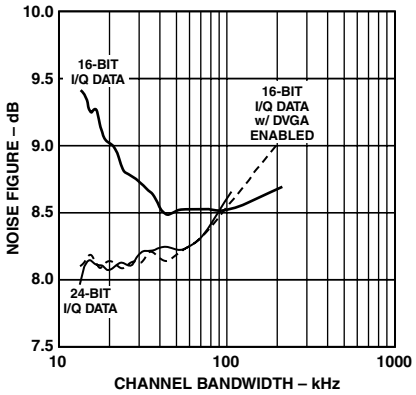
TPC 9b. IMD vs. IFIN (High Bias[2])



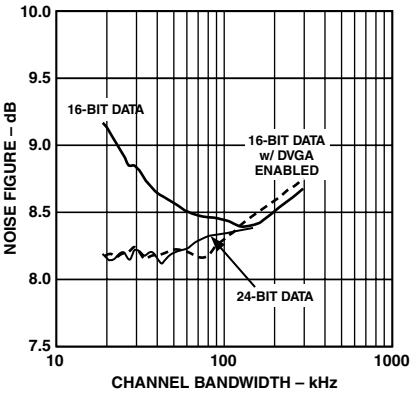
TPC 9c. IMD vs. IFIN (Low Bias[3])

[1]Data taken with Toko FSLM series 10 µH inductors
[2]High Bias corresponds to LNA_Mixer Setting of 33 in SPI Register 0x01
[3]Low Bias corresponds to LNA_Mixer Setting of 12 in SPI Register 0x01

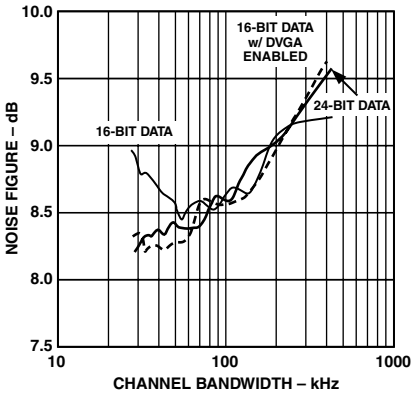
(VDDI = VDDF = VDDA = VDDC = VDDL = VDDD = VDDH = VDDx, VDDQ = VDDP = 5.0 V, f_{CLK} = 18 MSPS, f_{IF} = 109.56 MHz, f_{LO} = 107.4 MHz, T_A = 25°C, LO = –5 dBm, LO and CLK Synthesizer Disabled, 16-Bit Data with AGC and DVGA enabled, unless otherwise noted.)[1]



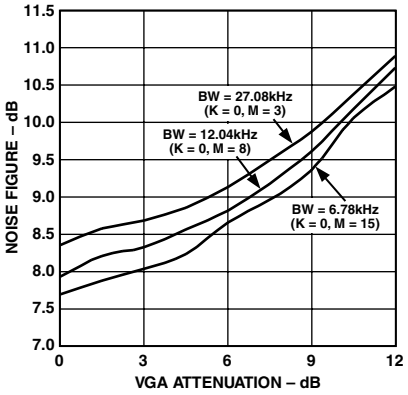
TPC 10a. Noise Figure vs. BW (Minimum Attenuation, f_{CLK} = 13 MSPS)



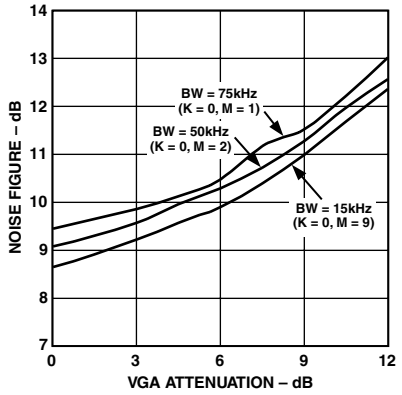
TPC 10b. Noise Figure vs. BW (Minimum Attenuation, f_{CLK} = 18 MSPS)



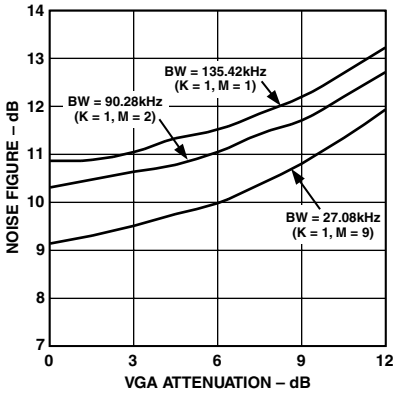
TPC 10c. Noise Figure vs. BW (Minimum Attenuation, f_{CLK} = 26 MSPS)



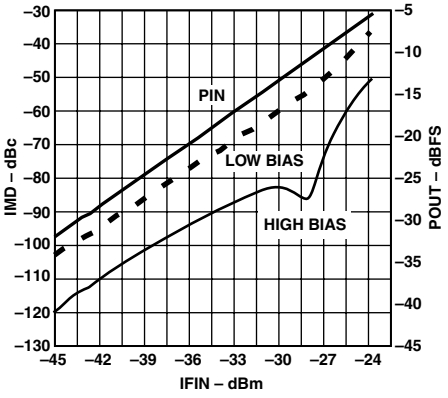
TPC 11a. Noise Figure vs. VGA Attenuation (f_{CLK} = 13 MSPS)



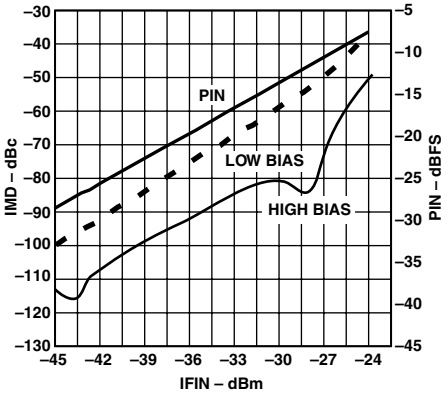
TPC 11b. Noise Figure vs. VGA Attenuation (f_{CLK} = 18 MSPS)



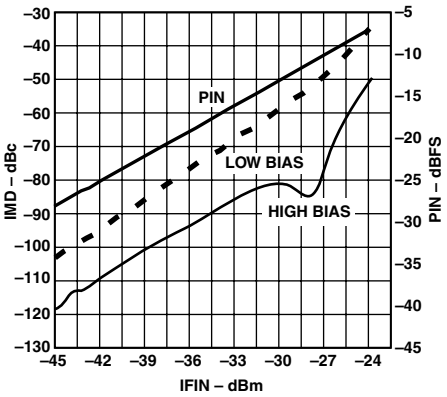
TPC 11c. Noise Figure vs. VGA Attenuation (f_{CLK} = 26 MSPS)



TPC 12a. IMD vs. IFIN (f_{CLK} = 13 MSPS)



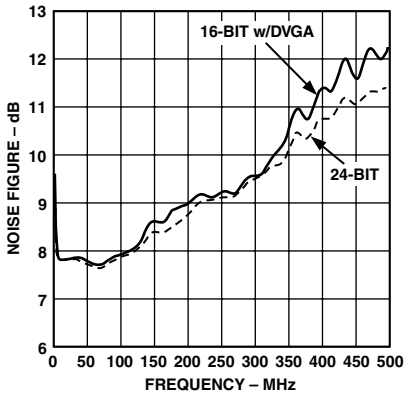
TPC 12b. IMD vs. IFIN (f_{CLK} = 18 MSPS)



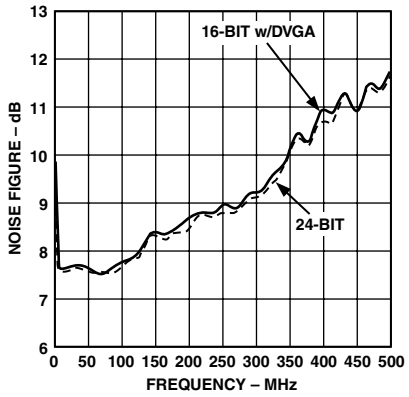
TPC 12c. IMD vs. IFIN (f_{CLK} = 26 MSPS)

[1]Data taken with Toko FSLM series 10 µH inductors
[2]High Bias corresponds to LNA_Mixer Setting of 33 in SPI Register 0x01
[3]Low Bias corresponds to LNA_Mixer Setting of 12 in SPI Register 0x01

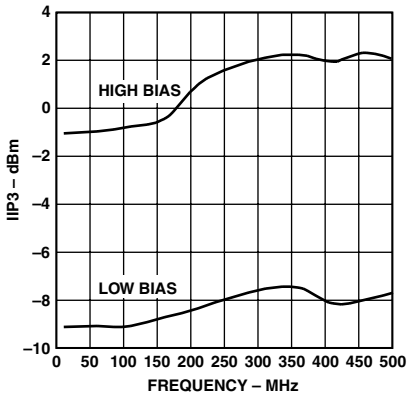
(VDDI = VDDF = VDDA = VDDC = VDDL = VDDD = VDDH = VDDx, VDDQ = VDDP = 5.0 V, f_{CLK} = 18 MSPS, f_{IF} = 109.56 MHz, f_{LO} = 107.4 MHz, T_A = 25°C, LO = –5 dBm, LO and CLK Synthesizer Disabled, 16-Bit Data with AGC and DVGA enabled, unless otherwise noted.)[1]



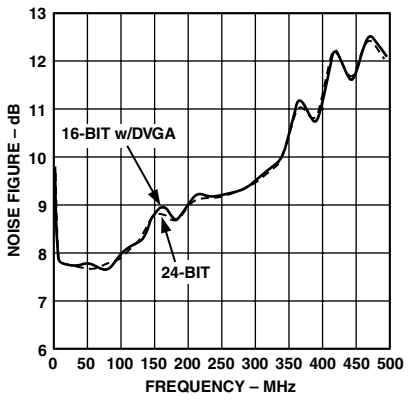
TPC 13a. Noise Figure vs. Frequency (Minimum Attenuation, f_{CLK} = 18 MSPS, BW = 10 kHz, High Bias)



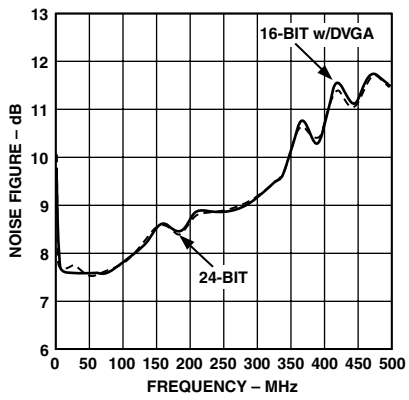
TPC 13b. Noise Figure vs. Frequency (Minimum Attenuation, f_{CLK} = 18 MSPS, BW = 10 kHz, Low Bias)



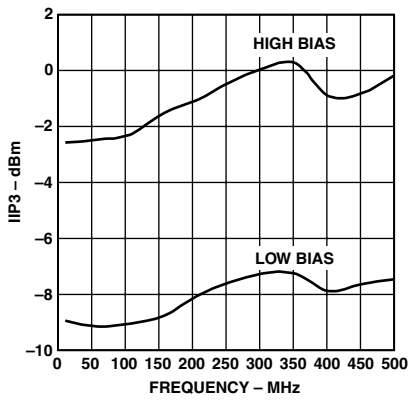
TPC 13c. Input IP3 vs. Frequency (f_{CLK} = 18 MSPS)



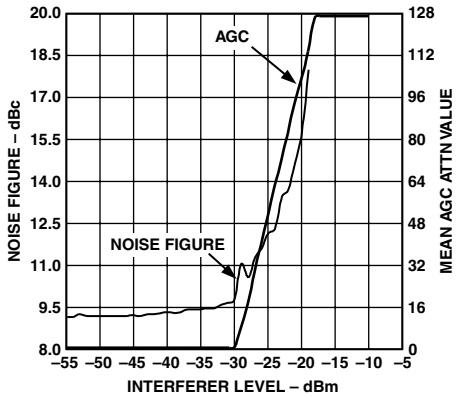
TPC 14a. Noise Figure vs. Frequency (Minimum Attenuation, f_{CLK} = 26 MSPS, BW = 24 kHz, High Bias)



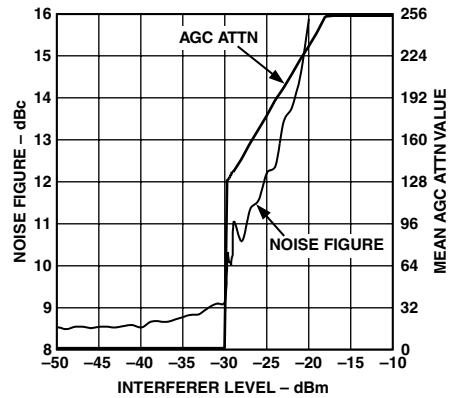
TPC 14b. Noise Figure vs. Frequency (Minimum Attenuation, f_{CLK} = 26 MSPS, BW = 24 kHz, Low Bias)



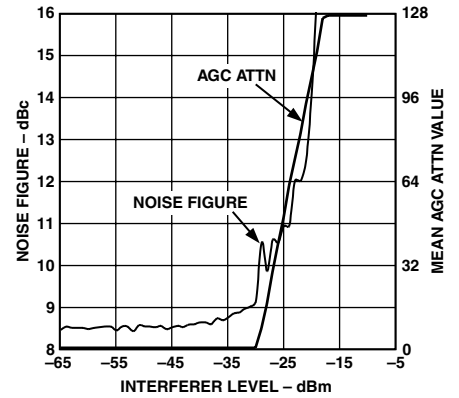
TPC 14c. Input IP3 vs. Frequency (f_{CLK} = 26 MSPS)



TPC 15a. Noise Figure vs. Interferer Level (16-Bit Data, BW = 12.5 kHz, AGCR = 1, $f_{interferer}$ = f_{IF} + 110 kHz)



TPC 15b. Noise Figure vs. Interferer Level (16-Bit Data with DVGA, BW = 12.5 kHz, AGCR = 1, $f_{interferer}$ = f_{IF} + 110 kHz)



TPC 15c. Noise Figure vs. Interferer Level (24-Bit Data, BW = 12.5 kHz, AGCR = 1, $f_{interferer}$ = f_{IF} + 110 kHz)

[1]Data taken with Toko FSLM series 10 µH inductors
[2]High Bias corresponds to LNA_Mixer Setting of 33 in SPI Register 0x01
[3]Low Bias corresponds to LNA_Mixer Setting of 12 in SPI Register 0x01

SERIAL PERIPHERAL INTERFACE (SPI)

The serial peripheral interface (SPI) is a bidirectional serial port. It is used to load configuration information into the registers listed below as well as to read back their contents. Table I provides a list of the registers that may be programmed through the SPI port. Addresses and default values are given in hexadecimal form.

Table I. SPI Address Map

Address (Hex)	Bit Breakdown	Width	Default Value	Name	Description
POWER CONTROL REGISTERS					
0x00	(7:0)	8	0xFF	STBY	Standby Control Bits (REF, LO, CKO, CK, GC, LNAMX, Unused, and ADC)
0x01	(7:6)	2	0	LNAB	LNA Bias Current (0 = 0.5 mA, 1 = 1 mA, 2 = 2 mA, 3 = 3 mA)
	(5:4)	2	0	MIXB	Mixer Bias Current (0 = 0.5 mA, 1 = 1.5 mA, 2 = 2.7 mA, 3 = 4 mA)
	(3:2)	2	0	CKOB	CK Oscillator Bias (0 = 0.25 mA, 1 = 0.35 mA, 2 = 0.40 mA, 3 = 0.65 mA)
	(1:0)	2	0	ADCB	Do Not Use
0x02	(7:0)	8	0x00	TEST	Factory Test Mode. Do not use.
AGC					
0x03	(7)	1	0	ATTEN	Apply 16 dB Attenuation in the Front End
	(6:0)	7	0x00	AGCG(14:8)	AGC Attenuation Setting (7 MSBs of a 15-Bit Unsigned Word)
0x04	(7:0)	8	0x00	AGCG(7:0)	AGC Attenuation Setting (8 LSBs of a 15-Bit Unsigned Word) Default corresponds to maximum gain
0x05	(7:4)	4	0	AGCA	AGC Attack Bandwidth Setting. Default yields 50 Hz raw loop bandwidth.
	(3:0)	4	0	AGCD	AGC Decay Time Setting. Default is decay time = attack time.
0x06	(7)	1	0	AGCV	Enable Digital VGA to increase AGC Range by 12 dB
	(6:4)	3	0	AGCO	AGC Overload Update Setting. Default is slowest update
	(3)	1	0	AGCF	Fast AGC (Minimizes resistance seen between GCP and GCN)
	(2:0)	3	0	AGCR	AGC Enable/Reference Level (Disabled, 3 dB, 6 dB, 9 dB, 12 dB, 15 dB below Clip)
DECIMATION FACTOR					
0x07	(7:5)	3		Unused	
	(4)	1	0	K	Decimation Factor = $60 \times (M + 1)$, if K = 0; $48 \times (M + 1)$, if K = 1
	(3:0)	4	4	M	Default is Decimate-by-300
LO SYNTHESIZER					
0x08	(5:0)	6	0x00	LOR(13:8)	Reference Frequency Divisor (6 MSBs of a 14-Bit Word)
0x09	(7:0)	8	0x38	LOR(7:0)	Reference Frequency Divisor (8 LSBs of a 14-Bit Word) Default (56) Yields 300 kHz from f_{REF} = 16.8 MHz
0x0A	(7:5)	3	0x5	LOA	"A" Counter (Prescaler Control Counter)
	(4:0)	5	0x00	LOB(12:8)	"B" Counter MSBs (5 MSBs of a 13-Bit Word) Default LOA and LOB values yield 300 kHz from 73.35 MHz–2.25 MHz
0x0B	(7:0)	8	0x1D	LOB(7:0)	"B" Counter LSBs (8 LSBs of a 13-Bit Word)
0x0C	(6)	1	0	LOF	Enable Fast Acquire
	(5)	1	0	LOINV	Invert Charge Pump (0 = Source Current to Increase VCO Frequency)
	(4:2)	3	0	LOI	Charge Pump Current in Normal Operation. $I_{PUMP} = (LOI + 1) \times 0.625$ mA
	(1:0)	2	3	LOTM	Manual Control of LO Charge Pump (0 = Off, 1 = Up, 2 = Down, 3 = Normal)
0x0D	(5:0)	4	0x0	LOFA(13:8)	LO Fast Acquire Time Unit (6 MSBs of a 14-Bit Word)
0x0E	(7:0)	8	0x04	LOFA(7:0)	LO Fast Acquire Time Unit (8 LSBs of a 14-Bit Word)

Table I. SPI Address Map (continued)

Address (Hex)	Bit Breakdown	Width	Default Value	Name	Description
CLOCK SYNTHESIZER					
0x10	(5:0)	6	00	CKR(13:8)	Reference Frequency Divisor (6 MSBs of a 14-Bit Word)
0x11	(7:0)	8	0x38	CKR(7:0)	Reference Frequency Divisor (8 LSBs of a 14-Bit Word) Default Yields 300 kHz from f_{REF} =16.8 MHz; Min = 3, Max = 16383.
0x12	(4:0)	5	0x00	CKN(12:8)	Synthesized Frequency Divisor (5 MSBs of a 13-Bit Word)
0x13	(7:0)	8	0x3C	CKN(7:0)	Synthesized Frequency Divisor (8 LSBs of a 13-Bit Word) Default Yields 300 kHz from f_{CLK} = 18 MHz; Min = 3, Max = 8191
0x14	(6) (5) (4:2) (1:0)	1 1 3 2	0 0 0 3	CKF CKINV CKI CKTM	Enable Fast Acquire Invert Charge Pump (0 = Source Current to Increase VCO Frequency) Charge Pump Current in Normal Operation. I_{PUMP} = (CKI + 1) × 0.625 mA Manual Control of CLK Charge Pump (0 = Off, 1 = Up, 2 = Down, 3 = Normal)
0x15	(5:0)	6	0x0	CKFA(13:8)	CK Fast Acquire Time Unit (6 MSBs of a 14-Bit Word)
0x16	(7:0)	8	0x04	CKFA(7:0)	CK Fast Acquire Time Unit (8 LSBs of a 14-Bit Word)
SSI CONTROL					
0x18	(7:0)	8	0x12	SSICRA	SSI Control Register A. See Table III. (Default is FS and CLKOUT Three-Stated)
0x19	(7:0)	8	0x07	SSICRB	SSI Control Register B. See Table III. (16-bit data, maximum drive strength)
0x1A	(3:0)	4	1	SSIORD	Output Rate Divisor. f_{CLKOUT} = f_{CLK}/SSIORD
ADC TUNING					
0x1C	(1) (0)	1 1	0 0	TUNE_LC TUNE_RC	Perform Tuning on the LC Portion of the ADC (Cleared When Done) Perform Tuning on the RC Portion of the ADC (Cleared When Done)
0x1D	(2:0)	3	0	CAPL1(2:0)	Coarse Capacitance Setting for LC Tank (LSB is 25 pF, Differential)
0x1E	(5:0)	6	0x00	CAPL0(5:0)	Fine Capacitance Setting for LC Tank (LSB is 0.4 pF, Differential)
0x1F	(7:0)	8	0x00	CAPR	Capacitance Setting for RC Resonator (64 LSBs of Fixed Capacitance)
TEST REGISTERS AND SPI PORT READ ENABLE					
0x37–0x39	(7:0)	8	0x00	TEST	Factory Test Mode. Do not use.
0x3A	(7:4, 2:0) (3)	7 1	0x0 0	TEST SPIREN	Factory Test Mode. Do not use. Enable Read from SPI Port
0x3B	(7:4, 2:0) (3)	7 1	0x0 0	TEST TRI	Factory Test Mode. Do not use. Three-state DOUTB
0x3C–0x3E	(7:0)	1	0x00	TEST	Factory Test Mode. Do not use.
0x3F	(7:0)	8	Subject to Change	ID	Revision ID (Read-Only); A write of 0x99 to this register is equivalent to a power-on reset.

SERIAL PORT INTERFACE (SPI)

The serial port of the AD9874 has 3-wire or 4-wire SPI capability, allowing read/write access to all registers that configure the device's internal parameters. The default 3-wire serial communication port consists of a clock (PC), peripheral enable (PE), and a bidirectional data (PD) signal. The inputs to PC, PE, and PD contain a Schmitt trigger with a nominal hysteresis of 0.4 V centered about the digital interface supply (i.e., VDDH/2).

A 4-wire SPI interface can be enabled by setting the MSB of the SSICRB register (Reg. 0x19, Bit 7) resulting in the output data also appearing on the DOUTB Pin. Note, since the default power-up state sets DOUTB low, bus contention is possible for systems sharing the SPI output line. To avoid any bus contention, the DOUTB Pin can be three-stated by setting the fourth control bit in the three-state bit (Reg 0x3B, Bit 3). This bit can then be toggled to gain access to the shared SPI output line.

An 8-bit instruction header must accompany each read and write SPI operation. Only the write operation supports an auto-increment mode allowing the entire chip to be configured in a single write operation. The instruction header is shown in Table I. It includes a read/not-write indicator bit, 6 address bits, and a Don't Care bit. The data bits immediately follow the instruction header for both read and write operations. Note, address and data are always given MSB first.

Table II. Instruction Header Information

MSB							LSB
I7	I6	I5	I4	I3	I2	I1	I0
R/W	A5	A4	A3	A2	A1	A0	X

Figure 1a illustrates the timing requirements for a write operation to the SPI port. After the peripheral enable (PE) signal goes low, data (PD) pertaining to the instruction header is read on the rising edges of the clock (PC). To initiate a write operation, the read/not-write bit is set low. After the instruction header is read, the eight data bits pertaining to the specified register are shifted into the data pin (PD) on the rising edge of the next eight clock cycles. PE stays low during the operation and goes high at the end of the transfer. If PE rises before the eight clock cycles have passed, the operation is aborted.

If PE stays low for an additional eight clock cycles, the destination address is incremented and another eight bits of data are shifted in. Again, should PE rise early, the current byte is ignored. By using this implicit addressing mode, the entire chip can be configured with a single write operation. Registers identified as being subject to frequent updates, namely those associated with power control and AGC operation, have been assigned adjacent addresses to minimize the time required to update them. Note, multibyte registers are "big-endian" (the most significant byte has the lower address) and are updated when a write to the least significant byte occurs.

Figure 1b illustrates the timing for a read operation to the SPI port. Although the AD9874 does not require read access for proper operation, it is often useful in the product development phase or for system authentication. Note, the readback enable bit (Register 0x3A, Bit 3) must be set for a read operation with a 3-wire SPI interface. After the peripheral enable (PE) signal goes low, data (PD) pertaining to the instruction header is read on the rising edges of the clock (PC). A read operation occurs if the read/not-write indicator is set high. After the address bits of the instruction header are read, the eight data bits pertaining to the specified register are shifted out of the data pin (PD) on the falling edges of the next eight clock cycles. If the 4-wire SPI interface is enabled, the eight data bits will also appear on the DOUTB Pin with the same timing relationship as those appearing at PD. After the last data bit is shifted out, the user should return PE high, causing PD to become three-stated and return to its normal status as an input pin. Since the auto-increment mode is not supported for read operations, an instruction header is required for each register read operation and PE must return high before initiating the next read operation.

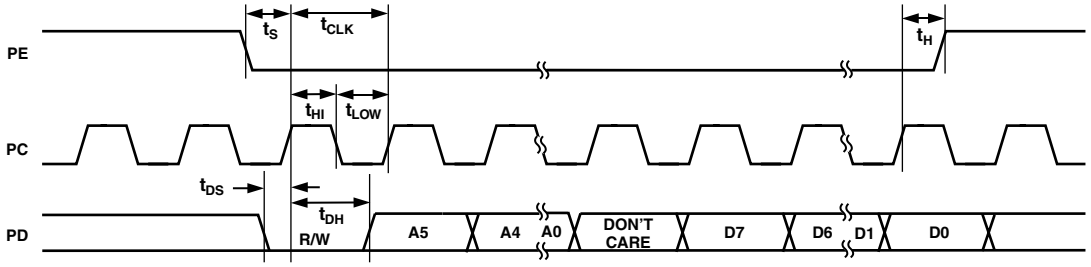


Figure 1a. SPI Write Operation Timing

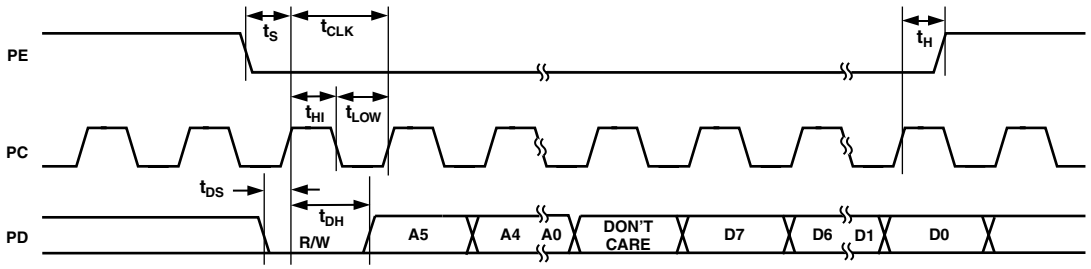


Figure 1b. SPI Read Operation Timing

SYNCHRONOUS SERIAL INTERFACE (SSI)

The AD9874 provides a high degree of programmability of its SSI output data format, control signals, and timing parameters to accommodate various digital interfaces. In a 3-wire digital interface, the AD9874 provides a frame sync signal (FS), a clock output (CLKOUT), and a serial data stream (DOUTA) signal to the host device. In a 2-wire interface, the frame sync information is embedded into the data stream, thus only a CLKOUT and DOUTA output signal are provided to the host device. The SSI control registers are SSICRA, SSICRB, and SSIORD. Table III shows the different bit fields associated with these registers.

The primary output of the AD9874 is the converted I and Q demodulated signal available from the SSI port as a serial bit stream contained within a frame. The output frame rate is equal to the modulator clock frequency (f_{CLK}) divided by the digital filter's decimation factor that is programmed in the Decimator Register (0x07). The bit stream consists of an I word followed by a Q word, where each word is either 24 bits or 16 bits long and is given MSB first in two's complement form. Two optional bytes may also be included within the SSI frame following the Q word. One byte contains the AGC attenuation and the other byte contains both a count of modulator reset events and an estimate of the received signal amplitude (relative to full scale of the AD9874's ADC). Figure 2 illustrates the structure of the SSI data frames in a number of SSI modes.

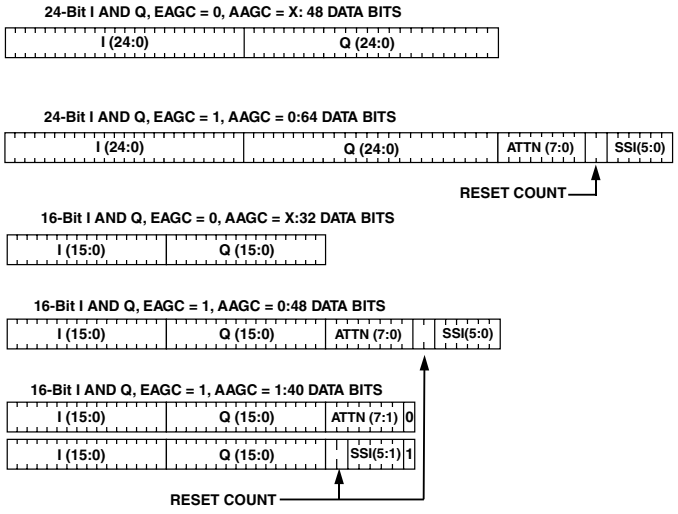


Figure 2. SSI Frame Structure

The two optional bytes are output if the EAGC bit of SSICRA is set. The first byte contains the 8-bit attenuation setting (0 = no attenuation, 255 = 24 dB of attenuation), while the second byte contains a 2-bit reset field and 6-bit received signal strength signal field. The reset field contains the number of modulator reset events since the last report, saturating at 3. The received signal strength (RSSI) field is a linear estimate of the signal strength at the output of the first decimation stage; 60 corresponds to a full-scale signal.

The two optional bytes follow the I and Q data as a 16-bit word providing that the AAGC bit of SSICRA is not set. If the AAGC bit is set, the two bytes follow the I and Q data in an alternating fashion. In this alternate AGC data mode, the LSB of the byte containing the AGC attenuation is a 0, while the LSB of the byte containing reset and RSSI information is always a 1.

In a 2-wire interface, the embedded frame sync bit (EFS) within the SSICRA Register is set to 1. In this mode, the framing information is embedded in the data stream with each eight bits of data surrounded by a start bit (low) and a stop bit (high), and each frame ends with at least 10 high bits. FS remains either low or three-stated (default) depending on the state of the SFST bit. Other control bits can be used to invert the frame sync (SFSI), to delay the frame sync pulse by one clock period (SLFS), to invert the clock (SCKI), or to three-state the clock (SCKT). Note that if EFS is set, SLFS is a don't care.

Table III. SSI Control Registers

Name	Width	Default	Description
SSICRA (ADDR = 0x18)			AAGC | EAGC | EFS | SFST | SFSI | SLFS | SCKT | SCKI
AAGC	1	0	Alternate AGC Data Bytes
EAGC	1	0	Embed AGC Data
EFS	1	0	Embed Frame Sync
SFST	1	1	Three-State Frame Sync
SFSI	1	0	Invert Frame Sync
SLFS	1	0	Late Frame Sync (1 = Late, 0 = Early)
SCKT	1	1	Three-State CLKOUT
SCKI	1	0	Invert CLKOUT
SSICRB (ADDR = 0x19)			4_SPI | | | | DW | DS_2 | DS_1 | DS_0
4_SPI	1	0	Enable 4-Wire SPI Interface for SPI Read operation via DOUTB
DW	1	0	I/Q data-word width (0 = 16 bit, 1 bit–24 bit) Automatically 16-bit when the AGCV=1
DS	3	7	FS, CLKOUT, and DOUT Drive Strength
SSIORD (ADDR = 0x1A)			| | | | DIV_3 | DIV_2 | DIV_1 | DIV_0
DIV	4	1	Output Bit Rate Divisor $f_{CLKOUT} = f_{CLK}$/SSIORD

The SSIORD Register controls the output bit rate (f_{CLKOUT}) of the serial bit stream. f_{CLKOUT} can be set to equal the modulator clock frequency (f_{CLK}) or an integer fraction of it. It is equal to f_{CLK} divided by the contents of the SSIORD Register. Note, f_{CLKOUT} should be chosen such that it does not introduce harmful spurs within the pass band of the target signal. Users must verify that the output bit rate is sufficient to accommodate the required number of bits per frame for a selected word size and decimation factor. Idle (high) bits are used to fill out each frame.

Table IV. Number of Bits per Frame for Different SSICR Settings

DW	EAGC	EFS	AAGC	Number of Bits per Frame
0 (16-bit)	0	0	NA	32
	0	1	NA	49*
	1	0	0	48
	1	0	1	40
	1	1	0	69*
	1	1	1	59*
1 (24-bit)	0	0	NA	48
	0	1	NA	69*
	1	0	0	64
	1	0	1	56
	1	1	0	89*
	1	1	1	79*

*The number of bits per frame with embedded frame sync (EFS = 1) assume at least 10 idle bits are desired.

The *maximum* SSIORD setting can be determined by the following equation:

$$SSIORD \leq TRUNC\{(Dec.\,Factor)\,/\,(\#\,of\,Bits\,per\,Frame)\} \quad (1)$$

where *TRUNC* is the truncated integer value.

Table IV lists the number of bits within a frame for 16-bit and 24-bit output data formats for all of the different SSICR settings. The decimation factor is determined by the contents of Register 0x07.

An example helps illustrate how the maximum SSIORD setting is determined. Suppose a user selects a decimation factor of 600 (Register 0x07, K = 0, M = 9) and prefers a 3-wire interface with a dedicated frame sync (EFS = 0) containing 24-bit data (DW = 1) with nonalternating embedded AGC data included (EAGC = 1, AAGC = 0). Referring to Table IV, each frame will consist of 64 data bits. Using Equation 1, the maximum SSIORD setting is 9 (= *TRUNC*(600/64)). Thus, the user can select any SSIORD setting between 1 and 9.

Figure 3a illustrates the output timing of the SSI port for several SSI control register settings with 16-bit I/Q data, while Figure 3b shows the associated timing parameters. Note, the same timing relationship holds for 24-bit I/Q data, with the exception that I and Q word lengths now become 24 bits. In the default mode of the operation, data is shifted out on rising edges of CLKOUT after a pulse equal to a clock period is output from the Frame Sync (FS) Pin. As described above, the output data consists of a 16- or 24-bit I sample followed by a 16- or 24-bit Q sample, plus two optional bytes containing AGC and status information.

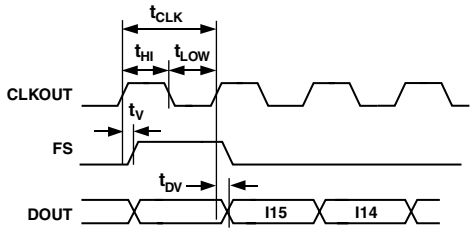


*Figure 3b. Timing Parameters for SSI Timing**

*Timing parameters also apply to inverted CLKOUT or FS modes with t_{DV} relative to the falling edge of the CLK and/or FS.

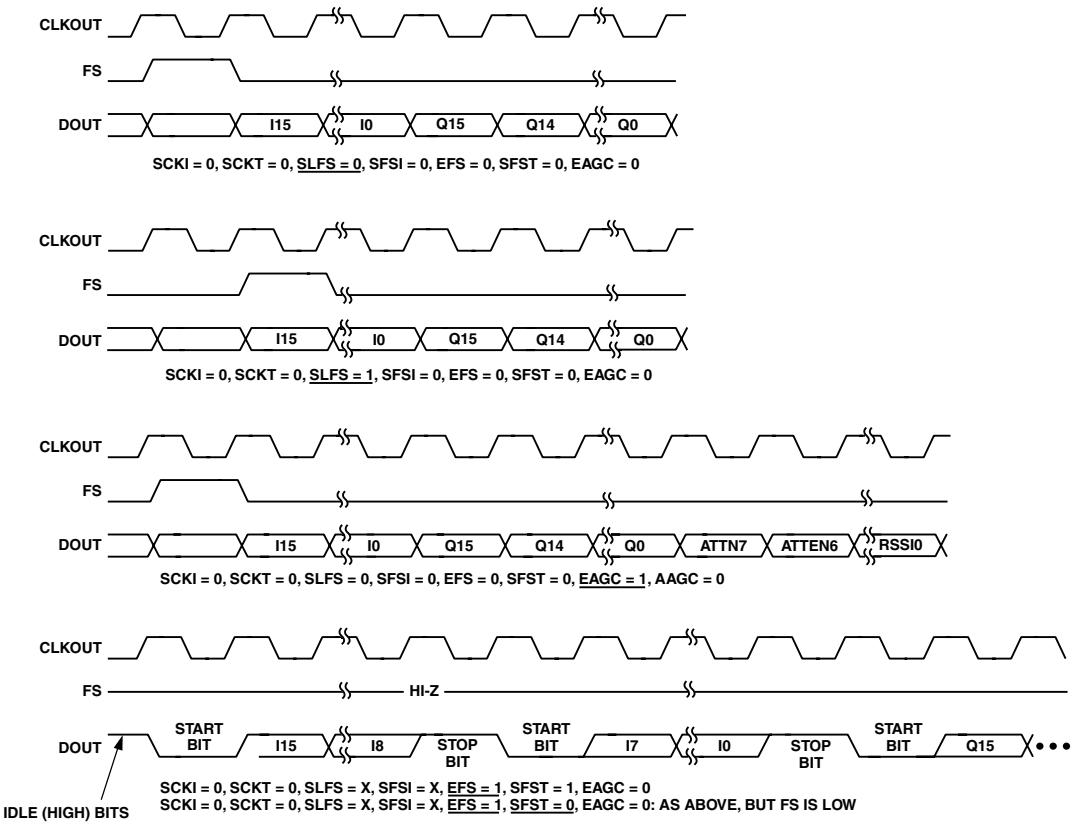


Figure 3a. SSI Timing for Several SSICRA Settings with 16-Bit I/Q Data

The AD9874 also provides the means for controlling the switching characteristics of the digital output signals via the DS (drive strength) field of the SSICRB. This feature is useful in limiting switching transients and noise from the digital output that may ultimately couple back into the analog signal path, potentially degrading the AD9874's sensitivity performance. Figures 3c and 3d show how the NF can vary as a function of the SSI setting for an IF frequency of 109.65 MHz. The following two observations can be made from these figures:

- The NF becomes more sensitive to the SSI output drive strength level at higher signal bandwidth settings.
- The NF is dependent on the number of bits within an SSI frame, becoming more sensitive to the SSI output drive strength level as the number of bits is increased. As a result, one should select the lowest possible SSI drive strength setting that still meets the SSI timing requirements.

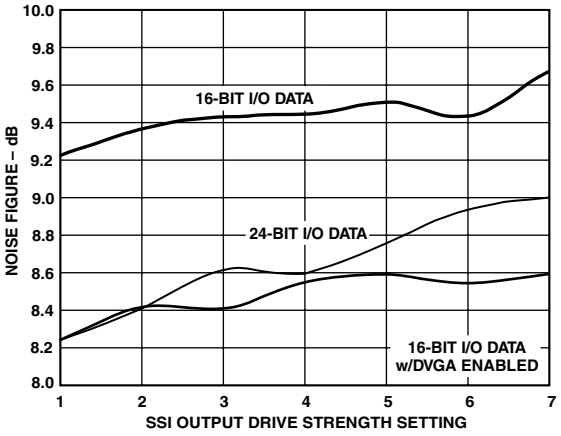


Figure 3c. NF vs. SSI Output Drive Strength (VDDx = 3.0 V, f_{CLK} = 18 MSPS, BW = 10 kHz)

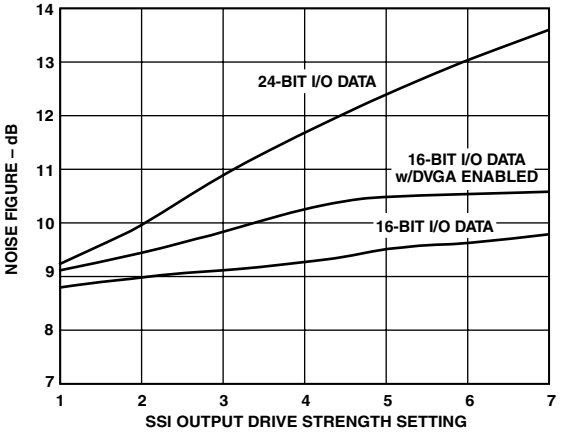


Figure 3d. NF vs. SSI Output Drive Strength (VDDx = 3.0 V, f_{CLK} = 18 MSPS, BW = 75 kHz)

Table V lists the typical output rise/fall times as a function of DS for a 10 pF load. Rise/fall times for other capacitor loads can be determined by multiplying the typical values presented in Table V by a scaling factor equal to the desired capacitive load divided by 10 pF.

Table V. Typical Rise/Fall times (±25 %) with a 10 pF Capacitive Load for Each DS Setting

DS	typ (ns)
0	13.5
1	7.2
2	5.0
3	3.7
4	3.2
5	2.8
6	2.3
7	2.0

Synchronization

Applications, such as receiver diversity, employing more than one AD9874 device may desire synchronization of the digital output data. SYNCB can be used for this purpose and applied upon system initialization. It is an active-low signal that clears the clock counters in both the decimation filter and the SSI port. The counters in the clock synthesizers are not reset, since it is presumed that the CLK signals of multiple chips would be connected together. SYNCB also clears the registers in the decimation filter and resets the modulator. As a result, valid data representative of the input signal will be available once the digital filters have been flushed.

Figure 4a shows the timing relationship between SYNCB and the SSI port's CLKOUT and FS signals. SYNCB is an asynchronous active-low signal that must remain low for at least half an input clock period (i.e., $1/(2 \times f_{CLK})$). CLKOUT returns high while FS remains low upon SYNCB going low. CLKOUT will become active within 1 to 2 output clock periods upon SYNCB returning high. FS will reappear several output clock cycles later, depending on the digital filter's decimation factor and the SSIORD setting. To verify proper synchronization, the FS signals of the multiple AD9874 devices should be monitored.

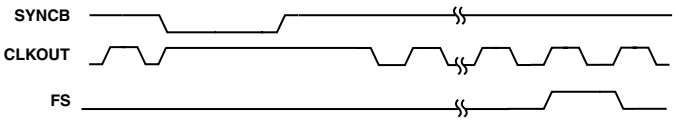


Figure 4a. SYNCB Timing

INTERFACING TO DSPs

The AD9874 connects directly to an Analog Devices programmable digital signal processor (DSP). Figure 4b illustrates an example with the Blackfin® series of ADSP-2153x processors. The Blackfin DSP series is a family of 16-bit products optimized for telecommunications applications with its dynamic power management feature making it well suited for portable radio products. The code compatible family members share the fundamental core attributes of high performance, low power consumption, and the ease-of-use advantages of microcontroller instruction set.

*Blackfin is a registered trademark of Analog Devices, Inc.

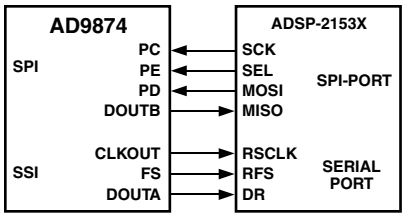


Figure 4b. Example of AD9874 and ADSP-2153x Interface

As shown in Figure 4b, AD9874's synchronous serial interface (SSI) links the receive data stream to the DSP's Serial Port (SPORT). For AD9874 set-up and register programming, the device connects directly to ADSP-2153x's SPI-PORT. Dedicated select lines (SEL) allow the ADSP-2153x to program and read back registers of multiple devices using only one SPI port. The DSP driver code pertaining to this interface is available on the AD9874 web page (http://products.analog.com/products/info.asp?product=AD9874).

POWER CONTROL

To allow power consumption to be minimized, the AD9874 possesses numerous SPI-programmable power-down and bias control bits. The AD9874 powers up with all of its functional blocks placed into a standby state (i.e., STBY Register default is 0xFF). Each major block may then be powered up by writing a 0 to the appropriate bit of the STBY Register. This scheme provides the greatest flexibility for configuring the IC to a specific application as well as for tailoring the IC's power-down and wake-up characteristics. Table VI summarizes the function of each of the STBY bits. Note, when all the blocks are in standby, the master reference circuit is also put into standby and thus the current is reduced by a further 0.4 mA.

Table VI. Standby Control Bits

STBY Bit	Effect	Current Reduction (mA)[1]	Wake-Up Time (ms)
7:REF	Voltage Reference OFF; all biasing shut down.	0.6	<0.1 (C_{REF} = 4.7 nF)
6:LO	LO Synthesizer OFF, IOUTL three-state.	1.2	Note 2
5:CKO	Clock Oscillator OFF	1.1	Note 2
4:CK	Clock Synthesizer OFF, IOUTC three-state. Clock buffer OFF if ADC is OFF.	1.3	Note 2
3:GC	Gain Control DAC OFF. GCP and GCN three-state.	0.2	Depends on C_{GC}
2:LNAMX	LNA and Mixer OFF. CXVM, CXVL, and CXIF three-state.	8.2	<2.2
1:Unused			
0:ADC	ADC OFF; Clock Buffer OFF if CLK synthesizer OFF; VCM three-state; Clock to the digital filter halted; Digital outputs static.	9.2	<0.1

NOTES
[1]When all blocks are in standby, the master reference circuit is also put into standby and thus the current is reduced by a further 0.4 mA.
[2]Wake-up time is dependent on programming and/or external components.

The AD9874 also allows control over the bias current in the LNA, mixer, and clock oscillator. The effects on current consumption and system performance are described in the section dealing with the affected block.

LO Synthesizer

The LO Synthesizer shown in Figure 5 is a fully programmable PLL capable of 6.25 kHz resolution at input frequencies up to 300 MHz and reference clocks of up to 25 MHz. It consists of a low noise digital phase-frequency detector (PFD), a variable output current charge pump (CP), a 14-bit reference divider, programmable A and B counters, and a dual-modulus 8/9 prescaler. The A (3-bit) and B (13-bit) counters, in conjunction with the dual 8/9 modulus prescaler, implement an N divider with N = 8 × B + A. In addition, the 14-bit reference counter (R Counter) allows selectable input reference frequencies, f_{REF}, at the PFD input. A complete PLL (phase-locked loop) can be implemented if the synthesizer is used with an external loop filter and VCO (voltage controlled oscillator).

The A, B, and R counters can be programmed via the following registers: LOA, LOB, and LOR. The charge pump output current is programmable via the LOI Register from 0.625 mA to 5.0 mA using the following equation:

$$IPUMP = (LOI + 1) \times 0.625\ mA \quad (2)$$

An on-chip fast acquire function (enabled by the LOF bit) automatically increases the output current for faster settling during channel changes. The synthesizer may also be disabled using the LO standby bit located in the STBY Register.

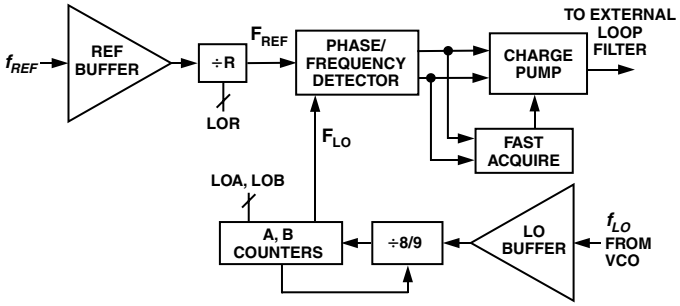


Figure 5. LO Synthesizer

The LO (and CLK) synthesizer works in the following manner. The externally supplied reference frequency, f_{REF}, is buffered and divided by the value held in the R counter. The internal f_{REF} is then compared to a divided version of the VCO frequency, f_{LO}. The phase/frequency detector provides UP and DOWN pulses whose widths vary depending upon the difference in phase and frequency of its two input signals. The UP/DOWN pulses control the charge pump making current available to charge the external low-pass loop filter when there is a discrepancy between the inputs of the PFD. The output of the low-pass filter feeds an external VCO whose output frequency, f_{LO}, is driven such that its divided down version, f_{LO}, matches that of f_{REF}, thus closing the feedback loop.

The synthesized frequency is related to the reference frequency and the LO Register contents as follows:

$$f_{LO} = (8 \times LOB + LOA) / LOR \times f_{REF} \quad (3)$$

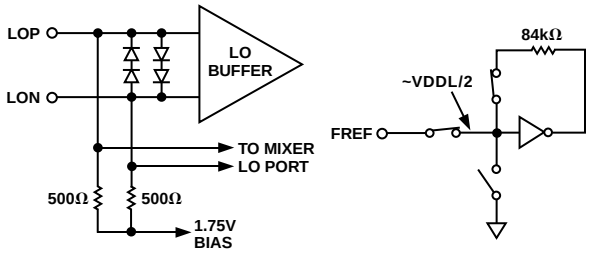
Note, the minimum allowable value in the *LOB* Register is 3 and its value must always be greater than that loaded into *LOA*.

An example may help illustrate how the values of *LOA*, *LOB*, and *LOR* can be selected. Consider an application employing a 13 MHz crystal oscillator (i.e., f_{REF} = 13 MHz) with the requirement that f_{REF} = 100 kHz and f_{LO} = 143 MHz (i.e., high side injection with f_{IF} = 140.75 MHz and f_{CLK} = 18 MSPS). LOR is selected to be 130 such that f_{REF} = 100 kHz. The N-divider factor is 1430, which can be realized by selecting LOB = 178 and LOA = 6.

The stability, phase noise, spur performance, and transient response of the AD9874's LO (and CLK) synthesizers are determined by the external loop filter, the VCO, the N-divide factor, and the reference frequency, FREF. A good overview of the theory and practical implementation of PLL synthesizers (featured as a three-part series in *Analog Dialogue*) can be found at:

- www.analog.com/library/analogDialogue/archives/33-03/phase/index.html
- www.analog.com/library/analogDialogue/archives/33-05/phase_locked/index.html
- www.analog.com/library/analogDialogue/archives/33-07/phase3/index.html

Also, a free software copy of the Analog Devices ADIsimPLL, a PLL synthesizer simulation tool, is available at www.analog.com/technology/RFComms/rfif/ADIsimPLL.html. Note, the ADF4112 model can be used as a close approximation to the AD9874's LO synthesizer when using this software tool.



NOTES
1. ESD DIODE STRUCTURES OMITTED FOR CLARITY.
2. FREF STBY SWITCHES SHOWN WITH LO SYNTHESIZER ON.

Figure 6. Equivalent Input of LO and REF Buffers

Figure 6 shows the equivalent input structures of the synthesizers' LO and REF buffers (excluding the ESD structures). The LO input is fed to the LO synthesizer's buffer as well as the AD9874's mixer's LO port. Both inputs are self-biasing and thus tolerate ac-coupled inputs. The LO input can be driven with a single-ended or differential signal. Single-ended dc-coupled inputs should ensure sufficient signal swing above and below the common-mode bias of the LO and REF buffers (i.e., 1.75 V and VDDL/2). Note, the FREF input is slew rate dependent and must be driven with input signals exceeding 6.4 V/msec to ensure synthesizer operation.

Fast Acquire Mode

The fast acquire circuit attempts to boost the output current when the phase difference between the divided-down LO (i.e., f_{LO}) and the divided-down reference frequency (i.e., f_{REF}) exceeds the threshold determined by the LOFA Register. The LOFA Register specifies a divisor for the f_{REF} signal that determines the period (T) of this divided-down clock. This period defines the time interval used in the fast acquire algorithm to control the charge pump current.

Assume for the moment that the nominal charge pump current is at its lowest setting (i.e., LOI = 0) and denote this minimum current by I_0. When the output pulse from the phase comparator exceeds T, the output current for the next pulse is 2 I_0. When the pulse is wider than 2 T, the output current for the next pulse is 3 I_0, and so forth, up to eight times the minimum output current. If the nominal charge pump current is more than the minimum value (i.e., LOI > 0), the preceding rule is only applied if it results in an increase in the instantaneous charge pump current. If the charge pump current is set to its lowest value (LOI = 0) and the fast acquire circuit is enabled, the instantaneous charge pump current will never fall below 2 I_0 when the pulsewidth is less than T. Thus, the charge pump current when fast acquire is enabled is given by:

$$I_{PUMP-FA} = I_0 \times \{1 + \max(1, LOI, Pulse\_Width/T)\} \quad (4)$$

The recommended setting for LOFA is LOR/16. Choosing a larger value for LOFA will increase *T*. Thus, for a given phase difference between the LO input and the f_{REF} input, the instantaneous charge pump current will be less than that available for a LOFA value of LOR/16. Similarly, a smaller value for LOFA will decrease *T*, making more current available for the same phase difference. In other words, a smaller value of LOFA will enable the synthesizer to settle faster in response to a frequency hop than will a large LOFA value. Care must be taken to choose a value for LOFA that is large enough (values greater than 4 recommended) to prevent the loop from oscillating back and forth in response to a frequency hop.

Table VII. SPI Registers Associated with LO Synthesizer

Address (Hex)	Bit Breakdown	Width	Default Value	Name
0x00	(7:0)	1	0xFF	STBY
0x08	(5:0)	6	0x00	LOR(13:8)
0x09	(7:0)	8	0x38	LOR(7:0)
0x0A	(7:5) (4:0)	3 5	0x5 0x00	LOA LOB(12:8)
0x0B	(7:0)	8	0x1D	LOB(7:0)
0x0C	(6) (5) (4:2) (1:0)	1 1 3 2	0 0 0 0	LOF LOINV LOI LOTM
0x0D	(3:0)	4	0x0	LOFA(13:8)
0x0E	(7:0)	8	0x04	LOFA(7:0)

CLOCK SYNTHESIZER

The clock synthesizer is a fully programmable integer-*N* PLL capable of 2.2 kHz resolution at clock input frequencies up to 18 MHz and reference frequencies up to 25 MHz. It is similar to the LO synthesizer described previously in Figure 4 with the following exceptions:

- It does not include an 8/9 prescaler nor an A counter.
- It includes a negative-resistance core that when used in conjunction with an external LC tank and varactor, serves as the VCO.

The 14-bit reference counter and 13-bit N-divider counter can be programmed via the following registers: CKR and CKN. The clock frequency, f_{CLK}, is related to the reference frequency by the following equation:

$$f_{CLK} = (CKN/CKR) \times f_{REF} \quad (5)$$

The charge pump current is programmable via the CKI register from 0.625 mA to 5.0 mA using the following equation:

$$I_{PUMP} = (CKI + 1) \times 0.625\ mA \quad (6)$$

The fast acquire subcircuit of the charge pump is controlled by the CKFA Register in the same manner as the LO synthesizer is controlled by the LOFA Register. An on-chip lock detect function (enabled by the CKF bit) automatically increases the output current for faster settling during channel changes. The synthesizer may also be disabled using the CK standby bit located in the STBY Register.

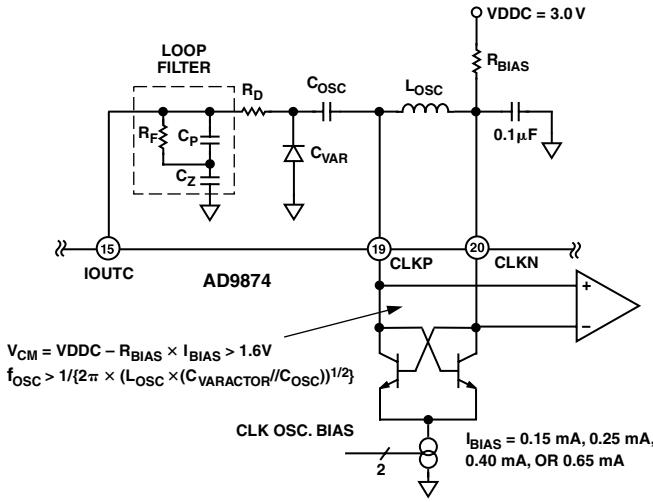


Figure 7a. External Loop Filter, Varactor, and LC Tank Are Required to Realize a Complete Clock Synthesizer

The AD9874 clock synthesizer circuitry includes a negative-resistance core so that only an external LC tank circuit with a varactor is needed to realize a voltage controlled clock oscillator (VCO). Figure 7a shows the external components required to complete the clock synthesizer along with the equivalent input circuitry of the CLK input. The resonant frequency of the VCO is approximately determined by L_{OSC} and the series equivalent capacitance of C_{OSC} and C_{VAR}. As a result, L_{OSC}, C_{OSC}, and C_{VAR} should be selected to provide a sufficient tuning range to ensure proper locking of the clock synthesizer.

The bias, I_{BIAS}, of the negative-resistance core has four programmable settings. Lower equivalent Q of the LC tank circuit may require a higher bias setting of the negative-resistance core to ensure proper oscillation. R_{BIAS} should be selected so the common-mode voltage at CLKP and CLKN is approximately 1.6 V. The synthesizer may be disabled via the CK standby bit to allow the user to employ an external synthesizer and/or VCO in place of those resident on the IC. Note, if an external CLK source or VCO is used, the clock oscillator must be disabled via the CKO standby bit.

The phase noise performance of the clock synthesizer is dependent on several factors, including the CLK oscillator I_{BIAS} setting, the charge pump setting, the loop filter component values, and the internal f_{REF} setting. Figures 7b and 7c show how the measured phase noise attributed to the clock synthesizer varies (relative to an external f_{CLK}) as a function of the I_{BIAS} setting and charge pump setting for a –31 dBm IFIN signal at 73.35 MHz with an external LO signal at 71.1 MHz. Figure 7b shows that the optimum phase noise is achieved with the highest I_{BIAS} (CKO) setting, while Figure 7c shows that the higher charge pump values provide the optimum performance for the given loop filter configuration. The AD9874 clock synthesizer and oscillator were set up to provide a f_{CLK} of 18 MHz from an external f_{REF} of 16.8 MHz. The following external component values were selected for the synthesizer: R_F = 390 Ω, R_D = 2 kΩ, C_Z = 0.68 µF, C_P = 0.1 µF, C_{OSC} = 91 pF, L_{OSC} = 1.2 µH, and C_{VAR} = Toshiba 1SV228 Varactor.

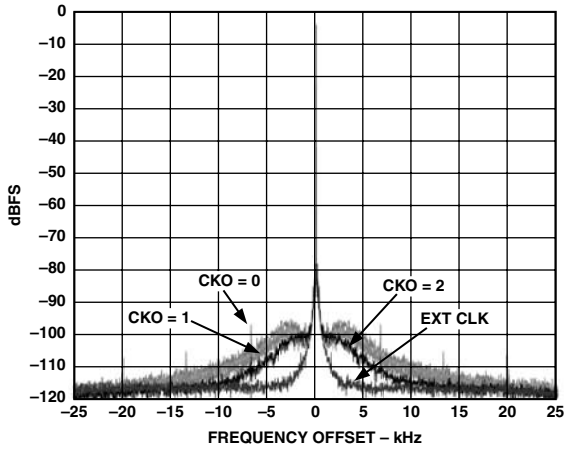


Figure 7b. CLK Phase Noise vs. I_{BIAS} Setting (CKO) (CLK SYN Settings: CKI = 7, CLR = 56, and CLN = 60 with f_{REF} = 100kHz)

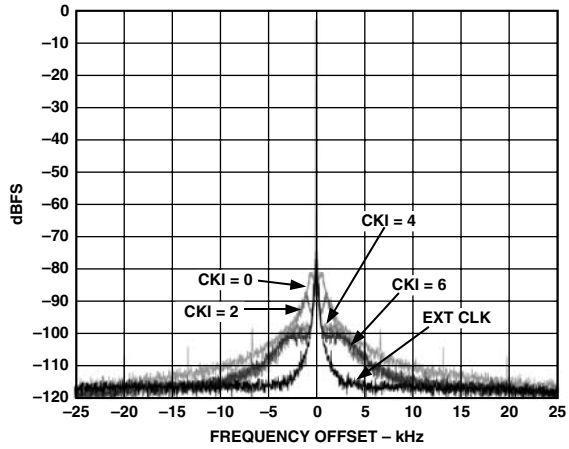


Figure 7c. CLK Phase Noise vs. Charge Pump Setting Bias (CLK SYN Settings: CKO Bias = 3, CKR = 56, and CKN = 60 with f_{REF} = 100kHz)

Table VIII. SPI Registers Associated with CLK Synthesizer

Address (Hex)	Bit Breakdown	Width	Default Value	Name
0x00	(7:0)	8	0xFF	STBY
0x01	(3:2)	2	0	CKOB
0x10	(5:0)	6	00	CKR(13:8)
0x11	(7:0)	8	0x38	CKR(7:0)
0x12	(4:0)	5	0x00	CKN(12:8)
0x13	(7:0)	8	0x3C	CKN(7:0)
0x14	(6) (5) (4:2) (1:0)	1 1 3 1	0 0 0 0	CKF CKINV CKI CKTM
0x15	(3:0)	4	0x0	CKFA(13:8)
0x16	(7:0)	8	0x04	CKFA(7:0)

IF LNA/MIXER

The AD9874 contains a single-ended LNA followed by a Gilbert-type active mixer, shown in Figure 8 with the required external components. The LNA uses negative shunt feedback to set its input impedance at the IFIN Pin, thus making it dependent on the LNA bias setting and input frequency. It can be modeled as approximately 370 Ω//1.4 pF (±20%) for the higher bias settings below 100 MHz. Figures 9a and 9b show the equivalent input impedance versus frequency characteristics of the AD9874 with all the LNA bias settings. The increase in shunt resistance versus frequency can be attributed to the reduction in bandwidth, thus the amount of negative feedback of the LNA. Note, the input signal into IFIN should be ac-coupled via a 10 nF capacitor since the LNA input is self-biasing.

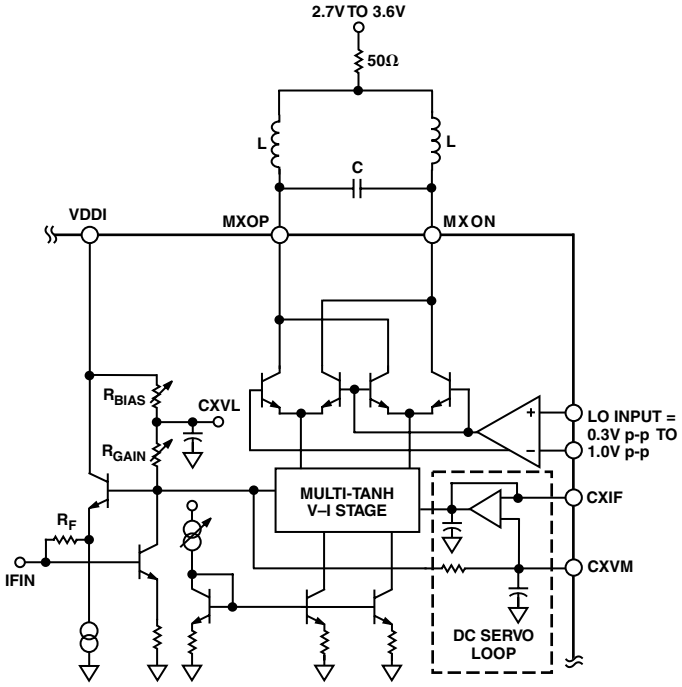


Figure 8. Simplified Schematic of AD9874's LNA/Mixer

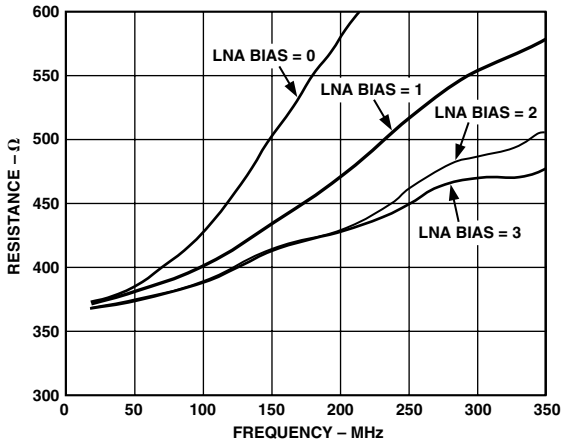


Figure 9a. The Shunt Input Resistance vs. the Frequency of the AD9874's IF1 Input

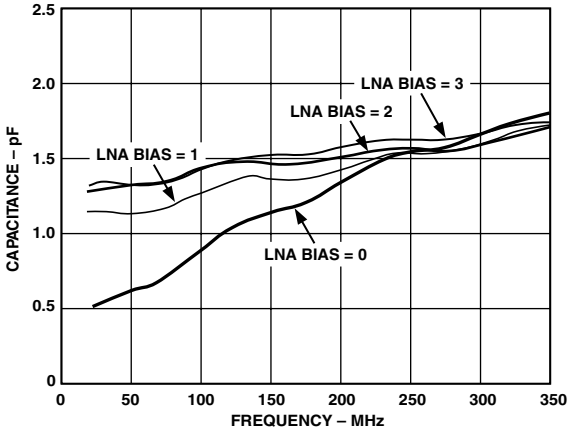


Figure 9b. The Shunt Capacitance vs. the Frequency of the AD9874's IF1 Input

The mixer's differential LO port is driven by the LO buffer stage shown in Figure 6 that can be driven single-ended or differential. Since it is self-biasing, the LO signal level can be ac-coupled and range from 0.3 V p-p to 1.0 V p-p with negligible effect on performance. The mixer's open-collector outputs, MXOP and MXON, drive an external resonant tank consisting of a differential LC network tuned to the IF of the band-pass Σ-Δ ADC (i.e., $f_{IF2\_ADC} = f_{CLK}/8$). The two inductors provide a dc bias path for the mixer core via a series resistor of 50 Ω, which is included to dampen the common-mode response. The mixer's output *must* be ac-coupled to the input of the band-pass Σ-Δ ADC, IF2P and IF2N, via two 100 pF capacitors to ensure proper tuning of the LC center frequency.

The external differential LC tank forms the resonant element for the first resonator of the band-pass Σ-Δ modulator, and so must be tuned to the $f_{CLK}/8$ center frequency of the modulator. The inductors should be chosen such that their impedance at $f_{CLK}/8$ is about 140 Ω (i.e., $L = 180/f_{CLK}$). An accuracy of 20% is considered to be adequate. For example, at f_{CLK} = 18 MHz, L = 10 µH is a good choice. Once the inductors have been selected, the required tank capacitance may be calculated using the relation $f_{CLK}/8 = 1/\{2 \times \pi \times (2L \times C)^{1/2}\}$.

For example, at f_{CLK} = 18 MHz and L = 10 µH, a capacitance of 250 pF is needed. However, in order to accommodate an inductor tolerance of ±10%, the tank capacitance must be adjustable from 227 pF to 278 pF. Selecting an external capacitor of 180 pF ensures that even with a 10% tolerance and stray capacitances as high as 30 pF, the total capacitance will be less than the minimum value needed by the tank. Extra capacitance is supplied by the AD9874's on-chip programmable capacitor array. Since the programming range of the capacitor array is at least 160 pF, the AD9874 has plenty of range to make up for the tolerances of low cost external components. Note, if f_{CLK} is increased by a factor of 1.44 MHz to 26 MHz so that $f_{CLK}/8$ becomes 3.25 MHz, reducing L and C by approximately the same factor (i.e., L = 6.9 µH and C = 120 pF), the above stated requirements are satisfied.

The selection of the inductors is an important consideration in realizing the full linearity performance of the AD9874. This is especially the case when operating the LNA and mixer at maximum bias and low clock frequency. Figure 10 shows how the two-tone input-referred IMD versus the input level performance at an IF of 109 MHz and f_{CLK} of 18 MHz varies between Toko's FSLM series and Coilcraft's 1812CS series inductors. The graph also shows the extrapolated point of intersection used to determine the IIP3 performance. Note, the Coilcraft inductor provides a 7 dB–8 dB improvement in performance and closely approximates the 3:1 slope associated with a third order linearity compared to the 2.65:1 slope associated with the Toko inductor. The Coilcraft 1008CS series showed similar performance to the 1812CS series. It is worth noting that the difference in IMD performance between these two inductor families with an f_{CLK} of 26 MHz is insignificant.

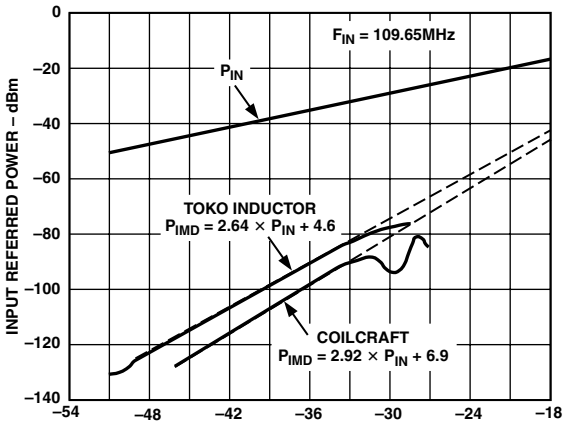


Figure 10. IMD Performance between Different Inductors with LNA and Mixer at Full Bias and f_{CLK} of 18 MHz

Both the LNA and mixer have four programmable bias settings so that current consumption can be minimized for a given application. Figures 11a, 11b, and 11c show how the LNA and mixer's noise figure (NF), linearity (IIP3), IF clip point, current consumption, and frequency response are all affected for a given LNA/mixer bias setting. The measurements were taken at an IF = 73.35 MHz and LO = 71.1 MHz with supplies set to 3 V.

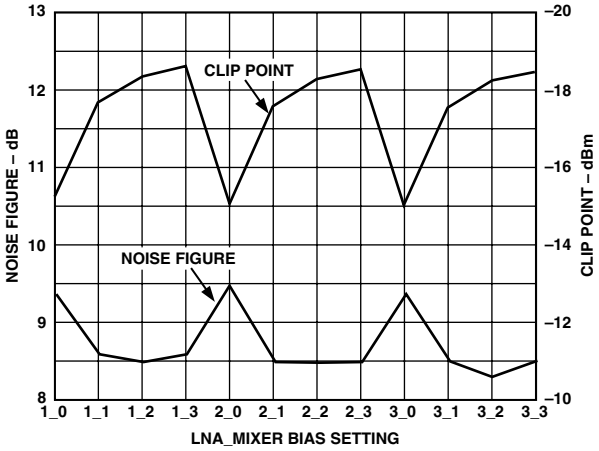


Figure 11a. LNA/Mixer Noise Figure and Conversion Gain vs. Bias Setting

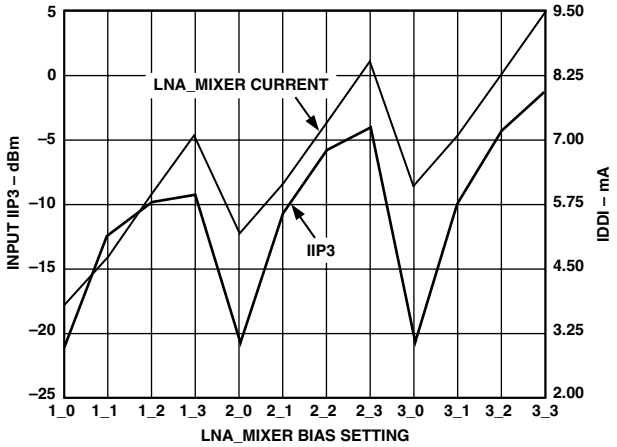


Figure 11b. LNA/Mixer IIP3 and Current Consumption vs. Bias Setting

Based on these characterization curves, a LNA/mixer bias setting of 3_3 is suitable for most applications since it will provide the greatest dynamic range in the presence of multiple unfiltered interferers. However, portable radio applications demanding the lowest possible power may benefit by changing the LNA/mixer bias setting based on the received signal strength power (i.e., RSSI) available from the SSI output data. For instance, selecting an LNA_Mixer bias setting of 1_2 for nominal input strength conditions (i.e., <–45 dBm) would result in a 4 mA current savings (i.e., 18% reduction). If the signal exceeds this level, a bias setting of 3_3 could be selected. Lastly, refer to the Typical Performance Characteristics (TPCs) for more performance graphs characterizing the LNA and mixer's effect upon the AD9874's noise and linearity performance under different operating conditions.

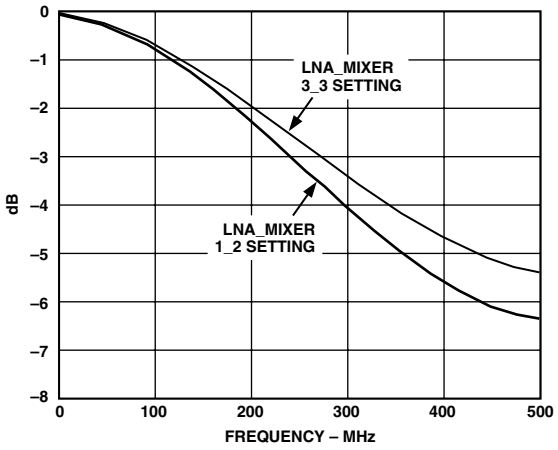


Figure 11c. LNA/Mixer Frequency Response vs. Bias Setting

A 16 dB step attenuator is also included within the LNA/mixer circuitry to prevent large signals (i.e., > –18 dBm) from overdriving the Σ-Δ modulator. In such instances, the Σ-Δ modulator will become unstable, thus severely desensitizing the receiver. The 16 dB step attenuator can be invoked by setting the ATTEN bit (Register 0x03, Bit 7), causing the mixer gain to be reduced by 16 dB. The 16 dB step attenuator could be used in applications in which a potential target or blocker signal could exceed the IF input clip point. Although the LNA will be driven into compression, it may still be possible to recover the desired signal if it is FM. Refer to TPC 7c to see the gain compression characteristics of the LNA and mixer with the 16 dB attenuator enabled.

Table IX. SPI Registers Associated with LNA/Mixer

Address (Hex)	Bit Breakdown	Width	Default Value	Name
0x00	(7:0)	8	0xFF	STBY
0x01	(7:6)	2	0	LNAB
0x01	(5:4)	2	0	MIXB
0x03	(7)	1	0	ATTEN

Band-Pass Sigma-Delta (Σ-Δ) ADC

The ADC of the AD9874 is shown in Figure 12. The ADC contains a sixth order multibit band-pass Σ-Δ modulator that achieves very high instantaneous dynamic range over a narrow frequency band. The loop filter of the band-pass Σ-Δ modulator consists of two continuous-time resonators followed by a discrete-time resonator, with each resonator stage contributing a pair of complex poles. The first resonator is an external LC tank, while the second is an on-chip active RC filter. The output of the LC resonator is ac-coupled to the second resonator input via 100 pF capacitors. The center frequencies of these two continuous-time resonators must be tuned to $f_{CLK}/8$ for the ADC to function properly. The center frequency of the discrete-time resonator automatically scales with f_{CLK}, thus no tuning is required.

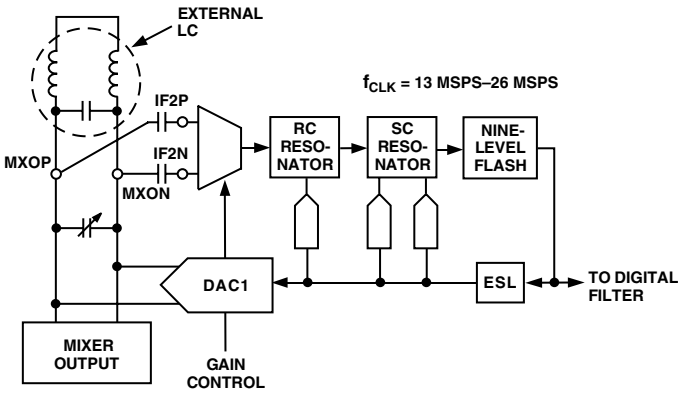


Figure 12. Equivalent Circuit of Sixth Order Band-Pass Σ-Δ Modulator

Figure 13a shows the measured power spectral density measured at the output of the undecimated band-pass Σ-Δ modulator. Note, the wide dynamic range achieved at the center frequency, $f_{CLK}/8$, is achieved once the LC and RC resonators of the Σ-Δ modulator have been successfully tuned. The out-of-band noise is removed by the decimation filters following quadrature demodulation.

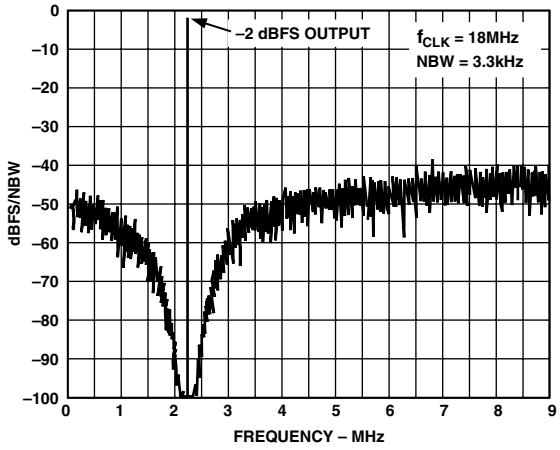


Figure 13a. Measured Undecimated Spectral Output of Σ-Δ Modulator ADC with f_{CLK} = 18 MSPS and Noise Bandwidth of 3.3 kHz

The signal transfer function of the AD9874 possesses inherent antialias filtering by virtue of the continuous-time portions of the loop filter in the band-pass Σ-Δ modulator. Figure 13b illustrates this property by plotting the nominal signal transfer function of the ADC for frequencies up to $2f_{CLK}$. The notches that naturally occur for all frequencies that alias to the $f_{CLK}/8$ pass band are clearly visible. Even at the widest bandwidth setting, the notches are deep enough to provide greater than 80 dB of alias protection. Thus, the wideband IF filtering requirements preceding the AD9874 will be mostly determined by the mixer's image band that is offset from the desired IF input frequency by $f_{CLK}/4$ (i.e., $2 \times f_{CLK}/8$), rather than any aliasing associated with the ADC.

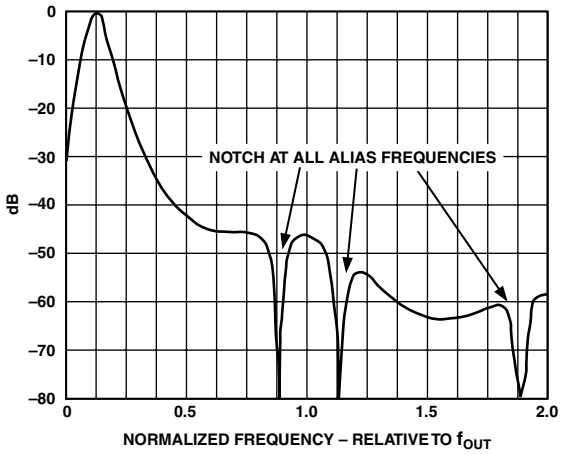


Figure 13b. Signal Transfer Function of the Band-Pass Σ-Δ Modulator from 0 f_{CLK} to 2 f_{CLK}

Figure 13c shows the nominal signal transfer function magnitude for frequencies near the $f_{CLK}/8$ pass band. The width of the pass band determines the transfer function droop, but even at the lowest oversampling ratio (48) where the pass band edges are at $\pm f_{CLK}/192$ ($\pm$ .005 f_{CLK}), the gain variation is less than 0.5 dB. Note, the amount of attenuation offered by the signal transfer function near f_{CLK} /8 should also be considered when determining the narrow-band IF filtering requirements preceding the AD9874.

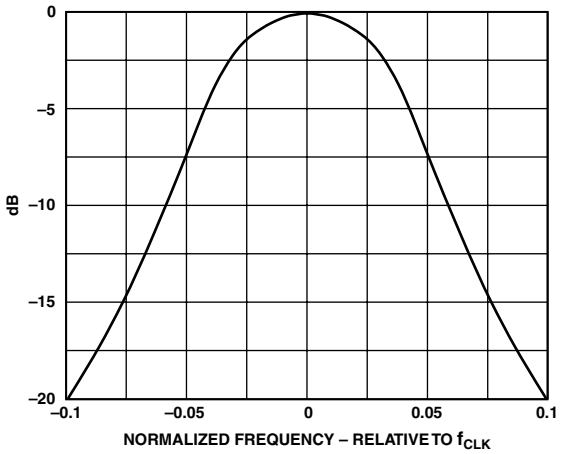


Figure 13c. Magnitude of the ADC's Signal Transfer Function near $f_{CLK}/8$

Tuning of the Σ-Δ modulator's two continuous-time resonators is essential in realizing the ADC's full dynamic range and must be performed upon system startup. To facilitate tuning of the LC tank, a capacitor array is internally connected to the MXOP and MXON pins. The capacitance of this array is programmable from 0 pF to 200 pF ± 20% and can be programmed either automatically or manually via the SPI port. The capacitors of the active RC resonator are similarly programmable. Note, the AD9874 can be placed in and out of its standby mode without retuning since the tuning codes are stored in the SPI Registers.

When tuning the LC tank, the sampling clock frequency must be stable and the LNA/mixer, LO synthesizer, and ADC must all be placed in standby. Tuning is triggered when the ADC is taken out of standby if the TUNE_LC bit of register 0x1C has been set. This bit will clear when the tuning operation is complete (less than 6 ms). The tuning codes can be read from the 3-bit CAPL1 (0x1D) and the 6-bit CAPL0 (0x1E) Registers.

In a similar manner, tuning of the RC resonator is activated if the TUNE_RC bit of register 0x1C is set when the ADC is taken out of standby. This bit will clear when tuning is complete. The tuning code can be read from the CAPR (0x1F) Register. Setting both the TUNE_LC and TUNE_RC bits tunes the LC tank and the active RC resonator in succession. During tuning, the ADC is not operational and neither data nor a clock is available from the SSI port. Table X lists the recommended sequence of the SPI commands for tuning the ADC, while Table XI lists all of the SPI Registers associated with band-pass Σ-Δ ADC.

Table X. Tuning Sequence

Address	Value	Comments
0x01	0x45	LO synthesizer, LNA/mixer, and ADC are placed in standby.*
0x01	0x03	Set TUNE_LC and TUNE_RC. Wait for CLK to stabilize if CLK synthesizer used.
0x03	0x44	Take the ADC out of standby. Wait for 0x1C to clear (<6 ms). LNA/mixer can now be taken out of standby.

*If external CLK VCO or source used, the CLK oscillator must also be disabled.

Table XI. SPI Registers Associated with Band-Pass Σ-Δ ADC

Address (Hex)	Bit Breakdown	Width	Default Value	Name
0x00	(7:0)	8	0xFF	STBY
0x1C	(1) (0)	1 1	0 0	TUNE_LC TUNE_RC
0x1D	(2:0)	3	0	CAPL1(2:0)
0x1E	(5:0)	6	0x00	CAPL1(5:0)
0x1F	(7:0)	8	0x00	CAPR

Once the AD9874 has been tuned, the noise figure degradation attributed solely to the temperature drift of the LC and RC resonators is minimal. Since the drift of the RC resonator is actually negligible compared to that of the LC resonator, the external L and C components' temperature drift characteristics tend to dominate. Figure 13d shows the degradation in noise figure as the product of the LC value is allowed to vary from –12.5% to +12.5%. Note, the noise figure remains relatively constant over a ±3.5% range (i.e., ±35,000 ppm) suggesting that most applications will not be required to retune over the operating temperature range.

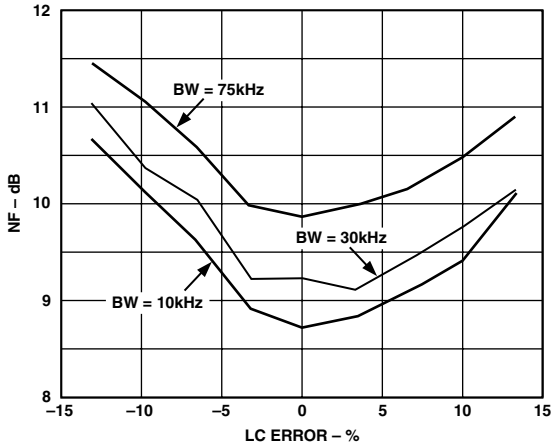


Figure 13d. Typical Noise Figure Degradation from L and C Component Drift (f_{CLK} = 18 MSPS, f_{IF} = 73.3501 MHz)

DECIMATION FILTER

The decimation filter shown in Figure 14 consists of an $f_{CLK}/8$ complex mixer and a cascade of three linear phase FIR filters: DEC1, DEC2, and DEC3. DEC1 downsamples by a factor of 12 using a fourth order comb filter. DEC2 also uses a fourth order comb filter, but its decimation factor is set by the M field of Register 0x07. DEC3 is either a decimate-by-5 FIR filter or a decimate-by-4 FIR filter depending on the value of the K Bit within Register 0x07. Thus, the composite decimation factor can be set to either 60 × M or 48 × M for K equal to 0 or 1, respectively.

The output data rate (f_{OUT}) is equal to the modulator clock frequency (f_{CLK}) divided by the digital filter's decimation factor. Due to the transition region associated with the decimation filter's frequency response, the decimation factor must be selected such that f_{OUT} is equal to or greater than twice the signal bandwidth. This ensures low amplitude ripple in the pass band along with the ability to provide further application-specific digital filtering prior to demodulation.

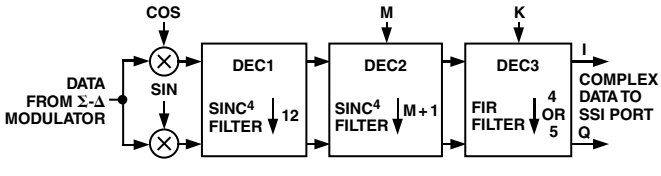


Figure 14. Decimation Filter Architecture

Figure 15a shows the response of the decimation filter at a decimation factor of 900 (K = 0, M = 14) and a sampling clock frequency of 18 MHz. In this example, the output data rate (f_{OUT}) is 20 kSPS, with a usable complex signal bandwidth of 10 kHz centered around dc. As this figure shows, the first and second alias bands (occurring at even integer multiples of $f_{OUT}/2$) have the least attenuation but provide at least 88 dB of attenuation. Note, signals falling around frequency offsets that are odd integer multiples of $f_{OUT}/2$ (i.e., 10 kHz, 30 kHz, and 50 kHz) will fall back into the transition band of the digital filter.

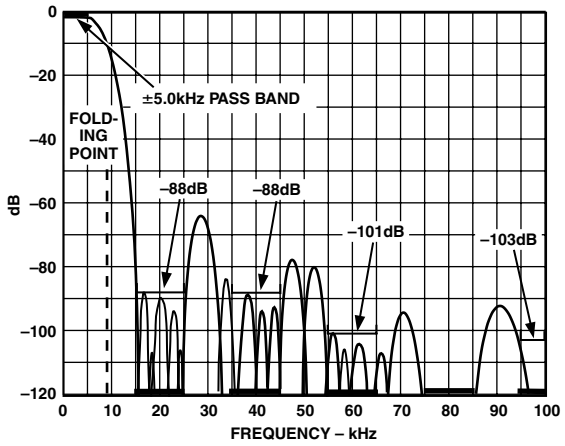


Figure 15a. Decimation Filter Frequency Response for f_{OUT} = 20 kSPS (f_{CLK} = 18 MHz, OSR = 900)

Figure 15b shows the response of the decimation filter with a decimation factor of 48 and a sampling clock rate of 26 MHz. The alias attenuation is now at least 94 dB, and this attenuation occurs for frequencies at the edges of the fourth alias band. The difference between the alias attenuation characteristics of Figure 15b and those of Figure 15a is due to the fact that the third decimation stage decimates by a factor of 5 for Figure 15a versus a factor of 4 for Figure 15b.

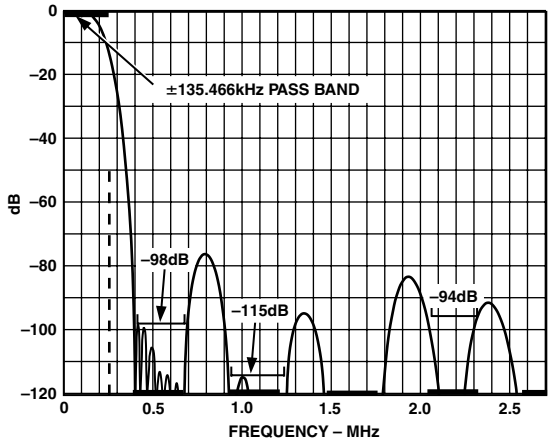


Figure 15b. Decimation Filter Frequency Response for f_{OUT} = 541.666 kSPS (f_{CLK} = 26 MHz, OSR = 48)

Figures 16a and 16b show expanded views of the pass band for the two possible configurations of the third decimation filter. When decimating by 60 *n* (K = 0), the pass-band gain variation is 1.2 dB; when decimating by 48 *n* (K = 1), the pass-band gain variation is 0.9 dB. Normalization of full scale at band center is accurate to within 0.14 dB across all decimation modes. Figures 17a and 17b show the folded frequency response of the decimator for K = 0 and K = 1, respectively.

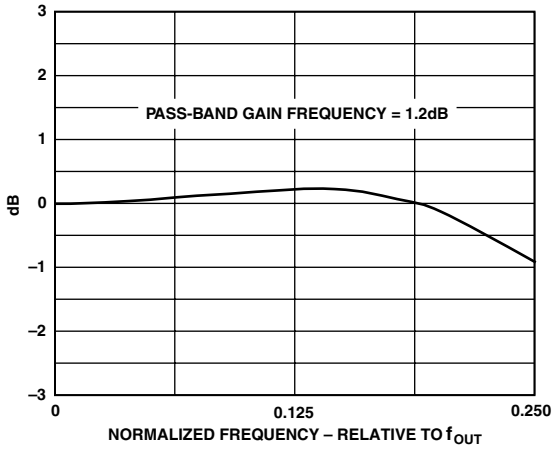


Figure 16a. Pass-Band Frequency Response of the Decimator for K = 0

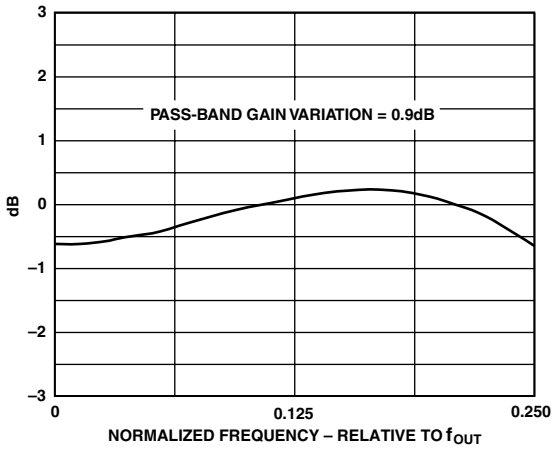


Figure 16b. Pass-Band Frequency Response of the Decimator for K = 1

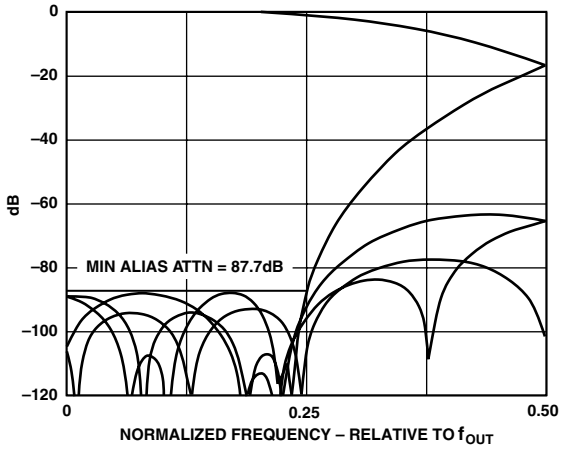


Figure 17a. Folded Decimator Frequency Response for K = 0

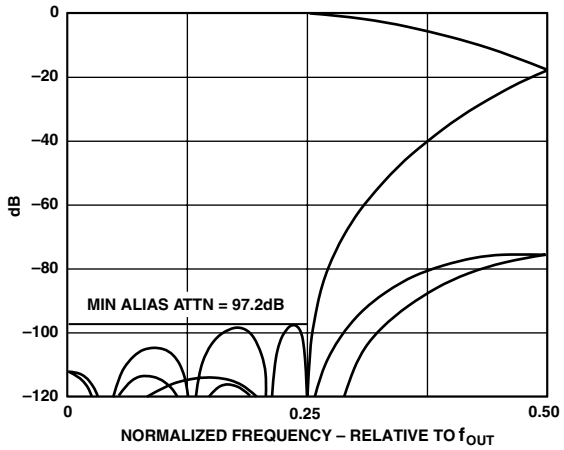


Figure 17b. Folded Decimator Frequency Response for K = 1

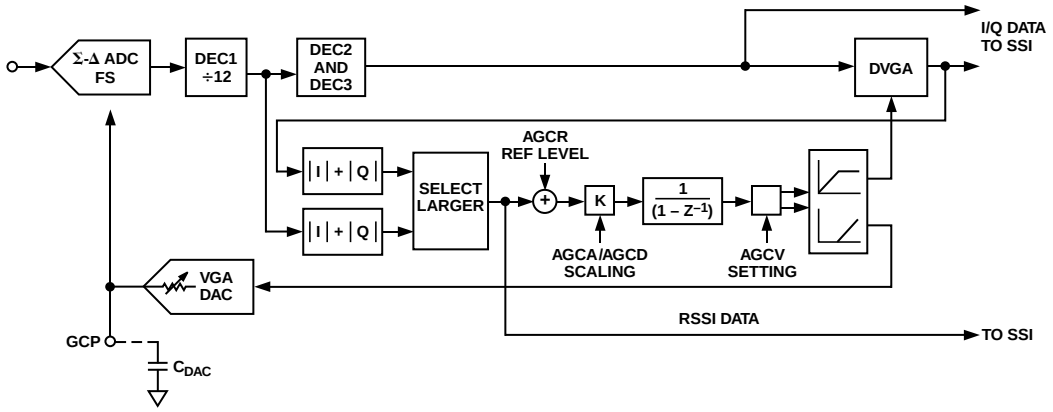


Figure 18. Functional Block Diagram of VGA and AGC

VARIABLE GAIN AMPLIFIER OPERATION WITH AUTOMATIC GAIN CONTROL

The AD9874 contains both a variable gain amplifier (VGA) and a digital VGA (DVGA) along with all of the necessary signal estimation and control circuitry to implement automatic gain control (AGC), as shown in Figure 18. The AGC control circuitry provides a high degree of programmability, allowing users to optimize the AGC response as well as the AD9874's dynamic range for a given application. The VGA is programmable over a 12 dB range and implemented within the ADC by adjusting its full-scale reference level. Increasing the ADC's full scale is equivalent to attenuating the signal. An additional 12 dB of digital gain range is achieved by scaling the output of the decimation filter in the DVGA. Note, a slight increase in the supply current (i.e., 0.67 mA) is drawn from VDDI and VDDF as the VGA changes from 0 dB to 12 dB attenuation.

The purpose of the VGA is to extend the usable dynamic range of the AD9874 by allowing the ADC to digitize a desired signal over a large input power range as well as recover a low level signal in the presence of larger unfiltered interferers without saturating or "clipping" the ADC. The DVGA is most useful in extending the dynamic range in narrow-band applications requiring a 16-bit I and Q data format. In these applications, quantization noise resulting from internal truncation to 16 bits as well as external 16-bit fixed point post-processing can degrade the AD9874's effective noise figure by 1 or more dB. The DVGA is enabled by writing a 1 to the AGCV field. The VGA (and the DVGA) can operate in either a user-controlled Variable Gain Mode or Automatic Gain Control (AGC) Mode.

It is worth noting that the VGA imparts negligible phase error upon the desired signal as its gain is varied over a 12 dB range. This is due to the bandwidth of the VGA being far greater than the down converted desired signal (centered about $f_{CLK}/8$) and remaining relatively independent of gain setting. As a result, phase modulated signals should experience minimal phase error as the AGC varies the VGA gain while tracking an interferer or the desired signal under fading conditions. Note, the envelope of the signal will still be affected by the AGC settings.

Variable Gain Control

The variable gain control is enabled by setting the AGCR field of Register 0x06 to 0. In this mode, the gain of the VGA (and the DVGA) can be adjusted by writing to the 16-bit AGCG Register. The maximum update rate of the AGCG Register via the SPI port is $f_{CLK}/240$. The MSB of this register is the bit that enables 16 dB of attenuation in the mixer. This feature allows the AD9874 to cope with large level signals beyond the VGA's range (i.e., > –18 dBm at LNA input) to prevent overloading of the ADC.

The lower 15 bits specify the attenuation in the remainder of the signal path. If the DVGA is enabled, the attenuation range is from –12 dB to +12 dB since the DVGA provides 12 dB of digital gain. In this case, all 15 bits are significant. However, with the DVGA disabled the attenuation range extends from 0 dB to 12 dB and only the lower 14 bits are useful. Figure 19 shows the relationship between the amount of attenuation and the AGC Register setting for both cases.

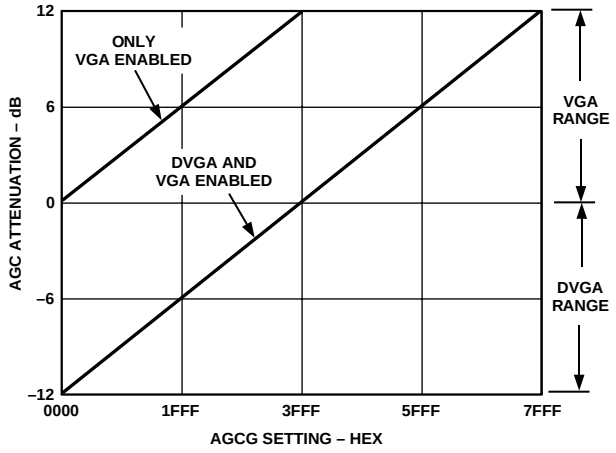


Figure 19. AGC Gain Range Characteristics vs. AGCG Register Setting with and without DVGA Enabled

Referring to Figure 18, the gain of the VGA is set by an 8-bit control DAC that provides a control signal to the VGA appearing at the gain control pin (GCP). For applications implementing automatic gain control, the DAC's output resistance can be reduced by a factor of 9 to decrease the attack time of the AGC response for faster signal acquisition. An external capacitor, C_{DAC}, from GCP to analog ground is required to "smooth" the DAC's output each time it updates as well as to filter wideband noise. Note, C_{DAC}, in combination with the DAC's programmable output resistance, sets the –3 dB bandwidth and time constant associated with this RC network.

A linear estimate of the received signal strength is performed at the output of the first decimation stage (DEC1) and output of the DVGA (if enabled) as discussed in the AGC section. This data is available as a 6-bit RSSI field within an SSI frame with 60 corresponding to a full-scale signal for a given AGC attenuation setting. The RSSI field is updated at $f_{CLK}/60$ and can be used with the 8-bit attenuation field (or AGCG attenuation setting) to determine the absolute signal strength.

The accuracy of the mean RSSI reading (relative to the IF input power) depends on the input signal's frequency offset relative to the IF frequency since both DEC1 filter's response as well as the ADC's signal transfer function attenuates the mixer's downconverted signal level centered at $f_{CLK}/8$. As a result, the estimated signal strength of input signals falling within proximity to the IF is reported accurately, while those signals at increasingly higher frequency offsets incur larger measurement errors. Figure 20 shows the normalized error of the RSSI reading as a function of the frequency offset from the IF frequency. Note, the significance of this error becomes apparent when determining the maximum input interferer (or blocker) levels with the AGC enabled.

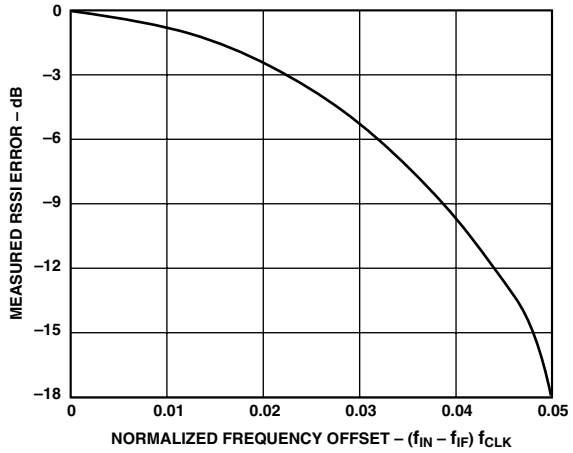


Figure 20. Normalized RSSI Error vs. Normalized IF Frequency Offset

Automatic Gain Control (AGC)

The gain of the VGA (and DVGA) is automatically adjusted when the AGC is enabled via the AGCR field of Register 0x06. In this mode, the gain of the VGA is continuously updated at $f_{CLK}/60$ in an attempt to ensure that the maximum analog signal level into the ADC does not exceed the ADC clip level and that the rms output level of the ADC is equal to a programmable reference level. With the DVGA enabled, the AGC control loop also attempts to minimize the effects of 16-bit truncation noise prior to the SSI output by continuously adjusting the DVGA's gain to ensure maximum digital gain while not exceeding the programmable reference level.

This programmable level can be set at 3 dB, 6 dB, 9 dB, 12 dB, and 15 dB below the ADC saturation (clip) level by writing values from 1 to 5 to the 3-bit AGCR field. Note, the ADC clip level is defined to be 2 dB below its full scale (i.e., –18 dBm at the LNA input for a matched input and maximum attenuation). If AGCR is 0, automatic gain control is disabled. Since clipping of the ADC input will degrade the SNR performance, the reference level should also take into consideration the peak-to-rms characteristics of the target (or interferer) signals.

Referring again to Figure 18, the majority of the AGC loop operates in the discrete time domain. The sample rate of the loop is $f_{CLK}/60$; therefore, registers associated with the AGC algorithm are updated at this rate. The number of overload and ADC reset occurrences within the final I/Q update rate of the AD9874, as well as the AGC value (8 MSBs), can be read from the SSI data upon proper configuration.

The AGC performs digital signal estimation at the output of the first decimation stage (DEC1) as well as the DVGA output that follows the last decimation stage (DEC3). The rms power of the I and Q signal is estimated by the following equation:

$$Xest[n] = Abs(I[n]) + Abs(Q[n]) \quad (7)$$

Signal estimation after the first decimation stage allows the AGC to cope with out-of-band interferers and in-band signals that could otherwise overload the ADC. Signal estimation after the DVGA allows the AGC to minimize the effects of the 16-bit truncation noise.

When the estimated signal level falls within the range of the AGC, the AGC loop adjusts the VGA (or DVGA) attenuation setting so that the estimated signal level is equal to the programmed level specified in the AGCR field. The absolute signal strength can be determined from the contents of the ATTN and RSSI field that is available in the SSI data frame when properly configured. Within this AGC tracking range, the 6-bit value in the RSSI field remains constant while the 8-bit ATTN field varies according to the VGA/DVGA setting. Note, the ATTN value is based on the 8 MSBs contained in the AGCG field of Registers 0x03 and 0x04.

A description of the AGC control algorithm and the user adjustable parameters follows. First, consider the case in which the in-band target signal is bigger than all out-of-band interferers and the DVGA is disabled. With the DVGA disabled, a control loop based only on the target signal power measured after DEC1 is used to control the VGA gain, and the target signal will be tracked to the programmed reference level. If the signal is too large, the attenuation is increased with a proportionality constant determined by the AGCA setting. Large AGCA values result in large gain changes, thus rapid tracking of changes in signal strength. If the target signal is too small relative to the reference level, the attenuation is reduced; but now the proportionality constant is determined by both the AGCA and AGCD settings. The AGCD value is effectively subtracted from AGCA, so a large AGCD results in smaller gain changes and thus slower tracking of fading signals.

The 4-bit code in the AGCA field sets the raw bandwidth of the AGC loop. With AGCA = 0, the AGC loop bandwidth is at its minimum of 50 Hz assuming f_{CLK} = 18 MHz. Each increment of AGCA increases the loop bandwidth by a factor of $2^{1/2}$, thus

the maximum bandwidth is 9 kHz. A general expression for the attack bandwidth is:

$$BW_A = 50 \times \left(f_{CLK}/18\ MHz\right) \times 2^{(AGCA/2)}\ Hz \quad (8)$$

and the corresponding attack time is:

$$t_{attack} = 2.2 \Big/ \left(100 \times \pi \times 2^{(AGCA/2)}\right) = 0.35/BW_A \quad (9)$$

assuming that the loop dynamics are essentially those of a single-pole system.

The 4-bit code in the AGCD field sets the ratio of the attack time to the decay time in the amplitude estimation circuitry. When AGCD is zero, this ratio is one. Incrementing AGCD multiplies the decay time constant by $2^{1/2}$, allowing a 180:1 range in the decay time relative to the attack time. The decay time may be computed from:

$$t_{decay} = t_{attack} \times 2^{(AGCD/2)} \quad (10)$$

Figure 21a shows the AGC response to a 30 Hz pulse-modulated IF burst for different AGCA and AGCD settings.

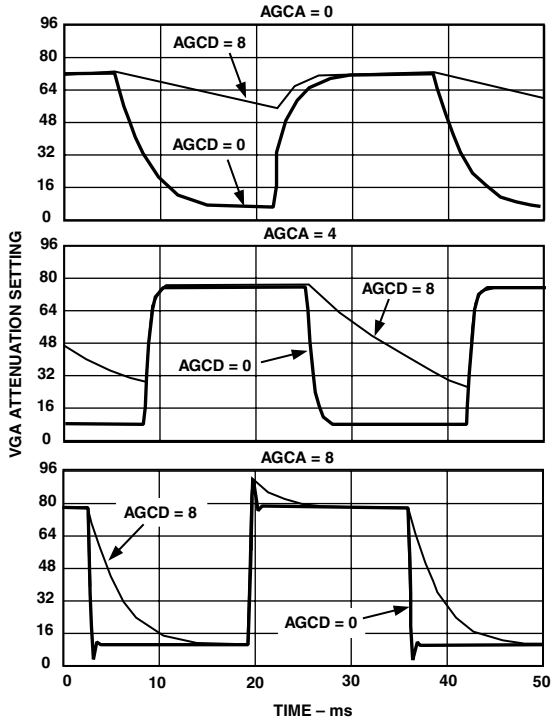


Figure 21a. AGC Response for Different AGCA and AGCD Settings with f_{CLK} = 18 MSPS, f_{CLKOUT} = 20 kSPS, Decimate by 900, and AGCO = 0

The 3-bit value in the AGCO field determines the amount of attenuation added in response to a reset event in the ADC. Each increment in AGCO doubles the weighting factor. At the highest AGCO setting, the attenuation will change from 0 dB to 12 dB in approximately 10 µs, while at the lowest setting the attenuation will change from 0 dB to 12 dB in approximately 1.2 ms. Both times assume f_{CLK} = 18 MHz. Figure 21b shows the AGC attack time response for different AGCO settings.

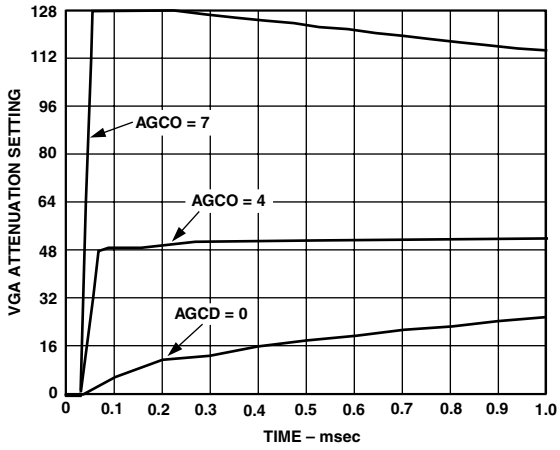


Figure 21b. AGC Response for Different AGCO Settings with f_{CLK} = 18 MSPS, f_{CLKOUT} = 300 kSPS, Decimate by 60, and AGCA = AGCD = 0

Lastly, the AGCF bit reduces the DAC source resistance by at least a factor of 10. This facilitates fast acquisition by lowering the RC time constant that is formed with the external capacitors connected from the GCP pin-to-ground (GCN Pin). For an overshoot-free step response in the AGC loop, the capacitor connected from the GCP pin to the GCN ground pin should be chosen so that the RC time constant is less than one quarter that of the raw loop. Specifically:

$$RC < 1/(8\pi BW) \quad (11)$$

where R is the resistance between the GCP Pin and ground (64 kW ±20% if AGCF = 0, < 7 kW if AGCF = 1) and BW is the raw loop bandwidth. Note that with C chosen at this upper limit, the loop bandwidth increases by approximately 30%.

Now consider the same case as above but with the DVGA enabled to minimize the effects of 16-bit truncation. With the DVGA enabled, a control loop based on the larger of the two estimated signal levels (i.e., output of DEC1 and DVGA) is used to control the DVGA gain. The DVGA multiplies the output of the decimation filter by a factor ranging from 1 to 4 (i.e., 0 dB to 12 dB). When signals are small, the DVGA gain is 4 and the 16-bit output is extracted from the 24-bit data produced by the decimation filter by dropping 2 MSBs and taking the next 16-bits. As signals get larger, the DVGA gain decreases until the point where the DVGA gain is 1 and the 16-bit output data is simply the 16 MSBs of the internal 24-bit data. As signals get even larger, attenuation is accomplished by the normal method of increasing the ADC's full scale.

The extra 12 dB of gain range provided by the DVGA reduces the input-referred truncation noise by 12 dB and makes the data more tolerant of LSB corruption within the DSP. The price paid for this extension to the gain range is that the start of AGC action is 12 dB lower and that the AGC loop will be unstable if its bandwidth is set too wide. The latter difficulty results from the large delay of the decimation filters, DEC2 and DEC3, when one implements a large decimation factor. As a result, given an option, the use of 24-bit data is preferable to using the DVGA.

Table XII indicates which AGCA values are reasonable for various decimation factors. The white cells indicate that the (decimation factor/AGCA) combination works well. The light gray cells indicate ringing and an increase in the AGC settling time, and the dark gray cells indicate that the combination results in instability or near instability in the AGC loop. Setting AGCF = 1 improves the time-domain behavior at the expense of increased spectral spreading.

Table XII. AGCA Limits if the DVGA is Enabled

DECIMATION FACTOR	M	AGCA 4	5	6	7	8	9	10	11	12	13	14	15
60	0												
120	1												
300	4												
540	8												
900	E												

Lastly, consider the case of a strong out-of-band interferer (i.e., –18 dBm to –32 dBm for matched IF input) that is larger than the target signal and large enough to be tracked by the control loop based on the output of the DEC1. The ability of the control loop to track this interferer and set the VGA attenuation to prevent clipping of the ADC is limited by the accuracy of the digital signal estimation occurring at the output of DEC1. The accuracy of the digital signal estimation is a function of the frequency offset of the out-of-band interferer relative to the IF frequency as shown in Figure 20. Interferers at increasingly higher frequency offsets incur larger measurement errors, potentially causing the control loop to inadvertently reduce the amount of VGA attenuation that may result in clipping of the ADC. Figure 21c shows the maximum measured interferer signal level versus the normalized IF offset frequency (relative to f_{CLK}) tolerated by the AD9874 relative to its maximum target input signal level (0 dBFS = –18 dBm). Note, the increase in allowable interferer level occurring beyond $0.04 \times f_{CLK}$ results from the inherent signal attenuation provided by the ADC's signal transfer function.

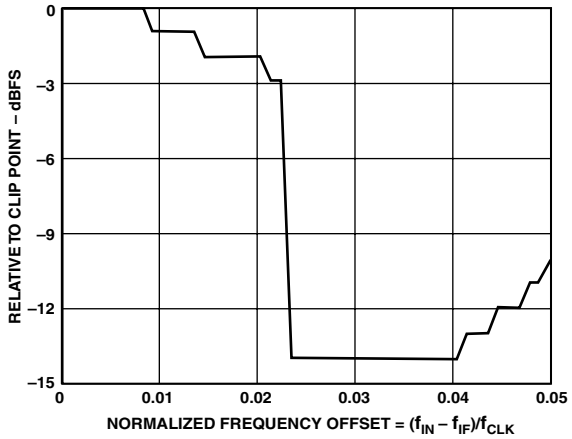


Figure 21c. Maximum Interferer (or Blocker) Input Level vs. Normalized IF Frequency Offset

Table XIII. SPI Registers Associated with AGC

Address (Hex)	Bit Breakdown	Width	Default Value	Name
0x03	(7)	1	0	ATTEN
	(6:0)	7	0x00	AGCG(14:8)
0x04	(7:0)	8	0x00	AGCG(7:0)
0x05	(7:4)	4	0	AGCA
	(3:0)	4	0x00	AGCD
0x06	(7)	1	0	AGCV
	(6:4)	3	0	AGCO
	(3)	1	0	AGCF
	(2:0)	3	0	AGCR

System Noise Figure (NF) vs. VGA (or AGC) Control

The AD9874's system noise figure is a function of the ACG attenuation and output signal bandwidth. Figure 22a plots the nominal system NF as a function of the AGC attenuation for both narrow-band (20 kHz) and wideband (150 kHz) modes with f_{CLK} = 18 MHz. Also shown on the plot is the SNR that would be observed at the output for a –2 dBFS input. The high dynamic range of the ADC within the AD9874 ensures that the system NF increases gradually as the AGC attenuation is increased. In narrow-band (BW = 20 kHz) mode, the system noise figure increases by less than 3 dB over a 12 dB AGC range, while in wideband (BW = 150 kHz) mode, the degradation is about 5 dB. As a result, the highest instantaneous dynamic range for the AD9874 occurs with 12 dB of AGC attenuation, since the AD9874 can accommodate an additional 12 dB peak signal level with only a moderate increase in its noise floor.

As Figure 22a shows, the AD9874 can achieve an SNR in excess of 100 dB in narrow-band applications. To realize the full performance of the AD9874 in such applications, it is recommended that the I/Q data be represented with 24 bits. If 16-bit data is used, the effective system NF will increase because of the quantization noise present in the 16-bit data after truncation.

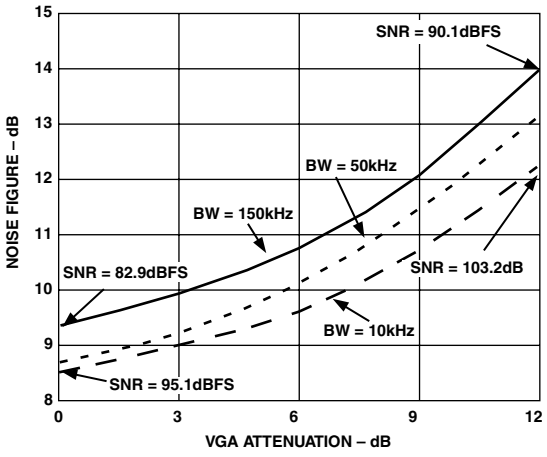


Figure 22a. Nominal System Noise Figure and Peak SNR vs. AGCG Setting (f_{IF} = 73.35 MHz, f_{CLK} = 18 MSPS, and 24-bit I/Q data)

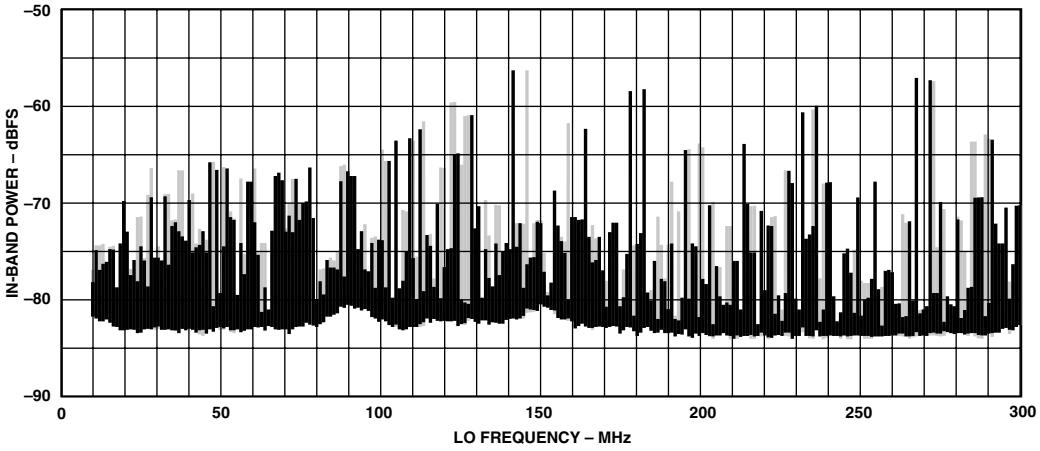


Figure 23a. Total In-Band Noise + Spur Power with No Signal Applied as a Function of the LO Frequency (f_{CLK} = 18 MHz and Output Signal Bandwidth of 150 kHz)

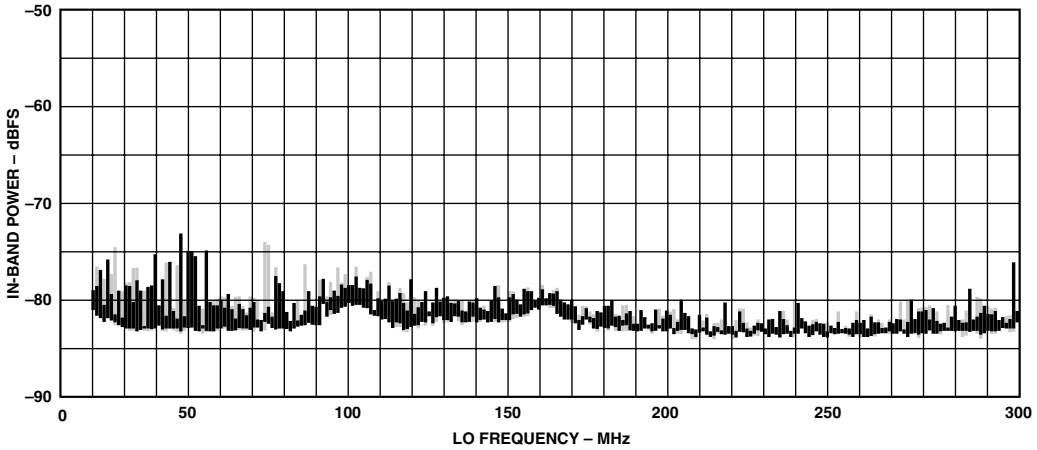


Figure 23b. Same as Figure 23a Excluding LO Frequencies Known to Produce Large In-Band Spurs

Figure 22b plots the nominal system NF with 16-bit output data as a function of AGC in both narrow-band and wideband mode. In wideband mode, the NF curve is virtually unchanged relative to the 24-bit output data because the output SNR before truncation is always less than the 96 dB SNR that 16-bit data can support.

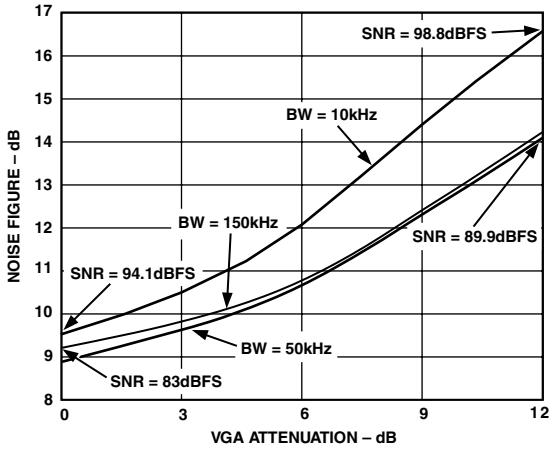


Figure 22b. Nominal System Noise Figure and Peak SNR vs. AGCG Setting (f_{IF} = 73.35 MHz, f_{CLK} = 18 MSPS, and 16-bit I/Q data)

However, in narrow-band mode, where the output SNR approaches or exceeds the SNR that can be supported with 16-bit data, the degradation in system NF is more severe. Furthermore, if the signal processing within the DSP adds noise at the level of an LSB, the system noise figure can be degraded even more than Figure 22b shows. For example, this could occur in a fixed 16-bit DSP whose code is not optimized to process the AD9874's 16-bit data with minimal quantization effects. To limit the quantization effects within the AD9874, the 24-bit data undergoes noise shaping just prior to 16-bit truncation, thus reducing the in-band quantization noise by 5 dB (with 2× oversampling). This explains why 98.8 dBFS SNR performance is still achievable with 16-bit data in a 10 kHz BW.

APPLICATION CONSIDERATIONS

Frequency Planning

The LO frequency (and/or ADC clock frequency) must be chosen carefully to prevent known internally generated spurs from mixing down along with the desired signal, thus degrading the SNR performance. The major sources of spurs in the AD9874 are the ADC clock and digital circuitry operating at 1/3 of f_{CLK}. Thus, the clock frequency (f_{CLK}) is the most important variable in determining which LO (and therefore IF) frequencies are viable.

Many applications have frequency plans that take advantage of industry-standard IF frequencies due to the large selection of low cost crystal or SAW filters. If the selected IF frequency and ADC clock rate result in a problematic spurious component, an alternative ADC clock rate should be selected by slightly modifying the decimation factor and CLK synthesizer settings (if used) such that the output sample rate remains the same. Also, applications requiring a certain degree of tuning range should take into consideration the location and magnitude of these spurs when determining the tuning range as well as optimum IF and ADC clock frequency.

Figure 23a plots the measured in-band noise power as a function of the LO frequency for f_{CLK} = 18 MHz and an output signal bandwidth of 150 kHz when no signal is present. Any LO frequency resulting in large spurs should be avoided. As this figure shows, large spurs result when the LO is $f_{CLK}/8$ = 2.25 MHz away from a harmonic of 18 MHz (i.e., $n\,f_{CLK} \pm f_{CLK}/8$). Also problematic are LO frequencies whose odd order harmonics (i.e., $m\,f_{LO}$) mix with harmonics of f_{CLK} to $f_{CLK}/8$. This spur mechanism is a result of the mixer being internally driven by a squared-up version of the LO input consisting of the LO frequency and its odd order harmonics. These spur frequencies can be calculated from the following relation:

$$m\,f_{LO} = \left(n \pm 1/8\right) f_{CLK} \qquad (12)$$

where m = 1, 3, 5... and n = 1, 2, 3...

A second source of spurs is a large block of digital circuitry that is clocked at $f_{CLK}/3$. Problematic LO frequencies associated with this spur source are given by:

$$f_{LO} = f_{CLK}/3 + n\,f_{CLK} \pm f_{CLK}/8 \qquad (13)$$

where n = 1, 2, 3 ...

Figure 23b shows that omitting the LO frequencies given by Equation 12 for m = 1, 3, and 5 and by Equation 13 accounts for most of the spurs. Some of the remaining low level spurs can be attributed to coupling from the SSI digital output. As a result, users are also advised to optimize the output bit rate (f_{CLKOUT} via the SSIORD Register) and the digital output driver strength to achieve the lowest spurious and noise figure performance for a particular LO frequency and f_{CLK} setting. This is especially the case for very narrow-band channels in which low level spurs can degrade the AD9874's sensitivity performance.

Despite the many spurs, sweet spots in the LO frequency are generally wide enough to accommodate the maximum signal bandwidth of the AD9874. As evidence of this property, Figure 24 shows that the in-band noise is quite constant for LO frequencies ranging from 70 MHz to 71 MHz.

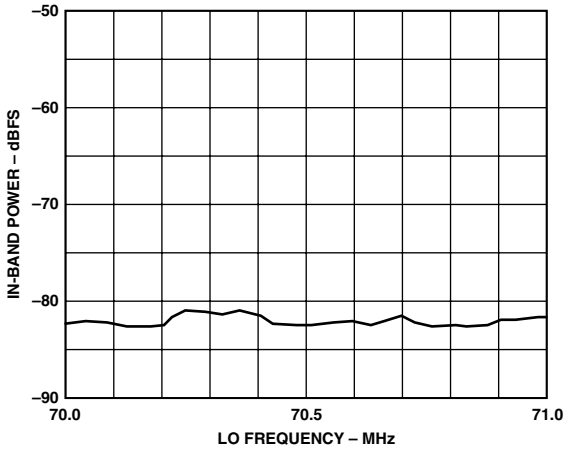


Figure 24. Expanded View from 70 MHz to 71 MHz

Spurious Responses

The spectral purity of the LO (including its phase noise) is an important consideration since LO spurs can mix with undesired signals present at the AD9874's IFIN input to produce an in-band response. To demonstrate the low LO spur level introduced within the AD9874, Figure 25 plots the demodulated output power as a function of the input IF frequency for an LO frequency of 71.1 MHz and a clock frequency of 18 MHz.

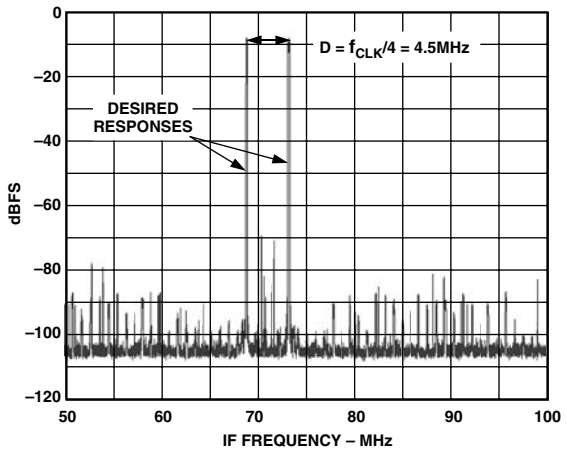


Figure 25. Response of AD9874 to a –20 dBm Input IF Input when f_{LO} = 71.1 MHz

The two large –10 dBFS spikes near the center of the plot are the desired responses at $f_{LO} \pm f_{IF2\_ADC}$ where $f_{IF2\_ADC} = f_{CLK}/8$, i.e., at 68.85 MHz and 73.35 MHz. LO spurs at $f_{LO} \pm f_{SPUR}$ would result in spurious responses at offsets of $\pm f_{SPUR}$ around the desired responses. Close-in spurs of this kind are not visible on the plot, but small spurious responses at $f_{LO} \pm f_{IF2\_ADC} \pm f_{CLK}$, i.e., at 50.85 MHz, 55.35 MHz, 86.85 MHz, and 91.35 MHz, are visible at the –90 dBFS level. This data indicates that the AD9874 does an excellent job of preserving the purity of the LO signal.

Figure 25 can also be used to gauge how well the AD9874 rejects undesired signals. For example, the half-IF response (at 69.975 MHz and 72.225 MHz) is approximately –100 dBFS, giving a selectivity of 90 dB for this spurious response. The largest spurious response at approximately –70 dBFS occurs with input frequencies of 70.35 MHz and 71.85 MHz. These spurs result from third order nonlinearity in the signal path (i.e., *abs* [3 × f_{LO} – 3 × f_{IF_Input}] = $f_{CLK}/8$).

EXTERNAL PASSIVE COMPONENT REQUIREMENTS

Figure 26 shows an example circuit using the AD9874 while Table XIV shows the nominal dc bias voltages seen at the different pins. The purpose is to show the various external passive components required by the AD9874 along with nominal dc voltages for troubleshooting purposes.

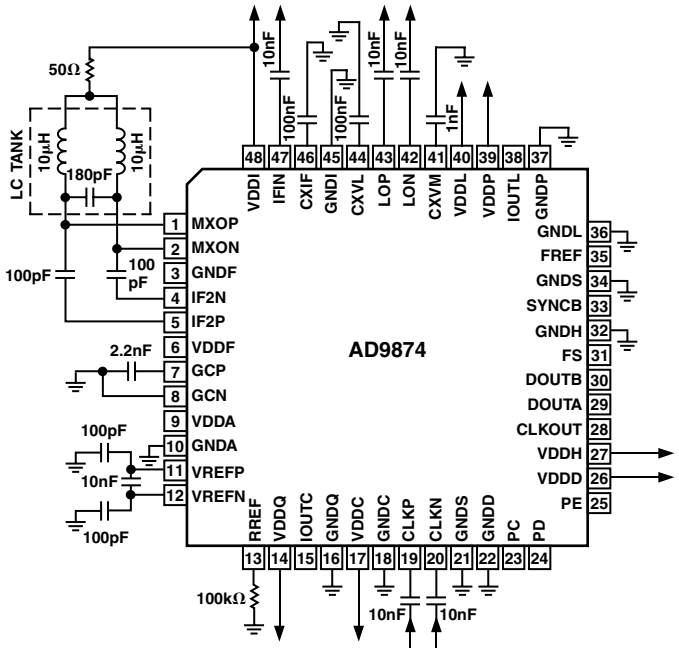


Figure 26. Example Circuit Showing Recommended Component Values

Table XIV. Nominal DC Bias Voltages

Pin Number	Pin Name (V)	Nominal DC Bias
1	MXOP	VDDI – 0.2
2	MXON	VDDI – 0.2
4	IF2N	1.3 – 1.7
5	IF2P	1.3 – 1.7
11	VREFP	VDDA/2 + 0.250
12	VREFN	VDDA/2 – 0.250
13	RREF	1.2
19	CLKP	VDDC – 1.3
20	CLKN	VDDC – 1.3
35	FREF	VDDC/2
41	CXVM	1.6 – 2.0
42	LON	1.65 – 1.9
43	LOP	1.65 – 1.9
44	CXVL	VDDI – 0.05
46	CXIF	1.6 – 2.0
47	IFIN	0.9 – 1.1

The LO, CLK, and IFIN signals are coupled to their respective inputs using 10 nF capacitors. The output of the mixer is coupled to the input of the ADC using 100 pF. An external 100 kΩ resistor from the RREF Pin to GND sets up the AD9874's internal bias currents. VREFP and VREFN provide a differential reference voltage to the AD9874's Σ-Δ ADC and must be decoupled by a 0.01 µF differential capacitor along with two 100 pF capacitors to GND. The remaining capacitors are used to decouple other sensitive internal nodes to GND.

Although power supply decoupling capacitors are not shown, it is recommended that a 0.1 µF surface-mount capacitor be placed as close as possible to each power supply pin for maximum effectiveness. Also not shown is the input impedance matching network used to match the AD9874's IF input to the external IF filter. Lastly, the loop filter components associated with the LO and CLK synthesizers are not shown.

LC component values for f_{CLK} = 18 MHz are given on the diagram. For other clock frequencies, the two inductors and the capacitor of the LC tank should be scaled in inverse proportion to the clock. For example, if f_{CLK} = 26 MHz, then the two inductors should be = 6.9 µH and the capacitor should be about 120 pF. A tolerance of 10% is sufficient for these components since tuning of the LC tank is performed upon system start-up.

APPLICATIONS

Superheterodyne Receiver Example

The AD9874 is well suited for analog and/or digital narrow-band radio systems based on a superheterodyne receiver architecture. The superheterodyne architecture is noted for achieving exceptional dynamic range and selectivity by using two or more downconversion stages to provide amplification of the target signal while filtering the undesired signals. The AD9874 greatly simplifies the design of these radio systems by integrating the complete IF strip (excluding the LO VCO) while providing an I/Q digital output (along with other system parameters) for the demodulation of both analog and digital modulated signals. The AD9874's exceptional dynamic range often simplifies the IF filtering requirements and eliminates the need for an external AGC.

Figure 27 shows a typical dual conversion superheterodyne receiver using the AD9874. An RF tuner is used to select and downconvert the target signal to a suitable first IF for the AD9874. A preselect filter may precede the tuner to limit the RF input to the band of interest. The output of the tuner drives an IF filter that provides partial suppression of adjacent channels and interferers that could otherwise limit the receiver's dynamic range. The conversion gain of the tuner should be set such that the peak IF input signal level into the AD9874 is no greater than –18 dBm to prevent clipping. The AD9874 downconverts the first IF signal to a second IF that is exactly 1/8 of the Σ-Δ ADC's clock rate (i.e., $f_{CLK}/8$) to simplify the digital quadrature demodulation process.

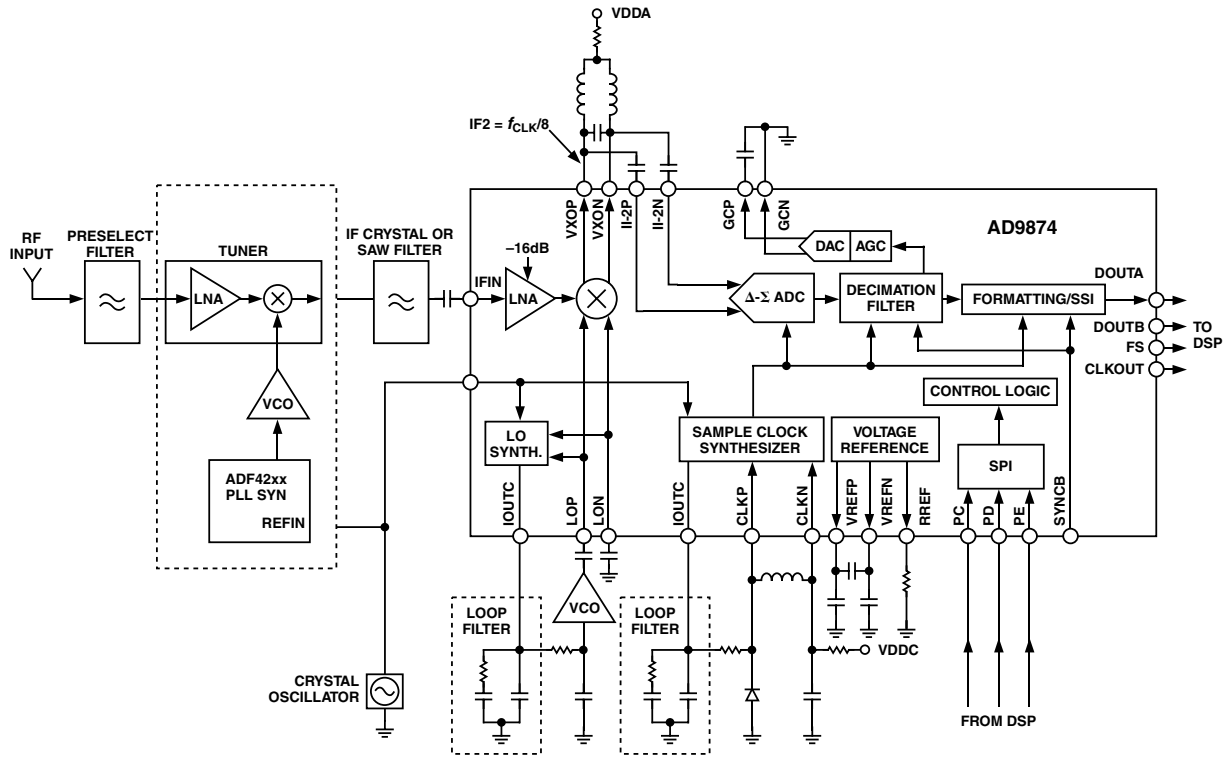


Figure 27. Typical Dual Conversion Superheterodyne Application Using the AD9874

This second IF signal is then digitized by the Σ-Δ ADC, demodulated into its quadrature I and Q components, filtered via matching decimation filters, and reformatted to enable a synchronous serial interface to a DSP. In this example, the AD9874's LO and CLK synthesizers are both enabled requiring some additional passive components (for the synthesizer's loop filters and CLK oscillator) and a VCO for the LO synthesizer. Note, not all of the required decoupling capacitors are shown. Refer to the previous section and Figure 26 for more information on required external passive components.

The selection of the first IF frequency is often based on the availability of low cost standard crystal or SAW filters as well as system frequency planning considerations. In general, crystal filters are often used for narrow-band radios having channel bandwidths below 50 kHz with IFs below 120 MHz, while SAW filters are more suited for channel bandwidths greater than 50 kHz with IFs greater than 70 MHz. The ultimate stop-band rejection required by the IF filter will depend on how much suppression is required at the AD9874's image band resulting from downconversion to the second IF. This image band is offset from the first IF by twice the second IF frequency (i.e., $\pm f_{CLK}/4$ depending on high or low side injection).

The selectivity and bandwidth of the IF filter will depend on both the magnitude and frequency offset(s) of the adjacent channel blocker(s) that could overdrive the AD9874's input or generate in-band intermodulation components. Further suppression is performed within the AD9874 by its inherent band-pass response and digital decimation filters. Note, some applications will require additional application-specific filtering performed in the DSP that follows the AD9874 to remove the adjacent channel and/or implement a matched filter for optimum signal detection.

The output data rate of the AD9874, f_{OUT}, should be chosen to be at least twice the bandwidth or symbol rate of the desired signal to ensure that the decimation filters provide a flat pass-band response as well as to allow for post-processing by a DSP. Once f_{OUT} is determined, the decimation factor of the digital filters should be set such that the input clock rate, f_{CLK}, falls between the AD9874's rated operating range of 13 MHz–26 MHz and no significant spurious products related to f_{CLK} fall within the desired pass band resulting in a reduction in sensitivity performance. If a spurious component is found to limit the sensitivity performance, the decimation factor can often be modified slightly to find a "spurious free" pass band. In general, selecting

a higher f_{CLK} is typically more desirable given a choice, since the first IF's filtering requirements often depend on the transition region between the IF frequency and the image band (i.e., $\pm f_{CLK}/4$). Lastly, the output SSI clock rate, f_{CLKOUT}, and digital driver strength should be set to their lowest possible settings to minimize the potential harmful effects of digital induced noise while preserving a reliable data link to the DSP. Note, the SSICRA, SSICRB, and SSIORD Registers (i.e., 0x18, 0x19, and 0x1A) provide a large degree of flexibility for optimization of the SSI interface.

Synchronization of Multiple AD9874s

Some applications such as receiver diversity and beam steering may require two or more AD9874s operating in parallel while maintaining synchronization. Figure 28 shows an example of how multiple AD9874s can be cascaded, with one device serving as the master and the other devices serving as the slaves. In this example, all of the devices have the exact same SPI register configuration since they share the same SPI interface to the DSP. Since the state of each of the AD9874's internal counters is unknown upon initialization, synchronization of the devices is required via a SYNCB pulse (see Figure 4) to synchronize their digital filters and ensure precise time alignment of the data streams. Although all of the devices' synthesizers are enabled, the LO and CLK signals for the slaves(s) are derived from the masters' synthesizers and are referenced to an external crystal oscillator. All of the necessary external components (i.e., loop filters, varactor, LC, and VCO) to ensure proper closed-loop operation of these synthesizers are included.

Note, while the VCO output of the LO synthesizer is ac-coupled to the slave's LO input(s), all of the CLK inputs of the devices must be dc-coupled if the AD9874's CLK oscillators are enabled. This is due to the dc current required by the CLK oscillators in each device. In essence, these negative impedance cores are operating in parallel, increasing the effective Q of the LC resonator circuit. Note, RBIAS should be sized such that the sum of the oscillators' dc bias currents maintains a common-mode voltage of around 1.6 V.

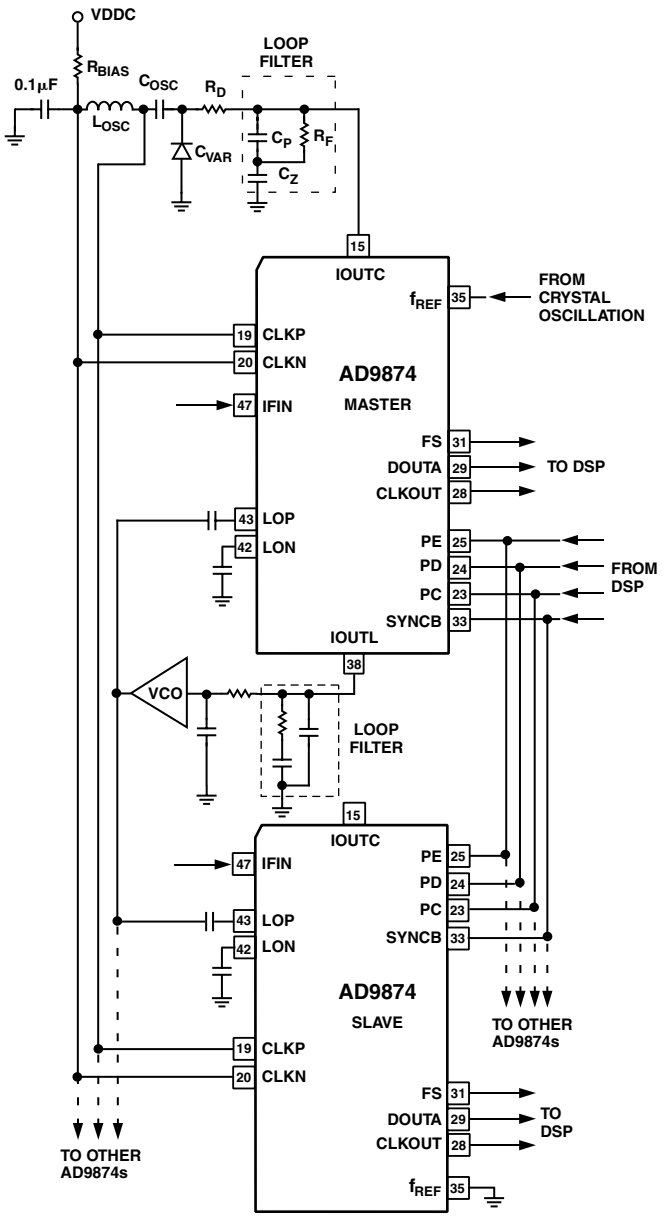


Figure 28. Example of Synchronizing Multiple AD9874s

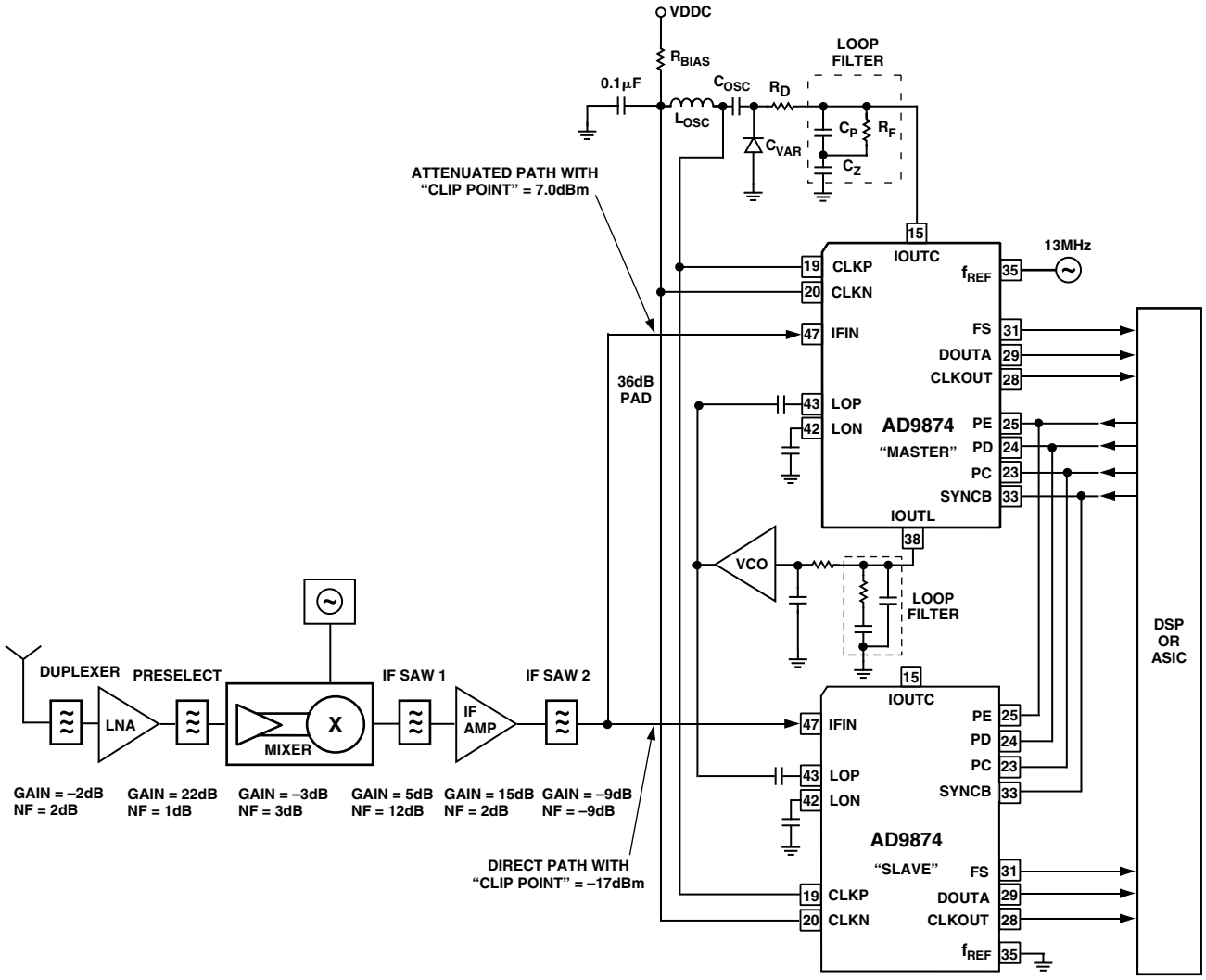


Figure 29. Example of Split Path Rx Architecture to Increase Receiver Dynamic Range Capabilities

"Split Path" Rx Architecture

A split path Rx architecture may be attractive for those applications whose instantaneous dynamic range requirements exceed the capability of a single AD9874 device. To cope with these higher dynamic range requirements, two AD9874s can be operated in parallel with their respective clip points offset by a fixed amount. Adding a fixed amount of attenuation in front of the AD9874, and/or programming the attenuation setting of its internal VGA, can adjust the input-referred clip point. To save power and simplify hardware, the LO and CLK circuits of the device can also be shared. Connecting the SYNCB pins of the two devices together and pulsing this line low synchronizes the two devices.

An example of this concept for possible use in a GSM base station is shown in Figure 29. The signal chain consists of a high linearity RF front end and IF stage followed by two AD9874s operating in parallel. The RF front end consists of a duplexer and preselect filter to pass the GSM RF band of interest. A high performance LNA isolates the duplexer from the preselect filter while providing sufficient gain to minimize system NF. An RF mixer is used to downconvert the entire GSM band to a suitable IF where much of the channel selectivity is accomplished. The 170.6 MHz IF is chosen to avoid any self-induced spurs from the AD9874. The IF stage consists of two SAW filters isolated by a 15 dB gain stage. The cascaded SAW filter response must provide sufficient blocker rejection in order for the receiver to meets its sensitivity requirements under worst-case blocker conditions. A composite response having 27, 60, and 100 dB rejection at frequency offsets of ±0.8 MHz, ±1.6 MHz, and ±6.5 MHz, respectively, provides enough blocker suppression to ensure that the AD9874 with the lower clip point will not be overdriven by any blocker. This configuration results in the best possible receiver sensitivity under all blocking conditions.

The output of the last SAW filters drives the two AD9874 via a direct signal path and an attenuated signal path. The direct path corresponds to the AD9874 having the lowest clip point and provides the highest receiver sensitivity with a system noise figure of 4.7 dB. The VGA of this device is set for maximum attenuation, so its clip point is approximately –17 dBm. Since conversion gain from the antenna to the AD9874 is 19 dB, the digital output of this path will nominally be selected unless the target signal's power exceeds –36 dBm at the antenna. The attenuated path corresponds to the AD9874 having the highest input-referred clip point and its digital output point of this path is set to 7 dBm by inserting a 30 dB attenuator and setting the AD9874's VGA to the middle of its 12 dB range. This setting

gives a ±6 dB adjustment of the clip point, allowing the clip point difference to be calibrated to exactly 24 dB so that a simple 5-bit shift would make up the gain difference. The attenuated path can handle signal levels up to –12 dB at the antenna before being overdriven. Since the SAW filters provide sufficient blocker suppression, the digital data from this path need only be selected when the target signal exceeds –36 dBm. Although the sensitivity of the receiver with the attenuated path is 20 dB lower than the direct path, the strong target signal ensures a sufficiently high carrier-to-noise ratio.

Since GSM is based on a TDMA scheme, digital data (or path) selection can occur on a slot-by-slot basis. The AD9874 would be configured to provide Serial I and Q data at a frame rate of 541.67 kSPS as well as some additional information including a 2-bit reset field and a 6-bit RSSI field. These two fields contain the information needed to decide whether the direct or the attenuated path should be used for the current time slot.

Hung Mixer Mode

The AD9874 can be operated in the "hung mixer" mode by tying one of the LO's self-biasing inputs to ground (i.e., GNDI) or the positive supply (VDDI). In this mode, the AD9874 acts as a narrow-band, band-pass Σ-Δ ADC, since its mixer passes the IFIN signal without any frequency translation. The IFIN signal must be centered about the resonant frequency of the Σ-Δ ADC (i.e., $f_{CLK}/8$) and the clock rate, f_{CLK}, and decimation factors must be selected to accommodate the bandwidth of the desired input signal. Note: the LO synthesizer can be disabled since it is no longer required.

Since the mixer does not have any losses associated with the mixing operation, the conversion gain through the LNA and mixer is higher resulting in a nominal input "clip point" of –24 dBm. The linearity or IIP3 performance of the LNA and mixer remains roughly unchanged and similar to that shown in Figure 11b. The SNR performance is dependent of the VGA attenuation setting, I/Q data resolution, and output bandwidth as shown in Figure 30. Applications requiring the highest instantaneous dynamic range should set the VGA for maximum attenuation. Also, several extra dB in SNR performance can be gained at lower signal bandwidths by using 24-bit I/Q data.

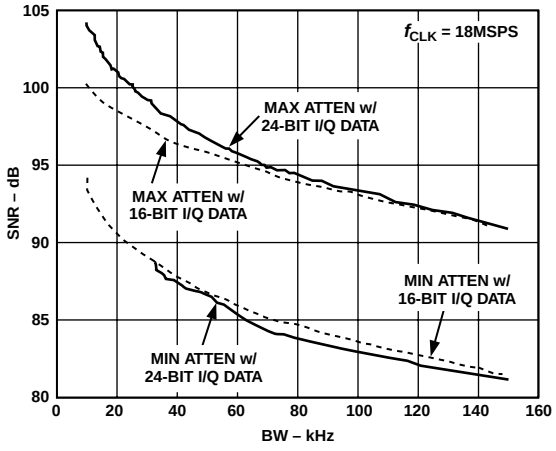


Figure 30. "Hung Mixer" SNR vs. BW and VGA

LAYOUT EXAMPLE, EVALUATION BOARD, AND SOFTWARE

The evaluation board and its accompanying software provide a simple way to evaluate the AD9874. The block diagram in Figure 31 shows the major blocks of the evaluation board. The evaluation board is designed to be flexible, allowing the user to configure it for different applications.

The power supply distribution block provides filtered, adjustable voltages to the various supply pins of the AD9874. In the IF input signal path, component pads are available to implement different IF impedance matching networks. The LO and CLK signals can be externally applied or internally derived from a user-supplied VCO module interface daughter board. The reference for the on-chip LO and CLK synthesizers can be applied via the external f_{REF} input or an on-board crystal oscillator.

The evaluation board is designed to interface to a PC via a National Instruments NI 6533 digital IO card. An XILINX FPGA formats the data between the AD9874 and digital I/O card.

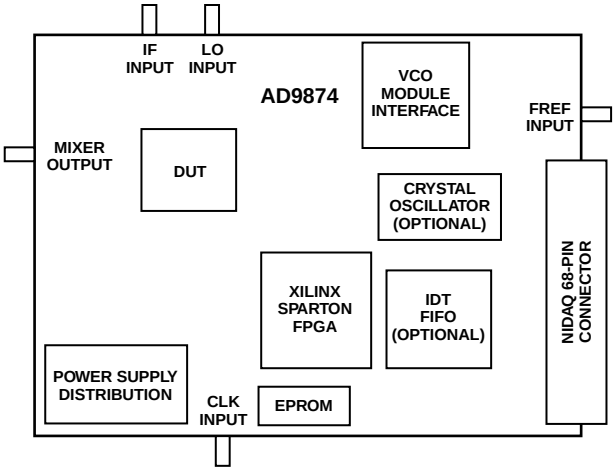


Figure 31. Evaluation Board Platform

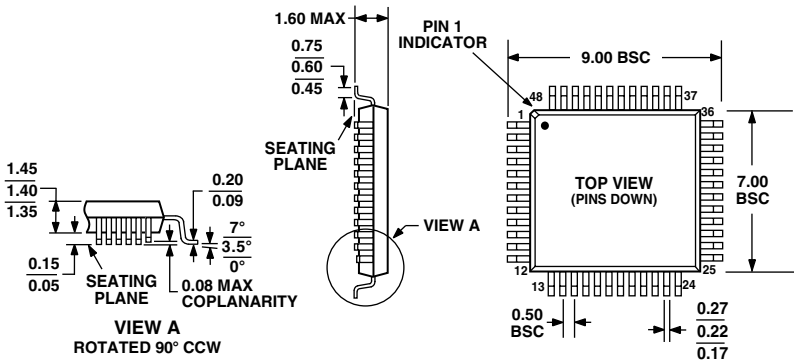
Software developed using National Instruments' LabVIEW™ (and provided as Microsoft® Windows® executable programs) is supplied for the configuration of the SPI port registers and evaluation of the AD9874 output data. These programs have a convenient graphical user interface allowing for easy access to the various SPI port configuration registers and realtime frequency analysis of the output data.

For more information on the AD9874 evaluation board, including an example layout, please refer to the EVAL-AD9874 EBI data sheet.

OUTLINE DIMENSIONS

48-Lead Plastic Quad Flatpack [LQFP]
(ST-48)

Dimensions shown in millimeters



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