XCR22LV10: 3V Zero Power, TotalCMOS, Universal PLD Device

DS047 (v1.1) February 10, 2000 Product Specification

Features

- Industry's first TotalCMOS™ SPLD - both CMOS design and process technologies
- Fast Zero Power (FZP™) design technique provides ultra-low power and high speed
  - Static current of less than 45 µA
  - Dynamic current substantially below that of competing devices
  - Pin-to-pin delay of only 10 ns
- True Zero Power device with no turbo bits or power down schemes
- Function/JEDEC map compatible with Bipolar, UVCMOS, EECMOS 22V10s
- Multiple packaging options featuring PCB-friendly flow-through pinouts (SOL and TSSOP)
  - 24-pin TSOIC–uses 93% less in-system space than a 28-pin PLCC
  - 24-pin SOIC
  - 28-pin PLCC with standard JEDEC pinout
- Available in commercial and industrial operating ranges
- Supports mixed voltage systems—5V tolerant I/Os
- Advanced 0.5µ E^2CMOS process
- 1000 erase/program cycles guaranteed
- 20 years data retention guaranteed
- Varied product term distribution with up to 16 product terms per output for complex functions
- Programmable output polarity
- Synchronous preset/asynchronous reset capability
- Security bit prevents unauthorized access
- Electronic signature for identification
- Design entry and verification using industry standard CAE tools
- Reprogrammable using industry standard device programmers

Description

The XCR22LV10 is the first SPLD to combine high performance with low power, without the need for "turbo bits" or other power down schemes. To achieve this, Xilinx has used their FZP design technique, which replaces conventional sense amplifier methods for implementing product terms (a technique that has been used in PLDs since the bipolar era) with a cascaded chain of pure CMOS gates. This results in the combination of low power and high speed that has previously been unattainable in the PLD arena. For 5V operation, Xilinx offers the XCR22V10 that offers high speed and low power in a 5V implementation.

The XCR22LV10 uses the familiar AND/OR logic array structure, which allows direct implementation of sum-of-products equations. This device has a programmable AND array which drives a fixed OR array. The OR sum of products feeds an "Output Macro Cell" (OMC), which can be individually configured as a dedicated input, a combinatorial output, or a registered output with internal feedback.

Functional Description

The XCR22LV10 implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility (Figure 1).

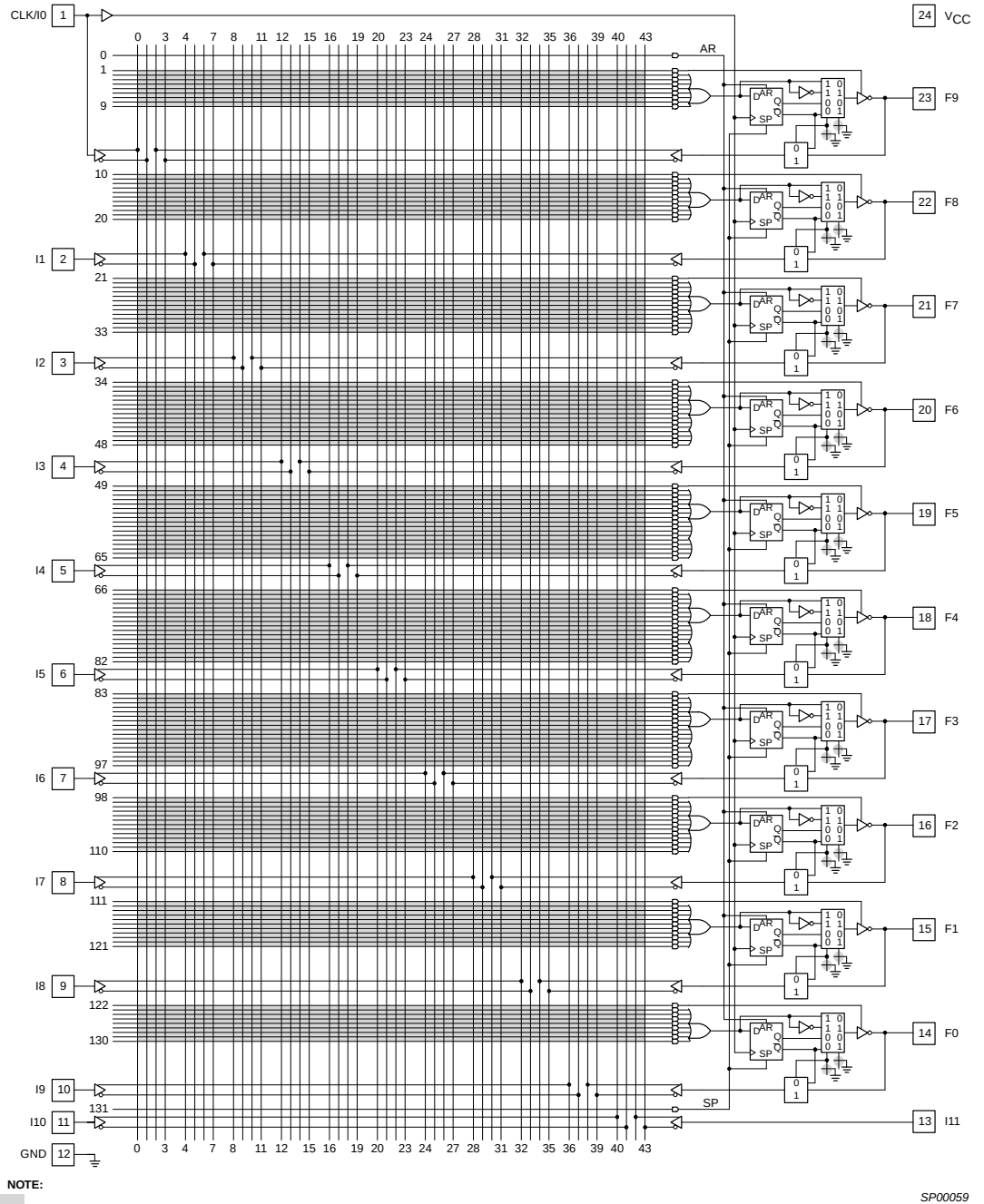


Figure 1: XCR22LV10 Logic Diagram

Architecture Overview

The XCR22LV10 architecture is illustrated in Figure. Twelve dedicated inputs and ten I/Os provide up to 22 inputs and ten outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed-OR array. With this structure, the XCR22LV10 can implement up to ten sum-of-products logic expressions.

Associated with each of the ten OR functions is an I/O macrocell which can be independently programmed to one of four different configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions with either active High or active Low polarity.

AND/OR Logic Array

The programmable AND array of the XCR22LV10 (shown in the Logic Diagram, Figure 1) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

44 input lines:

- 24 input lines carry the True and Complement of the signals applied to the 12 input pins
- 20 additional lines carry the True and Complement values of feedback or input signals from the ten I/Os
- 132 product terms:
- 120 product terms (arranged in two groups of 8, 10, 12, 14, and 16) used to form logical sums
- Ten output enable terms (one for each I/O)
- One global synchronous preset product term
- One global asynchronous clear product term

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input AND gate. A product term which is connected to both the True and Complement of an input signal will always be FALSE, and thus will not affect the OR function that it drives. When all the connections on a product term are opened, a Don't Care state exists and that term will always be TRUE.

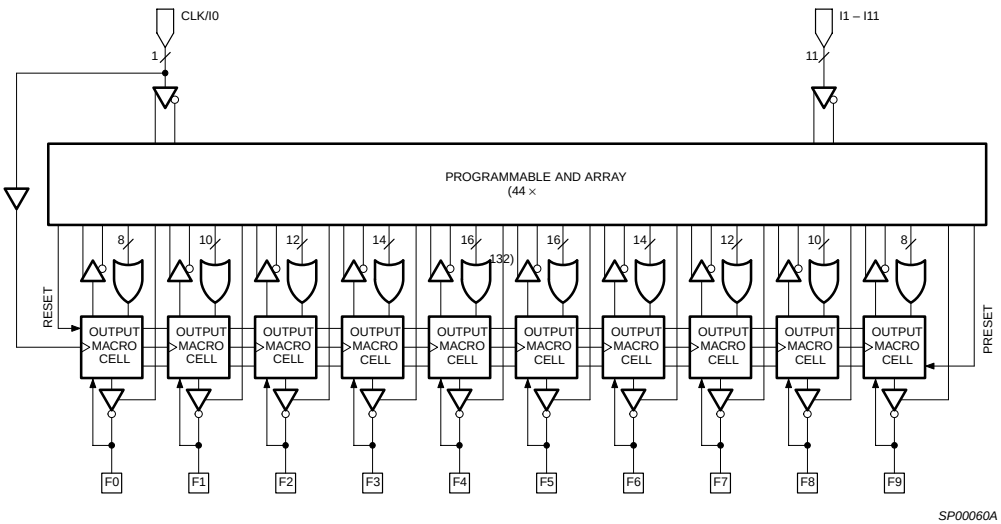


Figure 2: Functional Diagram

Variable Product Term Distribution

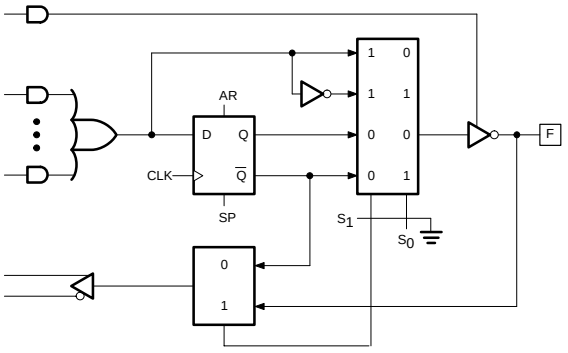
The XCR22LV10 provides 120 product terms to drive the ten OR functions. These product terms are distributed among the outputs in groups of 8, 10, 12, 14, and 16 to form logical sums (see Logic Diagram). This distribution allows optimum use of device resources.

Programmable I/O Macrocell

The output macrocell provides complete control over the architecture of each output. the ability to configure each output independently permits users to tailor the configuration of the XCR22LV10 to the precise requirements of their designs.

Macrocell Architecture

Each I/O macrocell, as shown in Figure 3 consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell of the XCR22LV10 is determined by the two EEPROM bits controlling these multiplexers. These bits determine output polarity, and output type (registered or non-registered). Equivalent circuits for the macrocell configurations are illustrated in Figure 4.



S_1	S_0	OUTPUT CONFIGURATION
0	0	Registered/Active-LOW/Macrocell feedback
0	1	Registered/Active-HIGH/Macrocell feedback
1	0	Combinatorial/Active-LOW/Pin feedback
1	1	Combinatorial/Active-HIGH/Pin feedback

0 = Unprogrammed fuse
1 = Programmed fuse

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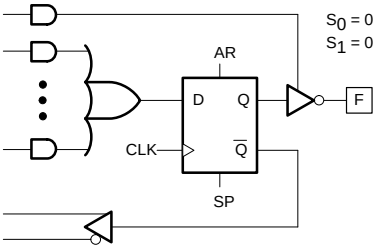
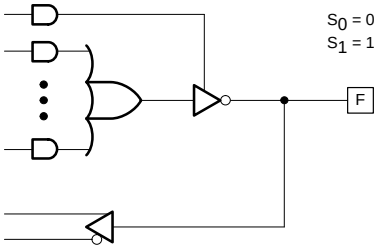
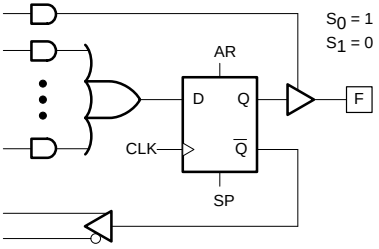
Figure 3: Output Macrocell Logic Diagram



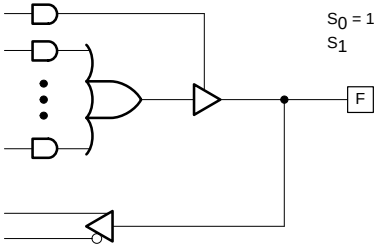
a. Registered/Active-LOW



c. Combinatorial/Active-LOW



b. Registered/Active-HIGH



d. Combinatorial/Active-HIGH

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Figure 4: Output Macrocell Configurations

Output Type

The signal from the OR array can be fed directly to the output pin (combinatorial function) or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set High at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Program/Erase Cycles

The XCR22LV10 is 100% testable, erases/programs in seconds, and guarantees 1000 program/erase erase cycles.

Output Polarity

Each macrocell can be configured to implement active High or active Low logic. Programmable polarity eliminates the need for external inverters.

Output Enable

The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bidirectional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will always be logically FALSE and the I/O will function as a dedicated input.

Register Feedback Select

When the I/O macrocell is configured to implement a registered function (S1=0) (Figure 4a or Figure 4b), the feedback signal to the AND array is taken from the Q output.

Bi-directional I/O Select

When configuring an I/O macrocell to implement a combinatorial function (S1=1) (Figure 4c or Figure 4d), the feedback signal is taken from the I/O pin. In this case, the pin can be used as a dedicated input, a dedicated output, or a bi-directional I/O.

Power-On Reset

To ease system initialization, all flip-flops will power-up to a reset condition and the Q output will be low. The actual output of the XCR22LV10 will depend on the programmed output polarity. The V_{CC} rise must be monotonic.

Design Security

The XCR22LV10 provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set, it is impossible to verify (read) or program the XCR22LV10 until the entire device has first been erased with the bulk-erase function.

TotalCMOS Design Technique for Fast Zero Power

Xilinx is the first to offer a TotalCMOS SPLD, both in process technology and design technique. Xilinx employs a cascade of CMOS gates to implement its Sum of Products instead of the traditional sense amp approach. This CMOS gate implementation allows Xilinx to offer SPLDs which are both high performance and low power, breaking the paradigm that to have low power, you must accept low performance. Refer to Figure 5 and Table 1 showing the I_{CC} vs. Frequency of our XCR22LV10 TotalCMOS SPLD.

Table 1: Typical I_{CC} vs. Frequency @ V_{CC} = 3.3V, 25°C

Frequency (MHz)	Tupical I_{CC} (mA)
1	0.2
10	1.5
20	3.0
30	4.5
40	6.0
50	7.4
60	8.9
70	10.4
80	11.8
90	13.2
100	14.5
110	15.8
120	17.0
130	18.2

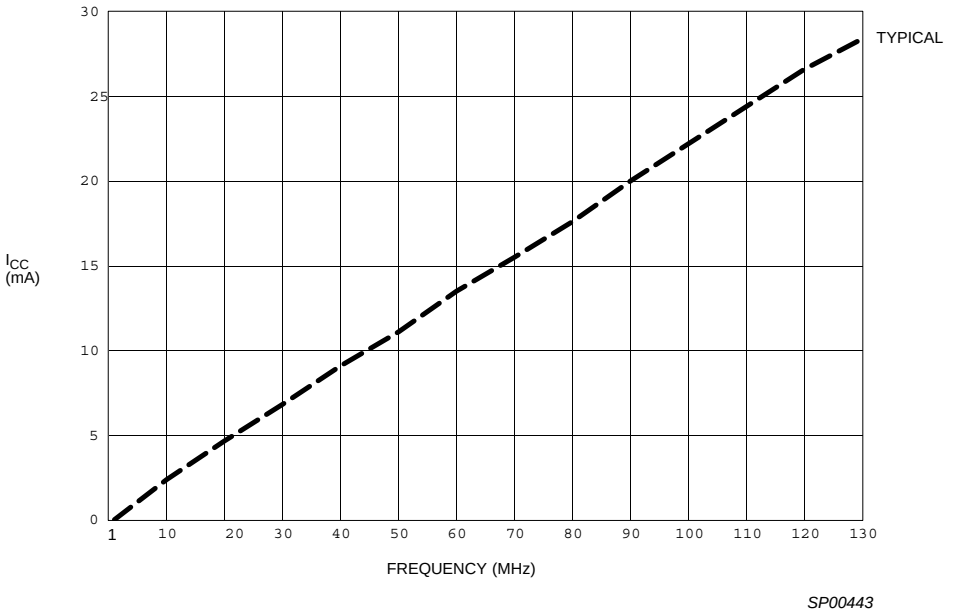


Figure 5: Typical I_{CC} vs. Frequency @ V_{CC} = 3.3V, 25°C (10-bit counter)

Absolute Maximum Ratings[1]

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	–0.5	4.6	V
V_I	Input voltage	–0.5	5.5[2]	V
V_{OUT}	Output voltage	–0.5	5.5[2]	V
I_{IN}	Input current	–30	30	mA
I_{OUT}	Output current	–100	100	mA
T_R	Allowale thermal rise ambient to junction	0	75	°C
T_J	Maximum junction temperature	–40	150	°C
T_{STG}	Storage temperature	–65	150	°C

Notes:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification is not implied..
2. Except F7, where max = V_{CC} + 0.5V.

Operating Range

Product Grade	Temperature	Voltage
Commercial	0 to +70°C	3.3V ± 10%
Industrial	–40 to +85°C	3.3V ± 10%

DC Electrical Characteristics For Commercial Grade Devices

Commercial: 0°C ≤ T_{AMB} ≤ +70°C; 3.03.6V ≤ V_{CC} ≤ 3.6V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input voltage Low	V_{CC} = 3.0V			0.8	V
V_{IH}	Input voltage High	V_{CC} = 3.6V	2			V
V_I	Input clamp voltage	V_{CC} = 3.0V, I_{IN} = –18 mA			–1.2	V
V_{OL}	Output voltage Low	V_{CC} = 3.0V, I_{OL} = 8 mA			0.5	V
V_{OH}	Output voltage High	V_{CC} = 3.0V, I_{OH} = –4 mA	2.4			V
I_I	Input leakage current	V_{IN} = 0V to V_{CC}	–10		10	µA
		V_{IN} = V_{CC} to 5.5V [2]	–10		10	
I_{OZL}	3-stated output leakage current	V_{IN} = 0V to V_{CC}	–10		10	µA
		V_{IN} = V_{CC} to 5.5V [2]	–10		10	
I_{CCQ}	Standby current	V_{CC} = 3.6V, T_{AMB} = 0°C		25	45	µA
I_{CCD} [1]	Dynamic current	V_{CC} = 3.6V, T_{AMB} = 0°C at 1 MHz		0.5	2	mA
		V_{CC} = 3.6V, T_{AMB} = 0°C at 50 MHz		10	15	mA
I_{OS}	Short circuit output current	One pin at a time for no longer than 1 second	–15		–100	mA
C_{IN}	Input pin capacitance	T_{AMB} = 25°C, f = 1 MHz			8	pF
C_{CLK}	Clock input capacitance	T_{AMB} = 25°C, f = 1 MHz	5		12	pF
$C_{I/O}$	I/O pin capacitance	T_{AMB} = 25°C, f = 1 MHz			10	pF

Notes:

1. This parameter measured with a 10-bit, with all outputs enabled and unloaded. Inputs are tied to V_{CC} or ground. This parameter is not 100% tested, but is calculated at initial characterization and at any time the design is modified where current may be affected.
2. Does not apply to F7.

AC Electrical Characteristics For Commercial Grade Devices

Commercial: $0°C \le T_{AMB} \le +70°C$; $3.0V \le V_{CC} \le 3.6V$

Symbol	Parameter	-B		-D		Unit
		Min.	Max.	Min.	Max.	
t_{PD}	Propagation delay time, input or feedback to non-registered output		15		10	ns
t_{SU}	Setup time from input, feedback or SP to Clock	4.5		3.5		ns
t_{CO}	Clock to output		10		9	ns
t_{CF}	Clock to feedback[1]		6		4.5	ns
t_H	Holt time		0		0	ns
t_{AR}	Asynchronous Reset to registered output		17		17	ns
t_{ARW}	Asynchronous Reset width	5		5		ns
t_{ARR}	Asynchronous Reset recovery time		6		6	ns
t_{SPF}	Synchronou Preset recovery time		6		6	ns
t_{WL}	Width of Clock Low	3		3		µs
t_{WH}	Width of Clock High	3		3		µs
t_R	Input rise time		20		20	ns
t_F	Input fall time		20		20	ns
f_{MAX1}	Maximum FF toggle rate[2] $(1/t_{SU} + t_{CF})$	95		125		MHz
f_{MAX2}	Maximum internal frequency[1] $(1/t_{SU} + t_{CO})$	69		80		MHz
f_{MAX3}	Maximum external frequency[1] $(1/t_{WL} + t_{WH})$	167		167		MHz
t_{EA}	Input to output enable		9		9	ns
t_{ER}	Input to output disable		9		9	ns
Capacitance						
C_{IN}	Input pin capacitance		10		10	pF
C_{OUT}	Output capacitance		10		10	pF

Notes:
1. This parameter is not 100% tested, but is calculated at initial characterization and at any time the design is modified where current may be affected.
2. This parameter measured with a 10-bit, with all outputs enabled and unloaded. Inputs are tied to V_{CC} or ground. This parameter is not 100% tested, but is calculated at initial characterization and at any time the design is modified where current may be affected.

DC Electrical Characteristics For Industrial Grade Devices

Industrial: $-40°C \le T_{AMB} \le +85°C$; $3.0V \le V_{CC} \le 3.6V$

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input voltage Low	V_{CC} = 3.0V			0.8	V
V_{IH}	Input voltage High	V_{CC} = 3.6V	2			V
V_I	Input clamp voltage	V_{CC} = 3.0V, I_{IN} = –18 mA			–1.2	V
V_{OL}	Output voltage Low	V_{CC} = 3.0V, I_{OL} = 8 mA			0.5	V
V_{OH}	Output voltage High	V_{CC} = 3.0V, I_{OH} = –4 mA	2.4			V
I_I	Input leakage current	V_{IN} = 0V to V_{CC}	–10		10	µA
		V_{IN} = V_{CC} to 5.5V [2]	–10		10	
I_{OZL}	3-stated output leakage current	V_{IN} = 0V to V_{CC}	–10		10	µA
		V_{IN} = V_{CC} to 5.5V [2]	–10		10	
I_{CCQ}	Standby current	V_{CC} = 3.6V, T_{AMB} = –40°C		30	45	µA
I_{CCD} [1]	Dynamic current	V_{CC} = 3.6V, T_{AMB} = –40°C at 1 MHz		0.5	3	mA
		V_{CC} = 3.6V, T_{AMB} = –40°C at 50 MHz		10	20	mA
I_{OS}	Short circuit output current	One pin at a time for no longer than 1 second	–15		–100	mA
C_{IN}	Input pin capacitance	T_{AMB} = 25°C, f = 1 MHz			8	pF
C_{CLK}	Clock input capacitance	T_{AMB} = 25°C, f = 1 MHz	5		12	pF
$C_{I/O}$	I/O pin capacitance	T_{AMB} = 25°C, f = 1 MHz			10	pF

Notes:

1. This parameter measured with a 10-bit, with all outputs enabled and unloaded. Inputs are tied to V_{CC} or ground. This parameter is not 100% tested, but is calculated at initial characterization and at any time the design is modified where current may be affected.
2. Does not apply to F7.

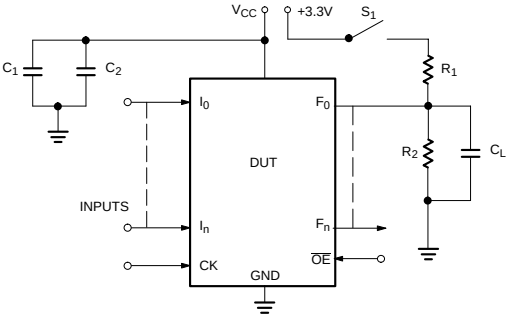
AC Electrical Characteristics For Industrial Grade Devices

Industrial: $-40°C \le T_{AMB} \le +85°C$; $3.0V \le V_{CC} \le 3.6V$

Symbol	Parameter	Min.	Max.	Unit
t_{PD}	Propagation delay time, input or feedback to non-registered output		15	ns
t_{SU}	Setup time from input, feedback or SP to Clock	5		ns
t_{CO}	Clock to output		10.5	ns
t_{CF}	Clock to feedback[1]		6	ns
t_H	Holt time		0	ns
t_{AR}	Asynchronous Reset to registered output		17	ns
t_{ARW}	Asynchronous Reset width	5		ns
t_{ARR}	Asynchronous Reset recovery time		6	ns
t_{SPF}	Synchronou Preset recovery time		6	ns
t_{WL}	Width of Clock Low	3		µs
t_{WH}	Width of Clock High	3		µs
t_R	Input rise time		20	ns
t_F	Input fall time		20	ns
f_{MAX1}	Maximum FF toggle rate[2] $(1/t_{SU} + t_{CF})$	91		MHz
f_{MAX2}	Maximum internal frequency[1] $(1/t_{SU} + t_{CO})$	65		MHz
f_{MAX3}	Maximum external frequency[1] $(1/t_{WL} + t_{WH})$	167		MHz
t_{EA}	Input to output enable		11	ns
t_{ER}	Input to output disable		11	ns
Capacitance				
C_{IN}	Input pin capacitance		10	pF
C_{OUT}	Output capacitance		12	pF

Notes:
1. This parameter is not 100% tested, but is calculated at initial characterization and at any time the design is modified where current may be affected.
2. This parameter measured with a 10-bit, with all outputs enabled and unloaded. Inputs are tied to V_{CC} or ground. This parameter is not 100% tested, but is calculated at initial characterization and at any time the design is modified where current may be affected.

Test Load Circuit



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.
R_1 = 300Ω, R_2 = 300Ω, C_L = 35pF.

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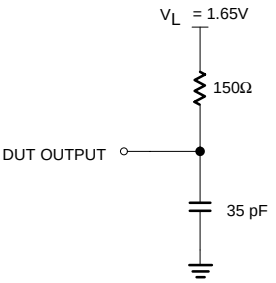
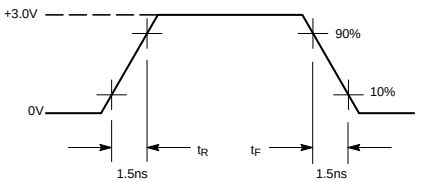
Thevenin Equivalent



Voltage Waveform



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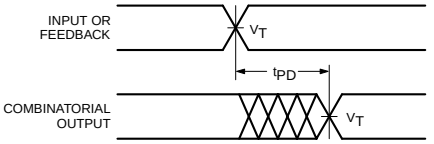
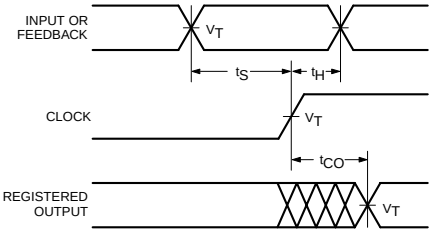
MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

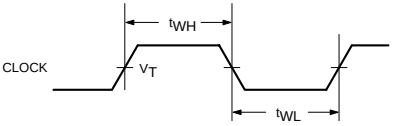
Switching Waveforms



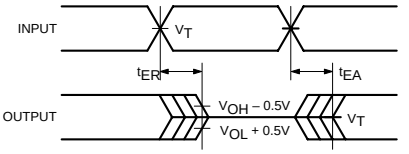
Combinatorial Output



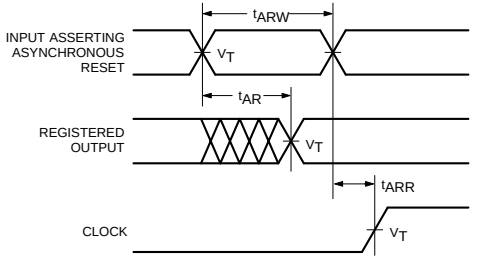
Registered Output



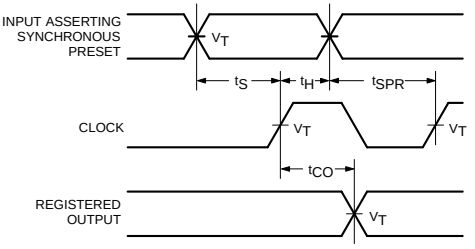
Clock Width



Input to Output Disable/Enable



Asynchronous Reset



Synchronous Preset

NOTES:
1. V_T = 1.5V.
2. Input pulse amplitude 0V to 3.0V.
3. Input rise and fall times 2.0 ns max.

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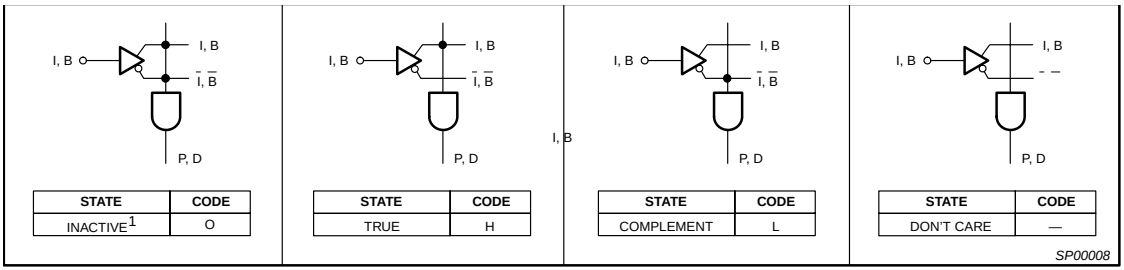
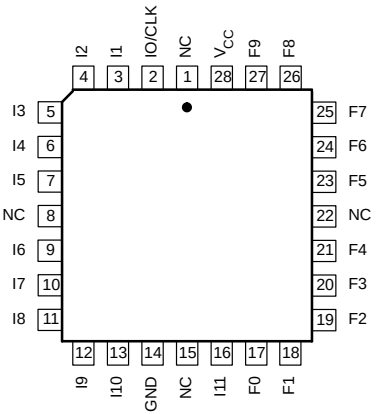
"AND" Array: (I,B)



Pin Configurations

28-pin PLCC



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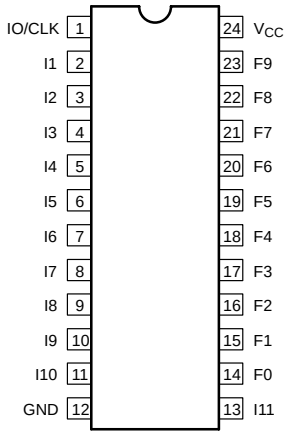
24-pin SOIC and 24-pin TSOIC

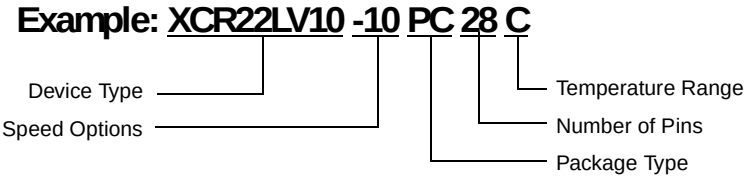


AP00475

Pin Descriptions

Pin Label	Description
I1-I11	Dedicated input
NC	Not Connected
F0-F9	Macrocell Input/Output
I0/CLK	Dedicated Input/Clock Output
V_{CC}	Supply Voltage
GND	Ground

Ordering Information



Speed Options
-15: 15 ns pin-to-pin delay
-10: 10 ns pin-to-pin delay

Temperature Range
C = Commercial, T_A = 0°C to +70°C
I = Industrial, T_A = –40°C to +85°C

Packaging Options
SO24: 24-pin SOIC
VO24: 24-pin TSOIC
PC28: 28-pin PLCC

Component Availability

Pins		24		28
Type		Plastic SOIC	Plastic Thin SOIC	Plastic PLCC
Code		SO24	VO24	PC28
XCR22LV10	-15		C, I	C, I
	-10		C	C

Revision History

Date	Version #	Revision
8/4/99	1.0	Initial Xilinx release.
2/10/00	1.1	Convert to Xilinx Format