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# NTE56065
# TRIAC, 600$V_{RM}$, 12A, High Commutation

**Description:**

The NTE56065 is a glass passivated, high commutation TRIAC in an isolated full–pack type package designed for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. This device will commutate the full rated RMS current at the maximum rated junction temperature, without the aid of a snubber.

**Absolute Maximum Ratings:**

Repetitive Peak Off–Sate Voltage (Note 1), $V_{DRM}$ . . . . . 600V

RMS On–State Current (Full Sine Wave, $T_{HS} \le 56°C$), $I_T(RMS)$ . . . . . 12A

Non–Repetitive Peak On–State Current, $I_{TSM}$

(Full Sine Wave, $T_J = +25°C$ prior to Surge)

t = 20ms . . . . . 95A

t = 16.7ms . . . . . 105A

$I^2t$ for Fusing (t = 10ms), $I^2t$ . . . . . $45A^2sec$

Repetitive Rate–of–Rise of On–State Current after Triggering, $dI_T/dt$

($I_{TM} = 20A$, $I_G = 0.2A$, $dI_G/dt = 0.2A/\mu s$) . . . . . 100A/µs

Peak Gate Current, $I_{GM}$ . . . . . 2A

Peak Gate Voltage, $V_{GM}$ . . . . . 5V

Peak Gate Power, $P_{GM}$ . . . . . 5W

Average Gate Power (Over Any 20ms Period), $P_{G(AV)}$ . . . . . 500mW

Operating Junction Temperature, $T_J$ . . . . . +125°C

Storage Temperature Range, $T_{stg}$ . . . . . –40° to +150°C

Thermal Resistance, Junction–to–Heatsink (Full or Half Cycle), $R_{thJHS}$

With Heatsink Compound . . . . . 4.0K/W

Without Heatsink Compound . . . . . 5.5K/W

Typical Thermal Resistance, Junction–to–Ambient, $R_{thJA}$ . . . . . 55K/W

Note 1. Although not recommended, off–state voltages up to 800V may be applied without damage, but the TRIAC may switch to the on–state. The rate–of–rise of current should not exceed 15A/µs.

**Electrical Characteristics:** ($T_J$ = +25°C unless otherwise specfied)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static Characteristics** | | | | | | |
| Gate Trigger Current<br>$MT_2$ (+), G (+) | $I_{GT}$ | $V_D$ = 12V, $I_T$ = 0.1A, Note 2 | 2 | 18 | 50 | mA |
| $MT_2$ (+), G (–) | | | 2 | 21 | 50 | mA |
| $MT_2$ (–), G (–) | | | 2 | 34 | 50 | mA |
| Latching Current<br>$MT_2$ (+), G (+) | $I_L$ | $V_D$ = 12V, $I_T$ = 0.1A | – | 31 | 60 | mA |
| $MT_2$ (+), G (–) | | | – | 34 | 90 | mA |
| $MT_2$ (–), G (–) | | | – | 30 | 60 | mA |
| Holding Current | $I_H$ | $V_D$ = 12V, $I_T$ = 0.1A | – | 31 | 60 | mA |
| On–State Voltage | $V_T$ | $I_T$ = 17A | – | 1.3 | 1.6 | V |
| Gate Trigger Voltage | $V_{GT}$ | $V_D$ = 12V, $I_T$ = 0.1A | – | 0.7 | 1.5 | V |
| | | $V_D$ = 400V, $I_T$ = 0.1A, $T_J$ = +125°C | 0.25 | 0.4 | – | V |
| Off–State Leakage Current | $I_D$ | $V_D$ = 600V, $T_J$ = +125°C | – | 0.1 | 0.5 | mA |
| **Dynamic Characteristics** | | | | | | |
| Critical Rate–of–Rise of Off–State Voltage | $dV_D/dt$ | $V_{DM}$ = 402V, $T_J$ = +125°C, Exponential Waveform, Gate Open | 1000 | 4000 | – | V/µs |
| Critical Rate–of–Change of Commutating Current | $dI_{com}/dt$ | $V_{DM}$ = 400V, $T_J$ = +125°C, $I_T$RMS = 12A, without Snubber, Gate Open | – | 24 | – | A/ms |
| Gate Controlled Turn–On Time | $t_{gt}$ | $I_{TM}$ = 12A, $V_D$ = $V_{DRM}$max, $I_G$ = 0.1A, $dI_G/dt$ = 5A/µs | – | 2 | – | µs |
| **Isolation Characteristics** | | | | | | |
| RMS Isolation Voltage from All 3 Pins to External Heatsink | $V_{ISOL}$ | f = 50 – 60Hz, Sinusoidal Waveform, R.H. ≤ 65%, Clean and Dustfree | – | – | 2500 | V |
| Capacitance from T2 to External Heatsink | $C_{ISOL}$ | f = 1MHz | – | 10 | – | pF |

Note 2. Device does not trigger in the $MT_2$ (–), G (+) quadrant.