

Features

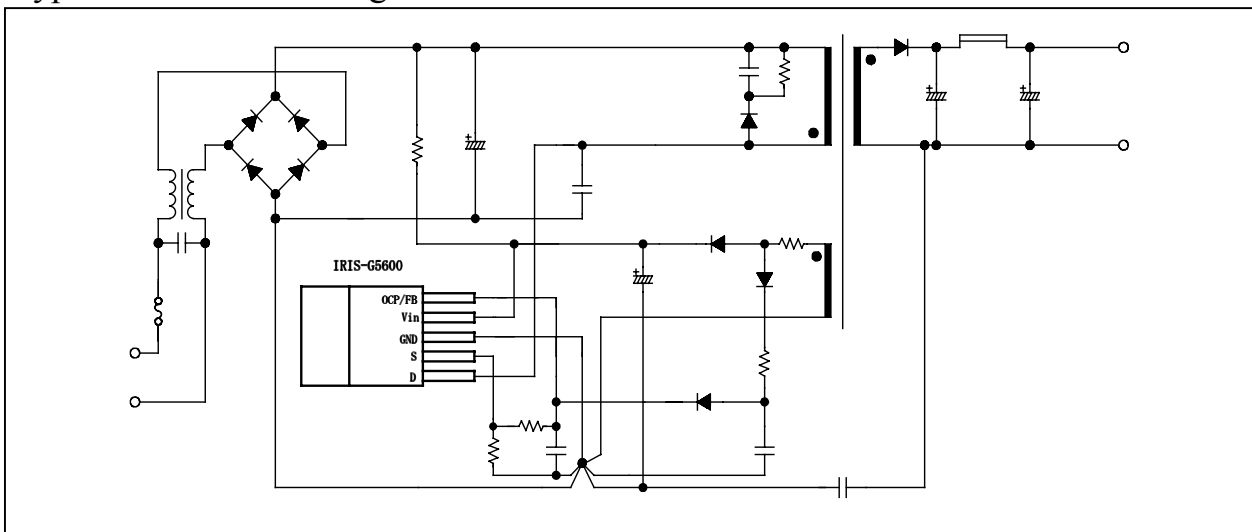
- Oscillator is provided on the monolithic control with adopting On-Chip-Trimming technology.
- Small temperature characteristics variation by adopting a comparator to compensate for temperature on the control part.
- Low start-up circuit current (100uA max)
- Built-in Active Low-Pass Filter for stabilizing the operation in case of light load
- Avalanche energy guaranteed MOSFET with high VDSS
- The built-in power MOSFET simplifies the surge absorption circuit since the MOSFET guarantees the avalanche energy.
- No VDSS de-rating is required.
- Built-in constant voltage drive circuit
- Built-in step drive circuit
- Built-in low frequency PRC mode ($\approx 20\text{kHz}$)
- Various kinds of protection functions
- Pulse-by-pulse Overcurrent Protection (OCP)
- Overvoltage Protection with latch mode (OVP)
- Thermal Shutdown with latch mode (TSD)

Descriptions

IRIS-G5653A is a hybrid IC consists from power MOSFET and a controller IC, designed for Indirect feed-back Quasi-Resonant (including low frequency PRC) fly-back converter type SMPS (Switching Mode Power Supply) applications. This IC realizes high efficiency, low noise, downsizing and standardizing of a power supply system reducing external components count and simplifying the circuit designs.

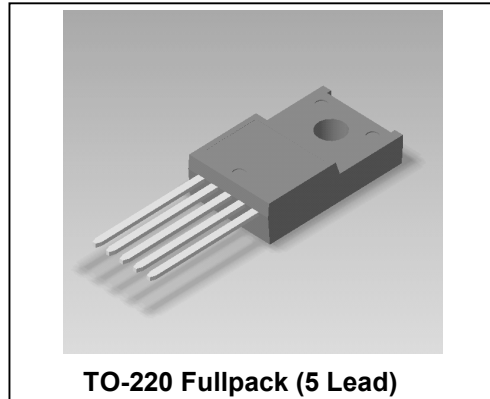
(Note). PRC is abbreviation of "Pulse Ratio Control" (On-width control with fixed OFF-time).

Typical Connection Diagram



INTEGRATED SWITCHER

Package Outline



Key Specifications

Type	MOSFET VDSS(V)	RDS(ON) MAX	AC input(V)	Pout(W) Note 1
IRIS-G5653	650	1.9 Ω	230 \pm 15%	125
			85 to 264	60

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to terminals stated, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Terminals	Max. Ratings	Units	Note
IDpeak	Drain Current *1	1-2	10	A	Single Pulse
IDMAX	Maximum switching current *5	1-2	10	A	V ₂₋₃ =0.78V Ta=-20~+125°C
EAS	Single pulse avalanche energy *2	1-2	80	mJ	Single Pulse VDD=99V, L=20mH IL peak=2.6A
Vin	Input voltage for control part	4-3	35	V	
Vth	O.C.P/F.B Pin voltage	5-3	6	V	
PD1	Power dissipation for MOSFET *3	1-2	26	W	With infinite heatsink
PD2	Power dissipation for control part (Control IC) *4	4-3	1.5	W	Without heatsink
TF	Internal frame temperature in operation	-	0.8	W	Specified by Vin × Iin
Top	Operating ambient temperature	-	-20 ~ +125	°C	Refer to recommended operating temperature
Tstg	Storage temperature	-	-40 ~ +125	°C	
Tch	Channel temperature	-	150	°C	

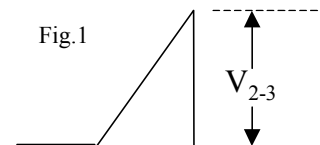
*1 Refer to MOS FET A.S.O curve

*2 MOS FET Tch-EAS curve

*3 Refer to MOS FET Ta-PD1 curve

*4 Refer to TF-PD2 curve for Control IC (See page 5)

*5 Maximum switching current.



The maximum switching current is the Drain current determined by the drive voltage of the IC and threshold voltage (Vth) of MOS FET. Therefore, in the event that voltage drop occurs between Pin 2 and Pin 3 due to patterning, the maximum switching current decreases as shown by V₂₋₃ in Fig.1 Accordingly please use this device within the decrease value, referring to the derating curve of the maximum switching current.

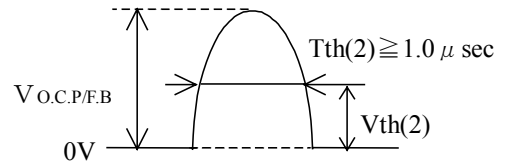
Electrical Characteristics (for Control IC)

Electrical characteristics for control part (Ta=25°C, Vin=18V, unless otherwise specified)

Symbol	Definition	Ratings			Units	Test Conditions
		MIN	TYP	MAX		
V _{in(ON)}	Operation start voltage	14.4	16	17.6	V	V _{in} =0→17.6V
V _{in(OFF)}	Operation stop voltage	9	10	11	V	V _{in} =17.6→9V
I _{m(ON)}	Circuit current in operation	-	-	20	mA	-
I _{m(OFF)}	Circuit current in non-operation	-	-	100	μA	V _{in} =14V
T _{OFF(MAX)}	Maximum OFF time	45	-	55	μsec	-
T _{th(2)}	Minimum time for input of quasi resonant signals *6	-	-	1	μsec	-
T _{OFF(MIN)}	Minimum OFF time *7	-	-	2	μsec	-
V _{th(1)}	O.C.P/F.B Pin threshold voltage 1	0.68	0.73	0.78	V	-
V _{th(2)}	O.C.P/F.B Pin threshold voltage 2	1.3	1.45	1.6	V	-
I _{OCP/FB}	O.C.P/F.B Pin extraction current	1.2	1.35	1.5	mA	-
V _{in(OVP)}	O.V.P operation voltage	34	36.5	39	V	V _{in} =0→39.0V
I _{in(H)}	Latch circuit sustaining current *8	-	-	400	μA	V _{in} =39.0→8.5V
V _{in(La.OFF)}	Latch circuit release voltage *8	6.6	-	8.4	V	V _{in} =39.0→6.6V
T _{j(TSD)}	Thermal shutdown operating temperature	140	-	-	°C	-
V _{in(SENSE)}	Detected Voltage	31.7	32	32.3	V	V _{in} =31.7→32.3V
-	Temperature coefficient of detected voltage	-	2.5	-	mV/°C	V _{in} =31.7→32.3V

*6 Recommended operating conditions

Time for input of quasi resonant signals
For the quasi resonant signal inputted to OCP/FB Pin at the time of quasi resonant operation, the signal shall be wider than T_{th(2)}.



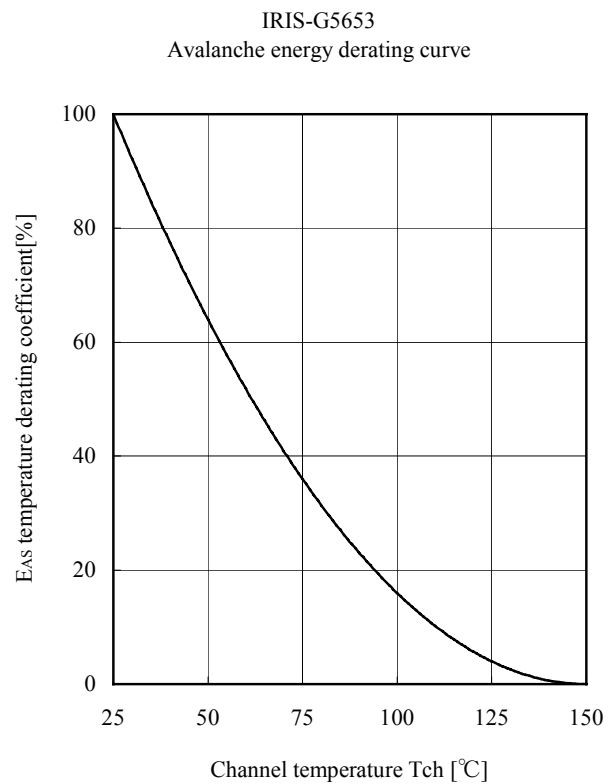
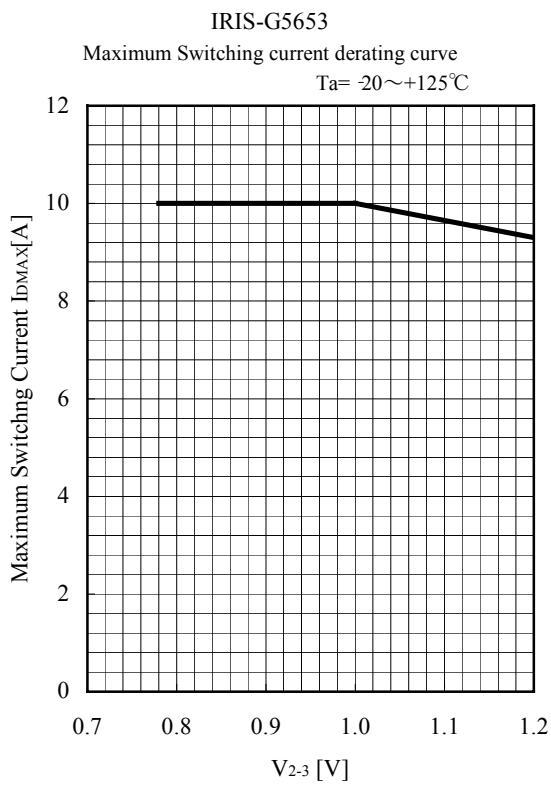
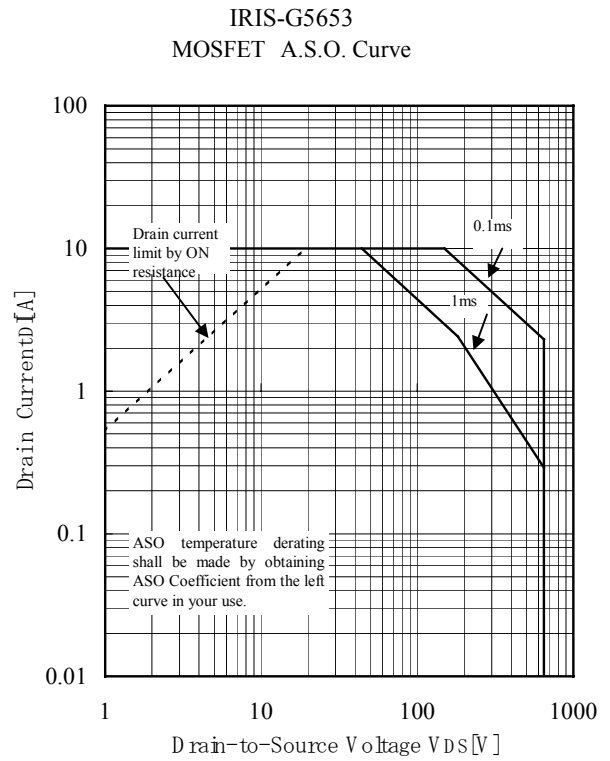
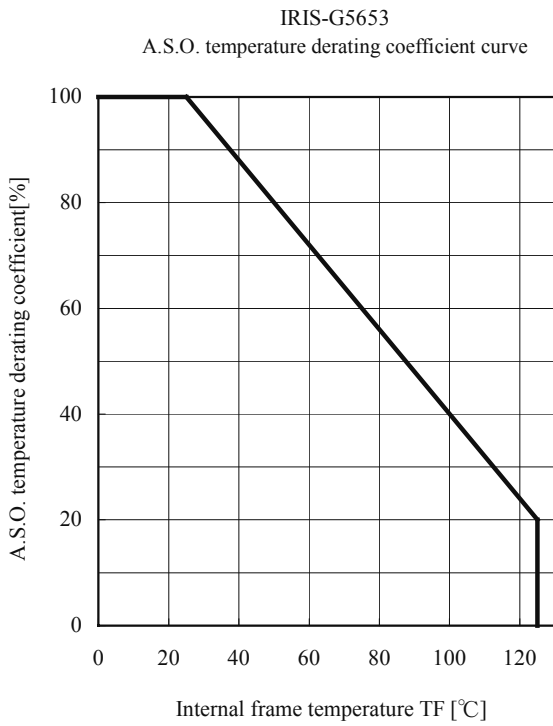
*7 The minimum OFF time means T_{OFF} width at the time when the minimum quasi resonant signal is inputted.

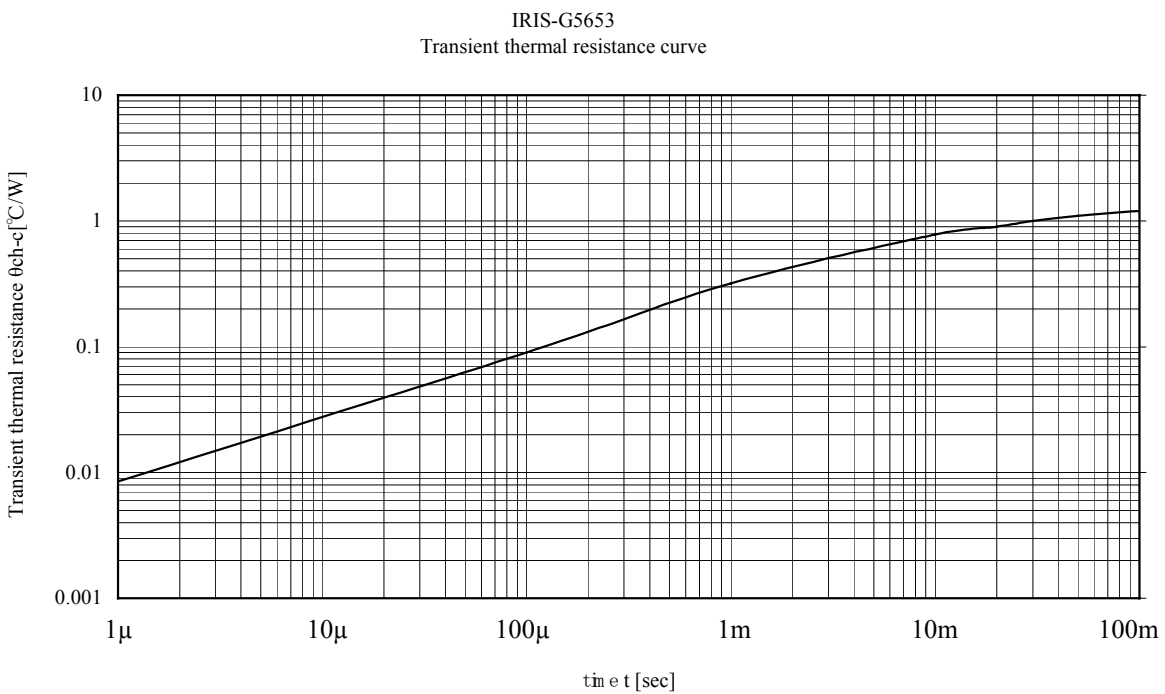
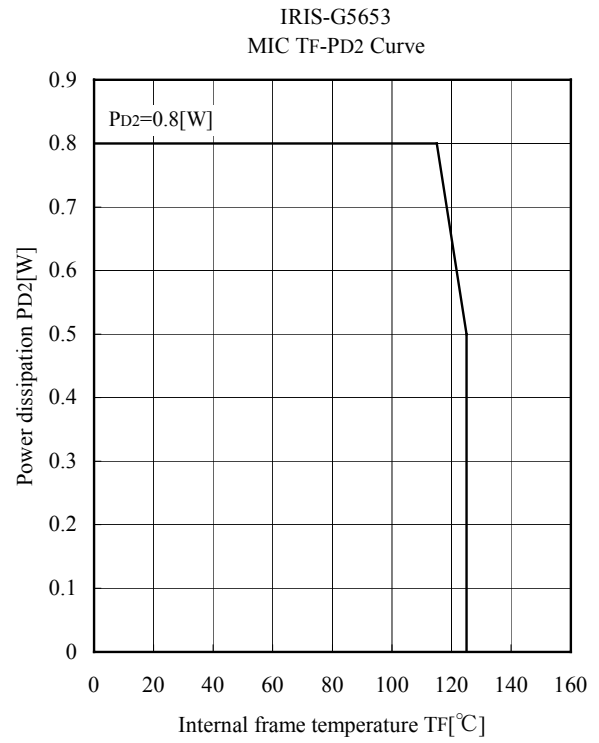
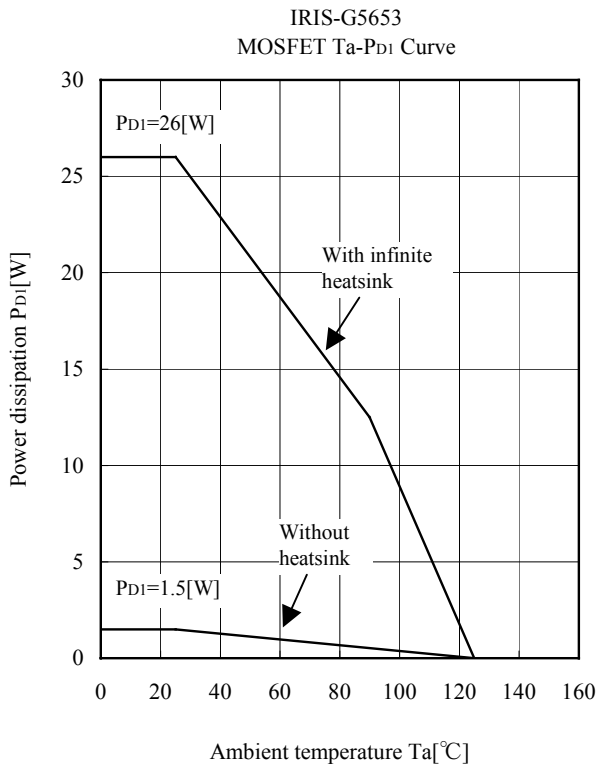
*8 The latch circuit means a circuit operated O.V.P and T.S.D.

Electrical Characteristics (for MOSFET)

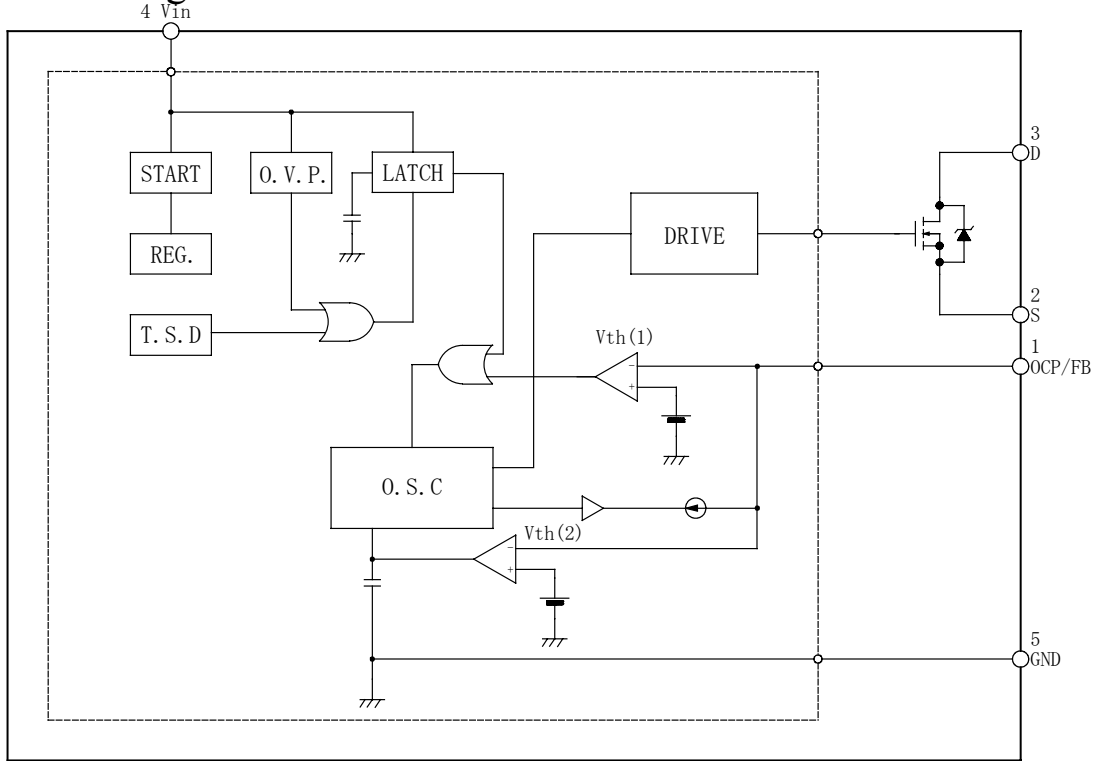
(Ta=25°C) unless otherwise specified

Symbol	Definition	Ratings			Units	Test Conditions
		MIN	TYP	MAX		
V _{DSS}	Drain-to-Source breakdown voltage	650	-	-	V	ID=300μA V3-2=0V(short)
I _{DSS}	Drain leakage current	-	-	300	μA	V _D =650V V3-2=0V(short)
R _{DS(ON)}	On-resistance	-	-	1.9	Ω	V3-2=10V ID=1.2A
t _f	Switching time	-	-	250	nsec	-
θ _{ch-F}	Thermal resistance	-	-	2	°C/W	Between channel and internal frame

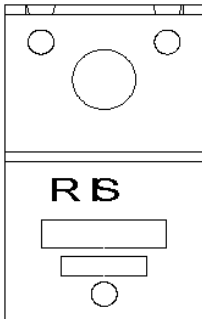




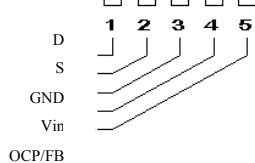
Block Diagram



Lead Assignments



Pin No.	Symbol	Description	Function
1	D	Drain Pin	MOSFET drain
2	S	Source Pin	MOSFET source
3	GND	Ground Pin	Ground
4	Vin	Power supply Pin	Input of power supply for control circuit
5	OCP/FB	Overcurrent / Feedback Pin	Input of overcurrent detection
			signal / constant voltage control signal



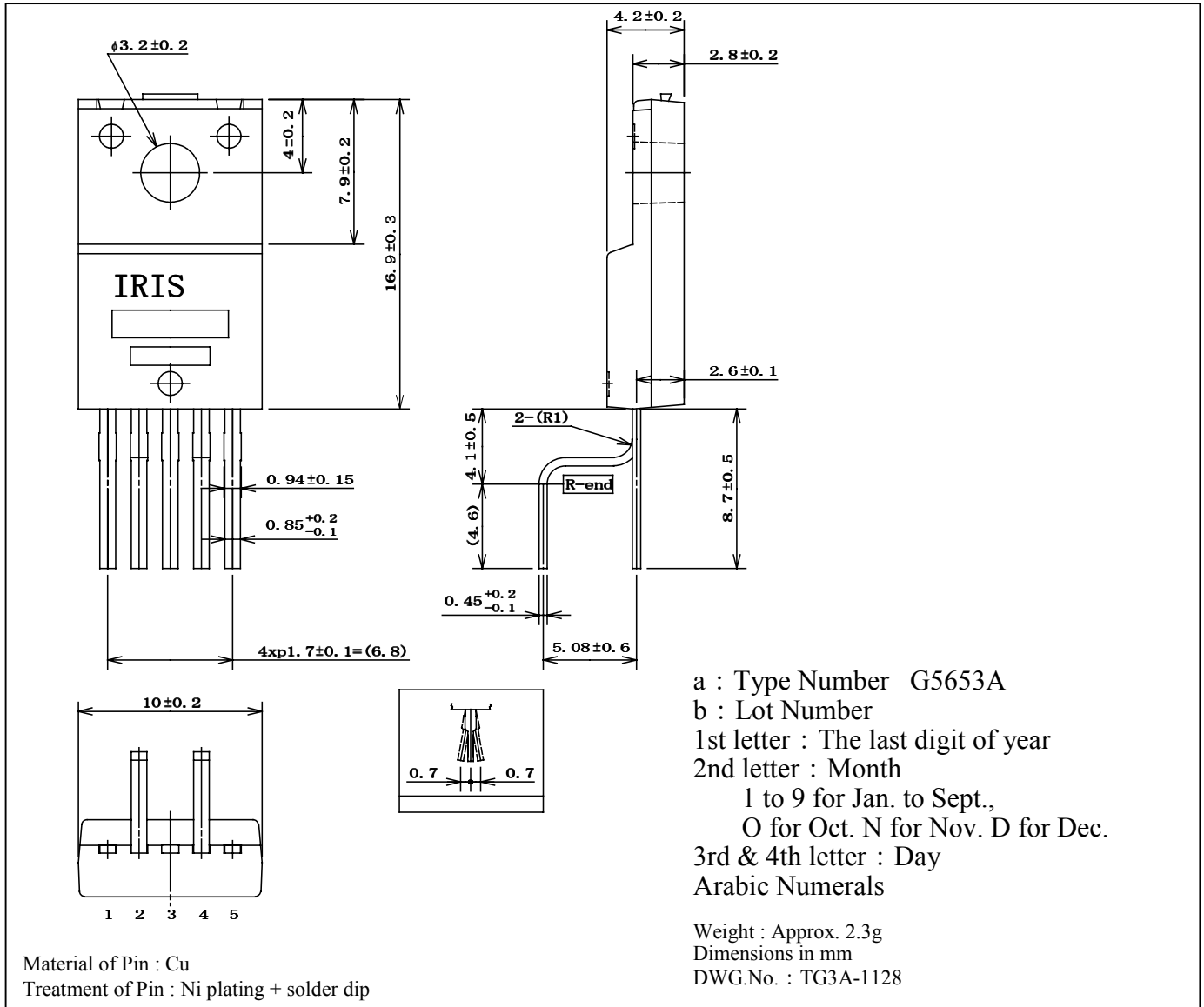
Other Functions

O.V.P. – Overvoltage Protection Circuit

T.S.D. – Thermal Shutdown Circuit

STEP DRV – 2 step drive circuit

Case Outline



a : Type Number G5653A
b : Lot Number
1st letter : The last digit of year
2nd letter : Month
1 to 9 for Jan. to Sept.,
O for Oct. N for Nov. D for Dec.
3rd & 4th letter : Day
Arabic Numerals

Data and specifications subject to change without notice.