Ordering number : ENN*7023

CMOS IC

LC74982W

LCD TV Scan Converter IC

Preliminary

Overview

The LC74982W is an LCD display scan converter IC that converts NTSC and PAL TV signals to XGA resolution. The video signal-processing circuits required to implement an LCD TV set can be easily formed by combining this IC with a digital decoder, a microcontroller, and an LCD panel. Since this IC does not require an external frame memory for resolution conversion, it can contribute to minimizing total costs. As additional functionality, it also provides inputs for personal computer video (up to XGA) and digital TV (480p/480i). Since LC74982W operation is based on expansion (resolution increasing) processing, depending on the input resolution, it can also support use of, for example, 800 × 600 and 800 × 480 dot resolution LCD panels. Thus the LC74982W can be used in a wide range of applications.

Features

- NTSC and PAL input support: 24-bit or 16-bit digital YCbCr signal input
- PC input support: Personal computer 24-bit digital RGB signal input at resolutions up to XGA
- DTV (480i / 480p) input: 24-bit or 16-bit digital YCbCr input
- Two-phase progressive scan RGB 18-bit (24 bit) and 36-bit (48 bit) signal output
- Simulated increased color-depth processing at 6-bit mode. Values in parentheses apply in 8-bit mode.
- YCbCr to RGB conversion
- Interlaced to progressive scan conversion
- Resolution conversion (enlargement)
- Variable display size and display position (independently settable in the horizontal and vertical directions)
- Image quality adjustments: brightness, contrast, color, sharpness, color phase, black balance, and white balance
- Built-in γ correction (LUT technique. Each 8-bit R, G, and B signal is independently programmable.)
- Built-in OSD function (8 colors, 253 characters)
- I^2C bus interface
- Constant frame-rate processing (identical frame periods in the input and output signals) adopted so that no external memory is required.

Specifications

- Supply voltage: 3.3 V (input pins are 5 V tolerant)
- Maximum operating frequency: 65.0 MHz
- Package: SQFP208

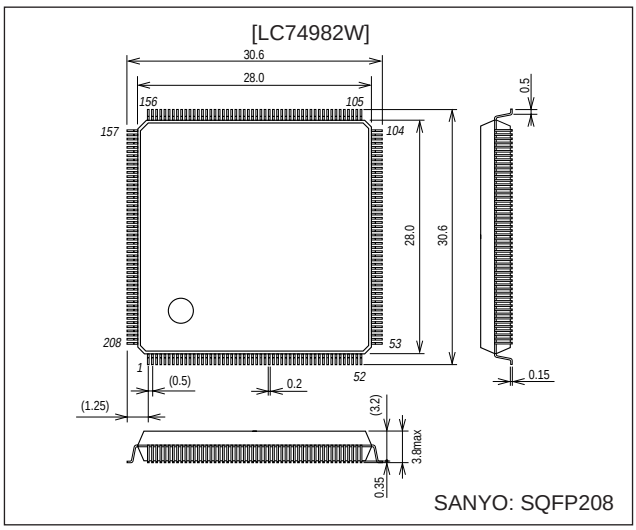
Applications

- LCD TVs, monitors, and projectors
- PDP displays
- Car television and car video monitors

Package Dimensions

unit: mm

3210-SQFP208



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I/O Specifications

Input Signal Overview

Signal type	Pin No.	Pin	Description	Notes
Video signals	6 to 13	YIN7 to 0	Y/Y/R	• NTSC, PAL, and DTV (480i and 480p) inputs YCbCr signals conform to the CCIR 601 standard. The YC C signal is a multiplexed CbCr signal (4:2:2). • PC input (up to XGA)
	54 to 61	RIN7 to 0		
	16 to 23	UIN7 to 0	C/Cb/G	
	64 to 71	GIN7 to 0		
	26 to 33	VIN7 to 0	–/Cr/B	
	74 to 81	BIN7 to 0		
Sync signals	90	HITV	NTSC/PAL horizontal sync signal	• Three independent systems for both horizontal and vertical sync signals • Any input polarity may be used. Internal automatic-discrimination.
	91	VITV	NTSC/PAL vertical sync signal	
	92	HIDTV	DTV horizontal sync signal	
	93	VIDTV	DTV vertical sync signal	
	94	HIPC	PC horizontal sync signal	
	95	VIPC	PC vertical sync signal	
Data enable signals	96	BLKIH	Horizontal enable	• Input with the same logic. The polarity can be inverted internally. • A composite video signal can be input to BLKIH. (BLKIV must be tied high in this case.)
	97	BLKIV	Vertical enable	
Pixel clocks	36	CLKITV	NTSC/PAL clock	• Three independent input systems
	39	CLKIDTV	DTV clock	
	42	CLKIPC	PC clock	
	167	XTAL	Display clock	• Fixed frequency crystal oscillator (65 MHz maximum)

Output Signal Overview

Signal type	Pin No.	Pin	Description	Notes
Video signals in 6-bit output mode	106 to 111	ROEVEN5 to 0	Even pixels, red	• Each of the RGB channels is an 6-bit 2-phase signal. • The output mode can be switched to single-phase output mode. (Output from the ODD pin)
	114 to 119	GOEVEN5 to 0	Even pixels, green	
	122 to 127	BOEVEN5 to 0	Even pixels, blue	
	130 to 135	ROODD5 to 0	Odd pixels, red	
	138 to 143	GOODD5 to 0	Odd pixels, green	
	146 to 151	BOODD5 to 0	Odd pixels, blue	
Video signals in 8-bit output mode	106 to 111, 114, 115	ROEVEN7 to 0	Even pixels, red	• Each of the RGB channels is an 8-bit 2-phase signal. • The output mode can be switched to single-phase output mode. (Output from the ODD pin)
	116 to 119, 122 to 125	GOEVEN7 to 0	Even pixels, green	
	126, 127, 130 to 135	BOEVEN7 to 0	Even pixels, blue	
	138 to 143, 146, 147	ROODD7 to 0	Odd pixels, red	
	182 to 189	GOODD7 to 0	Odd pixels, green	
	192 to 199	BOODD7 to 0	Odd pixels, blue	
Sync signals	162	HOUT	Horizontal sync signal	• The sync period, position, and polarity can be set. • A composite sync signal can be output from VOUT.
	163	VOUT	Vertical sync signal	
Data enable signals	102	BLKHOUT	Horizontal enable	• The enable period and the polarity can be set. • A composite signal can be output from BLKVOUT.
	103	BLKVOUT	Vertical enable	
Pixel clocks	154	DCLK1	Single-phase clock	• Outputs the same frequency as that of the crystal oscillator.
	155	DCLK1B	Single-phase clock (inverted)	
	158	DCLK2	Two-phase clock	• Outputs a frequency 1/2 that of the crystal oscillator.
	159	DCLK2B	Two-phase clock (inverted)	

Control Signal Overview

Signal type	Pin No.	Pin	Description	Notes
Three-wire bus	172	AICS	Chip select	• Used for OSD control and γ correction characteristics settings.
	173	AIDA	Data bus	
	174	AICK	Bus clock	
I^2C-bus	175	SDA	Data bus	• Used to set the internal control registers and to output internal status information. • The slave address is "0111000+ (R/W)".
	176	SCL	Bus clock	

Specifications

Absolute Maximum Ratings at V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +4.6	V
Input voltage	V_I		–0.5 to + 5.5	V
Output voltage	V_O		–0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta = 70°C	0.9	W
Storage temperature	Tstg		–55 to +125	°C
Operating temperature	Topr		–30 to +70	°C

Note: While the standard operating temperature is –30 to +70°C, for applications such as automotive applications, it can also be used over the range –40 to +85°C. Note, however, that the value of the allowable power dissipation differs somewhat between these two cases. Contact your SANYO representative for details if you need to use this device with the latter (wider) operating temperature range.

Allowable Operating Ranges at Ta = –30 to +70°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		3.0	3.3	3.6	V
Input voltage range	V_{IN}		0	—	5.5	V

I/O Pin Capacitances at Ta = 25°C, V_{DD} = V_I = 0 V

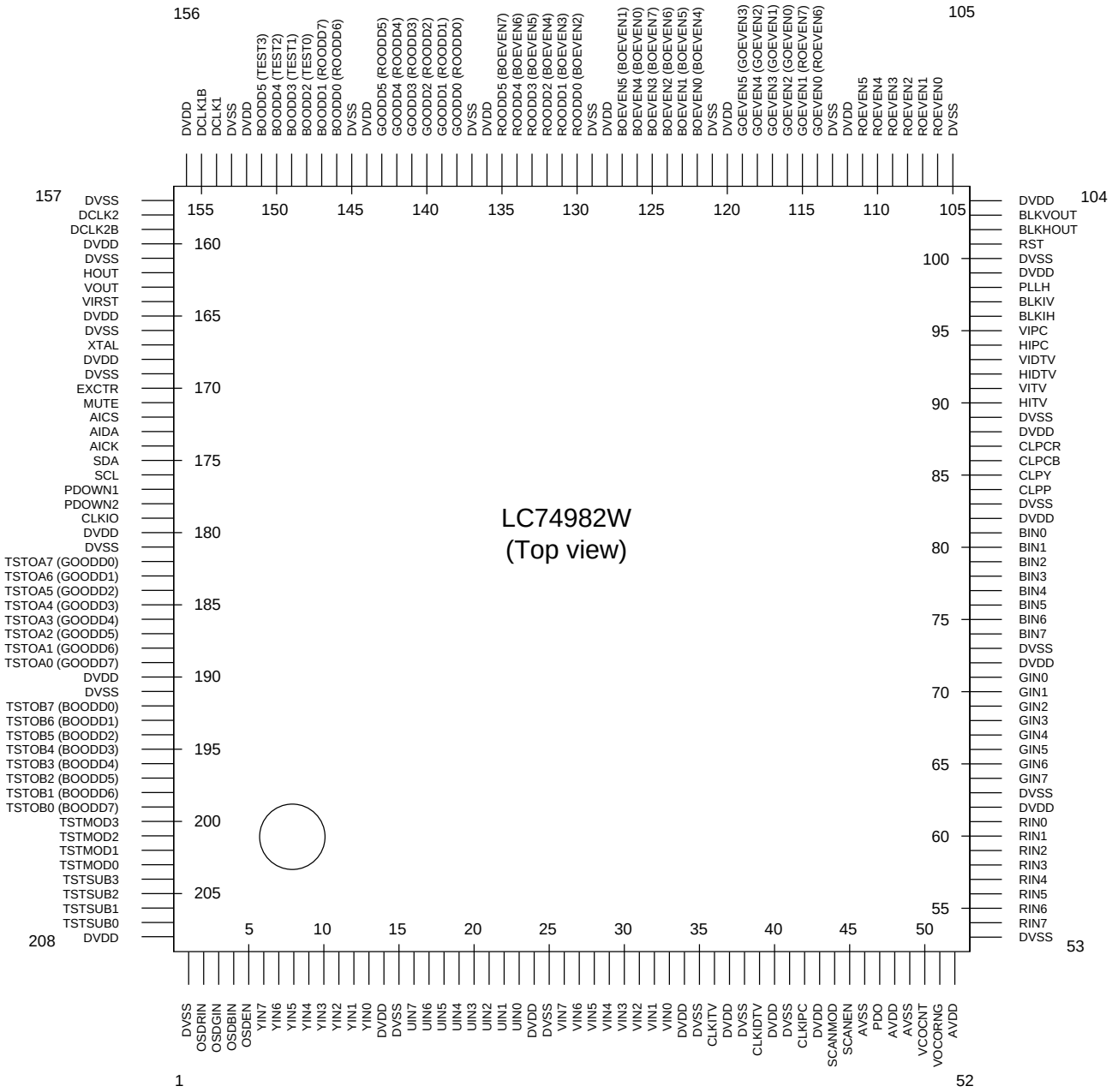
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input pins	C_{IN}	f = 1 MHz	—	—	10	pF
Output pins	C_{OUT}	f = 1 MHz	—	—	10	pF
Bidirectional pins	$C_{I/O}$	f = 1 MHz	—	—	10	pF

DC Characteristics at Ta = –30 to +70°C, V_{DD} = 3.0 to 3.6 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level voltage	V_{IH}	CMOS level	0.7 V_{DD}	—	—	V
		CMOS level Schmitt	0.75 V_{DD}	—	—	V
Input low-level voltage	V_{IL}	CMOS level	—	—	0.2 V_{DD}	V
		CMOS level Schmitt	—	—	0.15 V_{DD}	V
Input high-level current	I_{IH}	V_I = V_{DD}	–10	—	+10	μA
		V_I = V_{DD}, with pull-down resistors attached.	10	—	100	μA
Input low-level current	I_{IL}	V_I = V_{SS}	–10	—	+10	μA
Output high-level voltage	V_{OH}	Type B4, I_{OH} = –2 mA	V_{DD} – 0.8	—	—	V
		Type B8, I_{OH} = –4 mA	V_{DD} – 0.8	—	—	V
		Type B12, I_{OH} = –6 mA	V_{DD} – 0.8	—	—	V
Output low-level voltage	V_{OL}	Type B4, I_{OL} = 2 mA	—	—	0.4	V
		Type B8, I_{OL} = 4 mA	—	—	0.4	V
		Type B12, I_{OL} = 6 mA	—	—	0.4	V
Output leakage current	I_{OZ}	In the high-impedance output state	–10	—	+10	μA
Pull-down resistance	R_{DN}		35	70	140	kΩ
Quiescent current*	I_{DD}	Outputs open, V_I = V_{SS} or V_{DD}	—	—	100	μA

Note: * Certain of the input pins include built-in pull-down resistors. The quiescent current drain cannot be guaranteed in certain situations due to the structure of these circuits.

Pin Assignment



* ( ): Values in parentheses apply in 8-bit mode.

Pin Functions

Pin No.	Pin	I/O type		Connection	Notes
		I/O	Type		
1	DVSS	P		GND	Digital system ground
2	OSDRIN	I	g74980m03	Caption OSD microcontroller	OSD red input (NTSC only)
3	OSDGIN	I	g74980m03	Caption OSD microcontroller	OSD green input (NTSC only)
4	OSDBIN	I	g74980m03	Caption OSD microcontroller	OSD blue input (NTSC only)
5	OSDEN	I	g74980m03	Caption OSD microcontroller	OSD data enable (NTSC only)
6	YIN7	I	g74980m03	Digital decoder	MSB
7	YIN6	I	g74980m03	or	Y signal input
8	YIN5	I	g74980m03	ADC	or
9	YIN4	I	g74980m03	or	R signal input
10	YIN3	I	g74980m03	Digital Interface	
11	YIN2	I	g74980m03		
12	YIN1	I	g74980m03		
13	YIN0	I	g74980m03		LSB
14	DVDD	P		Power supply	Digital system power supply: 3.3 V
15	DVSS	P		GND	Digital system ground
16	UIN7	I	g74980m03	Digital decoder	MSB
17	UIN6	I	g74980m03	or	C (CbCr multiplexed) signal input
18	UIN5	I	g74980m03	ADC	or
19	UIN4	I	g74980m03	or	Cb signal input
20	UIN3	I	g74980m03	Digital Interface	or
21	UIN2	I	g74980m03		G signal input
22	UIN1	I	g74980m03		
23	UIN0	I	g74980m03		LSB
24	DVDD	P		Power supply	Digital system power supply: 3.3 V
25	DVSS	P		GND	Digital system ground
26	VIN7	I	g74980m03	Digital decoder	MSB
27	VIN6	I	g74980m03	or	Cr signal input
28	VIN5	I	g74980m03	ADC	or
29	VIN4	I	g74980m03	or	B signal input
30	VIN3	I	g74980m03	Digital Interface	
31	VIN2	I	g74980m03		
32	VIN1	I	g74980m03		
33	VIN0	I	g74980m03		LSB
34	DVDD	P		Power supply	Digital system power supply: 3.3 V
35	DVSS	P		GND	Digital system ground
36	CLKITV	I	g74980m05	Digital decoder	TV clock input (data rate)
37	DVDD	P		Power supply	Digital system power supply: 3.3 V
38	DVSS	P		GND	Digital system ground
39	CLKIDTV	I	g74980m05	PLL	DTV clock input
40	DVDD	P		Power supply	Digital system power supply: 3.3 V
41	DVSS	P		GND	Digital system ground
42	CLKIPC	I	g74980m05	Digital interface	PC clock input (data rate)
43	DVDD	P		Power supply	Digital system power supply: 3.3 V
44	SCANMOD	I	g74980m03	Open	Scan test mode
45	SCANEN	I	g74980m03	Open	Scan test enable
46	AVSS	P		GND	Analog system ground
47	PDO	O	zwp3vpll3	Loop filter	Charge pump output (open)
48	AVDD	P		Power supply	Analog system power supply: 3.3 V
49	AVSS	P		GND	Analog system ground
50	VCOCNT	I	g74100m06	Loop filter	VCO control input (Connect to AV_{SS}.)
51	VCORNG	I	g74100m06	Resistor	VCO bias resistor input (Connect to AV_{SS}.)
52	AVDD	P		Power supply	Analog system power supply: 3.3 V

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Pin No.	Pin	I/O type		Connection	Notes
		I/O	Type		
53	DVSS	P		GND	Digital system ground
54	RIN7	I	g74980m03	Digital Decoder	MSB
55	RIN6	I	g74980m03	or	Y signal input
56	RIN5	I	g74980m03	ADC	or
57	RIN4	I	g74980m03	or	R signal input
58	RIN3	I	g74980m03	Digital Interface	
59	RIN2	I	g74980m03		
60	RIN1	I	g74980m03		
61	RIN0	I	g74980m03		LSB
62	DVDD	P		Power supply	Digital system power supply: 3.3 V
63	DVSS	P		GND	Digital system ground
64	GIN7	I	g74980m03	Digital Decoder	MSB
65	GIN6	I	g74980m03	or	C (CbCr multiplexed) signal input
66	GIN5	I	g74980m03	ADC	or
67	GIN4	I	g74980m03	or	Cb signal input
68	GIN3	I	g74980m03	Digital Interface	or
69	GIN2	I	g74980m03		G signal input
70	GIN1	I	g74980m03		
71	GIN0	I	g74980m03		LSB
72	DVDD	P		Power supply	Digital system power supply: 3.3 V
73	DVSS	P		GND	Digital system ground
74	BIN7	I	g74980m03	Digital Decoder	MSB
75	BIN6	I	g74980m03	or	Cr signal input
76	BIN5	I	g74980m03	ADC	or
77	BIN4	I	g74980m03	or	B signal input
78	BIN3	I	g74980m03	Digital Interface	
79	BIN2	I	g74980m03		
80	BIN1	I	g74980m03		
81	BIN0	I	g74980m03		LSB
82	DVDD	P		Power supply	Digital system power supply: 3.3 V
83	DVSS	P		GND	Digital system ground
84	CLPP	O	POB4	ADC	Clamp pulse
85	CLPY	O	POT4	ADC	Y clamp level
86	CLPCB	O	POT4	ADC	Cb clamp level
87	CLPCR	O	POT4	ADC	Cr clamp level
88	DVDD	P		Power supply	Digital system power supply: 3.3 V
89	DVSS	P		GND	Digital system ground
90	HITV	I	g74980m04	TV decoder	TV horizontal synchronizing signal input
91	VITV	I	g74980m04	TV decoder	TV vertical synchronizing signal input
92	HIDTV	I	g74980m04	Digital interface	DTV horizontal synchronizing signal input
93	VIDTV	I	g74980m04	Digital interface	DTV vertical synchronizing signal input
94	HIPC	I	g74980m04	Digital interface	PC horizontal sync signal input
95	VIPC	I	g74980m04	Digital interface	PC vertical sync signal input
96	BLKIH	I	g74980m02	Digital interface	Horizontal blanking signal input (composite blanking signal)
97	BLKIV	I	g74980m02	Digital interface	Vertical blanking signal input (Held high in composite mode)
98	PLLH	O	POB4	PLL	PLL internal divider output
99	DVDD	P		Power supply	Digital system power supply: 3.3 V
100	DVSS	P		GND	Digital system ground
101	RST	I	g74980m01	Initialization circuit	System reset (reset to low)
102	BLKHOUT	O	POB8	LCD module	Horizontal data enable
103	BLKVOUT	O	POB8	LCD module	Vertical data enable or composite data enable
104	DVDD	P		Power supply	Digital system power supply: 3.3 V

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Pin No.	Pin	I/O type		Connection	Notes
		I/O	Type		
105	DVSS	P		GND	Digital system ground
106	ROEVEN0	O	POB4	LCD module	LSB (LSB)
107	ROEVEN1	O	POB4		Red signal output (even)
108	ROEVEN2	O	POB4		
109	ROEVEN3	O	POB4		(Red signal output (even))
110	ROEVEN4	O	POB4		
111	ROEVEN5	O	POB4		MSB
112	DVDD	P		Power supply	Digital system power supply: 3.3 V
113	DVSS	P		GND	Digital system ground
114	GOEVEN0 (ROEVEN6)	O	POB4	LCD module	LSB
115	GOEVEN1 (ROEVEN7)	O	POB4		(MSB)
116	GOEVEN2 (GOEVEN0)	O	POB4		Green signal output (even) (LSB)
117	GOEVEN3 (GOEVEN1)	O	POB4		
118	GOEVEN4 (GOEVEN2)	O	POB4		
119	GOEVEN5 (GOEVEN3)	O	POB4		MSB (Green signal output (even))
120	DVDD	P		Power supply	Digital system power supply: 3.3 V
121	DVSS	P		GND	Digital system ground
122	BOEVEN0 (GOEVEN4)	O	POB4	LCD module	LSB
123	BOEVEN1 (GOEVEN5)	O	POB4		Blue signal output (even)
124	BOEVEN2 (GOEVEN6)	O	POB4		(MSB)
125	BOEVEN3 (GOEVEN7)	O	POB4		(LSB)
126	BOEVEN4 (BOEVEN0)	O	POB4		
127	BOEVEN5 (BOEVEN1)	O	POB4		MSB
128	DVDD	P		Power supply	Digital system power supply: 3.3 V
129	DVSS	P		GND	Digital system ground
130	ROODD0 (BOEVEN2)	O	POB4	LCD module	LSB
131	ROODD1 (BOEVEN3)	O	POB4		Red signal output (odd) (B signal output (even))
132	ROODD2 (BOEVEN4)	O	POB4		or
133	ROODD3 (BOEVEN5)	O	POB4		Red signal single-phase output
134	ROODD4 (BOEVEN6)	O	POB4		
135	ROODD5 (BOEVEN7)	O	POB4		MSB (MSB)
136	DVDD	P		Power supply	Digital system power supply: 3.3 V
137	DVSS	P		GND	Digital system ground
138	GOODD0 (ROODD0)	O	POB4	LCD module	LSB (LSB)
139	GOODD1 (ROODD1)	O	POB4		Green signal output (odd)
140	GOODD2 (ROODD2)	O	POB4		or
141	GOODD3 (ROODD3)	O	POB4		Green signal single-phase output (Red signal output (odd)
142	GOODD4 (ROODD4)	O	POB4		or
143	GOODD5 (ROODD5)	O	POB4		MSB Red signal single-phase output)
144	DVDD	P		Power supply	Digital system power supply: 3.3 V
145	DVSS	P		GND	Digital system ground
146	BOODD0 (ROODD6)	O	POB4	LCD module	LSB
147	BOODD1 (ROODD7)	O	POB4		Blue signal output (odd) (MSB)
148	BOODD2 (TEST0)	O	POB4		or
149	BOODD3 (TEST1)	O	POB4	(OPEN)	Blue signal single-phase output (Test output (Outputs a fixed
150	BOODD4 (TEST2)	O	POB4		low level.))
151	BOODD5 (TEST3)	O	POB4		MSB
152	DVDD	P		Power supply	Digital system power supply: 3.3 V
153	DVSS	P		GND	Digital system ground
154	DCLK1	O	POB12	LCD module	Data clock 1 (for single-phase data output)
155	DCLK1B	O	POB12	LCD module	Inverted data clock 1 (for single-phase data output)
156	DVDD	P		Power supply	Digital system power supply: 3.3 V

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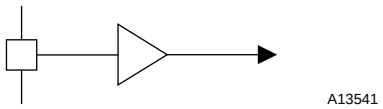
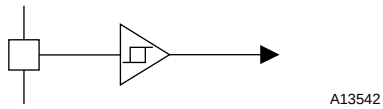
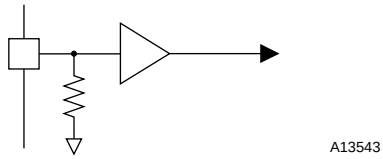
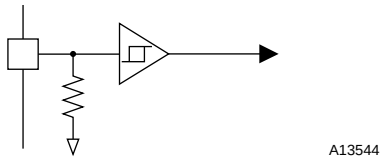
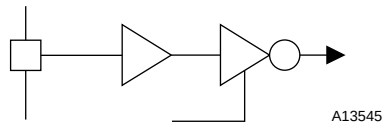
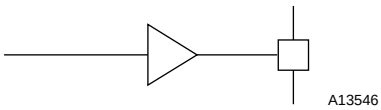
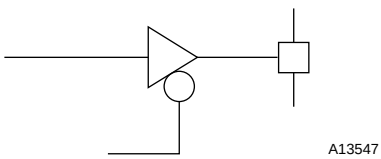
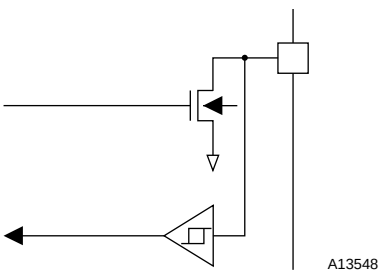
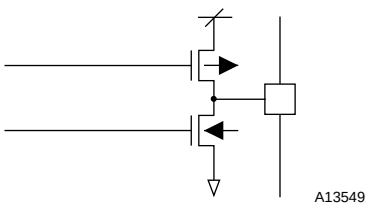
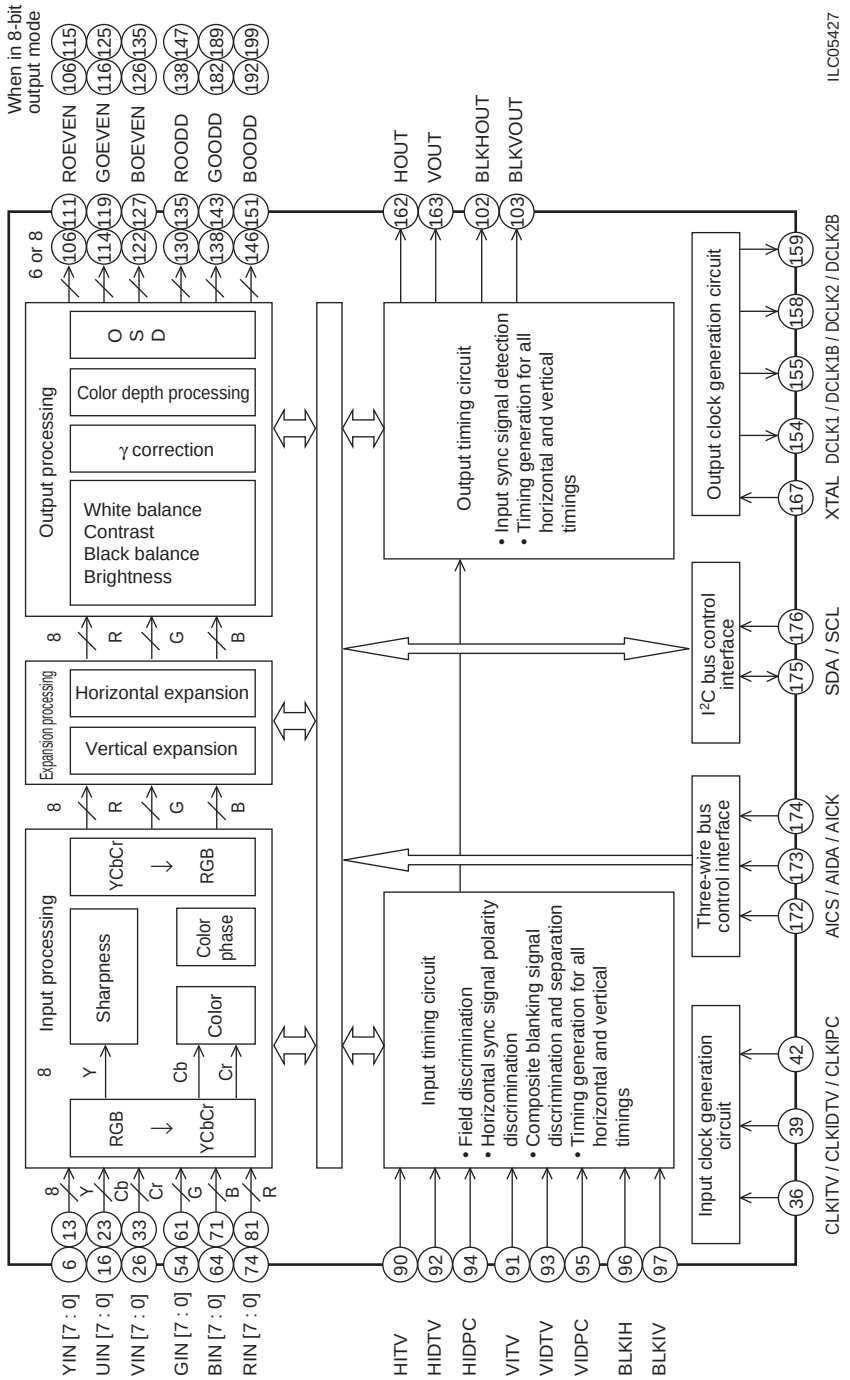
Pin No.	Pin	I/O type		Connection	Notes
		I/O	Type		
157	DVSS	P		GND	Digital system ground
158	DCLK2	O	POB12	—	Data clock 2 (for two-phase data output)
159	DCLK2B	O	POB12	—	Inverted data clock 2 (for two-phase data output)
160	DVDD	P		Power supply	Digital system power supply: 3.3 V
161	DVSS	P		GND	Digital system ground
162	HOUT	O	POB8	LCD module	Horizontal sync output
163	VOUT	O	POB8	LCD module	Vertical synchronizing signal output or composite synchronizing signal output
164	VIRST	O	POB4	—	Crystal oscillator reset
165	DVDD	P		Power supply	Digital system power supply: 3.3 V
166	DVSS	P		GND	Digital system ground
167	XTAL	I	g74980m01	VCO	Crystal oscillator circuit output
168	DVDD	P		Power supply	Digital system power supply: 3.3 V
169	DVSS	P		GND	Digital system ground
170	EXCTR	O	POB4	—	External control output (output controlled over the I^2C bus)
171	MUTE	I	g74980m02	Microcontroller	Mute control input (mute to low)
172	AICS	I	g74980m02	Microcontroller	3-wire bus control chip select
173	AIDA	I	g74980m02	Microcontroller	3-wire bus control bus data
174	AICK	I	g74980m02	Microcontroller	3-wire bus control bus clock
175	SDA	B	g74980m06	Microcontroller	I^2C control data
176	SCL	I	g74980m02	Microcontroller	I^2C control clock
177	PDOWN1	I	g74980m01	—	Must be tied high during normal operation.
178	PDOWN2	I	g74980m01	—	Must be tied high during normal operation.
179	CLKI0	O	POB12	—	Input system clock output
180	DVDD	P		Power supply	Digital system power supply: 3.3 V
181	DVSS	P		GND	Digital system ground
182	TSTOA7 (GOODD0)	O	POB4	OPEN	MSB (LSB)
183	TSTOA6 (GOODD1)	O	POB4		Test outputs (G signal output (odd)
184	TSTOA5 (GOODD2)	O	POB4	(LCD module)	or
185	TSTOA4 (GOODD3)	O	POB4		G signal single-phase output)
186	TSTOA3 (GOODD4)	O	POB4		
187	TSTOA2 (GOODD5)	O	POB4		
188	TSTOA1 (GOODD6)	O	POB4		
189	TSTOA0 (GOODD7)	O	POB4		LSB (MSB)
190	DVDD	P		Power supply	Digital system power supply: 3.3 V
191	DVSS	P		GND	Digital system ground
192	TSTOB7 (BOODD0)	O	POB4	OPEN	MSB (LSB)
193	TSTOB6 (BOODD1)	O	POB4		Test outputs (B signal output (odd)
194	TSTOB5 (BOODD2)	O	POB4	(LCD module)	or
195	TSTOB4 (BOODD3)	O	POB4		B signal single-phase output)
196	TSTOB3 (BOODD4)	O	POB4		
197	TSTOB2 (BOODD5)	O	POB4		
198	TSTOB1 (BOODD6)	O	POB4		
199	TSTOB0 (BOODD7)	O	POB4		LSB (MSB)
200	TSTMOD3	I	g74980m03	OPEN	Test mode (Must be left open in normal operation.)
201	TSTMOD2	I	g74980m03		
202	TSTMOD1	I	g74980m03		
203	TSTMOD0	I	g74980m03		
204	TSTSUB3	I	g74980m03	OPEN	Test sub-mode (Must be left open in normal operation.)
205	TSTSUB2	I	g74980m03		
206	TSTSUB1	I	g74980m03		
207	TSTSUB0	I	g74980m03		
208	DVDD	P		Power supply	Digital system power supply: 3.3 V

Pin Type

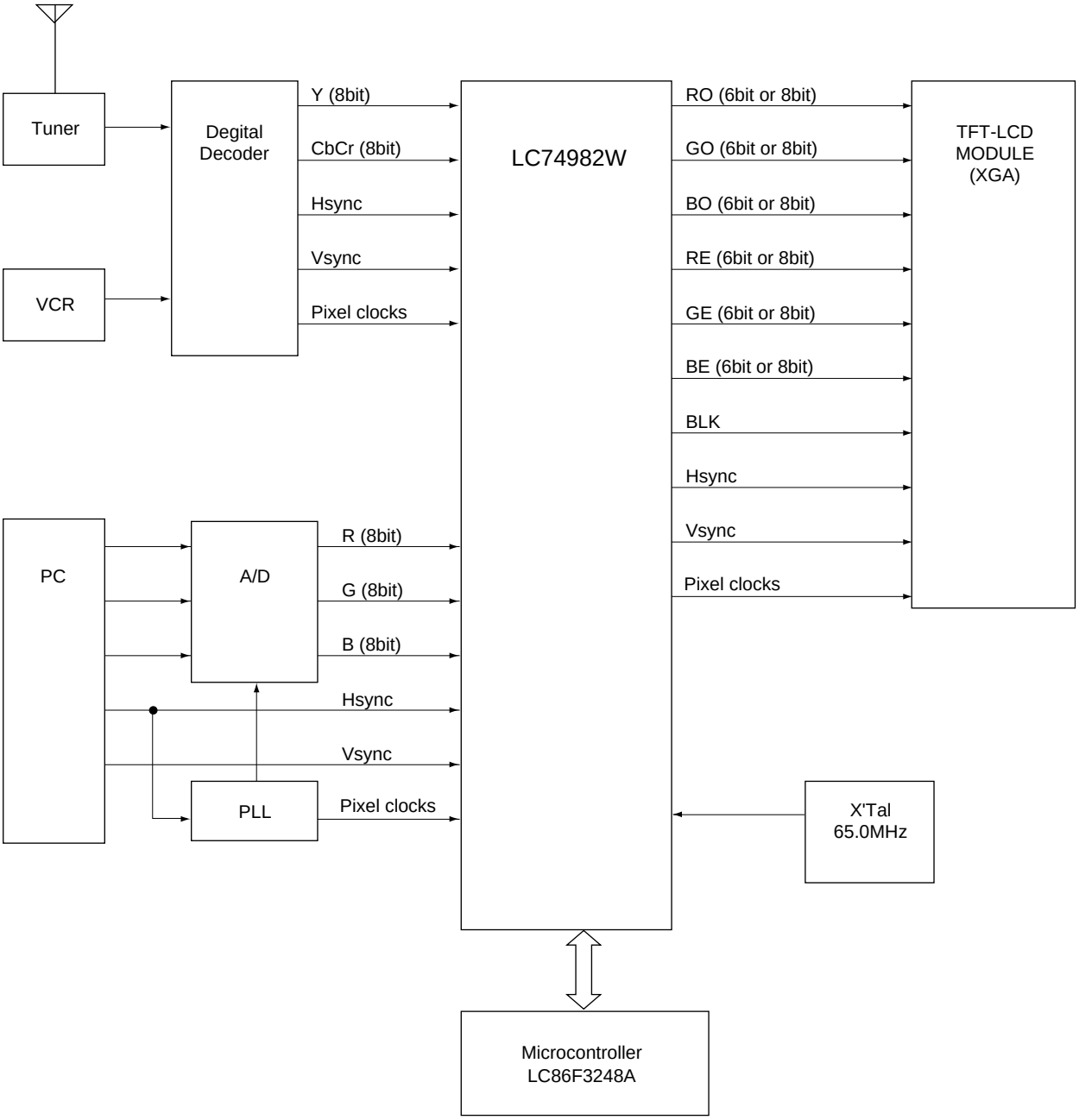
I/O type	Applicable pins	Function	Equivalent circuit
g74980m01	RST PDOWN1 to 2 XTAL	3 to 5 V voltage handling input	 A13541
g74980m02	AICS, AIDA, AICK SCL BLKIH, BLKIV MUTE	3 to 5 V voltage handling Schmitt input	 A13542
g74980m03	OSDRIN, OSDGIN, OSDBIN, OSDEN YIN0 to 7, UIN0 to 7, VIN0 to 7 SCANMOD, SCANEN RIN0 to 7, GIN0 to 7, BIN0 to 7 TSTMOD0 to 3, TSTSUB0 to 3 Leave open when unused.	3 to 5 V voltage handling pull-down input	 A13543
g74980m04	HITV, VITV HIDTV, VIDTV HIPC, VIPC	3 to 5 V voltage handling pull-down Schmitt input	 A13544
g74980m05	CLKITV CLKIDTV CLKIPC	3 to 5 V voltage handling OE input	 A13545
POB4	CLPP, PLLH, ROEVEN0 to 5 (7), GOEVEN0 to 5 (7), BOEVEN0 to 5 (7), ROODD0 to 5 (7), GOODD0 to 5 (7), BOODD0 to 5 (7), VIRST, EXCTR, TST0A0 to 7, TST0B0 to 7, (TEST0 to 3)	4 mA drive output	 A13546
POB8	BLKHOUT, BLKVOUT HOUT, VOUT	8 mA drive output	
POB12	DCLK1, DBLK1B, DCLK2, DCLK2B CLKI0	12 mA drive output	
POT4	CLPY, CLPCB, CLPCR	4 mA 3-state drive output	 A13547
g74980m06	SDA	Open-drain I/O	 A13548
g74100m06	VCOCNT, VCORNG	Analog through	
zwp3vpll3	PDO	Charge pump output	 A13549

Note: * All of the DV_{DD}, DV_{SS}, AV_{DD}, and AV_{SS} pins must be connected to the corresponding power or ground level. Do not leave any of these pins open.

IC Internal Block Diagram

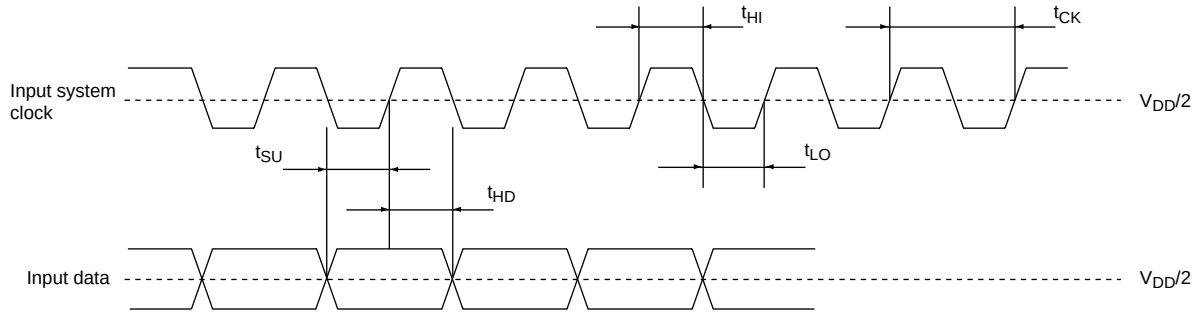


Sample Application Circuit (LCD TV/Monitor)



I/O Data Timing

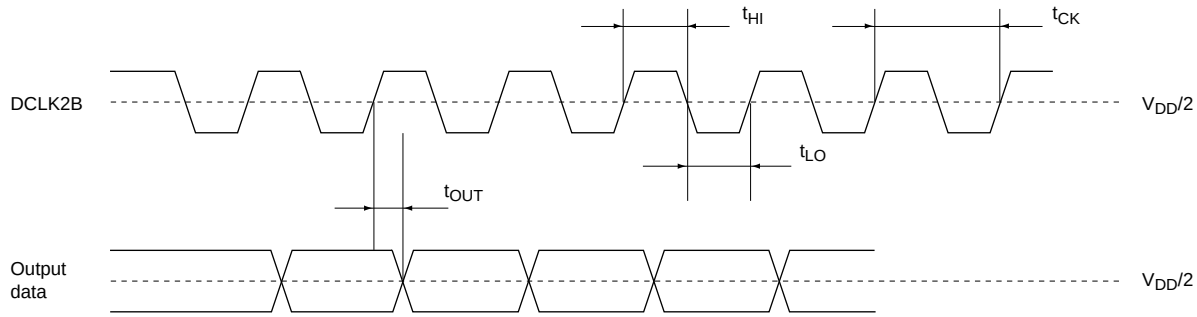
(1) Input data timing



Item	Pin	Parameter	min	max	Unit
Clock low-level period	CLKITV	t_{LO}	7.5	—	ns
Clock high-level period	CLKIDTV	t_{HI}	7.5	—	ns
Clock cycle	CLKIPC	t_{CK}	15.0	—	ns
Input data setup time	YIN [7:0], UIN [7:0] VIN [7:0], RIN [7:0] GIN [7:0], BIN [7:0]	t_{SU}	0	—	ns
Input data hold time	HITV, VITV, HIDTV, VIDTV HIPC, VIPC, BLKIH, BLKIV	t_{HD}	7.0	—	ns

Note: * We recommend using a duty of 50% for the input clock signal.

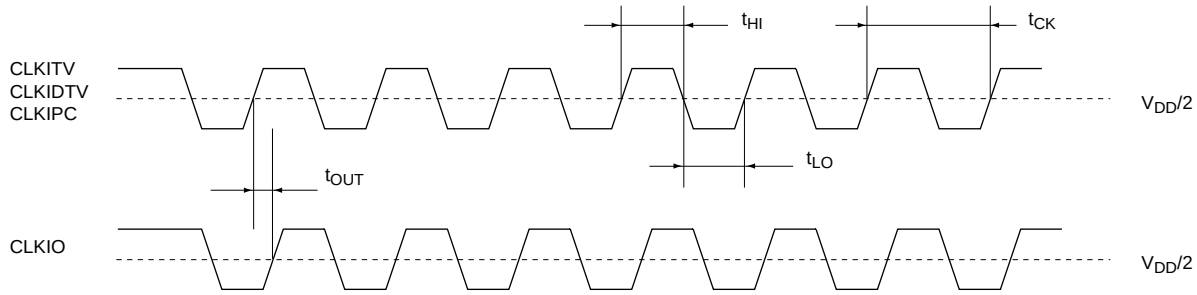
(2) Output data timing



Item	Pin	Parameter	min	max	Unit
Clock low-level period	DCLK2, DCLK2B	t_{LO}	15.0	—	ns
Clock high-level period		t_{HI}	15.0	—	ns
Clock cycle		t_{CK}	30.0	—	ns
Output data delay time	ROEVEN [5(7):0], GOEVEN [5(7):0] BOEVEN [5(7):0], ROODD [5(7):0] GOODD [5(7):0], BOODD [5(7):0] BLKHOUT, HOUT, VOUT	t_{OUT}	0	10	ns

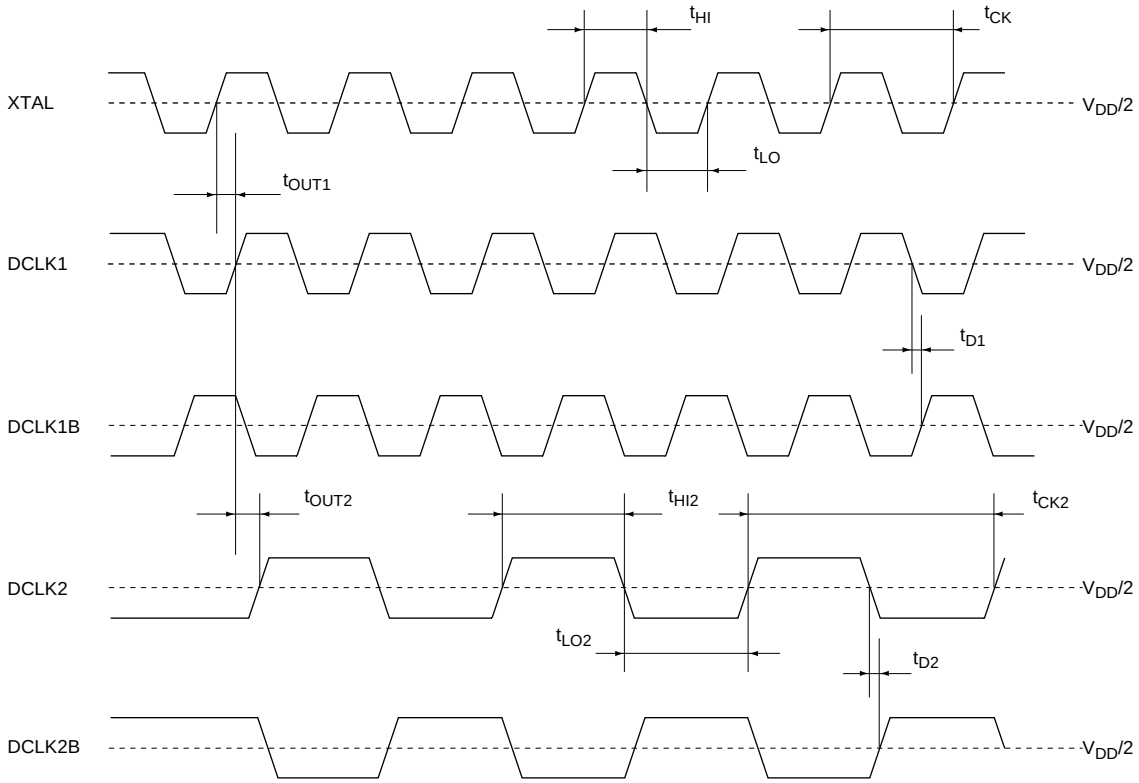
I/O Clock Timing

(1) Input system clock timing



Item	Pin	Parameter	min	max	Unit
Clock low-level period	CLKITV	t_{LO}	7.5	—	ns
Clock high-level period	CLKIDTV	t_{HI}	7.5	—	ns
Clock cycle	CLKIPC	t_{CK}	15.0	—	ns
Cock I/O delay time	CLKIO	t_{OUT}	5	10	ns

(2) Output system clock timing



Item	Pin	Parameter	min	max	Unit
Clock low-level period	XTAL	t_{LO}	7.5	—	ns
Clock high-level period		t_{HI}	7.5	—	ns
Clock cycle		t_{CK}	15.0	—	ns
DCLK1 delay time	DCLK1	t_{OUT1}	0	5	ns
DCLK1B delay time	DCLK1B	t_{D1}	–1	+1	ns
Clock low-level period	DCLK2	t_{LO2}	15.0	—	ns
Clock high-level period		t_{HI2}	15.0	—	ns
Clock cycle		t_{CK2}	30.0	—	ns
DCLK2 delay time	DCLK2	t_{OUT2}	0	2	ns
DCLK2B delay time	DCLK2B	t_{D2}	–1	+1	ns