SGS-THOMSON MICROELECTRONICS

STi3520A

MPEG AUDIO / MPEG-2 VIDEO INTEGRATED DECODER

SUMMARY DATA

- SINGLE CHIP IMPLEMENTING THE MPEG DECODING FUNCTIONS OF THE STi3500A VIDEO DECODER AND THE STi4500 AUDIO DECODER
- ON-CHIP PLL ALLOWING FULL CIRCUIT OPERATION WITH ONLY ONE EXTERNAL CLOCK
- ACCEPTS MPEG AUDIO, VIDEO AND PROGRAM STREAMS (PES)
- VIDEO DECODER FULLY SUPPORTS MPEG-2 MAIN PROFILE/MAIN LEVEL (MP@ML)
- MPEG-2 MAIN PROFILE CCIR601 DECODING IN 16 MBITS DRAM (INCLUDING OSD)
- MPEG-2 SIMPLE PROFILE DECODING IN 8MBITS DRAM
- AUTOMATIC ERROR CONCEALMENT
- ON-SCREEN DISPLAY GENERATOR : 16 COLORS/REGION, 6-BIT LUMA RESOLUTION (4 BITS/PEL, 4 BITS/2 PELS AND 2 BITS/PEL MODES). LINKED LIST MEMORY MANAGEMENT
- AUDIO DECODER SUPPORTS LAYERS 1 AND 2 OF MPEG
- ALL POPULAR AUDIO OUTPUT PCM FORMATS SUPPORTED
- INTEGRATED AUDIO BIT-BUFFER
- SUPPORT FOR SYNCHRONOUS AND HYPER-PAGE MODE (EDO) DRAMS
- PAL DECODING WITH OSD WITH 16 MBITS DRAM. FULL SCREEN, 16 COLOR OSD IN 20 MBITS USING 5 x 4MBIT STANDARD DRAMS
- STANDARD 8-BIT INTERFACE FOR MICROCONTROLLER AND COMPRESSED DATA INPUT
- 3.3V POWER SUPPLY, I/Os 5V COMPATIBLE, 0.5µM CMOS TECHNOLOGY

APPLICATIONS

- DBS AND DVB RECEIVERS
- DIGITAL TV RECEIVER
- DIGITAL CABLE TV RECEIVER

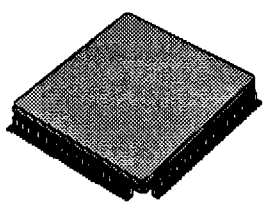
DESCRIPTION

The STi3520A contains an MPEG-2 video decoder, an MPEG audio decoder and a PLL. The STi3520A requires minimum support from an external microcontroller, which is mainly required to control the video decoder at the start of every picture.

The video decoder is a real-time video compression processor supporting the MPEG-1 and MPEG-2 standards at video rates up to 720 x 480 x 60Hz or 720 x 576 x 50Hz. Picture format conversion for display is performed by vertical and horizontal filters. The image can also be downsampled by up to a factor of 2. The audio decoder is compliant with layers 1 and 2 of the MPEG standard. Sampling rates of 32, 44.1 and 48kHz can be used.

Audio, video and PES data streams are input through the 8-bit data port. Time stamps are extracted automatically to aid audio/video synchronization. Undetected bitstream errors activate error concealment functions.

User-defined bitmaps may be superimposed on the displayed picture through use of the on-screen display function. These bitmaps are written directly into the DRAM memory by the microcontroller.



PQFP160
(Plastic Quad Flat Pack)

ORDER CODE : STi3520ACV

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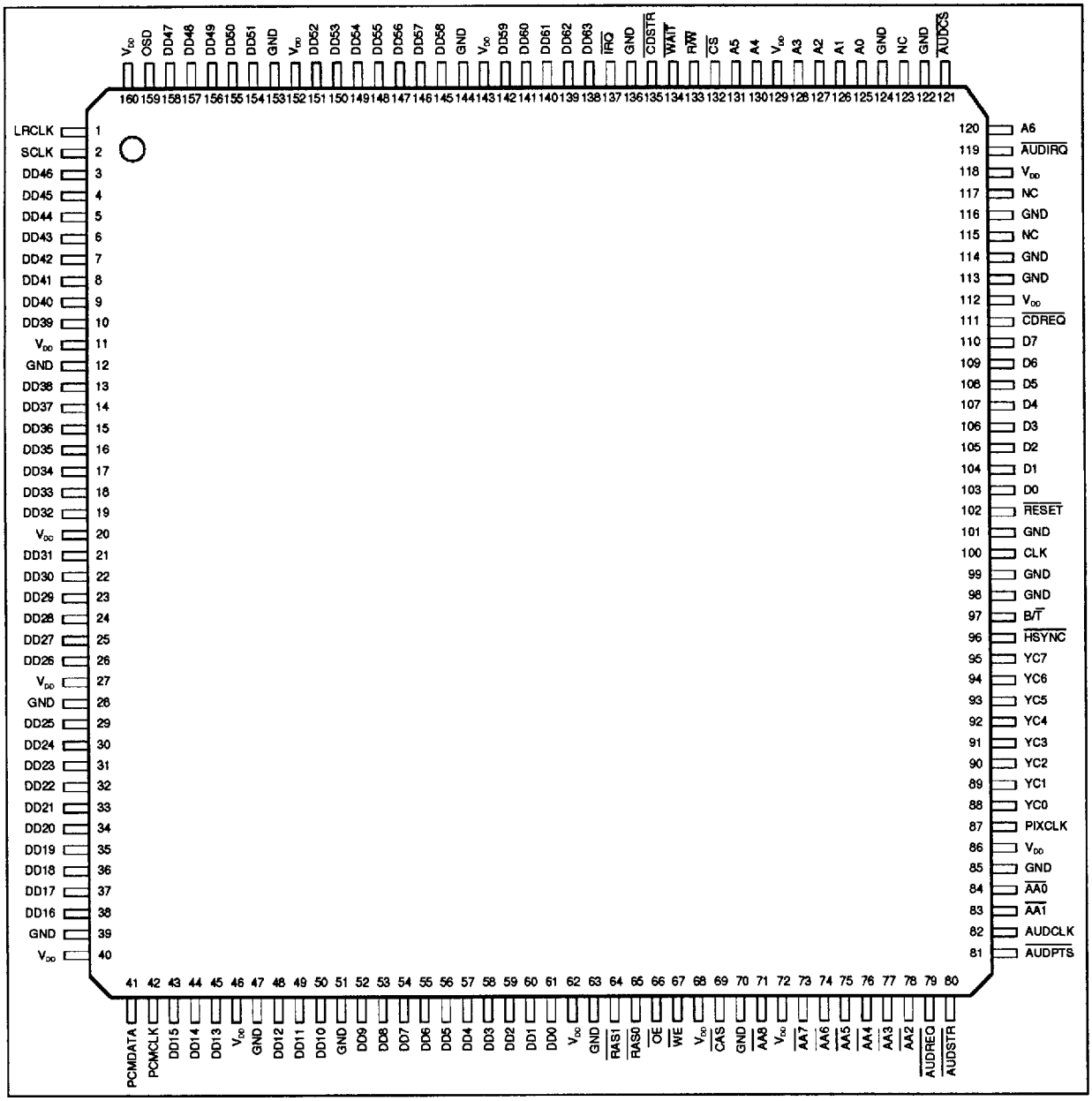
I - PIN DESCRIPTION

I.1 - Pin Connections



I.2 - Pin List

Pin Number	Name	Type	Function
SYSTEM SERVICES AND NON-FUNCTIONAL PINS			
2, 11, 20, 27, 46, 62, 68, 72, 86, 112, 129, 143, 152, 160	V_{DD}		Power Supply
1, 12, 28, 47, 51, 63, 70, 85, 101, 113, 136, 144, 153	GND		Ground
100	CLK	I	Video Decoder Clock
82	AUDCLK	I/O	Audio Decoder Clock
102	$\overline{\text{RESET}}$	I	Master Reset
115, 117, 123		N/C	Reserved Pin, Leave Unconnected
118		V_{DD}	Reserved Pin, Connect to V_{DD}
98, 99, 114, 116, 122, 124		GND	Reserved Pins, Connect to Ground
MICROCONTROLLER INTERFACE			
110-103	D7 - D0	I/O	Bidirectional Data Bus
120, 131, 130, 128-125	A6 - A0	I	Address
132	$\overline{\text{CS}}$	I	Chip Select (video)
121	$\overline{\text{AUDCS}}$	I	Chip Select (audio)
133	R/$\overline{\text{W}}$	I	Read/Write Selection
134	$\overline{\text{WAIT}}$	O (3-state)	Data Acknowledge
137	$\overline{\text{IRQ}}$	O (open-drain)	Interrupt Request (video)
119	$\overline{\text{AUDIRQ}}$	O (open-drain)	Interrupt Request (audio)
AUDIO TIME-STAMP FLAG			
81	$\overline{\text{AUDPTS}}$	O	Indicates Latching of Audio Time-Stamp
VIDEO OUTPUT INTERFACE			
95-88	YC7 - YC0	O	Multiplexed YC_BC_R Video Port
87	PIXCLK	I/O	Pel Clock
97	B/$\overline{\text{T}}$	I	Bottom/Top Field Selection (vertical sync)
96	$\overline{\text{HSYNC}}$	I	Horizontal Sync
159	OSD	I/O	OSD Enable/OSD Active
AUDIO OUTPUT INTERFACE			
39	LRCLK	O	Left/Right Channel Select Output
40	SCLK	O	PCM Clock Output
41	PCMDATA	O	PCM Serial Data Output
42	PCMCLK	I/O	PCM Clock Input
COMPRESSED DATA INPUT CONTROL			
111	$\overline{\text{CDREQ}}$	O	Video Compressed Data Request
135	$\overline{\text{CDSTR}}$	I	Video Compressed Data Strobe
79	$\overline{\text{AUDREQ}}$	O	Audio Compressed Data Request
80	$\overline{\text{AUDSTR}}$	I	Audio Compressed Data Strobe
STANDARD DRAM INTERFACE			
138-142, 145-151, 154-158, 3-10, 13-19, 21-26, 29-38, 43-45, 48-50, 52-61	DD63 - DD0	I/O	Bidirectional Data Port
71, 73-78, 83, 84	$\overline{\text{AA8}}$ - $\overline{\text{AA0}}$	O	Address
64, 65	$\overline{\text{RAS1}}$, $\overline{\text{RAS0}}$	O	Row Address Strobes for Banks 1 and 0
69	$\overline{\text{CAS}}$	O	Column Address Strobe
66	$\overline{\text{OE}}$	O	Output Enable
67	$\overline{\text{WE}}$	O	Write Enable

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I.3 - Pin Connections SDRAM and EDO DRAM

Pin Number	DRAM Name	STi3520A Name	Type	Function
SYNCHRONOUS DRAM INTERFACE				
21-26, 29-38	DD15 - DD0	DD16 - DD31	I/O	Bidirectional Data Port
52	$\overline{AA11}$	DD9	O	Address
53	$\overline{AA10}$	DD8	O	Address
54	$\overline{AA9}$	DD7	O	Address
55	$\overline{CS}$	DD6	O	Chip Select
56	$\overline{WE}$	DD5	O	Write Enable
57	$\overline{CAS}$	DD4	O	Column Address Strobe
58	$\overline{RAS}$	DD3	O	Row Address Strobe (single bank)
59	CKE	DD2	O	Clock Enable
60	$\overline{OE}$	DD1	O	Output Enable
61	CLK	DD0	O	Synchronous DRAM Clock
71, 73-78, 83, 84	$\overline{AA8}$ - $\overline{AA0}$	$\overline{AA8}$ - $\overline{AA0}$	O	Address
EDO DRAM INTERFACE				
158,3-10, 13-19	DD31 - DD16	DD47 - DD32	I/O	Bidirectional Data Port
21-26, 29-38	DD15 - DD0	DD16 - DD31	I/O	Bidirectional Data Port
52	$\overline{AA11}$	DD9	O	Address
53	$\overline{AA10}$	DD8	O	Address
54	$\overline{AA9}$	DD7	O	Address
56	$\overline{WE}$	DD5	O	Write Enable
57	$\overline{CAS}$	DD4	O	Column Address Strobe
58	$\overline{RAS}$	DD3	O	Row Address Strobe (single bank)
60	$\overline{OE}$	DD1	O	Output Enable
71, 73-78, 83, 84	$\overline{AA8}$ - $\overline{AA0}$	$\overline{AA8}$ - $\overline{AA0}$	O	Address

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II - BLOCK DIAGRAMS

Figure 1 : General Block Diagram

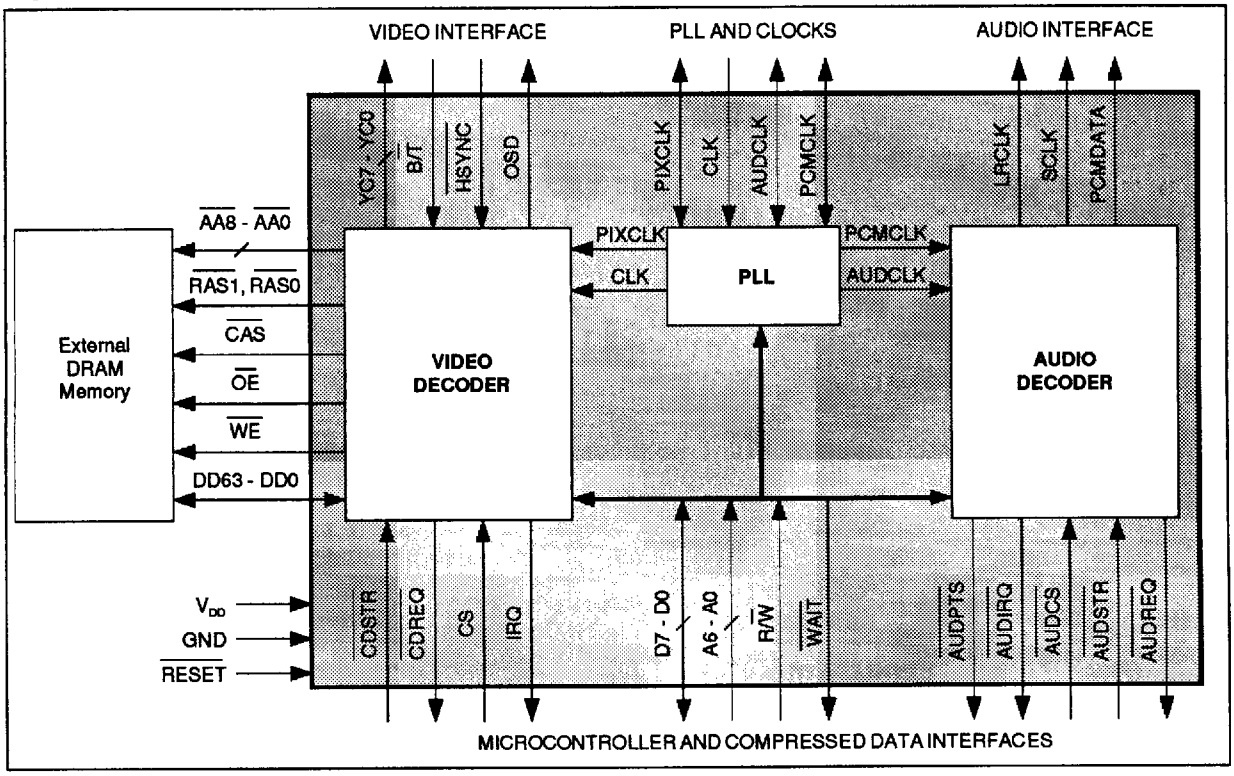


Figure 2 : Audio Decoder Block Diagram

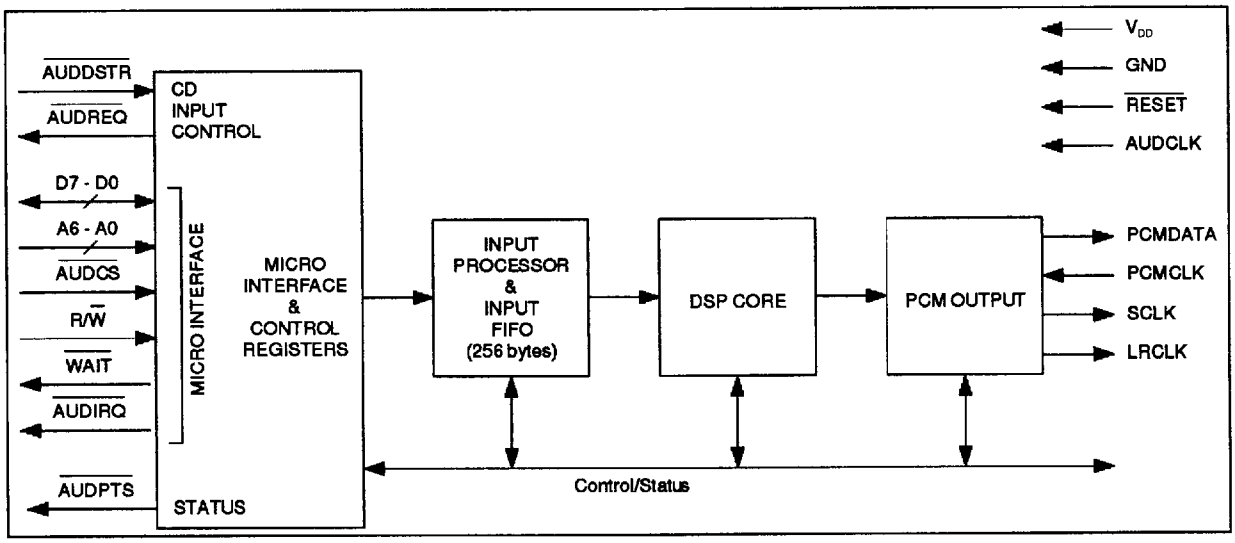


Figure 3 : Video Decoder Block Diagram

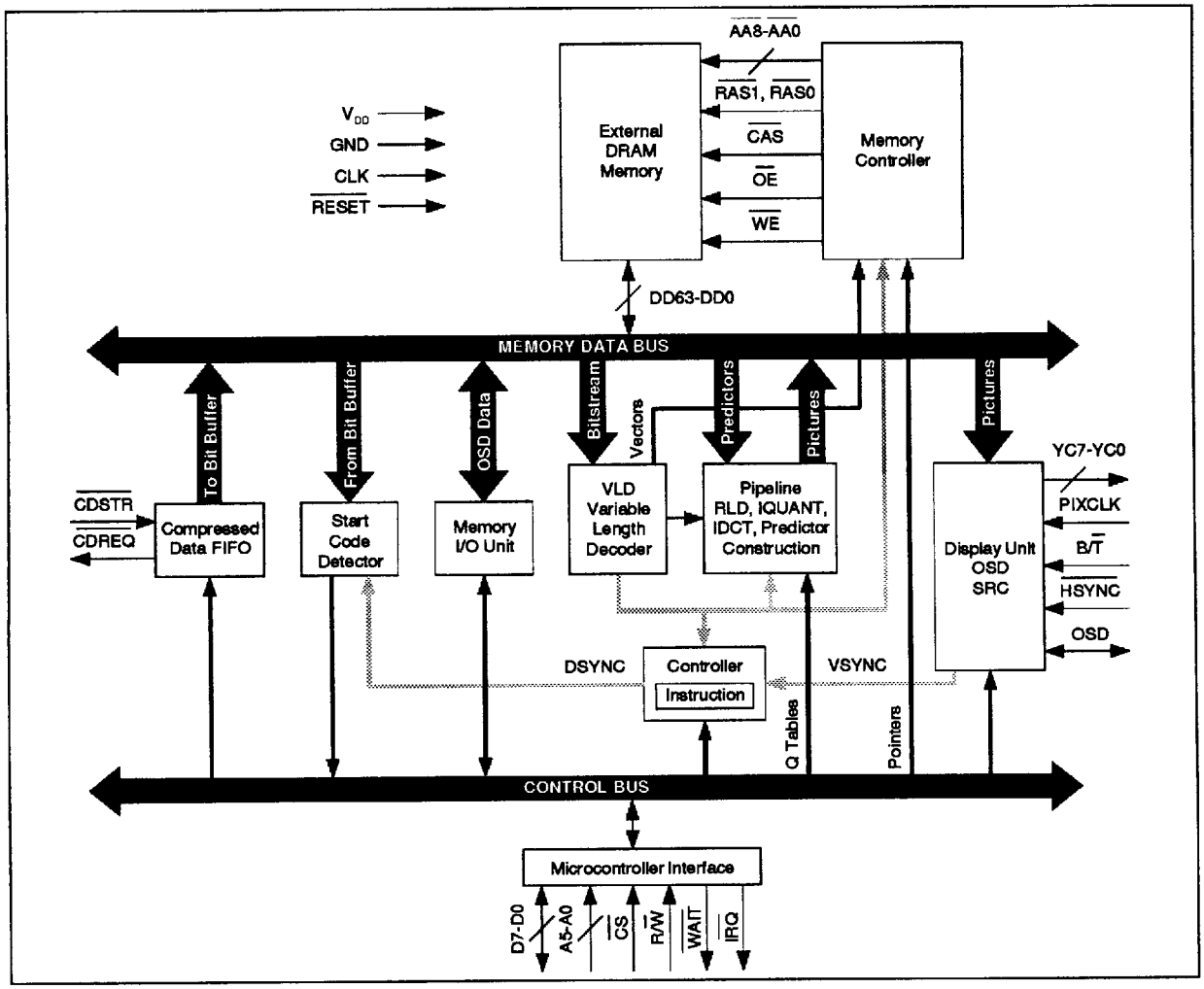
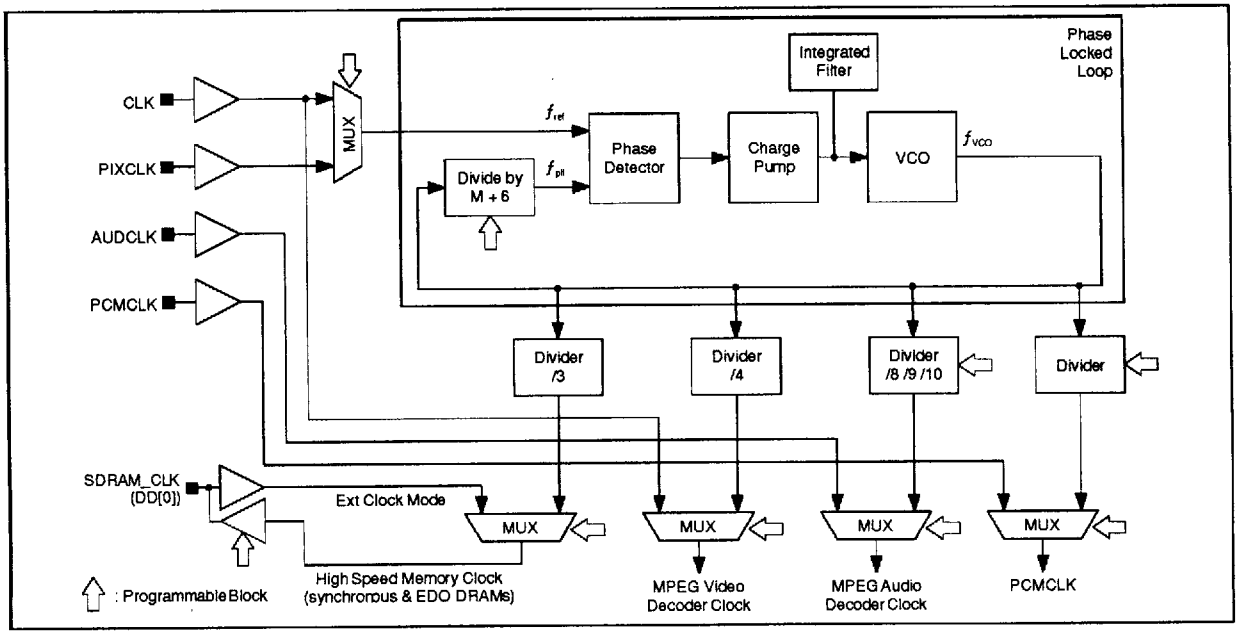


Figure 4 : Clock Generator Block Diagram



III - FUNCTIONAL DESCRIPTION

III.1 - STi3520A Architecture

A functional block diagram of the STi3520A is given in Figure 1. The four external interfaces to the microcontroller, DRAM memory, display and audio DACs are also shown. Together with a minimum of 8 or 16 Mbits of DRAM, a microcontroller, and some video and audio post processing, a complete audio/video decoder system can be constructed.

The STi3520A is similar to the STi3520 audio/video decoder but with a memory optimisation function, an audio bit-buffer integrated in DRAM, an enhanced PLL, an additional OSD mode and a PES parser. The memory optimisation function allows PAL decoding with OSD in 16Mbits of DRAM. The PLL allows full circuit operation using only one external clock (eg a system clock of 27MHz). The OSD has a new mode (4 bits/2 pixels), this allows a full screen, 16 color OSD for PAL operation in 16 MBits of memory. The STi3520A can accept packetised elementary stream (PES) data as defined in the International Standard ISO/IEC 13818-1 (MPEG-2)and ISO/IEC 11172-1 (MPEG-1).

The microcontroller interface has an 8-bit data bus and a 7-bit address bus. This access port has two functions :

- to pass the compressed data to the audio and video decoders,
- to enable control of the STi3520A by providing interrupts and a path for accessing internal registers.

III.2 - Packetised Elementary Stream Interface

The STi3520A can accept compressed data in the following formats :

- MPEG packetised elementary stream (PES) format as defined by ISO/IEC 13818-1,
- MPEG-2 video elementary stream, as defined by ISO/IEC 13818-2,
- MPEG audio elementary stream, as defined by ISO/IEC 11172-3, Layers I and II,
- MPEG video elementary stream, as defined by ISO/IEC 11172-2,
- ISO/IEC 11172-1 packets.

The pre-processor extracts the DTS/PTS time stamps from the packetised data streams and associates the timestamps with the appropriate access units. Other useful fields are extracted and placed in on-chip registers. Any header information which is not processed, such as private information, is placed in a small on-chip buffer which can be accessed by the external microprocessor.

III.3 - Video Decoder (see Figure 3)

The DRAM interface includes all of the signals necessary for control of the memory. Refresh is handled automatically by the video decoder. The memory is used to hold the bit buffer, store decoded pictures, and provide the display buffer. It also holds the user-defined on-screen display (OSD) bitmap and can be used by the microcontroller for private storage of data. For the decoding of MP@ML sequences, 16 Mbits of memory are required. An 8-Mbit mode is also available for the decoding of less demanding sequences.

The video interface outputs digital video in 8-bit serial C_BYC_R format under the control of an external clock and synchronization signals.

During the process of decoding, there are four concurrent activities :

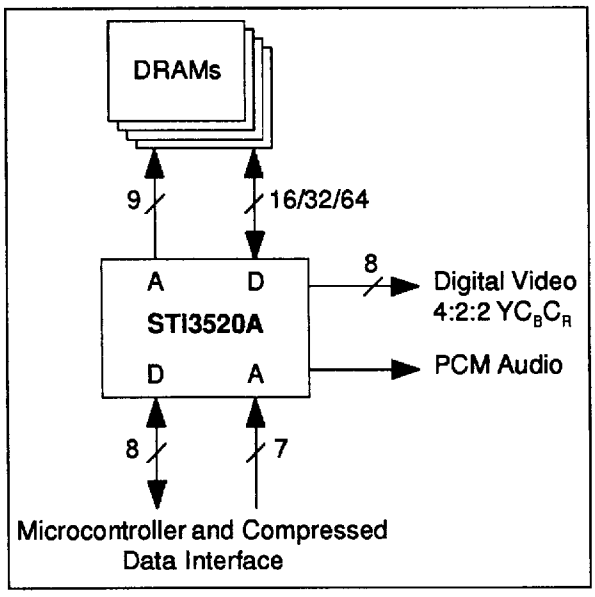
- buffering of the incoming bitstream,
- searching for start codes in the bitstream,
- decoding of a picture,
- display of a picture.

For each of these processes, the microcontroller must set up parameters and monitor events communicated by interrupts. The main features of each of these processes are summarized below.

III.3.1 - Bitstream Buffering

The STi3520A performs the video bitstream buffering needed by the decoder. The size of this buffer, which is located in the DRAM memory, is set up by the user. The bitstream is input through the 8-bit microcontroller data bus. The writing process is asynchronous to all other processes in the

Figure 5 : Decoder System



video decoder. The bitstream data passes through a 1kbit internal FIFO (the compressed data FIFO) before being transferred in packets to the bitstream buffer through the memory data bus. An output signal (and associated interrupt) indicate when this FIFO is full, enabling the use of DMA for bitstream input.

The maximum continuous bitstream input rate is application-dependent. A rate of 15Mbit/s (where 1Mbit/s = 10^6bit/s) is possible when decoding MPEG-2 MP@ML bitstreams. The maximum burst rate, for up to 1kbit bursts, is 228Mbit/s.

The video decoder only accepts MPEG video bitstreams; audio and systems data must not be input.

III.3.2 - Start Code Search

The video decoder is able to decode in its entirety a video bitstream from the slice layer downwards. The user must decode the higher layers (i.e. picture and upwards) in order to extract the information needed for decoding and appropriately set up the video decoder registers and quantization tables. Since the header information is byte-aligned and requires minimal interpretation, this task represents only a small load on the microcontroller.

The start code detector parses the bitstream stored in the bit buffer and locates start codes corresponding to picture layer and above. When one of these start codes has been found, the start code detector stops and raises an interrupt. The microcontroller is then able to read the header data following the start code. The start code detector starts automatically whenever the decoding of a new picture starts and on user command. In normal operation, start code parsing is performed one picture in advance of decoding.

III.3.3 - Decoding

The video decoder is a picture decoder ; it decodes a whole picture and then stops until instructed to decode the next picture present in the video bitstream.

Normally, the decoding of a new picture commences in response to the start of the displaying of a new picture. The registers whose contents can change from picture to picture are double-banked and are updated automatically when decoding starts. The bitstream is read from the bit buffer into the variable-length code decoder (VLD), and picture reconstruction can commence. Any predictors required are fetched from the appropriate area of the external memory, and the reconstructed picture is written back into the area of this memory assigned to the decoded picture.

While a picture is being decoded the start code detector is used to locate the start of next picture header, which the microcontroller then reads in order to set up the double-banked registers for the decoding of the next picture.

III.3.4 - Display

The video decoder is optimized for use with an interlaced display. However, it can also be programmed to produce a non-interlaced (line-sequential) output. The standard video clock rate is 27MHz, which corresponds to a pel rate of 13.5MHz. The active video data output format is compatible with ITU-R 656 ; 00 and FF codes are never generated.

In order to match the horizontal size of the decoded picture to the display line length, an 8-tap upsampling filter, or sample-rate converter (SRC), is provided for both luminance and chrominance. A 2-tap vertical filter is provided for reconstruction of chrominance samples for 4:2:2 output, and for vertical luminance interpolation when displaying half-resolution pictures. The vertical filter includes a data delay line of length 720.

III.3.5 - Enhanced OSD

An on-screen display (OSD) function allows the user to define a bitmap for each field which can be superimposed on the decoded picture output. An OSD bitmap is defined as a set of rectangular regions of programmable position and size, each of which has a unique palette.

OSD data is written into memory areas assigned for this purpose by the user. Reading and writing to and from the memory through the microcontroller interface can take place at any time. A block move feature allows OSD data to be moved from one part of memory to another without microcontroller intervention.

There are two OSD modes, STi3500A compatibility mode, and enhanced mode. In the first mode, each OSD region can use in its bitmap four colours selected from a palette of 4095 colours. The 4096th "colour" is transparency. In the enhanced mode, each region can use 16 colours chosen from a 16384 colour palette. In addition, each region has a "blending factor" defined to enable the mixing of OSD with picture data.

In enhanced mode, memory management by the user is more flexible since OSD regions can be organized in a linked list structure; they do not have to be contiguous in memory.

III.4 - Audio Decoder (see Figure 2)

The audio bit buffer is integrated in the shared DRAM.

The audio decoder has 4 principal blocks :

- *host interface and control registers* : the block implements the 8-bit interface to the host processor. All control registers are accessible through this block.
- *input processor* : the block is responsible for the parsing of the bitstream at the packet level, implementation of the synchronizing algorithms, decoding of time stamps, and the tagging of the audio bitstream with the appropriate PTS before storage in the DRAM. There is an internal 256-byte FIFO buffer.
- *DSP core* : this block performs bitstream decoding and synthesis subband filter execution, according to layers I and II of the MPEG algorithm.
- *PCM output* : this block organises the PCM audio output into the required serial format, and generates all of the D-A converter control signals.

III.5 - Phase Locked Loop and Clock Generation (see Figure 4)

The on-board clock generation consists of a patented frequency synthesizer circuit and fractional dividers which derive all of the required system clocks from a single selectable input, thus eliminating the need for external dividers and PLL circuitry.

The reference input frequency may be obtained from three possible sources :

- the audio DAC clock, PCMCLK,
- the pixel clock, PIXCLK,
- the system input clock CLK, (eg 27MHz).

The selected reference clock frequency is multiplied by a programmable integrated PLL and the output of the PLL is steered to a bank of five programmable fractional dividers to generate each of the five following output clocks :

- the internal MPEG audio decoder clock,
- the internal MPEG video decoder clock,
- the audio DAC clock, PCMCLK,
- the pixel clock, PIXCLK,
- the memory sub-system clock.

The PIXCLK and PCMCLK pins are bidirectional, this ensures compatibility with the STi3520. The CLK pin is input only. As shown above, the decoder clocks for the audio and video decoders in the STi3520A can both be generated internally by the PLL. Alternatively, perhaps needed for compatibility reasons, the PLL can be bypassed giving the following configuration :

Name	Function
CLK	Input Video Decoder Clock (nominally 60MHz)
AUDCLK	Input Audio Decoder Clock (nominally 24MHz)
PCMCLK	Input PCMCLK

Note that if the PLL is bypassed, it is not possible to use EDO or synchronous DRAM which both require the generation of a 80MHz memory clock using the PLL.

IV - MEMORY EXAMPLES

IV.1 - Standard DRAM

The memory interface consists of the following signals :

Name	Function
DD63 - DD0	Bidirectional Data Port
$\overline{AA8}$ - $\overline{AA0}$	Address
$\overline{RAS0}$	Row Address Strobe for Bank 0
$\overline{RAS1}$	Row Address Strobe for Bank 1
$\overline{CAS}$	Column Address Strobe
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable

These signals correspond directly to the standard DRAM signals of the same names. Note that the address output signals are inverted. Memories with multiplexed 9-bit row and 9-bit column addresses must be used. With a video decoder clock of 60MHz, "-80" or faster memories are required. Memory refresh is handled automatically by the STi3520A memory controller by inserting "$\overline{CAS}$ before $\overline{RAS}$" refresh cycles.

Normal (16-Mbit or higher) Mode

In normal mode all 64 bits of the data bus are connected to the memory. The three diagrams below illustrate the memory configurations possible in normal mode. Figure 6 shows the configuration in which there is a single bank of 16 Mbits. The second row address strobe ($\overline{RAS1}$) signal is not used.

Figure 7 shows the configuration in which an extra 4 Mbits is added in the second bank to give a total memory capacity of 20 Mbits. The memory space of the second bank is contiguous with that of the first.

Figure 8 shows the configuration in which both banks contain 16 Mbits giving 32 MBits of memory in total.

Figure 6 : 16-Mbit Memory Configuration

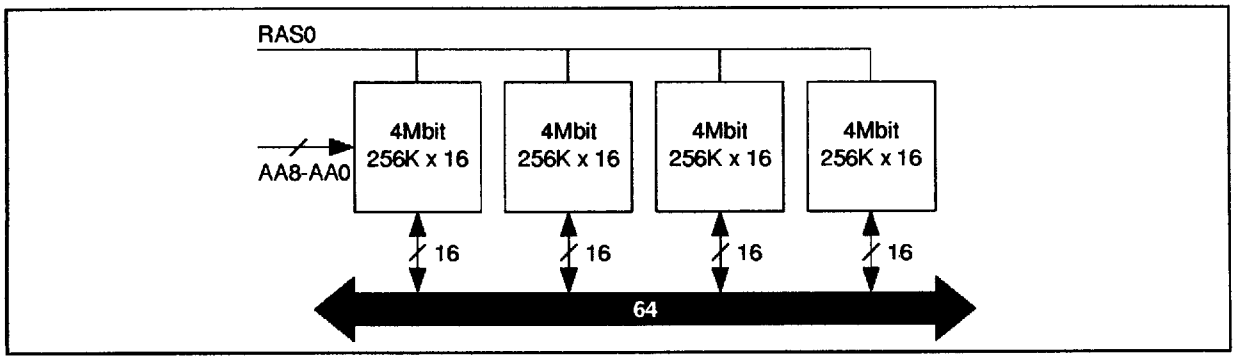


Figure 7 : 20-Mbit Memory Configuration

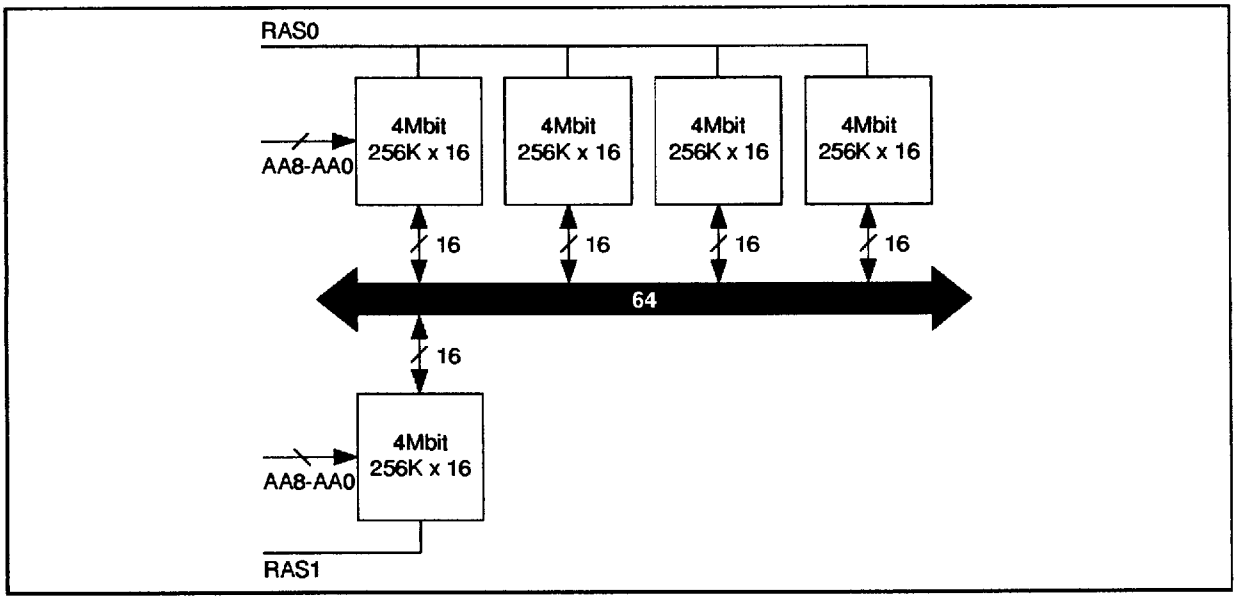
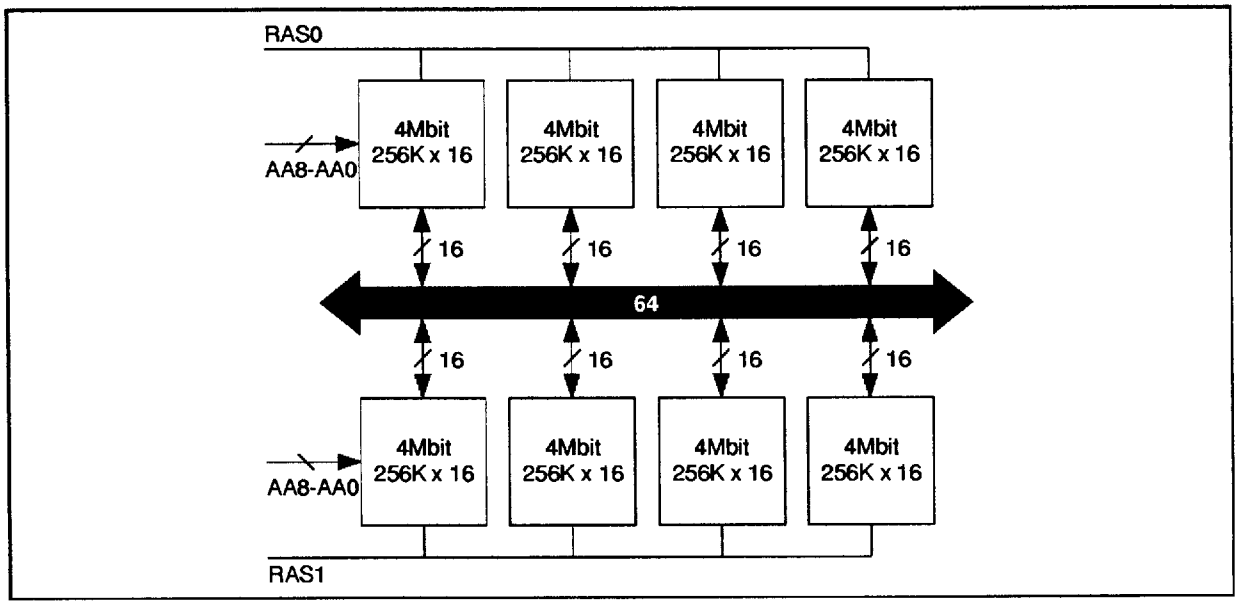


Figure 8 : 32-Mbit Memory Configuration



8-Mbit Mode

In 8-Mbit mode only bits DD47 to DD16 are used. Only one memory configuration is possible (a single bank connected as shown in Figure 9).

IV.2 - Extended Data Out (EDO) DRAM

Extended data out DRAMs (also known as Hyper page DRAMs) effectively place a latch on the data output. This allows the $\overline{CAS}$ signal to go high without having to wait for the data out to become valid as in normal DRAM. As soon as the $\overline{CAS}$ signal goes high precharge for the next column address can begin. This has the net effect of decreasing the page cycle time. The memory interface of the STi3520A takes advantage of this by using a special high frequency $\overline{CAS}$ signal thus allowing the data bus to operate as a 32-bit bus. The interface can support a 16-Mbit configuration as in Figure 10. In this mode only 32 bits of the 64-bit memory data bus are used. The exact pinout is given in Section I.3. The EDO memory interface does not use the same control signals ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$) as standard DRAM. The control signals use the unused data pins of the memory interface.

IV.3 - Synchronous DRAM

The interface can support a 16-Mbit configuration as shown in Figure 11. The exact connection of the memory is given in Section I.3. The control signals for synchronous DRAM (SDRAM) are all synchronous with a clock which is generated internally in the decoder and is output with the control signals via the unused data pins. The control of the SDRAM uses the same signal types as standard DRAM but the signals are all sampled using a clock and a chip select signal.

IV.4 - Memory Size Example

The STi3520A memory management system includes a compression feature which allows MPEG-2 MP@ML decoding in less than 3 frame buffers. This feature allows both PAL and NTSC systems (including OSD) to be implemented in 16-MBit DRAM.

The STi3520A includes a choice of compression modes. The first mode only optimises on luminance and involves no restrictions on output filtering options. The second mode gains more memory but at the expense of the loss of the inter field chrominance filtering on the display. It is expected that in most applications that the loss of this filter will have a negligible effect on image quality. The optimisation mode is selectable in a register.

Typical values for bit rate and PAL picture size have been used for the following example (an NTSC system will require less memory).

Typical OSD Requirements

Memory size required = no of pixels in OSD regions X no of bits per pixel.

Taking as an example a PAL system with a picture size of 720 x 576, the following memory space is required :

Bits/Pixel	Full Screen OSD	Half Screen OSD
2bits/pixel	829,440	414,720
4bits/pixel	1,658,880	829,440
4bits/2 pixels	829,440	414,710

Note that it is possible to change the number of bits per pixel for each region i.e it is possible to specify 4 bits per pixel in one region of the OSD and 2 bits per pixel in other regions.

Figure 9 : 8-Mbit Memory Configuration

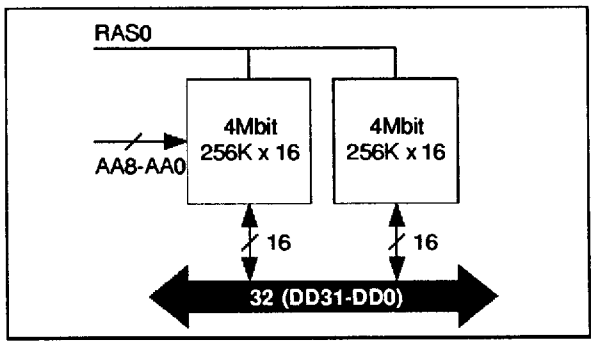


Figure 10 : 16-Mbit EDO DRAM Configuration

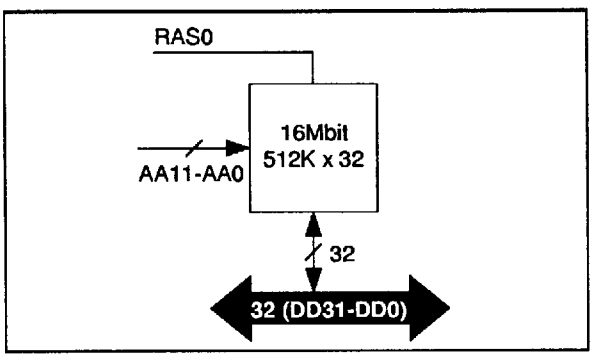
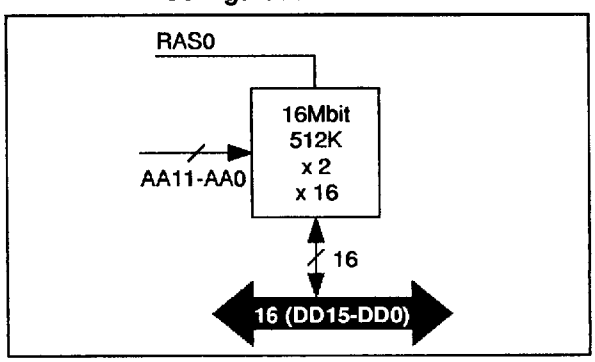


Figure 11 : 16-Mbit Synchronous DRAM Configuration



Optimisation modes

- Optimisation mode 1 (luminance only) :
  MPEG-2 MP @ ML decoding requires 13.640 Mbits.
  Total bit buffer size = 2,670,592 bits.
  Audio bit buffer (assumed 16 kbytes) = 131,072 bits.
  Frame buffers mode 1 : 13.640 Mbits.
  Therefore if there is only 16-MBit of memory, the space for OSD is 335,772 bits.

  Therefore it is not possible to have full screen OSD in this mode in 16 Mbits. It is possible to have full screen OSD in 16 Mbits if the MPEG-2 bitstream is limited at this point to simple profile (ie no B frames). It is also possible to add more memory (total external memory 5 x 4-Mbit DRAMs) to get full screen OSD for a MPEG-2 MP @ ML bitstream. Finally, it is possible to reduce the decoded picture size slightly so that less memory is needed for the decoding and more will be available for the OSD.

- Optimisation mode 2 (chrominance and luminance) :
  MPEG-2 MP @ ML decoding requires 12.995 Mbits.
  Total bit buffer size = 2,670,592 bits
  Audio bit buffer (assumed 16 kbytes) = 131,072 bits.
  Frame buffers mode 2 : 12.995 Mbits.

  Therefore space for OSD is 980,992 bits.
  Therefore it is possible to have a full screen OSD in 16-Mbit memory in this mode if the graphics are defined as 4 bits per 2 pixels (16 colours but less spatial resolution) or 2 bits per pixel (4 colours).
  If the full resolution OSD is required (4 bits per pixel) then one of the 3 techniques mentioned above must be used, ie increase memory up to 20-Mbit, do not allow B frames or reduce the coded image size.

V - SUMMARY SPECIFICATION

V.1 - Video Decoder

Bitstreams Accepted

MPEG-1 video (ISO/IEC 11172-2).

MPEG-2 video (ISO/IEC 13818-2).

MPEG-2 packetised elementary stream (PES) format as defined by ISO/IEC 13818-1.

MPEG-1 ISO/IEC 11172-1 packets.

MPEG-2 Profiles/Levels Supported

Main Profile @ Main Level (MP@ML).

Main Profile @ Low Level (MP @ LL).

Simple Profile @ Main Level (SP @ ML).

Maximum Picture Size

Width : 4080.

Number of macroblocks : 16,383.

Motion Vector Range

MPEG-1 : -1024 to 1023 (full pel), -512 to 511.5 (half pel) horizontal and vertical.

MPEG-2 : -1024 to 1023.5 horizontal and vertical. (vertical range must be reduced in 8-Mbit memory mode with certain picture sizes)

Compressed Data Input

8-bit asynchronous data port (shared with microcontroller interface).

Peak input rate : 28.5Mbyte/s (228Mbit/s).

Maximum sustained input rate (with 55MHz primary clock) : 100Mbit/s in 16-Mbit memory mode, 60Mbit/s in 8-Mbit memory mode.

Microcontroller Interface

8-bit data port with fixed length "WAIT" pulse acknowledge.

Single interrupt request pin.

DRAM Interface

External DRAM used for storage of picture buffers, bit buffer and on-screen display definitions.

16, 32 or 64 bit data bus.

Refresh handled by decoder.

DRAM directly accessible through microcontroller interface.

Configurations supported :

- DRAM : 4 Mbits (1 bank), 8 Mbits (1 bank), 16 Mbits (1 bank), 20 Mbits (2 banks), 32 Mbits (2 banks),
- SDRAM : 1M x 16.

Hyper-page-mode DRAM : 512k x 32.

Start Code Detection

Automatic detection of start codes of picture layer and above to enable microcontroller to access header data.

Counters provided for time-stamp tracking.

Decoding Pipeline

Instruction register set up each picture defines pipeline operation.

Double-buffered quantization matrices enable loading of new tables concurrently with decoding.

Error Concealment

Automatic concealment of errors detected by VLD and decoding pipeline by macroblock copy.

Video Output

8-bit 27MHz multiplexed C_BYC_R port, compatible with ITU-R 601 and 656 (00 and FF values never output).

External pel clock and horizontal/vertical synchronization required.

Interlaced or line-sequential output.

3:2 pulldown operation supported.

Programmable horizontal up-sampling by 8-tap filter.

Vertical chroma reconstruction or luma filtering by 2-tap filter including 720-sample delay line.

Pan & Scan Vectors

Horizontal : Maximum vector size : 512 pels, resolution : 1/8 pel.

Vertical : Maximum vector size : 508 lines, resolution : 4 lines.

On-Screen Display (OSD)

Bitmap separately definable for each field can be superimposed on final picture output.

OSD defined as rectangular regions, each with unique palette defining 4 or 16 colours (including transparency). Each region has a blending factor, which can be selectively applied to each colour in the palette.

Number of regions limited by memory space allocated to OSD. Regions definitions can be organized as a linked list.

Block move facility available for reduction of microcontroller loading.

Video Clock

60MHz maximum.

V.2 - Audio Decoder

Bitstreams Accepted

MPEG-1 audio ISO/IEC 11172-3 audio elementary stream.

MPEG-2 packetised elementary stream (PES) format as defined by ISO/IEC 13818-1.

MPEG-1 ISO/IEC 11172-1 packets.

Audio PCM data (for decoder bypass).

Performance

ISO/IEC 11172-3 Layers I & II.

All MPEG input bitrates supported with sampling rates of 32, 44.1 and 48kHz, free format at 32 & 48kHz sampling rates.

Decodes in single channel, dual channel, stereo, or joint stereo modes.

Audio System Clock

24MHz nominal.

Microcontroller Interface

8-bit interface with "WAIT" signal handshake. Interrupt request signal. Dedicated control inputs for "play" and "mute".

Compressed Data Input

Bit or byte-mode input.

Burst rate up to 20Mbit/s.

PCM Output

16 or 18-pit PCM output.

I^2S and other popular formats supported.

Error Concealment

Automatic error concealment on CRC or synchronization error detection.

V.3 - General

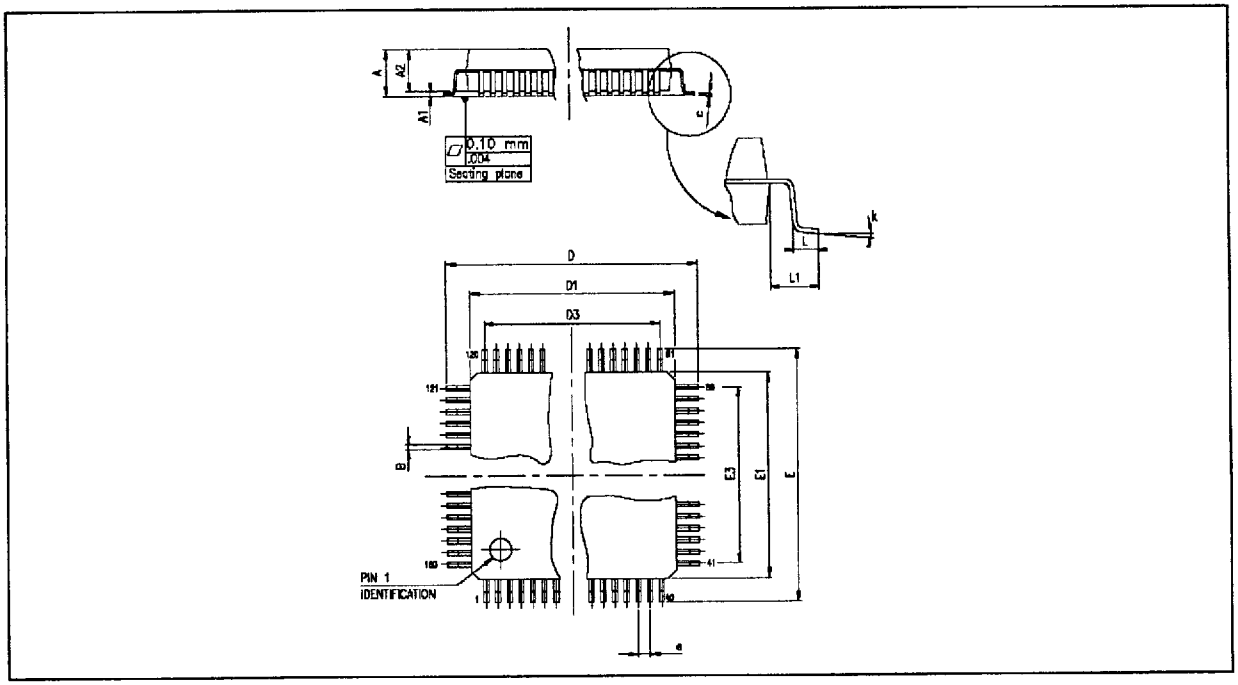
Support for A/V Sync

PTS/DTS extraction from MPEG packet layers with automatic association.

Downsampling

On chip downsampling with anti-aliasing filter.

PACKAGE MECHANICAL DATA
160 PINS - PLASTIC QUAD FLAT PACKAGE



PMPQF160.EPS

Dimensions	Millimeters			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			4.07			0.160
A1	0.25			0.010		
A2	3.17	3.42	3.67	0.125	0.135	0.145
B	0.22		0.38	0.008		0.015
C	0.13		0.23	0.005		0.009
D	30.95	31.20	31.45	1.218	1.228	1.238
D1	27.90	28.00	28.10	1.098	1.102	1.106
D3		25.35			0.998	
e		0.65			0.0256	
E	30.95	31.20	31.45	1.218	1.228	1.238
E1	27.90	28.00	28.10	1.098	1.102	1.106
E3		25.35			0.998	
L	0.65	0.80	0.95	0.026	0.031	0.037
L1		1.60			0.063	
K	0° (min.), 7° (max.)					

PQFP160.TBL