SGS-THOMSON MICROELECTRONICS

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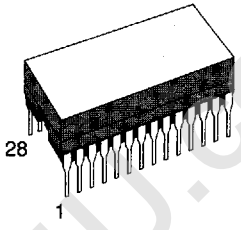
MK48T08
MK48T18

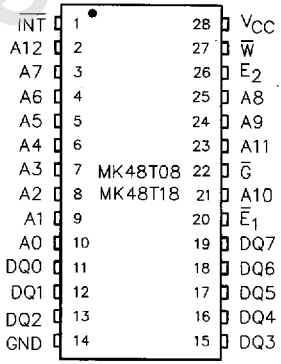
CMOS 8K x 8 TIMEKEEPER SRAM

- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK, CRYSTAL, POWER-FAIL CONTROL CIRCUIT AND BATTERY.
- BYTEWIDE RAM-LIKE CLOCK ACCESS.
- BCD CODED YEAR, MONTH, DAY, DATE, HOURS, MINUTES AND SECONDS.
- SOFTWARE CONTROLLED CLOCK CALIBRATION FOR HIGH ACCURACY APPLICATIONS.
- 10 YEARS OF DATA RETENTION IN THE ABSENCE OF POWER.
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 8K x 8 SRAMS.
- AUTOMATIC POWER-FAIL CHIP DESELECT/WRITE PROTECTION.
- CHOICE OF TWO WRITE PROTECT VOLTAGES:
  - MK48T08 - 4.50 ≤ V_{PFD} ≤ 4.75V
  - MK48T18 - 4.20 ≤ V_{PFD} ≤ 4.50V



PHDIP28 WITH BATTERY TOP HAT (B)

Figure 1. Pin Connections



DESCRIPTION

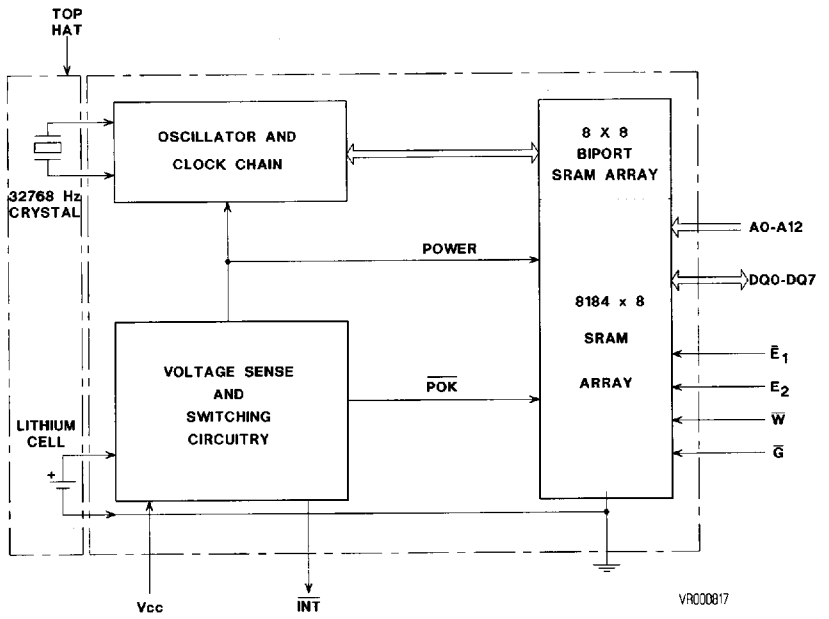
The MK48T08/18 TIMEKEEPER™ RAM combines an 8K x 8 full CMOS SRAM, a BYTEWIDE™ accessible Real Time Clock, a crystal and a long life lithium carbon mono-fluoride battery in a single plastic DIP package. The MK48T08/18 is a non-volatile pin and function equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many EPROM and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing, or limitations on the number of writes that can be performed.

Access to the clock is as simple as conventional BYTEWIDE RAM access because the RAM and the clock are combined on the same die. As Figure 2 indicates, the TIMEKEEPER registers are located in the upper eight locations of the RAM. The registers contain, beginning at the top: year, month, date, day, hour, minutes, and seconds data in 24 hour BCD format. Corrections for 28, 29 (Leap Year), 30 and 31 day months are made automatically. The eighth location is a control register. These registers are not the actual clock counters; they are BiPORT™ read/write Static RAM memory locations. The MK48T08/18 includes a clock control circuit that, once every second, transfers the counter information into the BiPORT RAM.

PIN NAMES

A0-A12	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
$\overline{INT}$	Power Fail Interrupt
$\overline{E}_1$	Chip Enable 1
E_2	Chip Enable 2
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
V_{CC}, GND	5 Volts, Ground

Figure 2. Block Diagram



DESCRIPTION (Continued)

Because the Clock Registers are constructed using BiPORT memory cells, access to the rest of the RAM proceeds unhindered by updates to the TIMEKEEPER registers, even if the TIMEKEEPER registers are being updated at the very moment another location in the memory array is accessed.

The MK48T08/18 also has its own Power-fail Detect circuit. The circuit deselects the device whenever Vcc is below tolerance, providing a high degree of data security in the midst of unpredictable system operations brought on by low Vcc.

TRUTH TABLE

Vcc	$\overline{E}_1$	E_2	$\overline{G}$	$\overline{W}$	Mode	DQ	Power
< Vcc (max)	V_{IH}	X	X	X	Deselect	High Z	Standby
	X	V_{IL}	X	X	Deselect	High Z	Standby
	V_{IL}	V_{IH}	X	V_{IL}	Write	D_{IN}	Active
	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
> Vcc (min)	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD} (min) > V_{SO}	X	X	X	X	Deselect	High Z	CMOS Standby
≤ V_{SO}	X	X	X	X	Deselect	High Z	Battery Back-up Mode

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
P_D	Total Power Dissipation	1.0	W
I_{OUT}	Output Current per Pin	20	mA
V_{DD}	Voltage on any Pin Relative to GND	−0.3 to +7.0	V
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Ambient Storage (V_{CC} Off, Oscillator Off) Temperature	−40 to 85	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

CAUTION: *Negative undershoots below −0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C)

Symbol	Parameter	Min.	Max.	Unit	Notes
V_{CC}	Supply Voltage (MK48T08)	4.75	5.5	V	1
V_{CC}	Supply Voltage (MK48T18)	4.5	5.5	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3V	V	1
V_{IL}	Logic "0" Voltage All Inputs	−0.3	0.8	V	1, 2

DC ELECTRICAL CHARACTERISTICS

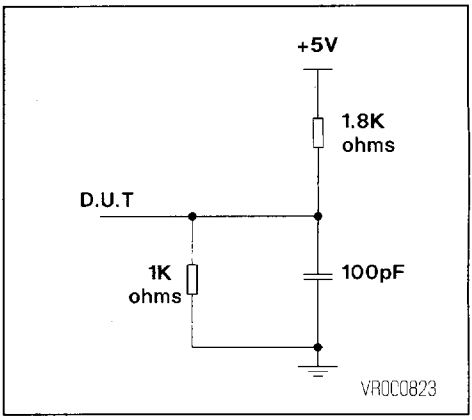
(0°C ≤ T_A ≤ +70°C; V_{CCmin} ≤ V_{CC} ≤ V_{CCmax})

Symbol	Parameter	Min.	Max.	Unit	Notes
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	3
I_{CC2}	TTL Standby Current ($\overline{E}_1$ = V_{IH} or E_2 = V_{IL})		3	mA	6
I_{CC3}	CMOS Standby Current ($\overline{E}_1$ = V_{CC} −0.2V)		3	mA	4, 6
I_{IL}	Input Leakage Current (Any Input)	−1	1	µA	5
I_{OL}	Output Leakage Current	−5	5	µA	5
V_{OH}	Output Logic "1" Voltage (I_{OUT} = −1.0mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = +2.1mA)		0.4	V	
V_{INT}	$\overline{INT}$ Logic "0" Voltage (I_{OUT} = +0.5mA)		0.4	V	

AC TEST CONDITIONS

Input Levels	0.0 V to 3.0 V
Transition Times	5 ns
Input and Output Timing Reference Levels	1.5 V

OUTPUT LOAD DIAGRAM



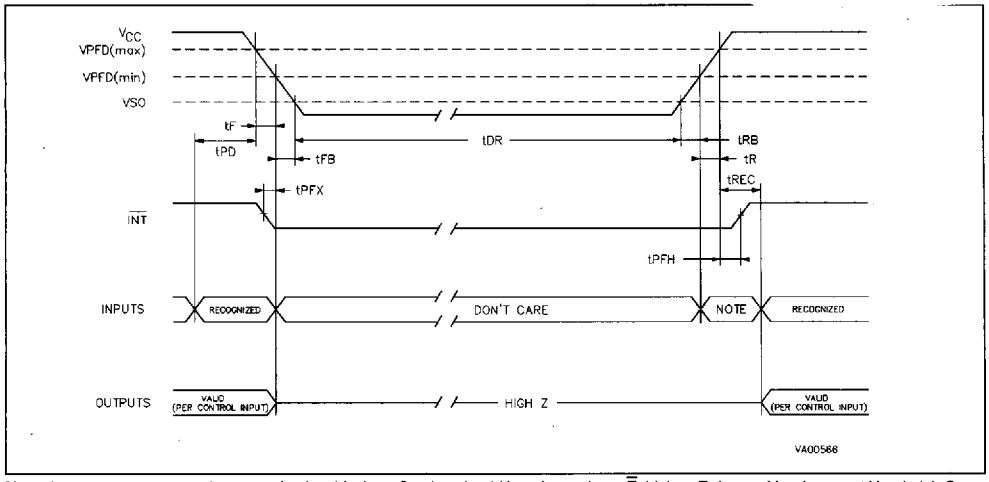
CAPACITANCE

(T_A = 25°C)

Symbol	Parameter	Max.	Unit	Notes
C_I	Capacitance On All Pins (except DQ)	10.0	pF	7
C_O	Capacitance On DQ Pins	10.0	pF	7, 8

Notes :
1. All voltages referenced to GND.
2. Negative spikes of -1.0 volt allowed for up to 10 ns once per Cycle.
3. I_{CC1} measured with outputs open.
4. 1 mA typical.
5. Measured with $V_{CC} \geq V_I \geq$ GND and outpus deselected.
6. Measured with Control Bits set as follows : R = 1 ; W, ST, FT = 0.
7. Effective capacitance calculated from the equation $C = I \Delta t/\Delta V$ with ΔV = 3 volts and power supply at 5.0 V.
8. Measured with outputs deselected.

Figure 3. Power Down/Up Timing



Note: Inputs may or may not be recognized at this time. Caution should be taken to keep $\overline{E}_1$ high or E_2 low as V_{CC} rises past V_{PFD}(min). Some systems may performs inadvertent write cycles after V_{CC} rises above V_{PFD}(min) but before normal system operations begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

AC ELECTRICAL CHARACTERISTICS (Power Up/Down Timing) ($0°C \le T_A \le +70°C$)

Symbol	Parameter	Min.	Max.	Units	Notes
t_{PD}	$\overline{E}_1$ or $\overline{W}$ at V_{IH} or E_2 at V_{IL} before Power Down	0		µs	
t_F	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs	2
t_{FB}	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs	3
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time	0		µs	
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs	
t_{REC}	$\overline{E}_1$ or $\overline{W}$ at V_{IH} or E_2 at V_{IL} after Power Up	1		ms	
t_{PFX}	$\overline{INT}$ Low to Auto Deselect	10	40	µs	
t_{PFH}	V_{PFD} (max) to $\overline{INT}$ High		120	µs	4

DC ELECTRICAL CHARACTERISTICS (Power Up/Down Trip Points) ($0°C \le T_A \le +70°C$)

Symbol	Parameter	Value			Units	Notes
		Min.	Typ.	Max.		
V_{PFD}	Power-fail Deselect Voltage (MK48T08)	4.5	4.6	4.75	V	1
V_{PFD}	Power-fail Deselect Voltage (MK48T18)	4.2	4.3	4.5	V	1
V_{SO}	Battery Back-up Switchover Voltage		3.0		V	1
t_{DR}	Expected Data Retention Time	10			YEARS	5

Notes : 1. All voltages referenced to GND.

2. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).

3. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

4. $\overline{INT}$ may go high anytime after V_{CC} exceeds V_{PFD} (min) and is guaranteed to go high t_{PFH} after V_{CC} exceeds V_{PFD} (max).

5. @ 25°C.

READ MODE

The MK48T08/18 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high, $\overline{E}_1$ (Chip Enable 1) is low, and E_2 (Chip Enable 2) is high. The device architecture allows ripple through access of data from eight of 65,536 locations in the static storage array. Thus, the unique address specified by the 13 Address Inputs defines which one of the 8,192 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} after the last address input signal is stable, providing that the Chip Enable and Output Enable access times are satisfied.

If Chip Enable or Output Enable access times are not yet met, valid data will be available at the latter of Chip Enable Access Time (t_{ELQV}) or at Output Enable Access Time (t_{GLQV}). The state of the eight three-state Data I/O signals is controlled by Chip Enable and Output Enable. If the Outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while Chip Enable and Output Enable remain low, output data will remain valid for Output Hold from Address (t_{AXQX}) but will go indeterminate until the next Address Access.

AC ELECTRICAL CHARACTERISTICS (Read Cycle)

($0°C \le T_A \le +70°C$; V_{CC} min $\le V_{CC} \le$ V_{CC} max)

Symbol	Parameter	MK48Tx8-10		MK48Tx8-15		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{E1LQX}	Chip Enable 1 to Q Low-Z	10		10		ns	
t_{E2HQX}	Chip Enable 2 to Q Low-Z	10		10		ns	
t_{AXQX}	Output Hold from Address	5		5		ns	
t_{GLQX}	Output Enable to Q Low-Z	5		5		ns	
t_{AVAV}	Read Cycle Time	100		150		ns	
t_{AVQV}	Address Access Time		100		150	ns	
t_{E1LQV}	Chip Enable 1 Access Time		100		150	ns	
t_{E2HQV}	Chip Enable 2 Access Time		100		150	ns	
t_{GLQV}	Output Enable Access Time		50		75	ns	
t_{E1HQZ}	Chip Enable 1 to Q High-Z		50		75	ns	
t_{E2LQZ}	Chip Enable 2 to Q High-Z		50		75	ns	
t_{GHQZ}	Output Disable to Q High-Z		40		60	ns	

Figure 4. Read Timing n° 1 (Address Access)

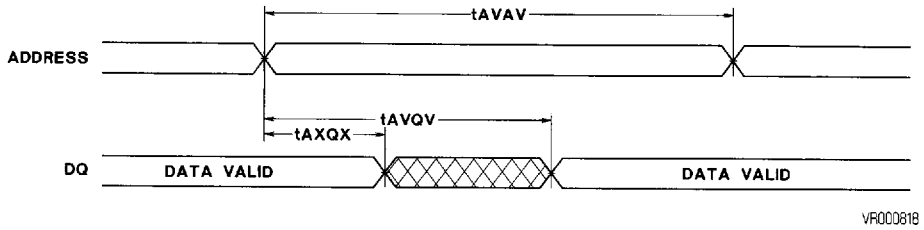
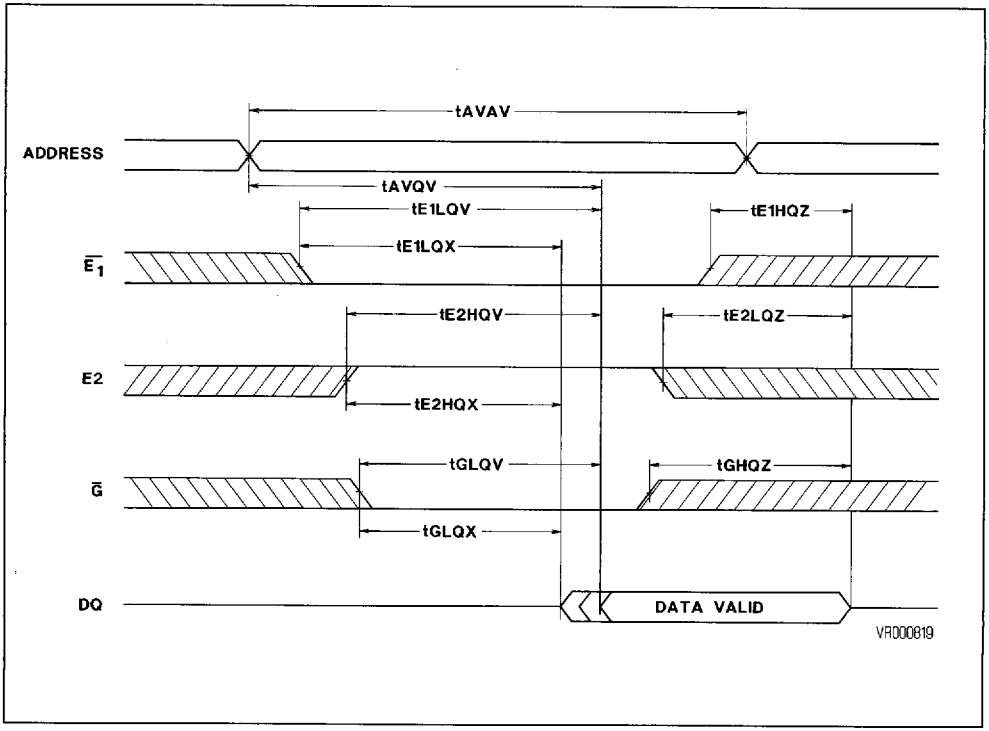


Figure 5. Read Timing n° 2



WRITE MODE

The MK48T08/18 is in the Write Mode whenever Write Enable and Chip Enable are active. The start of a write is referenced to the latter occurring falling edge of $\overline{W}$ or $\overline{E}_1$ or rising edge of E_2. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}_1$, or the falling edge of E_2. The addresses must be held valid throughout the cycle. $\overline{E}_1$ or $\overline{W}$ must return high or E_2 low for minimum of t_{E1HAX} or t_{E2LAX} prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward.

Because $\overline{G}$ is a Don't Care in the Write Mode and a low on $\overline{W}$ will return the outputs to High-Z, $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

AC ELECTRICAL CHARACTERISTICS (Write Cycle)

($0°C \le T_A \le +70°C$; V_{CC} min $\le V_{CC} \le$ V_{CC} max)

Symbol	Parameter	MK48Tx8-10		MK48Tx8-15		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{AVWL}	Address Set-Up Time to $\overline{W}$ Low	0		0		ns	
t_{AVE1L}	Address Set-Up Time to Chip Enable Active	0		0		ns	
t_{AVE2H}		0		0		ns	
t_{E1HAX}	Write Recovery from Chip Enable (Address Hold Time)	10		10		ns	2
t_{E2LAX}		10		10		ns	2
t_{WHDX}	Data Hold Time	5		5		ns	1, 2
t_{AVAV}	Write Cycle Time	100		150		ns	
t_{AVWH}	Address Valid to $\overline{W}$ High	80		130		ns	
t_{WLWH}	Write Pulse Width	80		100		ns	
t_{WHAX}	Address Hold after End of Write	10		10		ns	1
t_{E1LE1H}	Chip Enable Active to End of Write	80		130		ns	2
t_{E2HE2L}		80		130		ns	2
t_{DVWH}	Data Valid to End of Write	50		70		ns	1, 2
t_{WHQX}	End of Write to Q Low-Z	10		10		ns	
t_{WLQZ}	$\overline{W}$ Low to Q High-Z		50		75	ns	

Notes:

1. In a $\overline{W}$ Controlled Cyle.
2. In a $\overline{E}_1$, E_2 Controlled Cycle.

Figure 6. Write Control Write Cycle Timing

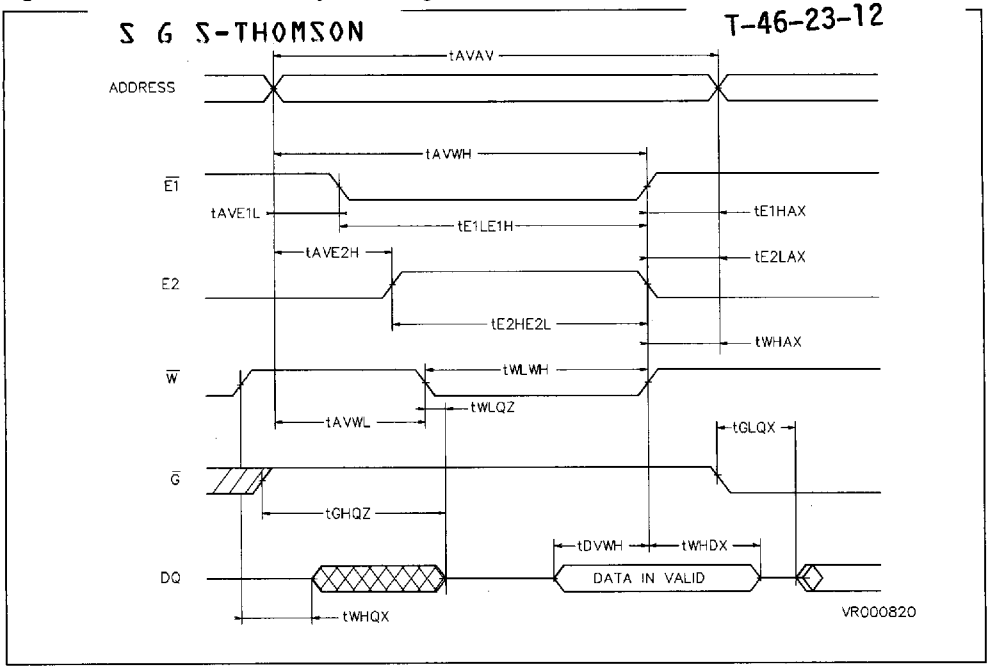
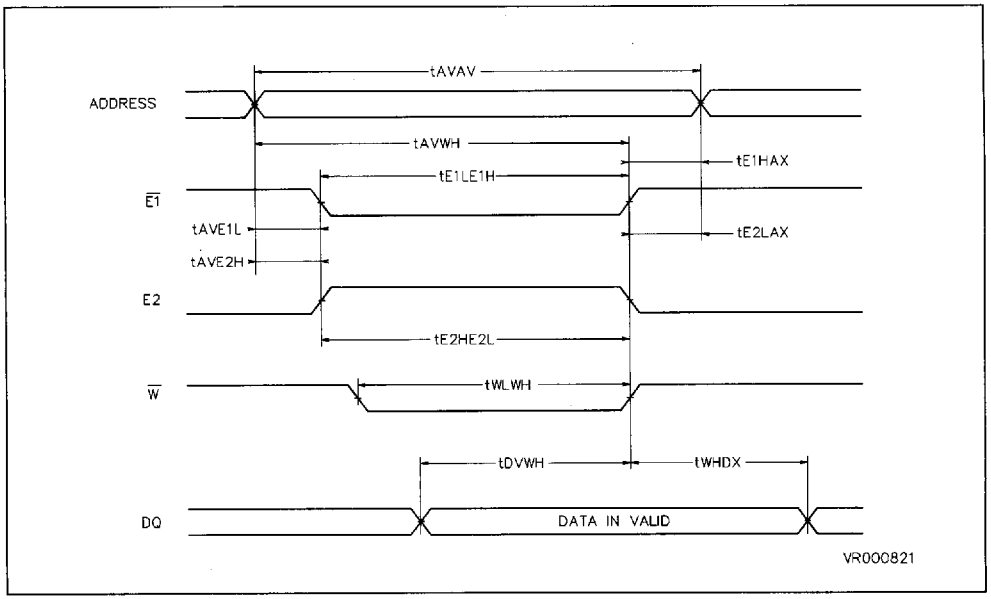


Figure 7. Chip Enable Control Write Cycle Timing



DATA RETENTION MODE

With V_{CC} applied, the MK48T08/18 operates as a conventional BYTEWIDE Static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(Max), V_{PFD}(Min) window.

Note: A mid-write cycle power failure may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(Min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The MK48T08/18 may respond to transient noise spikes on Vcc that reach into the deselect window if this should occur during the time the device is sampling V_{CC}. Therefore decoupling of the power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD}(Max). Caution should be taken to keep $\overline{E}_1$ high or E_2 low as Vcc rises past V_{PFD} (Min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

POWER FAIL INTERRUPT

The MK48T08/18 continuously monitors V_{CC}. When V_{CC} falls to the power-fail detect trip point of the MK48T08/18 an interrupt is immediately generated. An internal clock provides a delay no less than 10 µs but no greater than 40 µs before automatically deselecting the MK48T08/18. The $\overline{INT}$ pin is an open drain ouput and requires an external pull up resistor.

PREDICTING BACK-UP SYSTEM LIFE

The useful life of the battery in the MK48T08/18 is expected to ultimately come to an end for one of two reasons: either because it has been discharged while providing current to an external load; or because the effects of aging render the cell useless before it can actually be discharged. Fortunately, these two effects are virtually unrelated, allowing discharge, or Capacity Consumption, and the effects of aging, or Storage Life, to be treated as two independent but simultaneous mechanisms, the earlier of which defines Back-up System life.

The current drain that is responsible for Capacity Consumption can be reduced either by applying Vcc or turning off the oscillator. With the oscillator off, only the leakage currents required to maintain data in the RAM are flowing. With V_{CC} on, the battery is disconnected from the RAM. Because the leakage currents of the MK48T08/18 are so low, they can be neglected in practical Storage Life calculations.Therefore, application of Vcc or turning off the oscillator can extend the effective Back-up System life.

PREDICTING STORAGE LIFE

Figure 8 illustrates how temperature affects Storage Life of the MK48T08/18 battery. The life of the battery is controlled by temperature and is virtually unaffected by leakage currents drawn by the MK48T08/18.

Storage Life predictions presented in Figure 8 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. Obviously, temperature accelerated testing cannot identify non-temperature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of SGS-THOMSON's on going battery testing since it began in 1982, we believe the chance of such failure mechanisms surfacing is extremely small. For the purpose of the testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.4 volt closed-circuit voltage across a 250K load resistance.

Two end of life curves are presented in Figure 8. The are labeled "Average" ($t_{50\%}$) and ($t_{1\%}$). These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 70°C is at issue, Figure 8 indicates that a particular MK48T08,T18 has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 20 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience a battery failure within 11 years; 50% of them can be expected to experience a failure within 20 years.

The $t_{1\%}$ figure represents the practical onset of wear out, and is therefore suitable for use in what would normally be thought of as a worst-case analysis. The $t_{50\%}$ figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Each MK48T08/18 is marked with a nine digit manufacturing date code in the form H99XXYYZZ, example: H995B9231 is H - fabricated in Carrollton, TX; 9 - assembled in Muar, Malaysia;; 9 - tested in Muar, Malaysia; 5B - lot designator; 9231 - assembled in the year 1992, work week 31.

Calculating Predicted Storage Life of the Battery

As Figure 8 indicates, the predicted Storage Life of the battery in the MK48T08/18 is a function of temperature.

Because the ambient temperature profile is dependent upon application controlled variables, only the user can estimate predicted Storage Life in a given design. As long as ambient temperature is held reasonably constant, expected Storage Life can be read directly from Figure 8. If the MK48T08/18 spends an appreciable amount of time at a variety of temperatures, the following equation should be used to estimate Storage Life.

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Predicted Storage Life = $1 / \{ [(TA_1 / TT) / SL_1] + [(TA_2 / TT) / SL_2] + ... + [(TA_N / TT) / SL_N] \}$

Where TA_1, TA_2, TA_N, = Time at Ambient Temperature 1, 2, etc.

TT = Total Time = $TA_1 + TA_2 + ... + TA_N$

SL_1, SL_2, SL_N = Predicted Storage Life at Temp. 1, Temp. 2, etc. (See Figure 8)

Example Predicted Storage Life Calculation

A cash register/terminal operates in an environment where the MK48T08/18 is exposed to temperatures of 55°C or less for 8322 hrs./yr.; and temperatures greater than 60°C, but less than 70°C, for the remaining 438 hrs./yr.

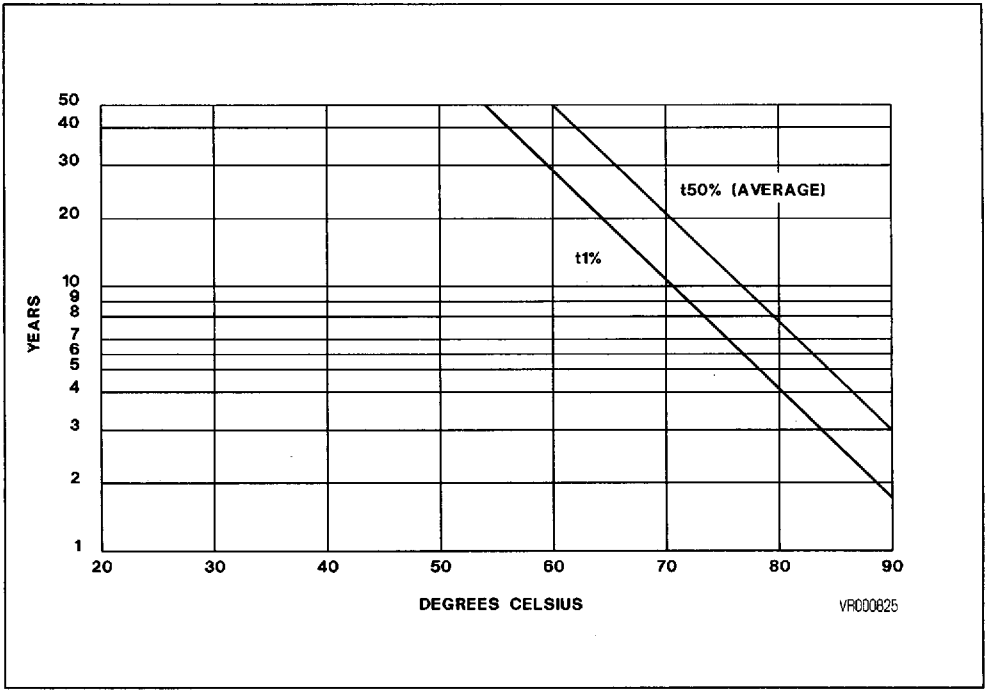
Reading Predicted $t_{1\%}$ values from Figure 8; SL_1 = 41 yrs., SL_2 = 11.4 yrs.,

Total Time (TT) = 8760 hrs./yr. TA_1 = 8322 hrs./yr. TA_2 = 438 hrs./yr. .

Predicted Typical Storage Life $\geq 1 / \{ [(8322 / 8760) / 41] + [(438 / 8760) / 11.4]$

Predicted Typical Storage Life $\geq$ 36 years

Figure 8. Predicted Battery Storage Life Versus Temperature



Calculating Predicted Capacity Consumption

The MK48T08/18 internal cell has a nominal capacity of 39mAh. The device places a nominal RAM and TIMEKEEPER load of less than 445nA at room temperature. At this rate, the Capacity Consumption life is 39E-3/445E-9=87640 hours or about 10 Years. The Capacity Consumption life can be extended by applying Vcc or turning off the oscillator. For example, if the oscillator runs 100% of the time but Vcc is applied 60% of the time, the Capacity Consumption life is 10/(1-.6) = 25 years.

Estimated Back-up System Life

Since either Storage or Capacity Consumption can end the Battery's life, System Life is marked by which-ever occurs first.

CLOCK OPERATIONS

Reading the Clock

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading of data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual counter, updating the registers can be halted without disturbing the clock itself.

Updating is halted when a "1" is written into the "Read" bit, the seventh bit in the Control Register. As long as a "1" remains in that position, updating is halted. After a Halt is issued, the registers reflect the count, that is the day, date, and time that were current at the moment the Halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A Halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a "0".

Setting the Clock

The eighth bit of the Control register is the "Write" bit. Setting the Write bit to a "1", like the Read bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date and time data in 24 Hour BCD format. Resetting the Write bit to a "0" then transfers those values to the actual TIMEKEEPER counters and allows normal operation to resume.

Stopping and Starting the Oscillator

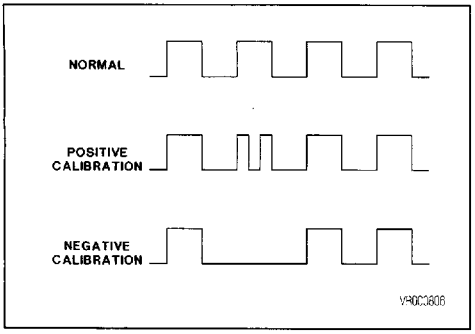
The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain from the battery. The "Stop" bit is the MSB for the Seconds Register. Setting it to a "1" stops the oscillator. The MK48T08/18 is shipped from SGS-Thomson with the "Stop" bit set to a "1". When reset to a "0", the MK48T08/18 oscillator starts within 3 seconds typically. Because of this delay, it is recommended to start the oscillator prior to setting the time.

Figure 9. The MK48T08/18 Register Map

Address	Data								Function/Range BCD Format	
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1FFF									Year	00-99
1FFE	0	0	0						Month	01-12
1FFD	0	0							Date	01-31
1FFC	0	FT	0	0	0				Day	01-07
1FFB	0	0							Hour	00-23
1FFA	0								Minutes	00-59
1FF9	ST								Seconds	00-59
1FF8	W	R	S						Control	

KEYS : **S** = SIGN BIT **FT** = FREQUENCY TEST BIT **R** = READ BIT
W = WRITE BIT **ST** = STOP BIT **0** = MUST BE WRITTEN TO 0

Figure 10.



Calibrating the Clock

The MK48T08/18 is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The crystal is mounted in the tophat along with the battery. A typical MK48T08/18 is accurate within ±1 minute per month at 25°C without calibration. The devices are tested not to exceed 35 PPM (parts per million) oscillator frequency error at 25°C, which equates to about ± 1.53 minutes per month. Of course the oscillation rate of any crystal changes with temperature. Figure 11 shows the frequency error that can be expected at various temperatures. Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The MK48T08/18 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 128 stage, as shown in Figure 10. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits in the Control register. This byte can be set to represent any value between 0 and 31 in binary form. The sixth bit is a sign bit; "1" indicates positive calibration, "0" indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary "1" is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

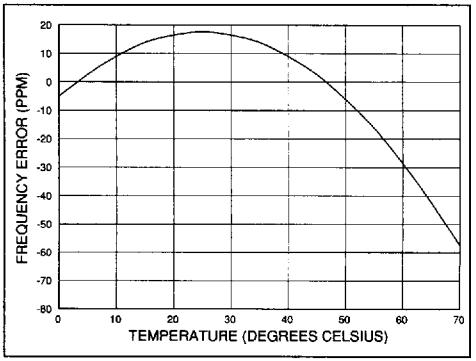
Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or -2.034 PPM of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the Calibration byte would represent +10.7 or - 5.35 seconds per month which corresponds to a total range of +5.5 or -2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given MK48T08/18 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accesses the Calibration byte. The utility could even be menu driven and made foolproof.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) bit, the seventh-most significant bit in the Day Register, is set to a "1", and the oscillator is running at 32,768 Hz, the LSB (DQ0) of the Seconds Register will toggle at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 PPM oscillator frequency error, requiring a -10(001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency. The device must be selected and addresses must stable at Address 1FF9 when reading the 512 Hz on DQ0.

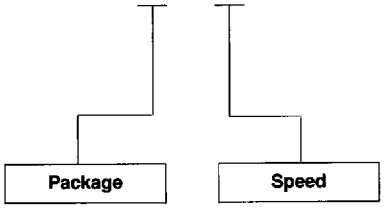
The FT bit must be set using the same method used to set the clock, using the Write bit. The LSB of the Seconds Register is monitored by holding the MK48T08/18 in an extended read of the Seconds Register, without having the Read bit set. The FT bit MUST be reset to "0" for normal clock operations to resume.

Figure 11. Frequency Error



ORDERING INFORMATION

Example: MK48T08 B 10



For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information or any aspect of this device, please contact our Sales Office nearest to you.