HA11883MP

T-77-17

Video Camera Encoder

HA11883MP is a video camera encoder IC. PAL or NTSC signals can be derived from B – Y, R – Y and Y signals.

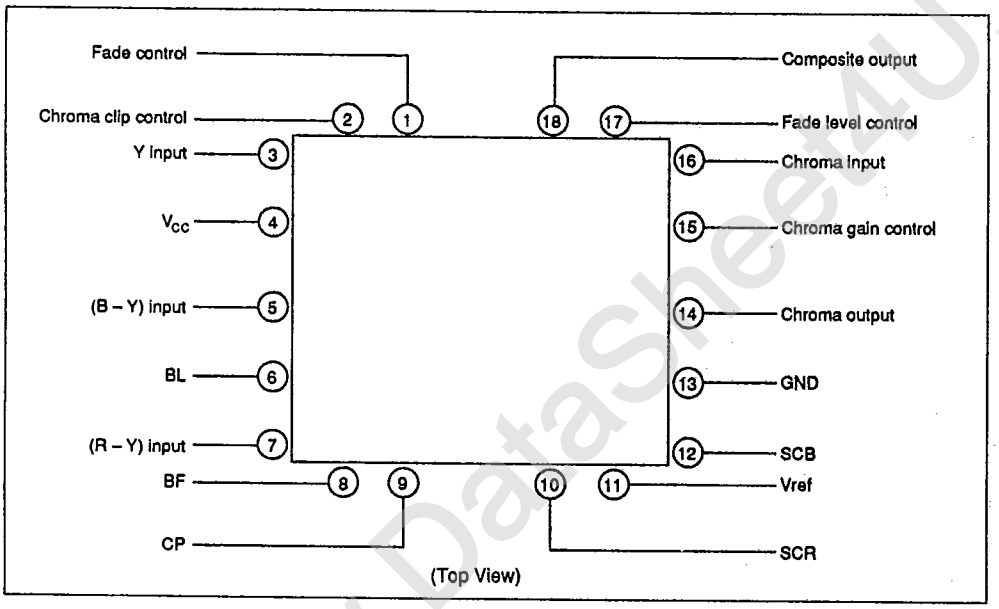
Features

- Lower supply current
- A host of on-chip functions
  - Adjustable fade level
  - Adjustable chroma gain
  - Adjustable chroma clip
- Applicable in both NTSC and PAL systems
- Compact package

Ordering Information

Type No.	Package
HA11883MP	MP-44

Pin Arrangement



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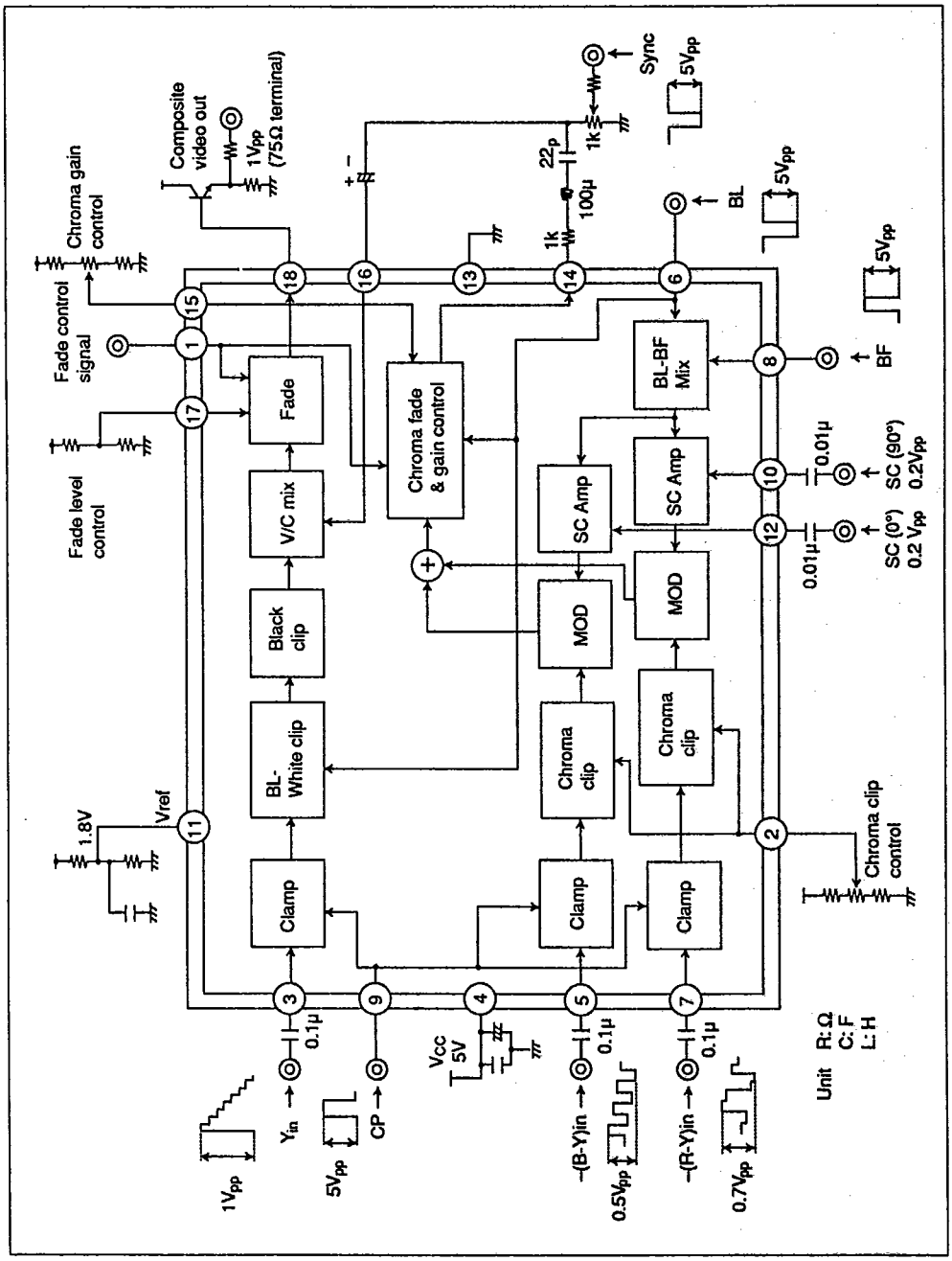
Block Diagram



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Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	7.0	V
Power Dissipation *1	P_T	220	mW
Operating Temperature	T_{opr}	−10 to +75	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Recommended Operating Voltage	V_{opr}	5.0 ± 25	V

Note: *1 Value when MSP connected under following conditions:
Base material : glass epoxy 40mm × 1.5mm
Wiring density : 30%

Electrical Characteristics (V_{CC} = 5V, Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Applicable Terminal
Supply Current	Icc	15	22	30	mA		4
Y Gain	G_Y	1.9	3.0	4.0	dB	f = 200kHz	3, 18
Y Frequency Characteristics	fcy	7	14	–	MHz		3, 18
Y Fade Sensitivity 1	△Gfy1	–	0	0.5	dB	V1 = 1V	1, 18
Y Fade Sensitivity 2	△Gfy2	2	7.5	13	dB	V1 = 2.5V	1, 18
Y Fade Sensitivity 3	△Gfy3	32	37	–	dB	V1 = 4V	1, 18
Y Input Clamp Voltage	V3	1.78	1.80	1.83	V		3
Composite Output Terminal Voltage	V18	1.7	2.46	3.0	V		18
No Signal Output Level	△V18	−5	17	37	mV	BL ON/OFF DC difference voltage	6, 18
White Clip Level	Wclo	111	125	131	%	V6 = 5V	6, 18
Fadeout Level 1	Vfo1	−50	0	50	mV	V17 = 1V	17, 18
Fadeout Level 2	Vfo2	0.55	0.75	0.95	V	V17 = 2.2V	17, 18
Fadeout Level 3	Vfo3	1.5	1.8	2.1	V	V17 = 4V	17, 18
Chroma Gain	Gc	10.0	11.2	12.2	dB	f = 3.58MHz	16, 18
Chroma Frequency Characteristics	fcc	7	18	–	MHz		16, 18
Chroma Fade Sensitivity 1	△Gfc1	–	0	0.5	dB	V1 = 1V	1, 18
Chroma Fade Sensitivity 2	△Gfc2	2	7.5	13	dB	V1 = 2.5V	1, 18
Chroma Fade Sensitivity 3	△Gfc3	30	–	–	dB	V1 = 4V	1, 18
Differential Gain	DG	–	–	10	%		3, 16, 18
Differential Phase 1	DP1	–	–	8	deg		3, 16, 18
Differential Phase 2	DP2	–	–	8	deg		3, 16, 18

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Item	Symbol	Min	Typ	Max	Unit	Test Condition	Applicable Terminal
Chroma Input Impedance	Zi16	3.6	5.0	7.2	kΩ		16
Composite Output Impedance	Zo18	–	125	240	Ω		18
(R – Y) Gain	G_R	10.5	12.2	13.5	dB	V15 = 0V	7, 14
(B – Y) Gain	G_B	10.5	12.2	13.5	dB	V15 = 0V	5, 14
(R – Y) (B - Y) Gain Deviation	$\triangle G_{RB}$	–	0	0.7	dB	V15 = 0V	5, 7, 14
(R – Y) Maximum Output	V_R MAX	1.5	1.82	–	Vpp	V15 = 0V	7, 14
(B – Y) Maximum Output	V_B MAX	1.3	1.64	–	Vpp	V15 = 0V	5, 14
Chroma Fade Sensitivity 4	△Gfc4	–	0	0.5	dB	V1 = 1V	1, 14
Chroma Fade Sensitivity 5	△Gfc5	1.0	4.0	8.0	dB	V1 = 2.5V	1, 14
Chroma Fade Sensitivity 6	△Gfc6	30	45	–	dB	V1 = 4V	1, 14
Sub-Carrier *** Deviation	$\triangle \theta_{RB}$	–	0	5	deg		10, 12, 14
R ch Minimum Carrier Level	VscR MIN	–	–	50	mV		10, 14
B ch Minimum Carrier Level	VscB MIN	–	–	50	mV		12, 14
Chroma Gain Sensitivity 1	△Gc1	1.0	3.0	5.0	dB	V15=2.1V	15, 14
Chroma Gain Sensitivity 2	△Gc2	5.0	7.0	9.5	dB	Pin 15 open	15, 14
Chroma Gain Sensitivity 3	△Gc3	6.0	9.0	12.0	dB	V15=2.65V	15, 14
Carrier Leak	V_{CAL}	–	–	60	mVpp		10, 12,14
(R – Y) Input Clamp Voltage	V7	2.8	2.95	3.1	V		7
(B – Y) Input Clamp Voltage	V5	2.8	2.95	3.1	V		5
Chroma Output Terminal Voltage	V14	1.87	2.32	2.77	V		14
R ch Carrier Input Terminal Voltage	V10	3.70	3.93	4.16	V		10
B ch Carrier Input Terminal Voltage	V12	3.70	3.93	4.16	V		12
Upper (R – Y) Clip Level A	CLrua	108	123	138	%	Pin 2 open	2, 14
Upper (R – Y) Clip Level B	CLrub	118	136	154	%	V2 = 3.3V	2, 14
Lower (R – Y) Clip Level A	CLrla	108	122	136	%	Pin 2 open	2, 14
Lower (R – Y) Clip Level B	CLrlb	121	136	151	%	V2 = 3.3V	2, 14
Upper (B – Y) Clip Level A	CLbua	110	125	138	%	Pin 2 open	2, 14
Upper (B – Y) Clip Level B	CLbub	125	140	155	%	V2 = 3.3V	2, 14
Lower (B - Y) Clip Level A	CLbla	114	129	142	%	Pin 2 open	2, 14
Lower (B – Y) Clip Level B	CLblb	129	144	159	%	V2 = 3.3V	2, 14
R ch Carrier Input Impedance	Zi10	6.5	10.3	–	kΩ		10
B ch Carrier Input Impedance	Zi12	6.5	10.3	–	kΩ		12
Chroma Output Impedance	Zo14	–	90	150	Ω		14
Clamp ON Level	Vcpon	2.1	–	–	V		9, 7
Clamp OFF Level	Vcpoff	–	–	0.9	V		9, 7

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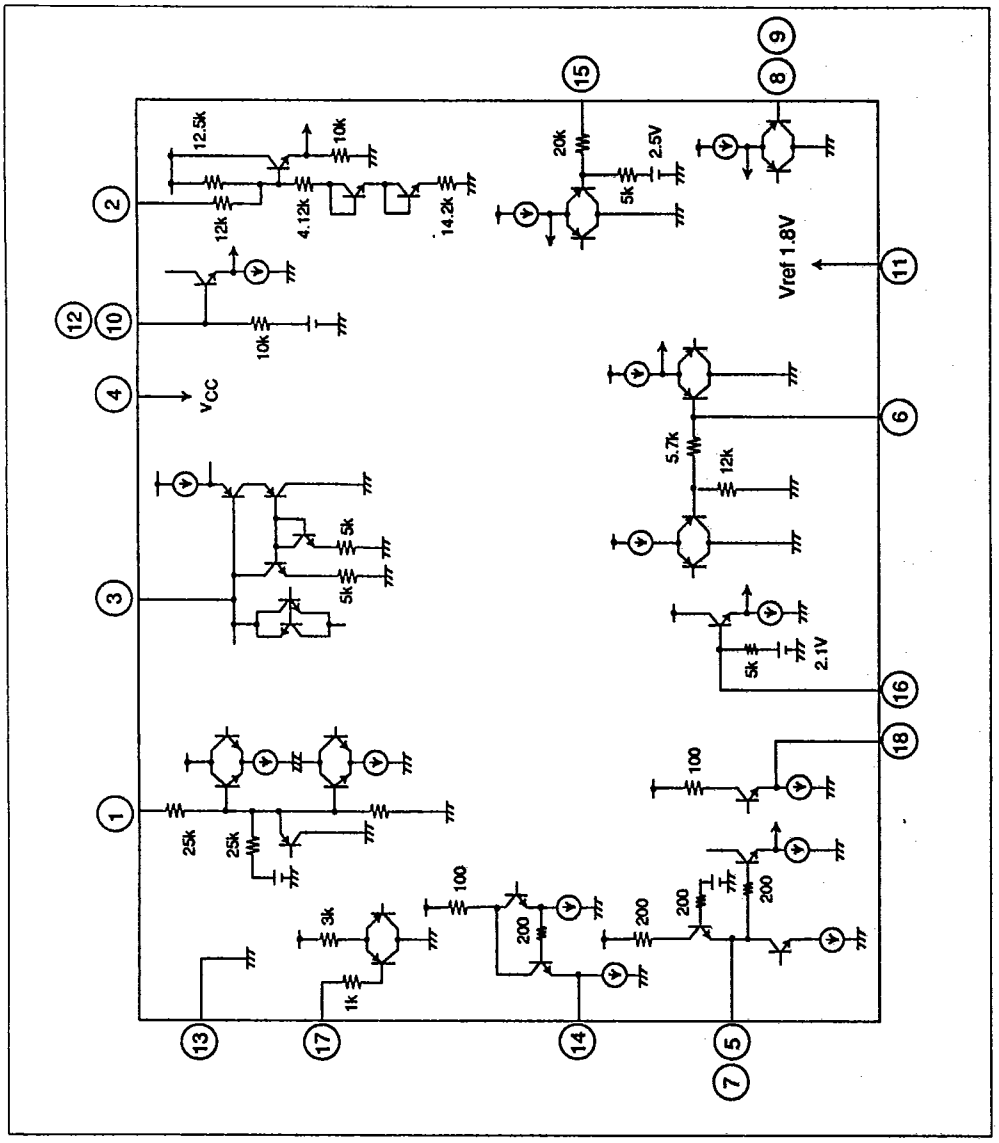
Input/Output Circuit



Chroma Modulator Circuit

This circuit, illustrated in figure 1, first clips the chroma signals that are input from pin 5 and pin 7 and them modulates them. R ch (pin 5) and B ch (pin 7) are of reverse polatiry (—(R – Y), —(B – Y)). Figure 2 shows the modulating waveforms and the modulated waveforms. In order to make figure 2 easier to understand, the B ch (—(B – Y)) input is 0. Figure 3 illustrates adjustment of the chroma clip level. The purpose of the clip circuit is to prevent overmodulation.

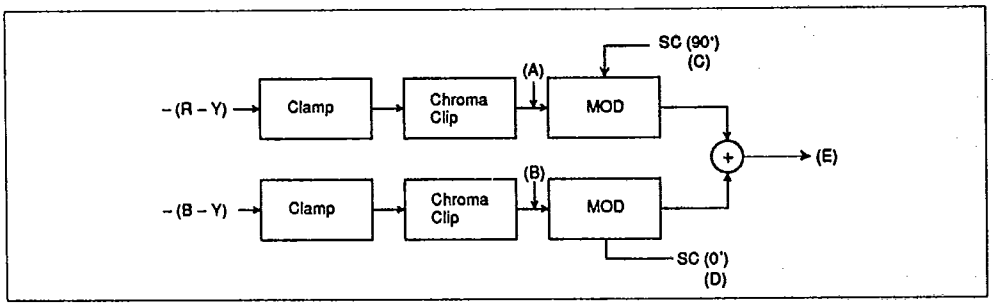


Figure 1. Chroma Modulator Circuit

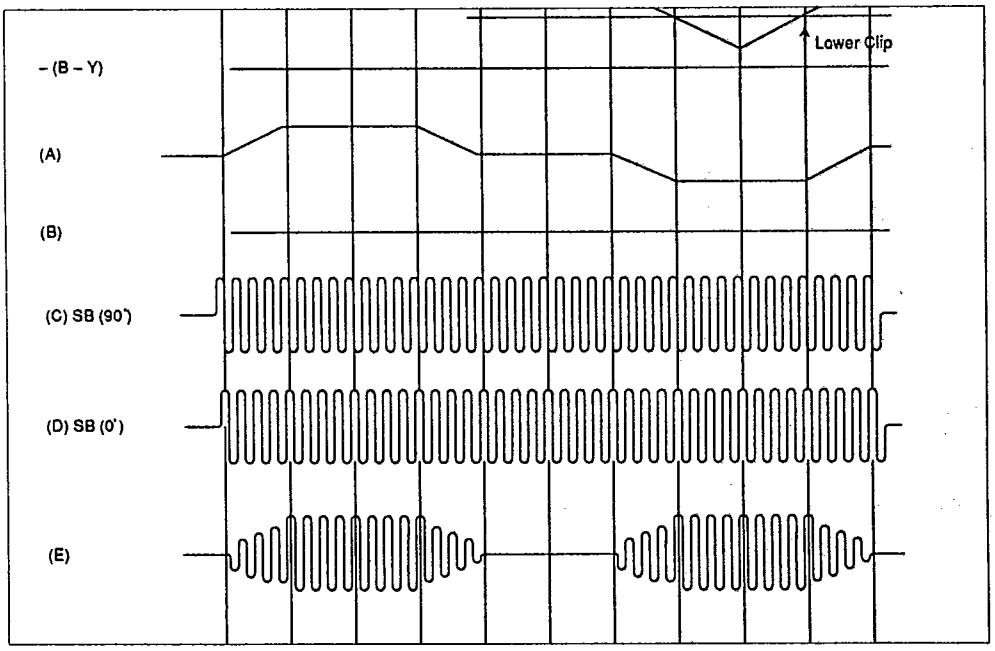


Figure 2. Chroma Modulation Block Waveforms

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Burst Signal Shaping

Burst signal shaping is performed as illustrated in figure 4. This example uses —(B – Y).

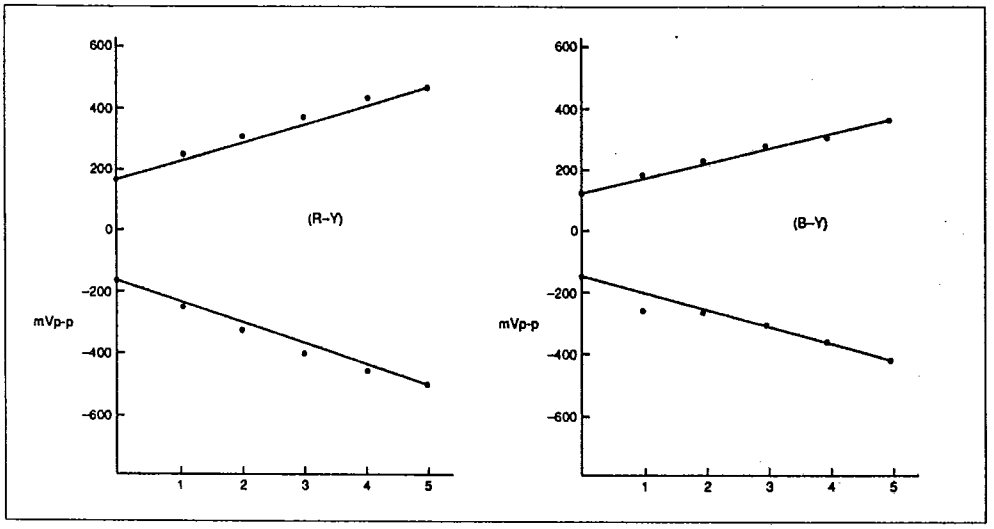

Figure 3. Clip Level Adjustment (V_{CC} = 5V)

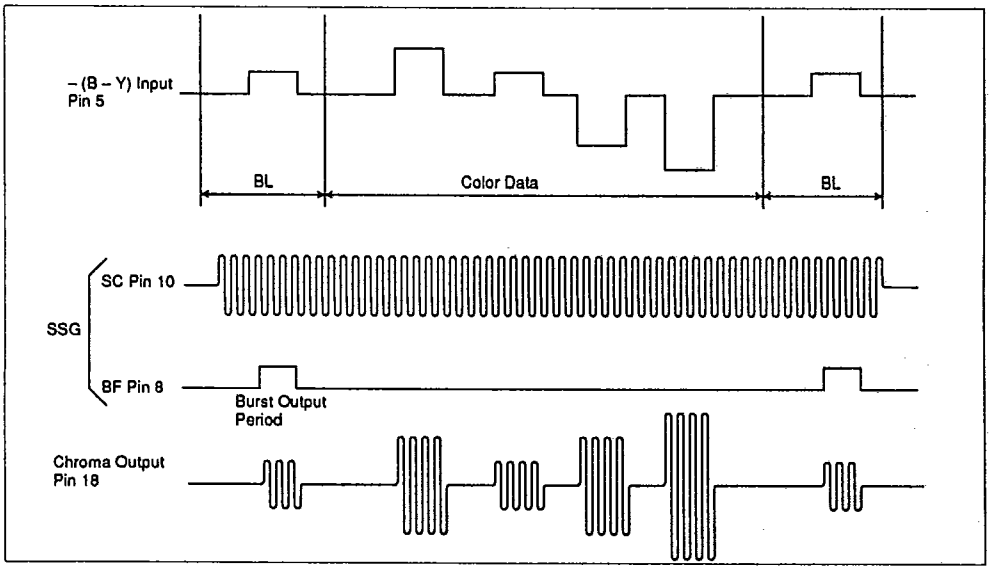

Figure 4. Burst Signal Shaping

In order to obtain a burst signal, a pulse which corresponds to the burst amplitude at the burst flag position, should be stacked on the burst flag at the color-difference signal input terminal. This stacked pulse should rise more quickly than the pre-green of the BF, and should fall simultaneously with or later than the post-green of the BF. Such a pulse can be obtained using the Hitachi HD440072 (SSG). Figure 5 shows an example of such a pulse, in which it should be noted that the burst signal is output when BF is high.

Luminance White Clip

Luminance white clip is controlled by altering the H level of the BL signal at pin 6. When the H level is 4.5V or higher, the clip level is determined internally by the IC.

Luminance Amplifier

Figure 6 illustrates the luminance signal processing waveform.

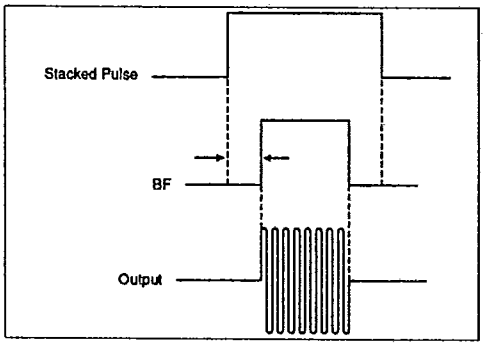

Figure 5. Stacked Pulse

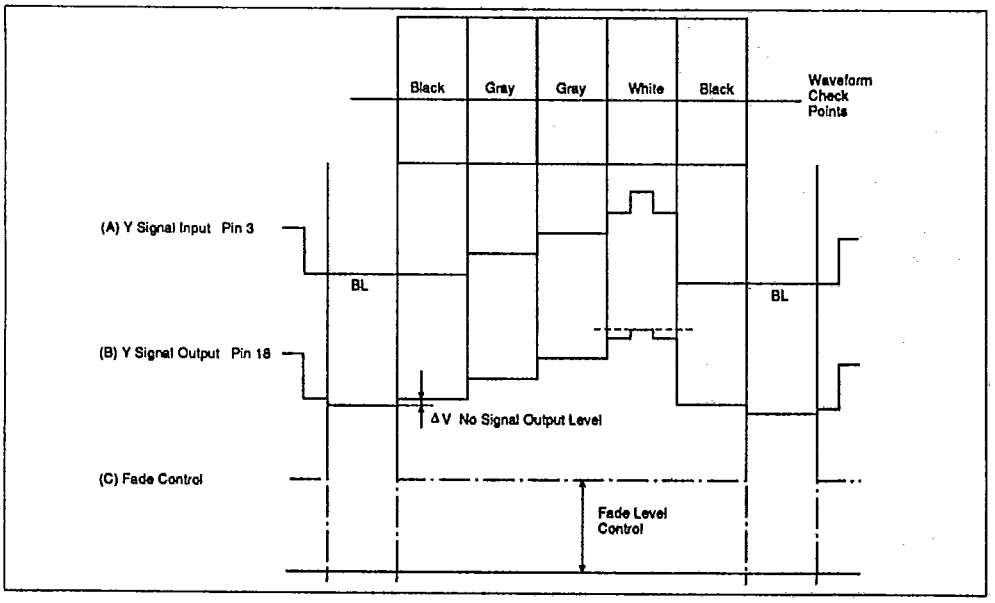

Figure 6. Luminance Signal Processing Waveform

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In (B) in figure 6, ΔV at the no signal output level is 17mV typ for BL ON/OFF DC difference voltage. Y signal input is 1.4Vpp for a 1 Vpp typ output. ΔV is 1.2% typ in this case.

(C) in figure 6 illustrates the Y signal waveform following fade ON. Fade level control can be used to set screen brightness at fade ON to a desired level as shown in figure 7.

Chroma Gain Control

Figure 8 shows the chroma gain control characteristic. Opening pin 15 causes chroma gain to grow ~6dB for the maximum gain.

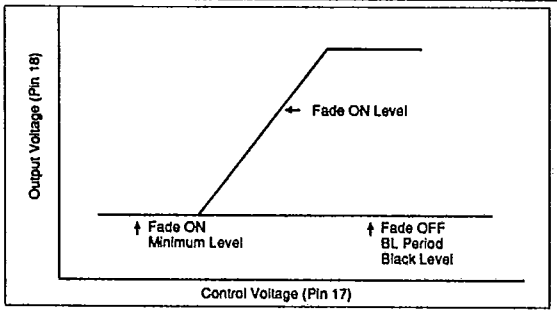

Figure 7. Fade Level Control

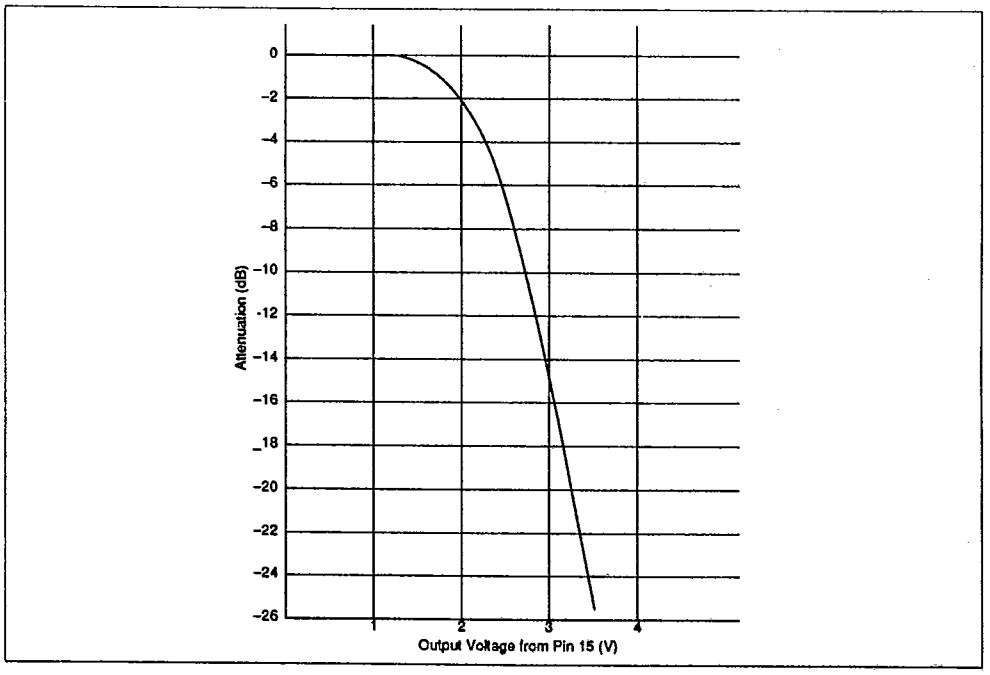

Figure 8. Chroma Gain Control Characteristic (V_{CC} = 4V)

Y/C Mixer Circuit

Figure 9 shows the internal equivalent circuit for the Y/C mixer circuit. When specifications of DG10% (worst), DP 8° (worst) are required, set the composit output terminal voltage at pin 18 to its optimal value. The DC voltage at pin 16 should be altered by changing the external resistance at RA, RB, and RC, and the V18 DC voltage output at pin 18 should be set at $2.16V \leq V18 \leq 2.24V$.

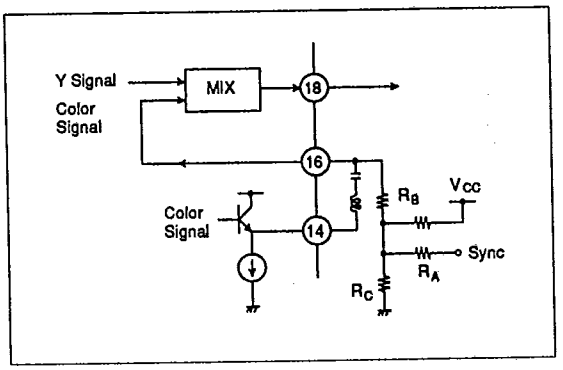

Figure 9. Y/C Adder Circuit