

Am29833-34/Am29853-54

Am29833-34/Am29853-54

Parity Bus Transceivers

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

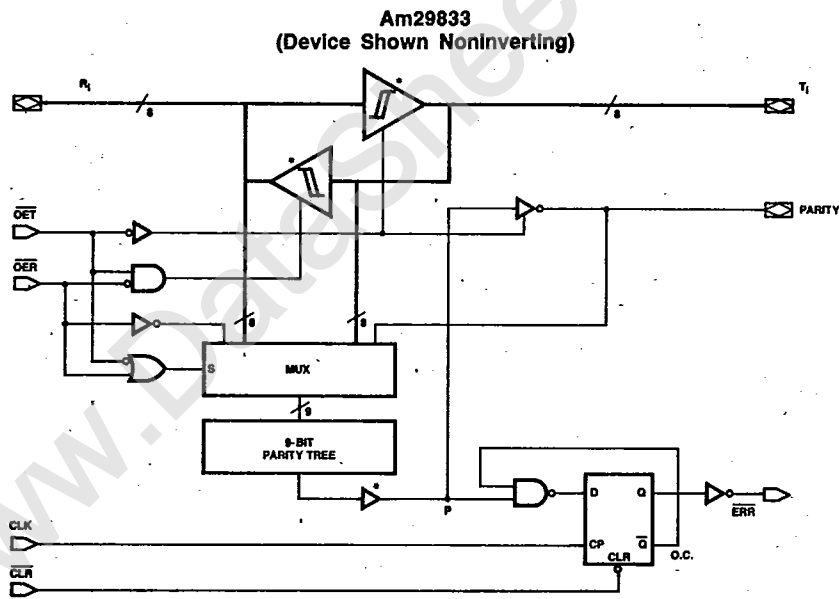
- High-speed bidirectional bus transceiver for processor organized devices
- Error flag with open-collector output
- Generates odd parity for all-zero protection
- Buffered direction three-state control
- Output short-circuit protected to VCC limits
- 200mV minimum input hysteresis on input data ports
- High-capacitance drive capability
48mA commercial IOL
32mA military IOL

GENERAL DESCRIPTION

The Am29833/34/53/54 are high-performance bus transceivers designed for two-way communications. They each contain an 8-bit data path from the R (port) to the T (port), a 9-bit data path from the T (port) to the R (port), and a 9-bit parity checker/generator. Two options are available. The Am29833/34 register option, and the Am29853/54 latch option. With the register option, the error flag can be clocked and stored in a register and read at the open-collector ERR output. The clear (CLR) input is used to clear the error flag register. With the latch option, the error can be either passed, stored, sampled or cleared at the error flag output by using the EN and CLR controls.

The output enables \overline{OET} and \overline{OER} are used to force the port outputs to the high-impedance state so that the device can drive bus lines directly. In addition, the \overline{OER} and \overline{OET} can be used to force a parity error by enabling both lines simultaneously. This transmission of inverted parity gives the designer more system diagnostic capability. The Am29833 and Am29853 are noninverting, while the Am29834 and Am29854 present inverting data at the outputs. The devices are specified at 48mA output sink current over the commercial range and 32mA over the military range.

BLOCK DIAGRAM



*Noninverting buffer for Am29833; inverting buffer for Am29834.

*Note that the inverting device converts the positive logic "R" bus levels to negative logic levels on the "T" bus.

00370B

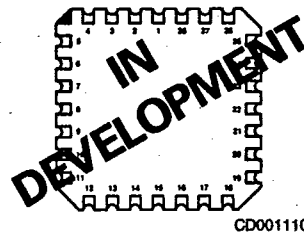
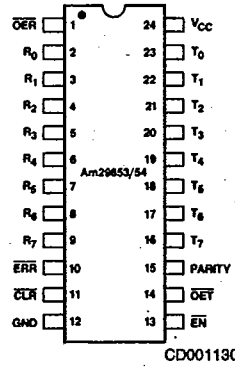
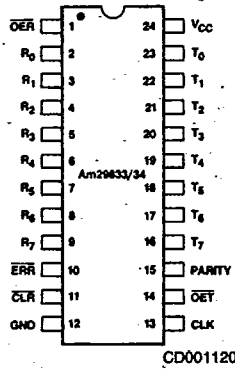
Am29833-34/Am29853-54

CONNECTION DIAGRAM
Top View

8-BIT TO 9-BIT PARITY TRANSCEIVERS

Leadless Chip Carrier

L-28-1



ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am29833-34
Am29853-54

D — Package
D-24-pin SLIM DIP (D-24-SLIM)
L-28-pin Leadless Chip Carrier (L-28-1)
X-Dice

C — Temperature (See Operating Range)
C - Commercial (0°C to +70°C)
M - Military (-55°C to +125°C)

B — Screening Option
Blank - Standard processing
B - Burn-in

Valid Combinations	
Am29833	DC, DCB, DM,
Am29834	DMB
Am29853	LC, LCB, LM,
Am29854	LMB
	XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

Device type
Parity Bus Transceivers

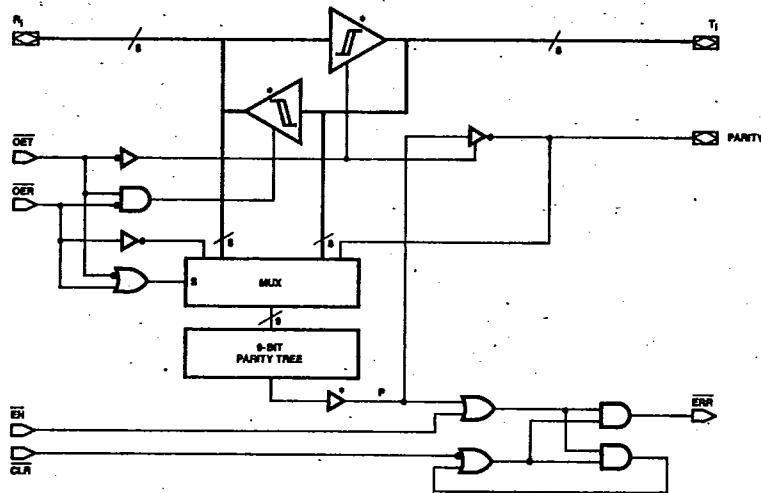
8

Am29833-34/Am29853-54

PIN DESCRIPTION

Pin No.	Name	I/O	Description
Am29833 - 34			
1	OER	I	RECEIVE enable input.
	R _i	O	8-bit RECEIVE data output.
10	ERR	O	Output from fault registers. Registers detection of odd parity fault on using clock edge (CLK). A registered ERR output remains LOW until cleared.
11	CLR	O	Clears the fault register output.
	T _i	O	8-bit TRANSMIT data output.
15	PARITY	O	1-bit PARITY output.
14	OET	I	TRANSMIT enable input.
13	CLK	I	External clock pulse input for fault register flag.
Am29853/54			
1	OER	I	RECEIVE enable input.
	R _i	O	8-bit RECEIVE data output.
10	ERR	O	Output from fault latches. Latches detection of odd parity fault on active enable EN. A latched ERR output remains LOW until cleared.
11	CLR	O	Clears the fault latch output.
	T _i	O	8-bit TRANSMIT data output.
15	PARITY	O	1-bit PARITY output.
14	OET	I	TRANSMIT enable input.
13	EN	I	Enable latch input for fault flag.

BLOCK DIAGRAM
Am29853
(Device Shown Noninverting)



BD001030

*Noninverting buffer for Am29853; inverting buffer for Am29854.

*Note that the inverting device converts the positive logic "R" bus levels to negative logic levels on the "T" bus.

Am29833-34/Am29853-54

FUNCTION TABLES

Am29833 NONINVERTING OPTION

Inputs						Outputs				Function
OET	OER	CLR	CLK	R _i (Σ of H's)	T _i Incl Parity (Σ of H's)	R _i	T _i	Parity	ERR ¹	
L	H	-	-	H (Odd)	NA	NA	H	L	NA	Transmit data from R Port to T Port with parity, receiving path is disabled
L	H	-	-	H (Even)	NA	NA	H	L	NA	
L	H	-	-	L (Odd)	NA	NA	L	L	NA	
L	H	-	-	L (Even)	NA	NA	L	H	NA	
H	L	H	↑	NA	H (Odd)	H	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag, transmitting path is disabled
H	L	H	↑	NA	H (Even)	H	NA	NA	L	
H	L	H	↑	NA	L (Odd)	L	NA	NA	H	
H	L	H	↑	NA	L (Even)	L	NA	NA	L	
-	-	L	-	-	-	-	NA	NA	H	Clear the state of error flag register
H	H	H	-	-	-	Z	Z	Z	NC	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode
H	H	H	↑	L (Odd)	-	Z	Z	Z	H	
H	H	H	↑	L (Even)	-	Z	Z	Z	L	
L	L	-	-	H (Odd)	NA	NA	H	H	NA	Forced-error checking
L	L	-	-	H (Even)	NA	NA	L	L	NA	
L	L	-	-	L (Odd)	NA	NA	H	H	NA	
L	L	-	-	L (Even)	NA	NA	L	L	NA	

Am29834 INVERTING OPTION*

Inputs						Outputs				Function
OET	OER	CLR	CLK	R _i (Σ of L's)	T _i Incl Parity (Σ of H's)	R _i	T _i	Parity	ERR ¹	
L	H	-	-	H (Odd)	NA	NA	L	H	NA	Transmit data from R Port to T Port with parity, receiving path is disabled
L	H	-	-	H (Even)	NA	NA	L	L	NA	
L	H	-	-	L (Odd)	NA	NA	H	H	NA	
L	H	-	-	L (Even)	NA	NA	H	L	NA	
H	L	H	↑	NA	H (Odd)	L	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag, transmitting path is disabled
H	L	H	↑	NA	H (Even)	L	NA	NA	L	
H	L	H	↑	NA	L (Odd)	H	NA	NA	H	
H	L	H	↑	NA	L (Even)	H	NA	NA	L	
-	-	L	-	-	-	-	-	-	H	Clear the state of error flag register
H	H	H	-	-	-	Z	Z	Z	NC	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode
H	H	H	↑	L (Odd)	-	Z	Z	Z	L	
H	H	H	↑	L (Even)	-	Z	Z	Z	H	
L	L	-	-	H (Odd)	NA	NA	L	L	NA	Forced-error checking
L	L	-	-	H (Even)	NA	NA	L	H	NA	
L	L	-	-	L (Odd)	NA	NA	H	L	NA	
L	L	-	-	L (Even)	NA	NA	H	H	NA	

H = High
 L = Low
 ↑ = Low to high transition of clock
 NC = No change
 Z = High Impedance
 NA = Not applicable
 - = Don't care or irrelevant
 Odd = Odd number of logic one's
 Even = Even number of logic one's
 1 = 0, 1, 2, 3, 4, 5, 6, 7

*Note that for the negative logic levels on the B Port, an "H" represents a logic "0" while an "L" represents a logic "1".
 1. Output state assumes HIGH output pre-state.

ERROR FLAG OUTPUT TRUTH TABLE

Am29833 - Am29834 (REGISTER OPTION)

Inputs		Internal to Device	Outputs Pre-state	Output	Function
CLR	CLK	Point "P"	ERR _{n-1}	ERR	
H	↑	H	H	H	Sample* (1's Capture)
H	↑	-	L	L	
H	↑	L	-	L	
L	-	-	-	H	Clear

Am29853/Am29854 (LATCH OPTION)

Inputs		Internal to Device	Outputs Pre-state	Output	Function
EN	CLR	Point "P"	ERR _{n-1}	ERR	
L	L	L	-	L	Pass
L	L	H	-	H	
L	H	L	-	L	Sample* (1's Capture)
L	H	H	H	H	
H	L	-	-	H	Clear
H	H	-	L	L	Store*
H	H	-	H	H	

*Enable is used as strobe for the latch in sampled operation.

8

Am29833-34/Am29853-54

Am29853 NONINVERTING OPTION										
Inputs						Outputs				Function
OET	OER	CLR	CLK	R _i (Σ of H's)	T _i Incl Parity (Σ of H's)	R _j	T _j	Parity	ERR ¹	
L	H	-	-	H (Odd)	NA	NA	H	L	NA	Transmit data from R Port to T Port with parity, receiving path is disabled
L	H	-	-	H (Even)	NA	NA	H	L	NA	
L	H	-	-	L (Odd)	NA	NA	L	L	NA	
L	H	-	-	L (Even)	NA	NA	L	H	NA	
H	L	L	L	NA	H (Odd)	H	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag, transmitting path is disabled
H	L	L	L	NA	H (Even)	L	NA	NA	L	
H	L	L	L	NA	L (Odd)	L	NA	NA	L	
H	L	L	L	NA	L (Even)	L	NA	NA	L	
H	L	H	L	NA	H (Odd)	H	NA	NA	H	Receive data from T Port to R Port, pass the error test resulting to error flag, transmitting path is disabled
H	L	H	L	NA	H (Even)	L	NA	NA	L	
H	L	H	L	NA	L (Odd)	L	NA	NA	L	
H	L	H	L	NA	L (Even)	L	NA	NA	L	
H	L	H	H	NA	-	-	NA	NA	ERR _{n-1}	Store the state of error flag register
-	-	L	H	-	-	-	NA	NA	H	Clear the state of error flag register
H	H	H	H	-	-	Z	Z	Z	NC	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode
H	H	L	H	-	-	Z	Z	Z	H	
H	H	L	L	L (Odd)	-	Z	Z	Z	H	
H	H	L	L	H (Even)	-	Z	Z	Z	L	
L	L	-	-	H (Odd)	NA	NA	H	H	NA	Forced-error checking
L	L	-	-	H (Even)	NA	NA	H	L	NA	
L	L	-	-	L (Odd)	NA	NA	L	H	NA	
L	L	-	-	L (Even)	NA	NA	L	L	NA	

Am29854 INVERTING OPTION*										
Inputs						Outputs				Function
OET	OER	CLR	CLK	R _i (Σ of H's)	T _i Incl Parity (Σ of H's)	R _j	T _j	Parity	ERR ¹	
L	H	-	-	H (Odd)	NA	NA	L	H	NA	Transmit data from R Port to T Port with parity, receiving path is disabled
L	H	-	-	H (Even)	NA	NA	L	L	NA	
L	H	-	-	L (Odd)	NA	NA	H	H	NA	
L	H	-	-	L (Even)	NA	NA	H	L	NA	
H	L	L	L	NA	H (Odd)	L	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag, transmitting path is disabled
H	L	L	L	NA	H (Even)	L	NA	NA	L	
H	L	L	L	NA	L (Odd)	H	NA	NA	H	
H	L	L	L	NA	L (Even)	H	NA	NA	L	
H	L	H	L	NA	H (Odd)	L	NA	NA	H	Receive data from T Port to R Port, pass the error test resulting to error flag, transmitting path is disabled
H	L	H	L	NA	H (Even)	L	NA	NA	L	
H	L	H	L	NA	L (Odd)	H	NA	NA	H	
H	L	H	L	NA	L (Even)	H	NA	NA	L	
H	L	H	H	NA	-	-	NA	NA	ERR _{n-1}	Store the state of error flag register
-	-	L	H	-	-	-	NA	NA	H	Clear the state of error flag register
H	H	H	H	-	-	Z	Z	Z	NC	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode
H	H	L	H	-	-	Z	Z	Z	H	
H	H	L	L	L (Odd)	-	Z	Z	Z	L	
H	H	L	L	L (Even)	-	Z	Z	Z	H	
L	L	-	-	H (Odd)	NA	NA	L	L	NA	Forced-error checking
L	L	-	-	H (Even)	NA	NA	L	H	NA	
L	L	-	-	L (Odd)	NA	NA	H	L	NA	
L	L	-	-	L (Even)	NA	NA	H	H	NA	

H = High
 L = Low
 Z = High impedance
 NC = No change
 NA = Not applicable
 ERR_{n-1} = Pre-state of ERR
 - = Don't care or irrelevant
 Odd = Odd number of logic one's
 Even = Even number of logic one's
 i = 0, 1, 2, 3, 4, 5, 6, 7

*Note that for the negative logic levels on the B Port, an "H" represents a logic "0" while an "L" represents a logic "1".

1. Output state assumes HIGH output pre-state.

Am29833-34/Am29853-54

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -65°C to +150°C
 Ambient Temperature with
 Power Applied -55°C to +125°C
 Supply Voltage to Ground Potential
 Continuous -0.5V to +7.0V
 DC Voltage Applied to Output
 for High Output State -1.5V to V_{CC}max
 DC Input Voltage -0.5V to +5.5V
 DC Output Current, into Outputs 100mA
 DC Input Current -30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
 Temperature 0°C to +70°C
 Supply Voltage +4.75V to +5.25V
 Military (M) Devices
 Temperature -55°C to +125°C
 Supply Voltage +4.5V to +5.5V
Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

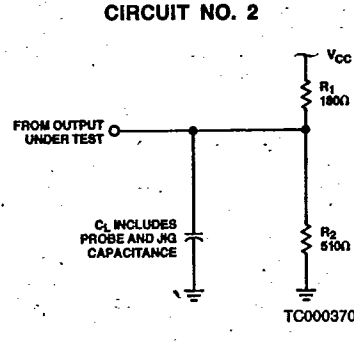
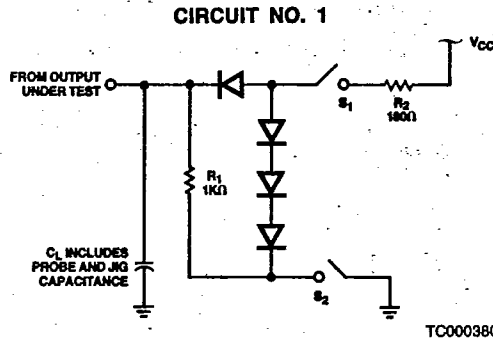
Parameters	Description	Test Conditions	Min	Typ (Note 1)	Max	Units
V _{OH}	Output HIGH Voltage (Except ERR)	V _{CC} = MIN V _{IN} = V _{IH} or V _{IL}	I _{OH} = -15mA	2.4		V
			I _{OH} = -24mA	2.0		
V _{OL}	Output LOW Voltage	V _{CC} = MIN	ERR I _{OL} = 48mA		0.5	V
			All Other Outputs V _{IN} = V _{IH} or V _{IL} I _{OL} = 48mA COM'L		0.5	
V _{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0		V
V _{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs			0.8	V
V _I	Input Clamp Voltage	V _{CC} = MIN, I _{IN} = -18mA			-1.2	V
V _{HYST}	Hysteresis for Inputs R _i , T _i	Output Connected to AC Test Load Circuit		200		mV
I _{IL}	Input LOW Current	V _{CC} = MAX V _{IN} = 0.4V	Data		-1.0	mA
			Control		-2.0	
I _{IH}	Input HIGH Current	V _{CC} = MAX, V _{IN} = 2.7V			50	μA
I _I	Input HIGH Current	V _{CC} = MAX, V _{IN} = 5.5V			1.0	mA
I _{OZH}	Off-State Output Current (High Impedance)	V _{CC} = MAX	V _O = 2.4V		+100	μA
			V _O = 0.4V		-1.0	
I _{SC}	Output Short Circuit Current	V _{CC} = MAX		75	250	mA
I _{CC}	Power Supply Current	V _{CC} = MAX (All Outputs Are Open)	Over Temperature Range		185	mA
			+70°C		180	
			+125°C		170	

Note: 1 Typical units are TA = 25°C, V_{CC} = 5V.

8

Am29833-34/Am29853-54

SWITCHING TEST CIRCUIT



Note: Test Circuit No. 1 is used with Propagation delay

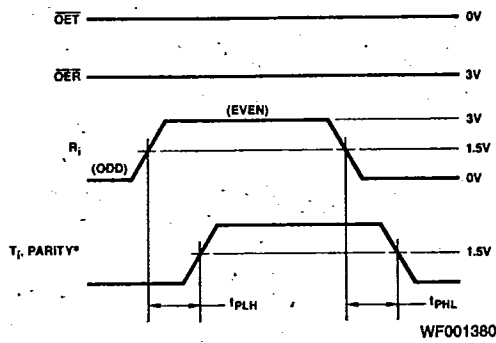
SWITCHING CHARACTERISTICS ($T_A = +25^\circ C, V_{CC} = 5.0V$)

Parameters	Description	Test Conditions	Min	Type	Max	Units
t_{PLH}	Propagation Delay R_i to T_i, T_i to R_i	$C_L = 50pF$			12	ns
t_{PHL}					12	ns
t_{PLH}	Propagation Delay R_i to T_i, T_i to R_i	$C_L = 300pF$			16	ns
t_{PHL}					16	ns
t_{PLH}	Propagation Delay R_i to PARITY	$C_L = 50pF$			15	ns
t_{PHL}					15	ns
t_{PLH}	Propagation Delay R_i to PARITY	$C_L = 300pF$			22	ns
t_{PHL}					22	ns
t_{ZH}	Output Enable Time $\overline{OER}, \overline{OET}$ to R_i, T_i	$C_L = 50pF$			15	ns
t_{ZL}					15	ns
t_{ZH}	Output Enable Time $\overline{OER}, \overline{OET}$ to R_i, T_i	$C_L = 300pF$			20	ns
t_{ZL}					23	ns
t_{HZ}	Output Disable Time $\overline{OER}, \overline{OET}$ to R_i, T_i	$C_L = 5pF$			9	ns
t_{HL}					10	ns
t_{HZ}	Output Disable Time $\overline{OER}, \overline{OET}$ to R_i, T_i	$C_L = 50pF$			17	ns
t_{HL}					12	ns
t_s	T_i, PARITY to CLK Setup Time*	$C_L = 50pF$	15			ns
t_h	T_i, PARITY to CLK Hold Time*		0			ns
t_r	Clear Recovery Time CLR to CLK**		15			ns
t_{PWH}	Clock Pulse Width*		HIGH	10		ns
t_{PWL}	Clear Pulse Width		LOW	10		ns
t_{PHL}	Propagation Delay CLK to ERR*	$C_L = 50pF$			15	ns
t_{PLH}	Propagation Delay CLR to ERR	$C_L = 50pF$			15	ns
t_{PLH}	Propagation-Delay $t_i, \text{PARITY ERR}$ (PASS Mode Only) Am29853/54	$C_L = 50pF$			22	ns
t_{PHL}	Propagation Delay \overline{OER} to Parity	$C_L = 50pF$ Test Ckt #1			15	ns
t_{PLH}					15	ns
t_{PHL}					22	ns
t_{PLH}	Propagation Delay \overline{OER} to Parity	$C_L = 300pF$ Test Ckt #1			15	ns
t_{PHL}					22	ns

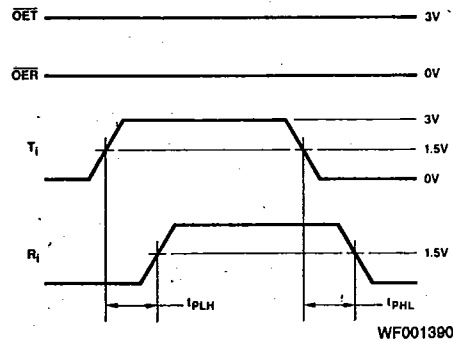
*For Am29853/54 replace CLK with EN.
 **Note: Not applicable to Am29853/54.

Am29833-34/Am29853-54

Am29833/53 SWITCHING WAVEFORMS (NONINVERTING OPTION)

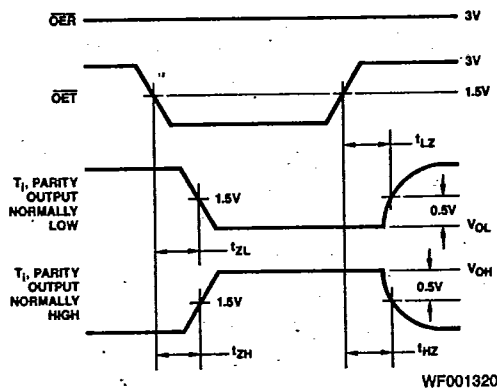


a. R_j to T_j, PARITY

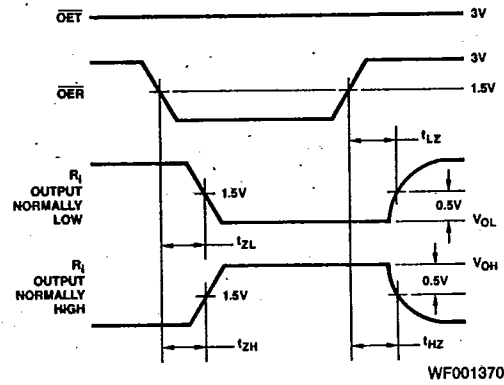


b. T_j to R_j

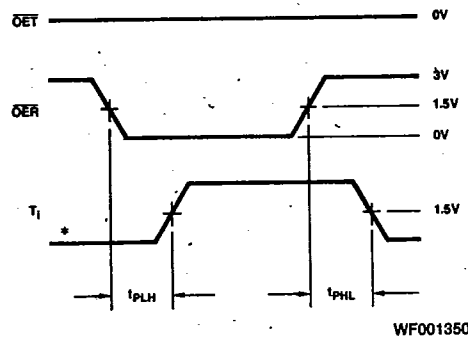
*Calculation must be done from last arriving signal.



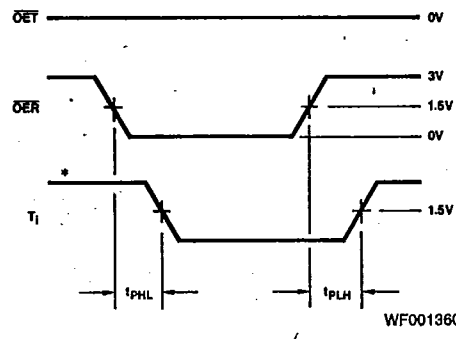
c. \overline{OET} to T_j, PARITY



d. \overline{OER} to R_j



WF001350



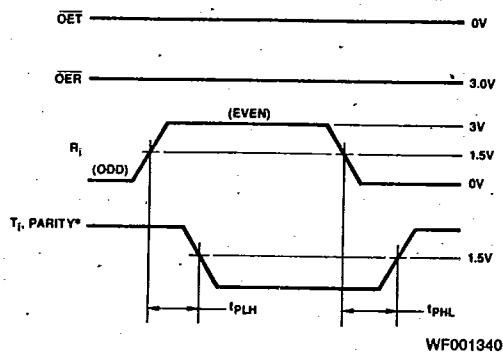
WF001360

e. \overline{OER} to PARITY

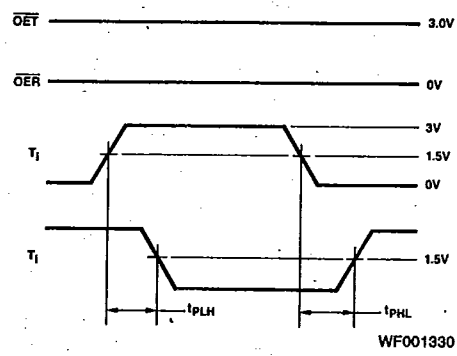
8

Am29833-34/Am29853-54

Am29834/54 SWITCHING WAVEFORMS (INVERTING OPTION)

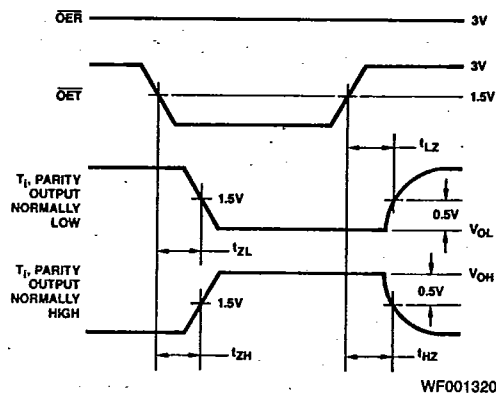


a. R_i to T_i , PARITY

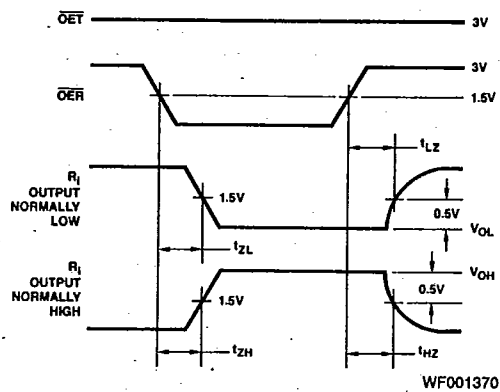


b. T_i to R_i

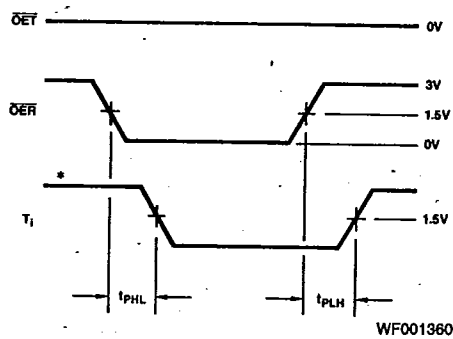
*Calculation must be done from last arriving signal.



c. OET to T_i , PARITY



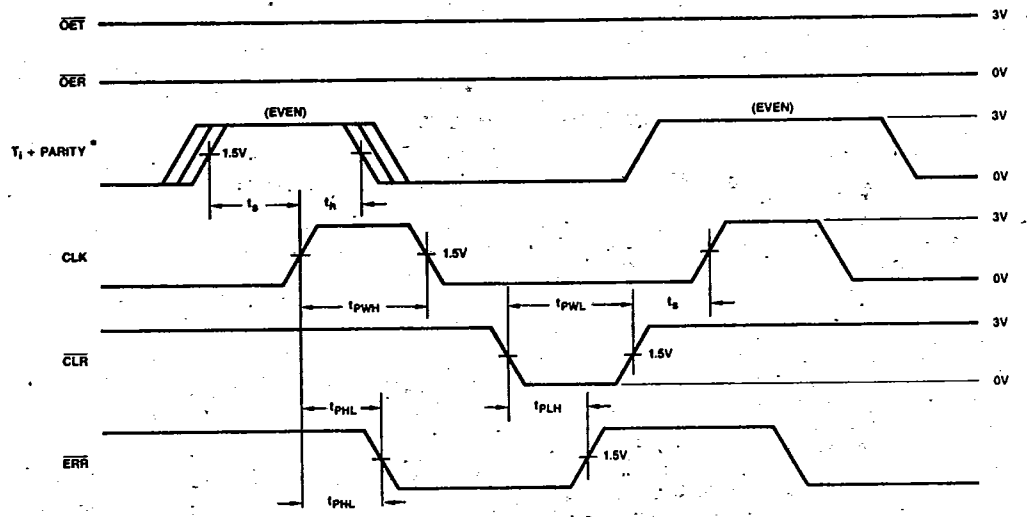
d. OER to R_i



e. OER to PARITY

00370B

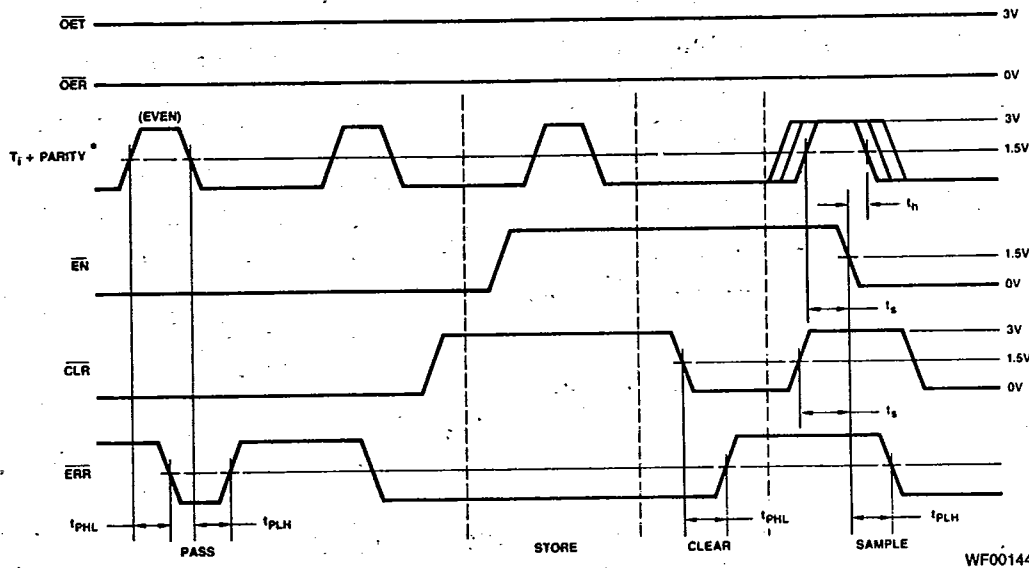
SWITCHING WAVEFORMS (REGISTER OPTION, Am29833/34)



WF001430

a. CLK, $\overline{\text{CLR}}$ to $\overline{\text{ERR}}$

SWITCHING WAVEFORMS (LATCH OPTION, Am29853/54)



WF001440

b. T_i , PARITY, $\overline{\text{EN}}$, $\overline{\text{CLR}}$ to $\overline{\text{ERR}}$

*Calculation must be done from last arriving signal.