Techwell, Inc.

TW9920 – Analog Video Decoder / Encoder

Preliminary Data Sheet

Techwell Confidential. Information may change without notice.

Disclaimer

This document provides technical information for the user. Techwell, Inc. reserves the right to modify the information in this document as necessary. The customer should make sure that they have the most recent data sheet version. Techwell, Inc. holds no responsibility for any errors that may appear in this document. Customers should take appropriate action to ensure their use of the products does not infringe upon any patents. Techwell, Inc. respects valid patent rights of third parties and does not infringe upon or assist others to infringe upon such rights.

Techwell, Inc. **1**
Features **4**
Functional Description **5**
General description 6
Analog Front-end 6
Video Source Selection 6
Clamping and Automatic Gain Control 7
Analog to Digital Converter 7
Sync Processing 7
Horizontal sync processing 7
Vertical sync processing 7
Color Decoding 8
Y/C separation 8
Color demodulation 8
Automatic Chroma Gain Control 9
Low Color Detection and Removal 9
Automatic standard detection 9
Video Format support 10
Component Processing 10
Luminance Processing 10
Gamma 10
Sharpness 10
The Hue and Saturation 11
Color Transient Improvement 11
Power Management 11
Control Interface 11
Down-scaling and Cropping 11
TW9920 Down-Scaling 11
TW9920 Cropping 12
VDELAY + VACTIVE < Total number of lines per field 13
Output Interface 14
ITU-R BT.656 14
VIP (Video Interface Port) 14
Horizontal Down Scaling Output 15
Vertical Down Scaling Output 16
Raw VBI data output 16
VBI Data Processing 17
Raw VBI data output 17
VBI Data Slicer 17
Sliced VBI Data output format 18
Audio clock generation 24
Analog Video Encoder 26
Timing Interface and Control 29
Two Wire Serial Bus Interface 30
Test Modes 32
Filter Curves 33
Decimation filter 33
Anti-alias filter 33
Chroma Band Pass Filter Curves 34
Luma Notch Filter Curve for NTSC and PAL/SECAM 35
Chrominance Low-Pass Filter Curve 35
Horizontal Scaler Pre- Filter curves 36
Vertical Interpolation Filter curves 36
Peaking Filter Curves 37
Control Register **38**
TW9920 Register SUMMARY 38
0x00 – Product ID Code Register (ID) 41
0x01 – Chip Status Register I (STATUS1) 41
0x02 – Input Format (INFORM) 42
0x03 – Output Format Control Register (OPFORM) 43
0x04 – GAMMA and HSYNC Delay Control 43
0x05 – Output Control I 44
0x06 – Analog Control Register (ACNTL) 45
0x07 – Cropping Register, High (CROP_HI) 45
0x08 – Vertical Delay Register, Low (VDELAY_LO) 46
0x09 – Vertical Active Register, Low (VACTIVE_LO) 46
0x0A – Horizontal Delay Register, Low (HDELAY_LO) 46
0x0B – Horizontal Active Register, Low (HACTIVE_LO) 46
0x0C – Control Register I (CNTRL1) 47
0x0D – Vertical Scaling Register, Low (VSCALE_LO) 47
0x0E – Scaling Register, High (SCALE_HI) 47
0x0F – Horizontal Scaling Register, Low (HSCALE_LO) 48
0x10 – BRIGHTNESS Control Register (BRIGHT) 48
0x11 – CONTRAST Control Register (CONTRAST) 48
0x12 – SHARPNESS Control Register I (SHARPNESS) 48
0x13 – Chroma (U) Gain Register (SAT_U) 49
0x14 – Chroma (V) Gain Register (SAT_V) 49
0x15 – Hue Control Register (HUE) 49
0x16 – Sharpness Control II (SHARP2) 49
0x17 – Vertical Sharpness (VSHARP) 50
0x18 – Coring Control Register (CORING) 50
0x19 – VBI Control Register (VBICNTL) 51
0x1A – Analog Control II 52
0x1B – Output Control II 52
0x1C – Standard Selection (SDT) 53
0x1D – Standard Recognition (SDTR) 54
0x1E – Component Video Format (CVFMT) 54
0x1F – Test Control Register (TEST) 55
0x20 – Clamping Gain (CLMPG) 56
0x21 – Individual AGC Gain (IAGC) 56
0x22 – AGC Gain (AGCGAIN) 56
0x23 – White Peak Threshold (PEAKWT) 56
0x24– Clamp level (CLMPL) 56
0x25– Sync Amplitude (SYNCT) 57
0x26 – Sync Miss Count Register (MISSCNT) 57
0x27 – Clamp Position Register (PCLAMP) 57
0x28 – Vertical Control I (VCNTL1) 58
0x29 – Vertical Control II (VCNTL2) 58
0x2A – Color Killer Level Control (CKILL) 58
0x2B – Comb Filter Control (COMB) 59
0x2C – Luma Delay and H Filter Control (LDLY) 59
0x2D – Miscellaneous Control I (MISC1) 60
0x2E – LOOP Control Register (LOOP) 60
0x2F – Miscellaneous Control II (MISC2) 61
0x30 – Macrovision Detection (MVSN) 62
0x31 – Chip STATUS II (STATUS2) 62
0x32 – H monitor (HFREF) 63
0x33 – CLAMP MODE (CLMD) 63
0x34 – ID Detection Control (IDCNTL) 63
0x35 – Clamp Control I (CLCNTL1) 64
0x40 – 0x48 AUDIO CLOCK 65
0x40 – Audio Clock Increment (ACKI) 65
0x41 – Audio Clock Increment (ACKI) 65
0x42 – Audio Clock Increment (ACKI) 65
0x43 – Audio Clock Number (ACKN) 65
0x44 – Audio Clock Number (ACKN) 65
0x45 – Audio Clock Number (ACKN) 65
0x46 – Serial Clock Divider (SDIV) 66
0x47 – Left/Right Clock Divider (LRDIV) 66
0x48 – Audio Clock Control (ACCNTL) 66
0x4E – HBLEN 67
0x4F – WSS3 67
0x50 – FILLDATA 67
0x51 – SDID 67
0x52 – DID 68
0x53 – WSS1 68
0x54 – WSS2 68
0x55 – VVBI 69
0x56~6A LCTL6~LCTL26 69
0x6B – HSGEGIN 70
0x6C – HSEND 70
0x6D – OVSDLY 70
0x6E – OVSEND 70
0x6F – VBIDELAY 71
0x70 – ENCODER CONTROL1 71
0x71 – ENCODER CONTROL2 72

0x72 – ENCODER CONTROL3 73
0x73 – ENCODER CONTROL4 73
0x74 – ENCODER CONTROL5 74
0x75 – ENCODER CONTROL6 74
0x76 – ENCODER & DAC Power Down 75
0x77 – DAC Control1 76
0x78 – DAC Control12 76
0x79 – DAC Control13 77
0x7a – Encoder YDEL 77
0x7b – Encoder SYNC_L & BLK_L 78
0x7c – Encoder YBRT 78
0x7d – Encoder CBURST 79
Pin Diagram 80
Pin Description 81
Encoder 82
Power and Ground Pins 83
Parametric Information 84
AC/DC Electrical Parameters 84
Clock Timing Diagram 86
Mechanical Data 87
Copyright Notice 88
Disclaimer 88
Life Support Policy 88

TW9920 – Analog Video Decoder / Encoder

Features

Video decoder

- NTSC (M, 4.43) and PAL (B, D, G, H, I, M, N, N combination), PAL (60), SECAM support with automatic format detection
- Software selectable analog inputs allows any of the following combinations, e.g. 4 CVBS or (3 CVBS and 1 Y/C).
- Two 9-bit ADCs and analog clamping circuit.
- Fully programmable static gain or automatic gain control for the Y channel
- Programmable white peak control for the Y or CVBS channel
- 4-H adaptive comb filter Y/C separation
- PAL delay line for color phase error correction
- Image enhancement with 2D peaking and CTI.
- Digital sub-carrier PLL for accurate color decoding
- Digital Horizontal PLL for synchronization processing and pixel sampling
- Advanced synchronization processing and sync detection for handling non-standard and weak signal
- Programmable hue, brightness, saturation, contrast, sharpness, Gamma control, and noise suppression
- Automatic color control and color killer
- Detection of level of copy protection according to Macrovision standard
- Programmable output cropping
- ITU-R 601 or ITU-R 656 compatible YCbCr(4:2:2) output format
- VBI slicer supporting industrial standard data services
- VBI data pass through, raw ADC data for Intercast™

Video scaler

- High quality horizontal filtered scaling with arbitrary scale down ratio
- Phase accuracy better than 1/32 pixel
- Selectable anti-alias filter
- Vertical down scaling by line dropping

Video Encoder

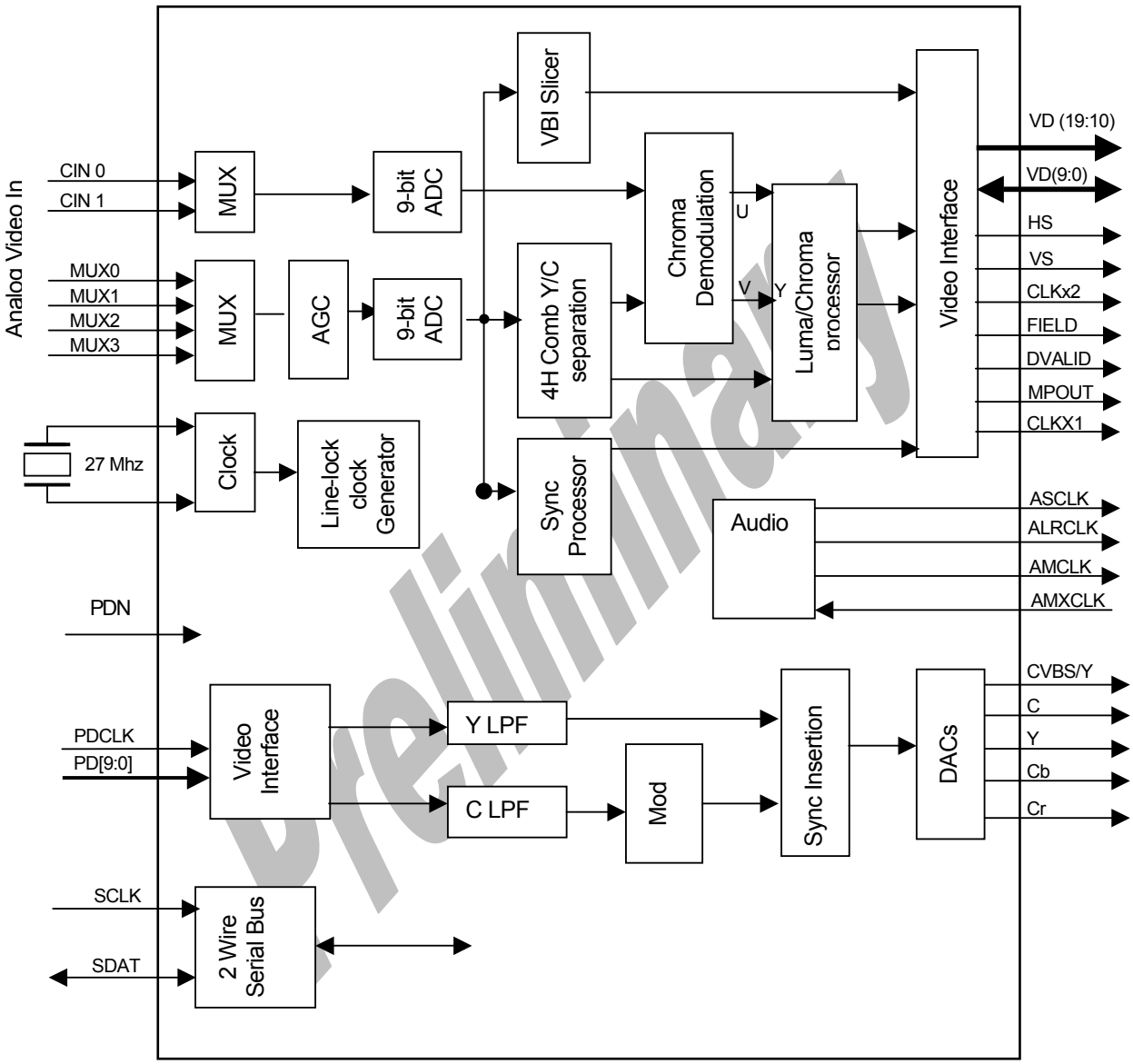
- Support NTSC/PAL and its sub-standard format output
- ITU-R 656 compatible video interface
- Luminance and chrominance filter
- Stable 27MHz crystal clock for subcarrier generation
- Five 10-bit Digital-to-Analog Converters at 27Mhz sample rate for generating CVBS or Y/C and YCbCr simultaneously

Miscellaneous

- Two wire MPU serial bus interface
- Power-down mode
- Field locked audio clock generation
- Typical power consumption 0.62W
- Single 27MHz crystal for all standards
- Supports 24.54MHz and 29.5MHz crystal for high resolution square pixel format decoding
- 3V tolerant I/O
- 2.5/3.3 V power supply
- VFBGA package

Functional Description

Figure 1: TW9920 Block Diagram



General description

The TW9920 is a multi-standard video decoder and encoder chip that is designed for multimedia applications. It uses the mixed-signal 2.5V CMOS technology to provide a low-power integrated solution.

The video encoder is used to encoder digital YCbCr input into analog CVBS or S-video output. With five built-in DACs, it can simultaneously support analog YCbCr output in addition to S-video output for various applications. It can support both NTSC (60Hz) and PAL (50Hz) output. A stable crystal generated 27MHz clock is used for all necessary sub-carrier generation. It accepts ITU-R 656 compatible digital input externally.

The video decoder decodes the analog CVBS or S-video signals into digital YCbCr for output. It consists of analog front-end with input source selection, variable gain amplifier and analog-to-digital converters, Y/C separation circuit, multi-standard color decoder (PAL BGHI, PAL M, PAL N, combination PAL N, NTSC M, NTSC 4.43 and SECAM) and synchronization circuitry. The Y/C separation is done with highly adaptive 4H comb filter for reduced cross color and cross luminance. The advanced synchronization processing circuitry can produce stable pictures for non-standard signal as well as weak signal. A video scaler is provided to arbitrarily scale down the output video. The output of the decoder is formatted to the ITU-R 656 compatible output. It includes various control circuits like brightness, contrast, saturation, and dynamic aperture correction for best video quality.

A 2-wire serial MPU interface is used to simplify system integration. All the functions can be controlled through this interface.

Analog Front-end

The analog front-end converts analog video signals to the required digital format. There are two analog channels with clamping circuits and ADCs. The Y channel has 4-input multiplexer, and a variable gain amplifier for automatic gain control (AGC). Its four inputs are identified as MUX0, MUX1, MUX2, and MUX3. The C channel has a 2-input multiplexer. Its two inputs are identified as Cin0 and Cin1. The C channel is internally clamped to the zero level of the bipolar input source when enabled.

Video Source Selection

All analog signals should be AC-coupled to these inputs.

The Y channel analog multiplexer selects one of the four inputs MUX[0-3]. MUX[0-3] can be connected to composite video inputs or the Y signal of an S-Video or component input. When decoding a S-Video input, the Y signal should connect to one of the MUX inputs and the C signal to Cin0 or Cin1.

Software selectable analog inputs allow several possible input combinations:

1. Up to four composite video inputs. 2. Three composites and one S-video input. 3. Two composite and two S-Video inputs.

The input video signals in any certain channel maybe momentarily connected together through the equivalent of a 200 ohm resistor during multiplexer switching. Therefore, the multiplexer cannot be used for switching on a real-time pixel-by-pixel basis.

Clamping and Automatic Gain Control

All two analog channels have built-in clamping circuit that restores the signal DC level. The Y channel restores the back porch of the digitized video to a level of 60 or a programmable level. The C channel restores the back porch of the digitized video to a level of 128. This operation is automatic through internal feedback loop.

The Automatic Gain Control (AGC) of the Y channel adjusts input gain so that the sync tip is at a desired level. A programmable white peak protection logic is included to prevent saturation in the case of abnormal proportion between sync and white peak level.

Analog to Digital Converter

TW9920 contains two 9-bit pipelined ADCs that consume less power than conventional flash ADC. The output of the Clamp and AGC connects to one ADC that digitizes the composite input or the Y signal of the S-Video input. The second ADC digitizes the C signal when decoding S-video signal.

Sync Processing

The sync processor of TW9920 detects horizontal synchronization and vertical synchronization signals in the composite video or in the Y signal of an S-video or component signal. The processor contains a digital phase-locked-loop and decision logic to achieve reliable sync detection in stable signal as well as in unstable signals such as those from VCR fast forward or backward.

Horizontal sync processing

The horizontal synchronization processing contains a sync separator, a phase-locked-loop (PLL), and the related decision logic.

The horizontal sync detector detects the presence of a horizontal sync tip by examining low-pass filtered input samples whose level is lower than a threshold. After sufficient low levels are detected, a horizontal sync is recognized. Additional logic is also used to avoid false detection on glitches.

The horizontal PLL locks onto the extracted horizontal sync in all conditions to provide jitter free image output. From there, the PLL also provides orthogonal sampling raster for the down stream processor. The PLL has free running frequency that matches the standard raster frequency. It also has wide lock-in range for tracking any non-standard video signal.

In case the horizontal sync is missing, a “free-wheel” mechanism keeps generating horizontal sync signal until horizontal sync is detected again. This option can also be turned off for some applications that determine video loss by detecting the existence of horizontal sync.

Vertical sync processing

The vertical sync separator detects the vertical synchronization pattern in the input video signals. In addition, the actual sync determination is controlled by a detection window to provide more reliable synchronization. It achieves the functionality of a PLL without the complexity of a PLL. An option is available to provide faster responses for certain applications. The field status is determined at vertical synchronization time. When the location of the detected vertical sync is inline with a horizontal sync, it indicates a frame start or the odd field

start. Otherwise, it indicates an even field. The field logic can also be controlled to toggle automatically while tracking the input.

Color Decoding

Y/C separation

The color-decoding block contains the luma/chroma separation for the composite video signal and multi-standard color demodulation. For NTSC and PAL standard signals, the luma/chroma separation can be done either by comb filter or notch/band-pass filter combination. For SECAM standard signals, only notch/band-pass filter is available. The default selection for NTSC/PAL is comb filter. The characteristics of the band-pass filter are shown in the filter curve section.

In the case of comb filter, the TW9920 separates luma (Y) and chroma © of a NTSC composite video signal using a proprietary 2H adaptive comb filter. The filter uses a two-line buffer. Adaptive logic combines the upper-comb and the lower-comb results based on the signal changes among the previous, current and next lines. This technique leads to good Y/C separation with small cross luma and cross color at both horizontal and vertical edges. Due to the 90-degree phase difference on adjacent lines of a PAL chroma signal, the 4H adaptive comb filter is used to give better performance.

Due to the line buffer used in the comb filter, there is always two lines processing delay in the output images no matter what standard or filter option is chosen.

If notch/band-pass filter is selected, the characteristics of the filters are shown in the filter curve section.

Color demodulation

The color demodulation for NTSC and PAL standard is done by first quadrature mixing the chroma signal to the base band. The mixing frequency is equal to the sub-carrier frequency for NTSC and PAL. After the mixing, a low-pass filter is used to remove carrier signal and yield chroma components. The low-pass filter characteristic can be selected for optimized transient color performance. For the PAL system, the PAL ID or the burst phase switching is identified to aid the PAL color demodulation.

For SECAM, the mixing frequency is 4.286Mhz. After the mixer and low-pass filter, it yields the FM modulated chroma. The SECAM demodulation process therefore consists of low-pass filter, FM demodulator and de-emphasis filter. The filter characteristics are shown in filter curve section. During the FM demodulation, the chroma carrier frequency is identified and used to control the SECAM color demodulation.

The sub-carrier signal for use in the color demodulator is generated by direct digital synthesis PLL that locks onto the input sub-carrier reference (color burst). This arrangement allows any sub-standard of NTSC and PAL to be demodulated easily with single crystal frequency.

During S-video operation, the Y signal bypasses the comb filter. The C signal connects directly to the color demodulator. During component input operation, all the chroma processing and color demodulator blocks are bypassed.

Automatic Chroma Gain Control

The Automatic Chroma Gain Control (ACC) compensates for reduced amplitudes caused by high-frequency loss in video signal. In the NTSC/PAL standard, the color reference signal is the burst on the back porch. This color-burst amplitude is calculated and compared to standard amplitude. The chroma (Cx) signals are then increased or decreased in amplitude accordingly. The range of ACC control is –6db to +26db.

This function is always enabled to provide consistent image quality under different signal conditions.

Low Color Detection and Removal

For low color amplitude signals, black and white video, or very noisy signals, the color will be "killed". The color killer uses the burst amplitude measurement to switch-off the color when the measured burst amplitude falls below a programmed threshold. The threshold has programmed hysteresis to prevent oscillation of the color killer function. The color killer function can be disabled by programming a low threshold value.

Automatic standard detection

The TW9920 has build-in automatic standard discrimination circuitry. The circuit uses burst-phase, burst-frequency and frame rate to identify NTSC, PAL or SECAM color signals. The standards that can be identified are NTSC (M), NTSC (4.43), PAL (B, D, G, H, I), PAL (M), PAL (N), PAL (60) and SECAM (M). Each standard can be included or excluded in the standard recognition process by software control. The identified standard is indicated by the Standard Selection (SDT) register. Automatic standard detection can be overridden by software controlled standard selection.

Video Format support

TW9920 supports all common video formats as shown in Table 1. The video decoder needs to be programmed appropriately for each of the composite video input formats.

Table 1. Video Input Formats Supported by the TW9920

Format	Lines	Fields	Fsc	Country
NTSC-M	525	60	3.579545 MHz	U.S., many others
NTSC-Japan (1)	525	60	3.579545 MHz	Japan
PAL-B, G, N	625	50	4.433619 MHz	Many
PAL-D	625	50	4.433619 MHz	China
PAL-H	625	50	4.433619 MHz	Belgium
PAL-I	625	50	4.433619 MHz	Great Britain, others
PAL-M	525	60	3.575612 MHz	Brazil
PAL-CN	625	50	3.582056 MHz	Argentina
SECAM	625	50	4.406MHz 4.250MHz	France, Eastern Europe, Middle East, Russia
PAL-60	525	60	4.433619 MHz	China
NTSC (4.43)	525	60	4.433619 MHz	Transcoding

Notes: (1). NTSC-Japan has 0 IRE setup.

Component Processing

Luminance Processing

The TW9920 adjusts brightness by adding a programmable value (in register BRIGHTNESS) to the Y signal. It adjusts the picture contrast by changing the gain (in register CONTRAST) of the Y signal.

The TW9920 video decoder also performs a coring function. It can force all values below a certain level, programmed in the Coring Control Register, to zero. This is useful because human eyes are sensitive to variations in nearly black images. Changing levels near black to true black, can make the image appears clearer.

Gamma

Y Gamma function is provided to compensate for different display types. Four pre-programmed Gamma levels can be selected through registers.

Sharpness

The TW9920 also provides a sharpness control function through control registers. It provides the control in 16 steps up to +12db. The center frequency of the enhancement curve is around 3.5Mhz. It also provides a high frequency coring function to minimize the amplification of high frequency noise. The coring level is adjustable through the Coring Control register. The same

function can also be used to soften the images. This can be used to provide noise reduction on noisy signal.

To further enhance the image, a programmable vertical peaking function is provided for up to +6db of enhancement. A programmable coring level can be adjusted to minimize the noise enhancement.

The Hue and Saturation

When decoding NTSC signals, TW9920 can adjust the hue of the chroma signal. The hue is defined as a phase shift of the subcarrier with respect to the burst. This phase shift can be programmed through a control register.

The color saturation can be adjusted by changing the gain of Cb and Cr signals for all NTSC, PAL and SECAM formats. The Cb and Cr gain can be adjusted independently for flexibility.

Color Transient Improvement

A programmable Color Transient Improvement circuit is provided to enhance the color bandwidth. Low level noise enhancement can be suppressed by a programmable coring logic. Overshoot and undershoot are also removed by special circuit to prevent false color generation at the color edge.

Power Management

The TW9920 can be put into power-down mode in which its clock is turned off for most of the circuits. The Y and C path can be separately powered down.

Control Interface

The TW9920 registers are accessed via 2-WIRE SERIAL MPU interface. It operates as a slave device. Serial clock and data lines, SCL and SDA, transfer data from the bus master at a rate of 400 Kbits/s. The TW9920 has one serial interface address select pins to program up to two unique serial addresses TW9920. This allows as many as two TW9920 to share the same serial bus. Reset signals are also available to reset the control registers to their default values.

Down-scaling and Cropping

The TW9920 provides two methods to reduce the amount of output video pixel data, downscaling and cropping. The downscaling provides full video image at lower resolution. Cropping provides only a portion of the video image output. All these mechanisms can be controlled independently to yield maximum flexibility in the output stream.

TW9920 Down-Scaling

The TW9920 can independently reduce the output video image size in both horizontal and vertical directions using arbitrary scaling ratios up to 1/16 in each direction. The horizontal scaling employs a dynamic 6-tap 32-phase interpolation filter for luma and a 2-tap 8-phase interpolation filter for chroma because of the limited bandwidth of the chroma data. The vertical scaling uses the simple line dropping method. It is recommended to choose integer vertical scaling ratio for best result.

Downscaling is achieved by programming the horizontal scaling ratio register (HSCALE) and vertical scaling ratio register (VSCALE). When outputting unscaled video, the TW9920 will output CCIR601 compatible 720 pixels per line or any number of pixels per line as specified by the HACTIVE register. The standard output for Square Pixel mode is 640 pixels for 60 Hz system and 768 pixels for 50 Hz systems. If the number of output pixels required is smaller than 720 in CCIR601 compatible mode or the number specified by the HACTIVE register. The 12-bit HSCALE register, which is the concatenation of two 8-bit registers SCALE_HI and HSCALE_LO, is used to reduce the output pixels to the desired number.

Following is an example using pixel ratio to determine the horizontal scaling ratio. These equations should be used to determine the scaling ratio to be written into the 12-bit HSCALE register assuming HACTIVE is programmed with 720 active pixels per line:

NTSC: $HSCALE = [720/N_{pixel\_desired}] * 256$

PAL: $HSCALE = [(720/N_{pixel\_desired})] * 256$

Where: $N_{pixel\_desired}$ is the nominal number of pixel per line.

For example, to output a CCIR601 compatible NTSC stream at SIF resolution, the HSCALE value can be found as:

$HSCALE = [(720/320)] * 256 = 576 = 0x0240$

However, to output a SQ compatible NTSC stream at SIF resolution, the HSCALE value should be found as:

$HSCALE = [(640/320)] * 256 = 512 = 0x200$

In this case, with total resolution of 768 per line, the HACTIVE should have a value of 640.

The vertical scaling determines the number of vertical lines output by the TW9920. The vertical scaling register (VSCALE) is a 12-bit register, which is the concatenation of a 4-bit register SCALE_HI and an 8-bit register VSCALE_LO. The maximum scaling ratio is 16:1. Following equations should be used to determine the scaling ratio to be written into the 12-bit VSCALE register assuming VACTIVE is programmed with 240 or 288 active lines per field.

60Hz system: $VSCALE = [240/ N_{line\_desired}] * 256$

50Hz system: $VSCALE = [288/ N_{line\_desired}] * 256$

Where: $N_{line\_desired\ is}$ the number of active lines output per field.

The scaling ratios for some popular formats are listed in Table 3.

TW9920 Cropping

Cropping allows only subsection of a video image to be output. The VACTIVE signal can be programmed to indicate the number of active lines to be displayed in a video field, and the HACTIVE signal can be programmed to indicate the number of active pixels to be displayed in a video line. The start of the field or frame in the vertical direction is indicated by the leading edge of VSYNC. The start of the line in the horizontal direction is indicated by the leading edge of the HSYNC. The start of the active lines from vertical sync edge is indicated by the VDELAY register. The start of the active pixels from the horizontal edge is indicated by the HDELAY register. The sizes and location of the active video are determined by HDELAY, HACTIVE, VDELAY, and VACTIVE registers. These registers are 8-bit wide, the lower 8-bits is,

respectively, in HDELAY_LO, HACTIVE_LO, VDELAY_LO, and VACTIVE_LO. Their upper 2-bit shares the same register CROP_HI.

The Horizontal delay register (HDELAY) determines the number of pixels delay between the leading edge of HSYNC and the leading edge of the HACTIVE. Note that this value is referenced to the unscaled pixel number. The Horizontal active register (HACTIVE) determines the number of active pixels to be output or scaled after the delay from the sync edge is met. This value is also referenced to the unscaled pixel number. Therefore, if the scaling ratio is changed, the active video region used for scaling remain unchanged as set by the HACTIVE register, but the valid pixels output are equal or reduced due to down scaling. In order for the cropping to work properly, the following equation should be satisfied.

HDELAY + HACTIVE < Total number of pixels per line.

For NTSC output at 13.5 MHz pixel rate, the total number of pixels is 858. The HDELAY should be set to 106 and HACTIVE set to 720. For PAL output at 13.5 MHz rate, the total number of pixels is 864. The HDELAY should be set to 108 and HACTIVE set to 720.

The Vertical delay register (VDELAY) determines the number of lines delay between the leading edge of the VSYNC and the start of the active video lines. It indicates number of lines to skip at the start of a frame before asserting the VACTIVE signal. This value is referenced to the incoming scan lines before the vertical scaling. The number of scan lines is 525 for the 60Hz systems and 625 for the 50Hz systems. The Vertical active register (VACTIVE) determines the number of lines to be used in the vertical scaling. Therefore, the number of scan lines output is equal or less than the value set in this register depending on the vertical scaling ratio. In order for the vertical cropping to work properly, the following equation should be observed.

VDELAY + VACTIVE < Total number of lines per field

Table 3 shows some popular video formats and its recommended register settings. The CCIR601 format refers to the sampling rate of 13.5 MHz. The SQ format for 60 Hz system refers to the sampling rate of 12.27 MHz, and the SQ format for 50 Hz system refers to the use of sampling rate of 14.75 MHz.

Scaling Ratio	Format	Total Resolution	Output Resolution	HSCALE values	VSCALE (frame)
1:1	NTSC SQ	780x525	640x480	0x0100	0x0100
	NTSC CCIR601	858x525	720x480	0x0100	0x0100
	PAL SQ	944x625	768x576	0x0100	0x0100
	PAL CCIR601	864x625	720x576	0x0100	0x0100
2:1 (CIF)	NTSC SQ	390x262	320x240	0x0200	0x0200
	NTSC CCIR601	429x262	360x240	0x0200	0x0200
	PAL SQ	472x312	384x288	0x0200	0x0200
	PAL CCIR601	432x312	360x288	0x0200	0x0200
4:1 (QCIF)	NTSC SQ	195x131	160x120	0x0400	0x0400
	NTSC CCIR601	214x131	180x120	0x0400	0x0400
	PAL SQ	236x156	192x144	0x0400	0x0400
	PAL CCIR601	216x156	180x144	0x0400	0x0400

Table 3. HSCALE and VSCALE value for some popular video formats.

Output Interface

ITU-R BT.656

ITU-R BT.656 defines strict EAV/SAV Code, video data output timing, H blanking timing, and V Blanking timing. In this mode, VD[19:12] pins are effective and VCLK pin should be used for data clock signal. MSB bit of forth byte in EAV/SAV code must be "1" in ITU-R BT.656 standard. For that reason, VIPCFG Register bit must be set to "1".

ITU-R BT.656 SAV and EAV code sequence

	VD19	VD18	VD17	VD16	VD15	VD14	VD13	VD12
First byte	1	1	1	1	1	1	1	1
Second byte	0	0	0	0	0	0	0	0
Third byte	0	0	0	0	0	0	0	0
Forth byte	*C	F	V	H	V XOR H	F XOR H	F XOR V	F XOR V XOR H
H = 0 - SAV, 1 – EAV			**V = 1 – blanking, 0 – elsewhere**			**F = 0 – field 1, 1 – field 2**		

*C is set by VIPCFG register bit.

For complete ITU-R BT.656 standard,following registers are required.

ITU-R BT.656 Register set up.

Register	525 line system	625 line system
MODE	1	1
LEN	0	0
VDELAY	0x012	0x018
VACTIVE	0X0F4	0x120
HACTIVE	0x2D0	0x2D0
HA_EN	1	1
VIPCFG	1	1
NTSC656	1	0

ITU-R BT.656 for 525-line system has 244 video active lines in odd field and 243 vide active lines in even field. NTSC656 register bit controls this video active line length.

VIP (Video Interface Port)

Video port in VIP standard is the upgraded standard that has more functions in addition to ITU-R BT.656. Invalid data is set to 0x00 during the period from SAV to EAV if CTL656 register is set to "1" for this VIP application. In case of Vertical down Scaling mode, invalid line does NOT have EAV/SAV code by default setting. This mode is most popular in current VIP application. TW9920 also supports all line EAV/SAV output modes optionally. In this case, VSCTL register should be set to "1". All data will be 0x00 invalid data from SAV to EAV on invalid line in this mode. Starting position of vertical active output video line is programmable by VDELAY register. The number of active video lines is also programmable by VACTIVE register.

Horizontal Down Scaling Output

TW9920 generates Horizontal down scaling output data. Figure 9 shows 8 bit mode Horizontal Down Scaling output timing and Figure 10 shows 16 bit mode Horizontal Down Scaling output timing. As shown Figure 9 and Figure 10, Horizontal Down Scaled data are generated by continuous data stream. The trailing edge of DVALID signal changes with the trailing edge of HACTIVE signal. Data value from the leading edge of HACTIVE to the leading edge of DVALID is programmable by CNTL656 register. If CNTL656 is set to "1", all Y and CbCr data will be 0x00. If CNTL656 is set to "0", all Y data will be 0x10 and all CbCr data will be 0x80. VIP application normally uses 0x00 data as invalid data. Figure9 and Figure 10 show 360 active pixels output timing after horizontal downscaling.

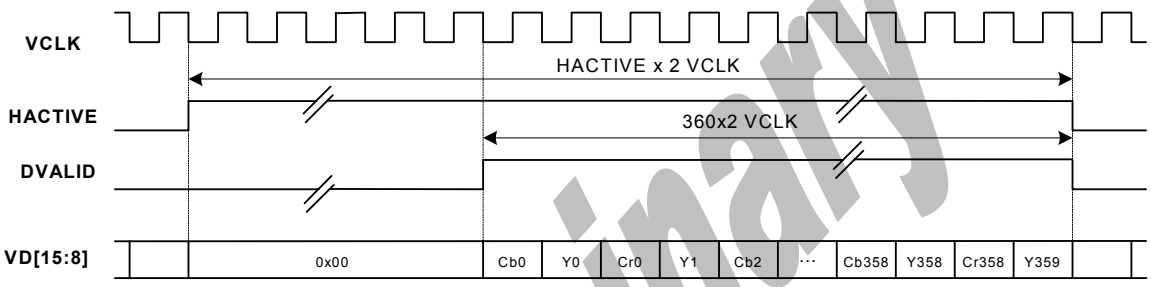


Figure 9. 8 bit mode Horizontal Down Scaling Output

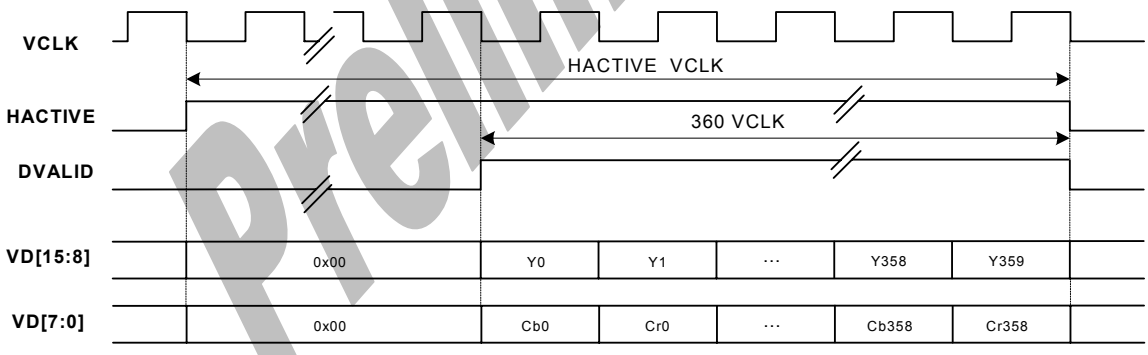


Figure 10. 16 bit mode Horizontal Down Scaling Output

Vertical Down Scaling Output

TW9920 generates Vertical Down Scaling output data. Figure 11 shows its timing. As shown on Figure 11, HACTIVE is NOT generated on invalid line as default (VSCTL is “0”). If VSCTL is set to “1”, HACTIVE is generated on every lines during VACTIVE active period. DVALID is not generated on invalid lines in each setting. Invalid lines for Vertical down scaling are generated during VACTIVE active period. If MODE bit is set to “1” for VIP mode, EAV/SAV codes are not generated on those lines without HACTIVE signal. All CbCr data will be 80H and all Y data will be 10H the same as H-blanking data in ITU-R BT.656 data stream.

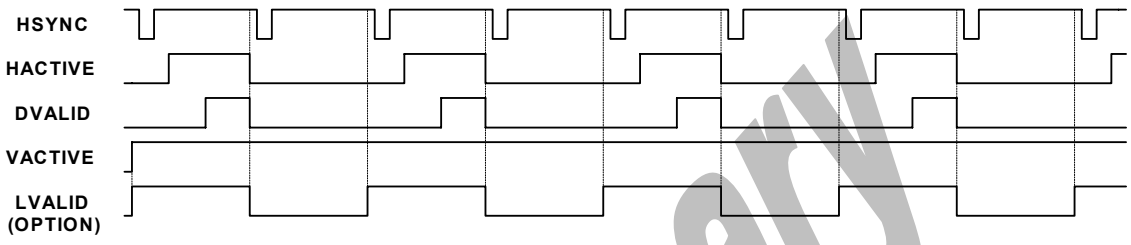


Figure 11. Vertical Down Scaling Output

Raw VBI data output

TW9920 supports raw VBI data output. Raw VBI data output has the same vertical line delay timing as video output. Horizontal output timing is also programmable by VBIDELAY register. Raw VBI data is generated during HACTIVE active period (from SAV to EAV) as Video data output. Total pixel number of raw VBI data per line is twice as many as HACTIVE register value. If VBI EN register is set to “1”, all vertical blanking output while VACTIVE is inactive will be raw VBI data output. If VVBI registers are set to more than “1”, the VVBI number lines from top video active lines will also be raw VBI data output lines.

VBI Data Processing

Raw VBI data output

TW9920 supports raw VBI data output. Raw VBI data output has the same vertical line delay timing as video output. Horizontal output timing is also programmable by VBIDELAY register. Raw VBI data is generated during HACTIVE active period (from SAV to EAV) as Video data output. Total pixel number of raw VBI data per line is twice as many as HACTIVE register value. If VBI EN register is set to "1", all vertical blanking output while VACTIVE is inactive will be raw VBI data output. If VVBI registers are set to more than "1", the VVBI number lines from top video active lines will also be raw VBI data output lines.

VBI Data Slicer

The following VBI standards are supported by VBI Data slicer. The VBI Data slicing is controlled by the registers LCTL6 to LCTL26. Registers LCTL6 to LCTL26 are controlling the slicing process itself. LCTL6 to LCTL26 defines the Data Type to be decoded. The Data Type can be specified on a line by line basis for line6 to line26 and for even and odd field depending on the detected TV system standard. The setting for LCTL26 is valid for the rest of the corresponding field. Normally no text data 0H (video data) should be selected to render the VBI Data slicer inactive during active video. LCTRL26 is useful for Full-Field Teletext mode in the case of NABTS.

NABTS is 525 Teletext-C. Japan's MOJI is 525 Teletext-D. Didon Antiope is 625 Teletext-A. VBI Data slicer supports up to Physical layer, Link layer in ITU-R BT.653-2. Japan's EIAJ CPR-1204 shown as 525 WSS has the same physical layer protocol as that of CGMS.

The sliced VBI data is embedded in the ITU-R BT.656 output stream, using the intervals between the End of Active Video (EAV) and the Start of Active Vide(SAV) codes of each line and formatted according to ITU-R BT.1364 Ancillary data packet Type 2.

Table 4. VBI Standard.

STANDARD TYPE	TV Systems (lines/freq)	Bit Rate (Mbits/s)	Modulation	Data Type
625 Teletext-B	625/50	6.9375	NRZ	1H
525 Teletext-B	525/60	5.727272	NRZ	1H
625 Teletext-C	625/50	5.734375	NRZ	2H
525 Teletext-C	525/60	5.727272	NRZ	2H
625 Teletext-D	625/50	5.6427875	NRZ	3H
525 Teletext-D	525/60	5.727272	NRZ	3H
625 CC	625/50	0.500	NRZ	4H
525 CC	525/60	0.503	NRZ	4H
625 WSS	626/50	5	Bi-phase	5H
525 WSS(CGMS)	525/60	0.447443	NRZ	5H
625 VITC	625/50	1.8125	NRZ	6H
525 VITC	525/60	1.7898	NRZ	6H
Gemstar 2x	525/60	1.007	NRZ	7H
Gemstar 1x	525/60	0.503	NRZ	8H
VPS	625/50	5	Bi-phase	9H
625 Teletext-A	625/50	6.203125	NRZ	AH

Sliced VBI Data output format

After 4 bytes of EAV code, sliced VBI ANC data packets are generated by following format. Byte1 to Byte4N+7 data stream is formatted according to ITU-R BT.1364 ANC data packet type2. BC data byte is optional and not included in ANC data packet type 2 BC data byte is inserted after ANC data packet type2.

Table 5. Sliced VBI ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary data flag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	NEP	EP	DC5	DC4	DC3	DC2	DC1	DC0	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	DT3	DT2	DT1	DT0	IDI2. UDW 2
9	Sliced VBI Data byte 1								Sliced VBI Data No.1. UDW3
10	Sliced VBI Data byte 2								Sliced VBI Data No.2. UDW4
11	Sliced VBI Data byte 3								Sliced VBI Data No.3 UDW5
12	Sliced VBI Data byte 4								Sliced VBI Data No.4. UDW6
13	Sliced VBI Data byte 5								Sliced VBI Data No.5. UDW7
.	.								
.	.								
4N+6	Sliced VBI Data byte last or FILLDATA								Sliced VBI Data Last or FILLDATA. UDW 4N
4N+7	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
4N+8	OP	0	BC5	BC4	BC3	BC2	BC1	BC0	BC

1. EP is Even Parity of bits 5 to 0 in same 1 byte.
2. NEP is inverted EP in same 1 byte.
3. {DID4,DID3,DID2,DID1,DID0} is DID register value.
4. {SDID5,SDID4,SDID3,SDID2,SDID1,SDID0} is SDID register value.
5. {DC5,DC4,DC3,DC2,DC1,DC0} is the number of DOWRD data length from UDW1 to UDW4N.On this table, {DC5,DC4,DC3,DC2,DC1,DC0} is N(decimal).
6. OP is Odd Parity of bits 6 to 0 in same 1 byte.
7. FID=0: odd field ; FID=1: even field.
8. {LN8,LN7,LN6,LN5,LN4,LN3,LN2,LN1,LN0} is the line number of current sliced VBI data.
9. {DT3,DT2,DT1,DT0} is the Data Type shown on Table
10. NCS6 is inverted CS6.
11. {CS6,CS5,CS4,CS3,CS2,CS1,CS0} is the checksum value calculated from DID to UDW4N.
12. UDW1 to UDW4N are the User data words(UDW) shown on ITU-R BT.1364 ANC data packet type 2.
13. [BC5,BC4,BC3,BC2,BC1,BC0] is the number of valid bytes from UDW1 to UDW4N.
14. FILLDATA is FILLDATA register value. FILLDATA is inserted after last valid bytes to make 4N number byte stream sometimes.

Following shows various type of ANC data packet to be outpu

Table 6. Closed Captioning ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary data flag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	0	1	0	0	0	0	0	1	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	1	0	0	IDI2. UDW 2
9	1st Character byte								UDW3
10	2nd Character byte								UDW4
11	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
12	0	0	0	0	0	1	0	0	BC

Table 7. CGMS ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	0	1	0	0	0	0	1	0	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	1	0	1	IDI2. UDW 2
9	WSS[7:0]								UDW3
10	WSS[15:8]								UDW4
11	{0H,WSS[19:16]}								UDW5
12	CRCERRORCODE								UDW6
13	FILLDATA								UDW7
14	FILLDATA								UDW8
15	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
16	1	0	0	0	0	1	1	0	BC

1.CRCERRORCODE is optional byte. 41H means “this wss data has CRC Error”. 80H means no CRC error.

Table 8. 625 line Wide Screen signaling ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	0	1	0	0	0	0	0	1	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	1	0	1	IDI2. UDW 2
9	WSS[7:0]								UDW3
10	{00b,WSS[13:8]								UDW4
12	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
13	0	0	0	0	0	1	0	0	BC

Table 9. 625 Teletext-A ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	0	1	0	0	1	0	1	1	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	1	0	1	0	IDI2. UDW 2
9	FRAME CDDE								UDW3
10	BYTE4								UDW4
11	BYTE5								UDW5
.	.								
.	.								
46	BYTE40								UDW40
47	HAMM84ERROR								UDW41
48	FILLDATA								UDW42
49	FILLDATA								UDW43
50	FILLDATA								UDW44
51	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
52	0	0	1	0	1	0	0	1	BC

1.FRAME CODE is E7H if it's received correctly.
2.HAMM84ERROR is 41H if more than 1 8/4 Hamming code error in this packet,80H means no 8/4 Hamming error.

Table 10. 625 Teletext-B ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	1	0	0	0	1	1	0	0	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	0	0	1	IDI2. UDW 2
9	FRAME CDDE								UDW3
10	BYTE4								UDW4
11	BYTE5								UDW5
.	.								
.	.								
50	BYTE44								UDW44
51	BYTE45								UDW45
52	HAMM84ERROR								UDW46
53	FILLDATA								UDW47
54	FILLDATA								UDW48
55	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
56	1	0	1	0	1	1	1	0	BC

1.FRAME CODE is 27H if it's received correctly.
2.HAMM84ERROR is 41H if more than 1 8/4 Hamming code error in this packet,80H means no 8/4 Hamming error.

Table 11. 525 Teletext-B ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	1	0	0	0	1	0	1	0	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	0	0	1	IDI2. UDW 2
9	FRAME CDDE								UDW3
10	BYTE4								UDW4
11	BYTE5								UDW5
.	.								
.	.								
30	BYTE36								UDW36
31	BYTE37								UDW37
32	HAMM84ERROR								UDW38
33	FILLDATA								UDW39
34	FILLDATA								UDW40
35	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
36	1	0	1	0	0	1	1	0	BC

1.FRAME CODE is 27H if it's received correctly.
2.HAMM84ERROR is 41H if more than 1 8/4 Hamming code error in this packet,80H means no 8/4 Hamming error.

Table 12. 625 Teletext-C and 525 Teletext-C ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	1	0	0	0	1	0	1	0	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	0	1	0	IDI2. UDW 2
9	FRAME CDDE								UDW3
10	BYTE4								UDW4
11	BYTE5								UDW5
.	.								
.	.								
42	BYTE36								UDW36
43	HAMM84ERROR								UDW37
44	FILLDATA								UDW38
45	FILLDATA								UDW39
46	FILLDATA								UDW40
47	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
48	0	0	1	0	0	1	0	1	BC

1.FRAME CODE is E7H if it's received correctly.
2.HAMM84ERROR is 41H if more than 1 8/4 Hamming code error in this packet,80H means no 8/4 Hamming error.

Table 13. 625 Teletext-D and 525 Teletext-D ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	1	0	0	0	1	0	1	0	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	1	1		IDI2. UDW 2
9	FRAME CDDE								UDW3
10	BYTE4								UDW4
11	BYTE5								UDW5
.	.								
.	.								
42	BYTE36								UDW36
43	BYTE37								UDW37
44	FILLDATA								UDW38
45	FILLDATA								UDW39
46	FILLDATA								UDW40
47	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
48	0	0	1	0	0	1	0	1	BC

1.FRAME CODE is A7H if it's received correctly.

Table 14. Line16 VPS ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	1	0	0	0	0	1	0	1	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	1	0	0	1	IDI2. UDW 2
9	START CDDE1(51H)								UDW3
10	START CODE2(99H)								UDW4
11	BYTE3								UDW5
.	.								
.	.								
22	BYTE14								UDW16
23	BYTE15								UDW17
24	BI-PHASEERROR								UDW18
25	FILLDATA								UDW19
26	FILLDATA								UDW20
27	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
28	1	0	0	1	0	0	1	0	BC

1.START CODE1 is the first byte of Start Code by 5Mbps slicing.
2.START CODE2 is the second byte of Start Code by 5Mbps slicing.
3.BYTE3~BYTE15 are data bytes by 5/2 Mbps Bi-phase slicing.
4.BI-PHASEEROOR is Bi-phase coding error detection.80H means No error.41H means Bi-phase coding error is detected.

Table 15. VITC ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	1	0	0	0	0	0	1	1	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	1	1	0	IDI2. UDW 2
9	Bit[9:2]								UDW3
10	Bit[19:12]								UDW4
11	Bit[29:22]								UDW5
12	.Bit[39:32]								UDW6
13	.Bit[49:42]								UDW7
14	Bit[59:52]								UDW8
15	Bit[69:62]								UDW9
16	Bit[79:72]								UDW10
17	Bit[89:82]								UDW11
18	CRCERROR								UDW12
19	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
20	1	0	0	0	1	1	0	0	BC

1.CRCERROR is CRC Error information.41H means CRC Error is deteced.80H means no CRC error.

Table 16. Gemstar 1X ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	0	1	0	0	0	0	0	1	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	1	0	0	0	IDI2. UDW 2
9	1st Character byte								UDW3
10	2nd Character byte								UDW4
11	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
12	0	0	0	0	0	1	0	0	BC

Table 17. Gemstar 2X ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	0	1	0	0	0	0	1	0	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	1	1	1	IDI2. UDW 2
9	FRAMECODE1								UDW3
10	FRAMECODE2								UDW4
11	Data Byte 1								UDW5
12	Data Byte 2								UDW6
13	Data Byte 3								UDW7
14	Data Byte 4								UDW8
15	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
16	0	0	0	0	1	0	0	0	BC

1.FRAMCODE1 is B9H if Frame Code is correctly received.
2.FRAMCODE2 is 05H if Frame Code is correctly received.

Audio clock generation

(Register 40 to 48)

TW9920 has built-in field locked audio clock generator for use in video capture applications. The circuitry will generate the same predefined number of audio sample clocks per field to ensure synchronous playback of video and audio after digital recording or compression. The audio clock is digitally synthesized from the crystal clock input with reference to the incoming video.

The master audio clock frequency is programmable through ACKN and ACKI register based following two equations.

ACKN = round (F audio / F field), it gives the Audio master Clock Per Field.

ACKI = round (F audio / F crystal * 2^23), it gives the Audio master Clock Nominal Increment.

Following table provides setting example of some common used audio frequency assuming crystal frequency of 27MHz.

AMCLK(Mhz)	FIELD[Hz]	ACKN dec	ACKN hex	ACKI dec	ACKI hex
256 x 48 KHz					
12.288	50	245760	3-C0-00	3817749	3A-41-15
12.288	59.94	205005	3-20-CD	3817749	3A-41-15
256 x 44.1KHz					
11.2896	50	225792	3-72-00	3507556	35-85-65
11.2896	59.94	188348	2-DF-BC	3507556	35-85-65
256 x 32 KHz					
8.192	50	163840	2-80-00	2545166	26-D6-0E
8.192	59.94	136670	2-15-DE	2545166	26-D6-0E
256 x 8 KHz					
2.048	50	40960	A0-00	636291	9-B5-83
2.048	59.94	34168	85-78	636291	9-B5-83

Two further divided down clocks are available on pin ASCLK and pin ALRCLK. These two clocks are derived from AMXCLK input based on following two equations. The frequency of these two slower digital clocks can be controlled by registers SDIV and LRDIV as shown.

$$f_{asclk} = \frac{f_{amxclk}}{(SDIV+1) * 2}$$

$$f_{alrclk} = \frac{f_{asclk}}{LRDIV * 2}$$

Some other Audio Clock related control functions are explained here.

ACPL Audio PLL control
0 – PLL loop closed
1 – PLL loop open

SRPH ASCLK phase control
0 – Invert AMXCLK, ASCLK transition is triggered by falling edge of AMXCLK
1 – Normal AMXCLK, ASCLK transition is triggered by rising edge of AMXCLK

LRPH ALRCLK phase control
0 – Invert ASCLK, ALRCLK transition is triggered by falling edge of ASCLK
1 – Normal ASCLK, ALRCLK transition is triggered by rising edge of ASCLK

APG, APZ Audio PLL dynamic control

Analog Video Encoder

The TW9920 supports analog video output using built-in video encoder which generates composite or S-video and YCbCr with five10 bits DACs. The incoming digital video are adjusted for gain and offset according to NTSC or PAL standard. Both the luminance and chrominance are band-limited and interpolated to 27MHz sampling rate for digital to analog conversion. The NTSC output can be selected to include a 7.5IRE pedestal. The TW9920 also provides internal test color bar generation.

Output Standard Selection

The TW9920 supports various video standard outputs via SYS5060 (1x70) and FSC, PHALT, PED (1x70) registers as described in the following table.

Table 18. Supporting analog video standards

Format	Line/Fv (Hz)	Fh (KHz)	Fsc (MHz)	SYS5060	FSC	PHALT	PED
NTSC-M	525/59.94	15.734	3.579545	0	0	0	1
NTSC-J							0
NTSC-4.43	525/59.94	15.734	4.43361875	0	1	0	1
NTSC-N	625/50	15.625	3.579545	1	0	0	0
PAL-BDGHI	625/50	15.625	4.43361875	1	1	1	0
PAL-N							1
PAL-M	525/59.94	15.734	3.57561149	0	2	1	0
PAL-NC	625/50	15.625	3.58205625	1	3	1	0
PAL-60	525/59.94	15.734	4.43361875	0	1	1	0

If ALTRST (1x70) register is set to “1”, phase alternation can be reset every 8 field so that phase alternation keeps same phase every 8 field.

Luminance Filter

The luminance signal keeps flat up to 6MHz as shown in the following Fig 12.

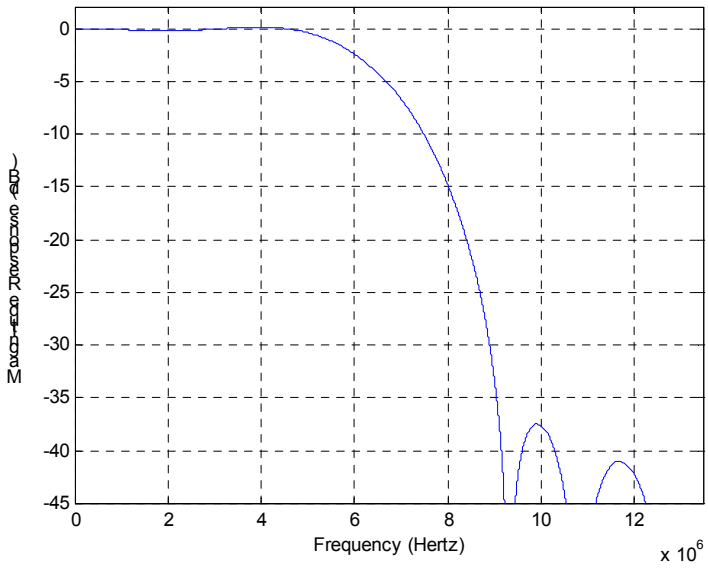


Fig 12. Characteristics of luminance filter

Chrominance Filter

The band of chrominance signal can be selected as shown in the following Fig 13.

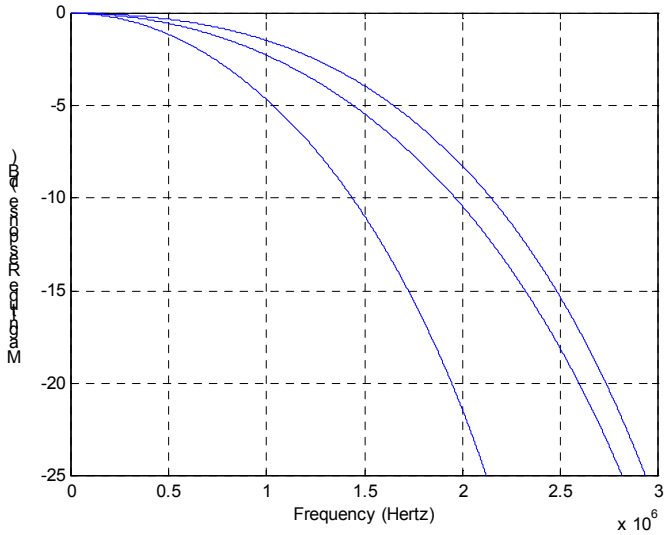


Fig 13. Characteristics of chrominance Filter

Digital-to-Analog Converter

Digital video data from video encoder is converted to analog video signal by DAC (Digital to Analog Converter). Analog video signal format can be selected for composite or Y out via DAC_OUT (1x75) register. Each DAC can be disabled independently to save power by DAC_PD 0,1,2,3,4 (1x76) register.

A simple reconstruction filter is required externally to reject noise as shown in Fig 14.

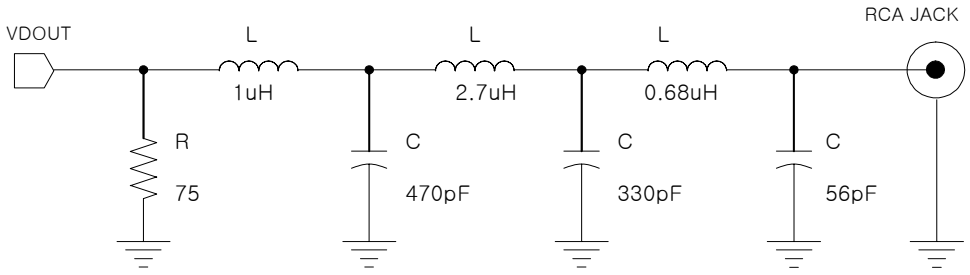


Fig 14. Example of reconstruction filter

Timing Interface and Control

The TW9920 can be operated in slave mode. In master mode, TW9920 receives all of timing information from ITU-R 656 video input data in slave mode.

The polarity of horizontal, vertical sync and field flag can be controlled by HSPOL, VSPOL and FLDPOL (1x71) register respectively for slave mode. The TW9920 can detect field polarity from vertical sync and horizontal sync via ENC_FLD (1x71) register or can detect vertical sync from field flag via ENC_VS (1x71) register.

The TW9920 extracts the timing information from input video data streams. To adjust these timing, TW9920 has ENC_HSDEL (1x73), ENC_VSDEL and ENC_VSOFF (1x72) register which control only the related signal timing regardless of digital video input data. The detailed timing diagram is illustrated in following FIG 15.

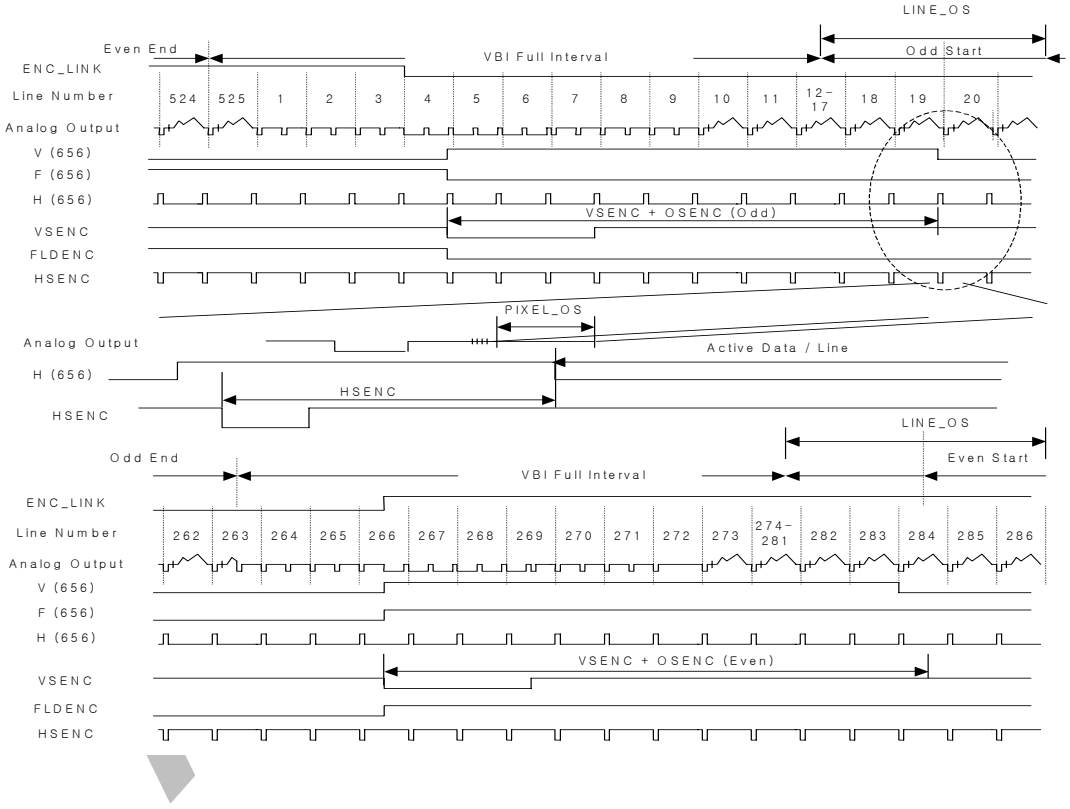


Fig 15. Horizontal and vertical timing control

Two Wire Serial Bus Interface

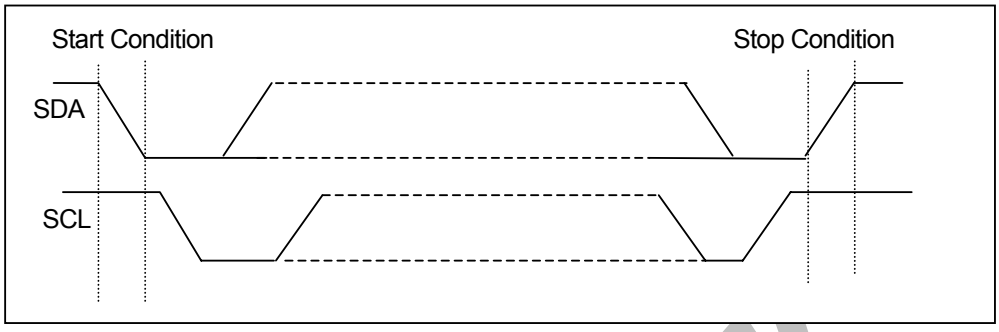


Figure 16. Definition of the serial bus interface bus start and stop

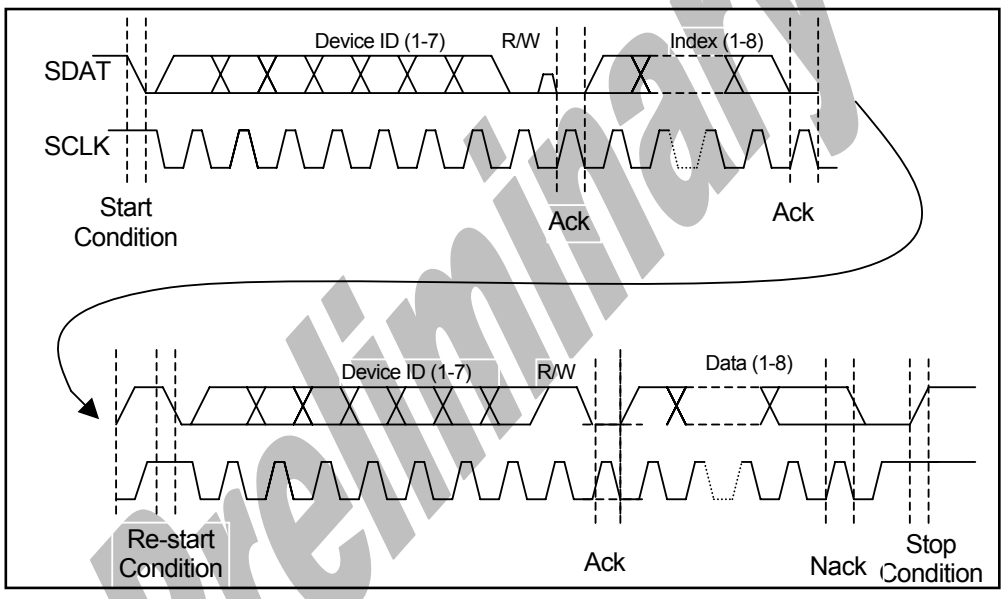


Figure 17. One complete register read sequence via the serial bus interface

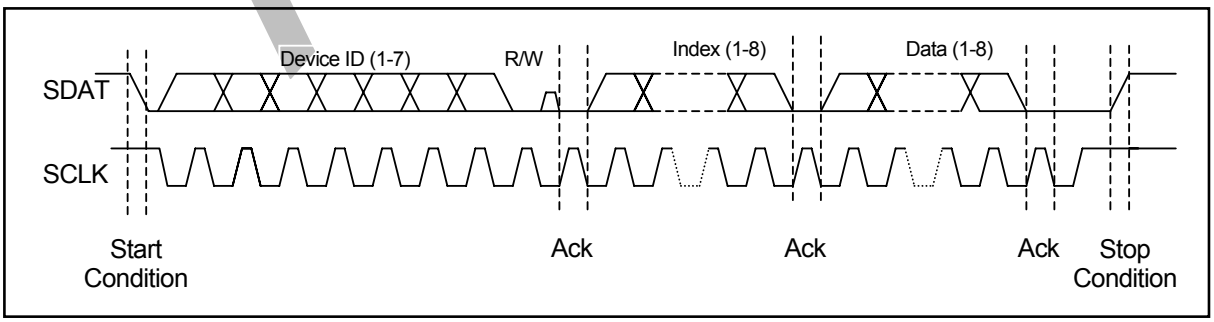


Figure 18. One complete register write sequence via the serial bus interface

The two wire serial bus interface is used to allow an external micro-controller to write control data to, and read control or other information from the TW9920 registers. SCLK is the serial clock and SDAT is the data line. Both lines are pulled high by resistors connected to VDD. ICs communicate on the bus by pulling SCLK and SDAT low through open drain outputs. In normal operation the master generates all clock pulses, but control of the SDAT line alternates back and forth between the master and the slave. For both read and write, each byte is transferred MSB first, and the data bit is valid whenever SCLK is high.

The TW9920 is operated as a bus slave device. It can be programmed to respond to one of two 7-bit slave device addresses by tying the SIAD (Serial Interface Address) pin ether to VDD or VSS (See Table 19). If the SIAD pin is tied to VDD, then the least significant bit of the 7-bit address is a "1". If the SIAD pin is tied to VSS then the least significant bit of the 7-bit address is a "0". The most significant 6-bits are fixed. The 7-bit address field is concatenated with the read/write control bit to form the first byte transferred during a new transfer. If the read/write control bit is high the next byte will be read from the slave device. If it is low the next byte will be a write to the slave. When a bus master (the host microprocessor) drives SDA from high to low, while SCL is high, this is defined to be a start condition (See Figure 16.). All slaves on the bus listen to determine when a start condition has been asserted.

After a start condition, all slave devices listen for the their device addresses. The host then sends a byte consisting of the 7-bit slave device ID and the R/W bit. This is shown in Figure 8. (For the TW9920, the next byte is normally the index to the TW9920 registers and is a write to the TW9920 therefore the first R/W bit is normally low.)

After transmitting the device address and the R/W bit, the master must release the SDAT line while holding SCLK low, and wait for an acknowledgement from the slave. If the address matches the device address of a slave, the slave will respond by driving the SDAT line low to acknowledge the condition. The master will then continue with the next 8-bit transfer. If no device on the bus responds, the master transmits a stop condition and ends the cycle. Notice that a successful transfer always includes nine clock pulses.

To write to the internal register of theTW9920, the master sends another 8-bits of data, the TW9920 loads this to the register pointed by the internal index register. The TW9920 will acknowledge the 8-bit data transfer and automatically increment the index in preparation for the next data. The master can do multiple writes to the TW9920 if they are in ascending sequential order. After each 8-bit transfer the TW9920 will acknowledge the receipt of the 8-bits with an acknowledge pulse. To end all transfers to the TW9920 the host will issue a stop condition.

Serial Bus Interface 7-bit Slave Address							Read/Write bit
1	0	0	0	1	0	SIAD0	1=Read 0=Write

Table 19 TW9920 serial bus interface 7-bit slave address and read write bit

A TW9920 read cycle has two phases. The first phase is a write to the internal index register. The second phase is the read from the data register. (See figure 17). The host initiates the first phase by sending the start condition. It then sends the slave device ID together with a 0 in the R/W bit position. The index is then sent followed by either a stop condition or a second start condition. The second phase starts with the second start condition. The master then resends the same slave device ID with a 1 in the R/W bit position to indicate a read. The slave will transfer the contents of the desired register. The master remains in control of the clock. After transferring eight bits, the slave releases and the master takes control of the SDAT line and

acknowledges the receipt of data to the slave. To terminate the last transfer the master will issue a negative acknowledge (SDAT is left high during a clock pulse) and issue a stop condition.

Test Modes

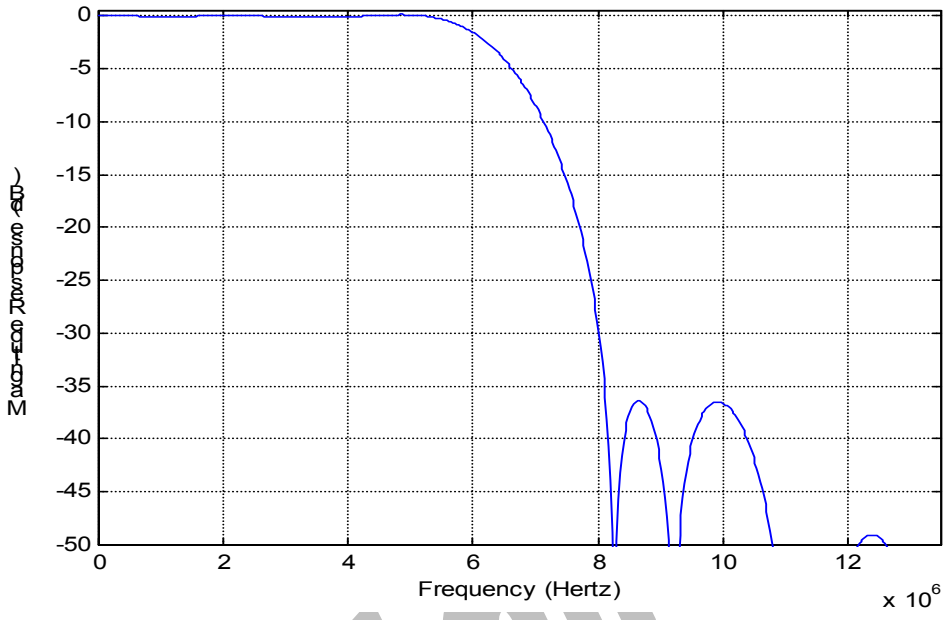
The input pin TMODE combining with RESET# provide different test modes selection. If this pin is low at the rising edge of the RESET# pin and remaining low afterwards, TW9920 is in the normal operating mode. Other test modes can be obtained as shown in Table 20.

Table 20. Test mode selection and description

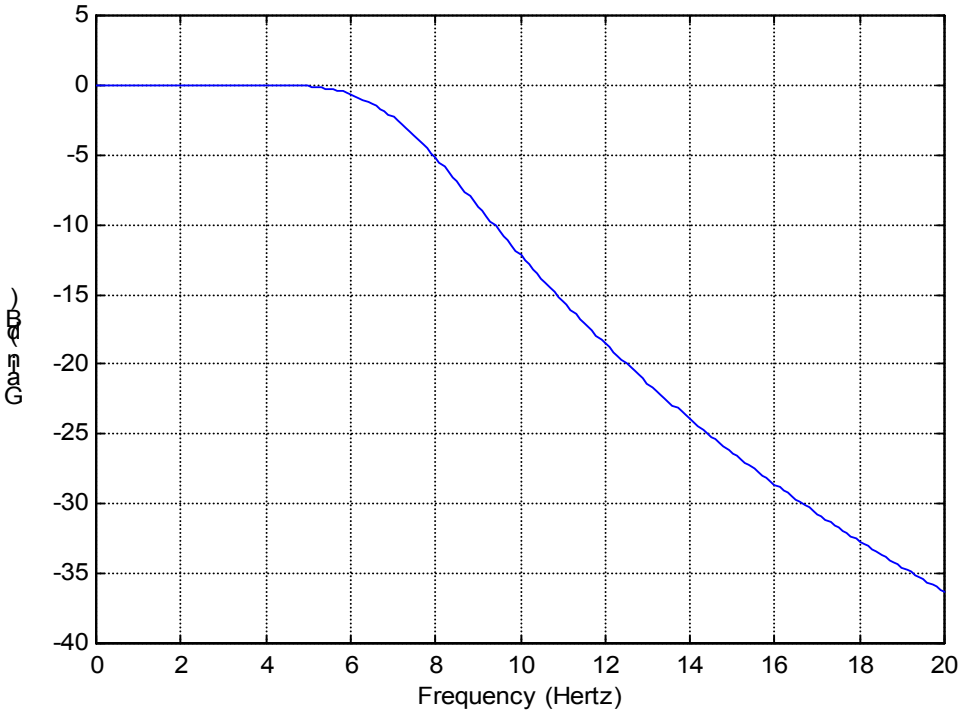
Test mode	TMODE before RESET# rising edge	TMODE after RESET# rising edge	Description
Normal	0	0	Normal operation mode.
Pin tri-state	0	1	In this mode, all pin output drivers are tri-stated. Pin leakage current parameters can be measured.
Outputs high	1	0	In this mode, all pin output drivers are forced to the high output state. Pin output high voltage, V_{OH} and I_{OH}, can be measured.
Outputs low	1	1	In this mode, all pin output drivers are forced to the low output state. Pin output low voltage, V_{OL} and I_{OL}, can be measured.

Filter Curves

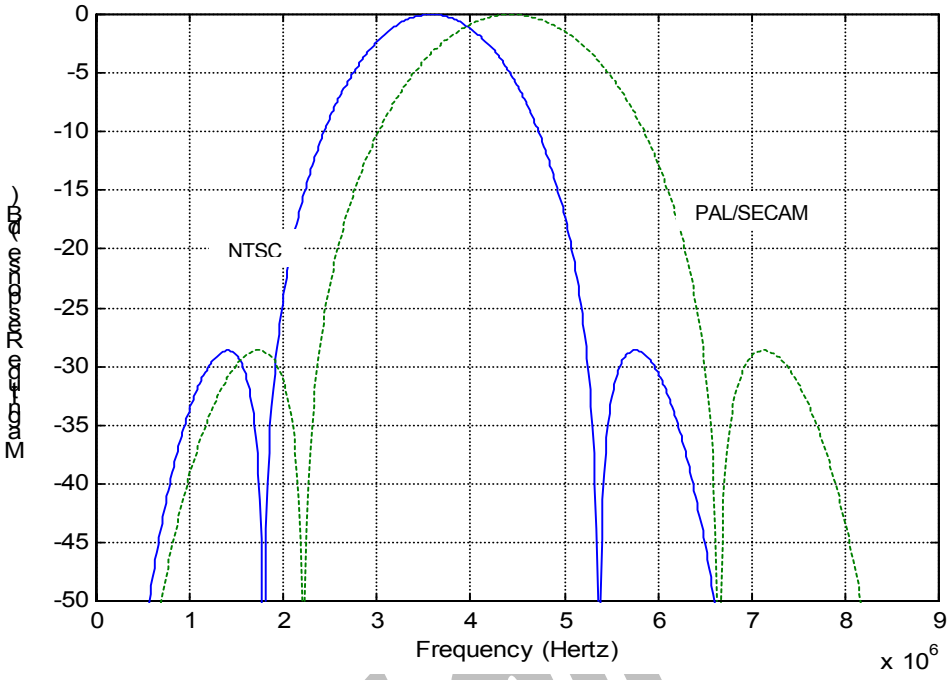
Decimation filter



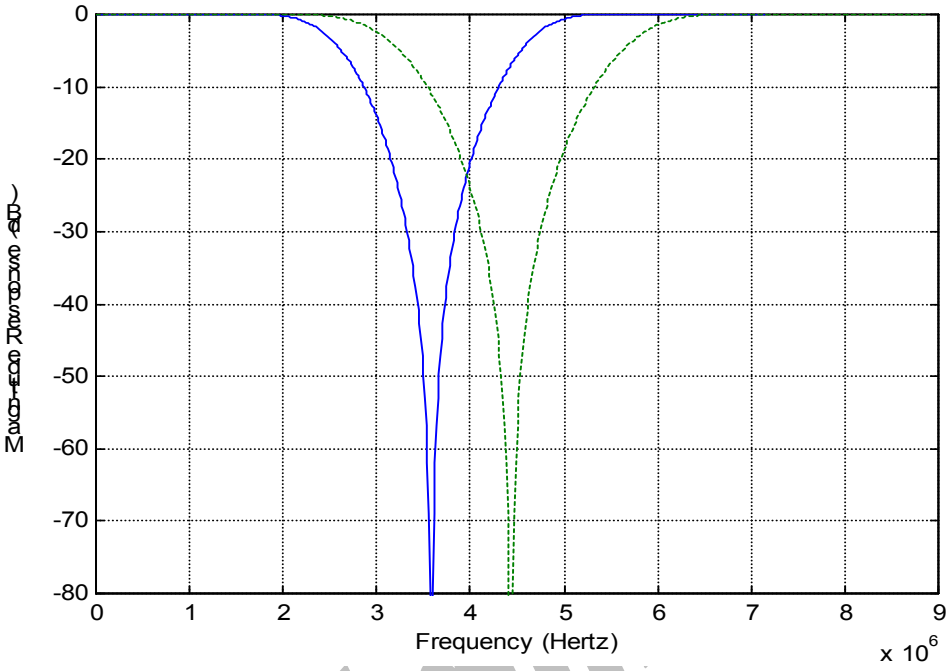
Anti-alias filter



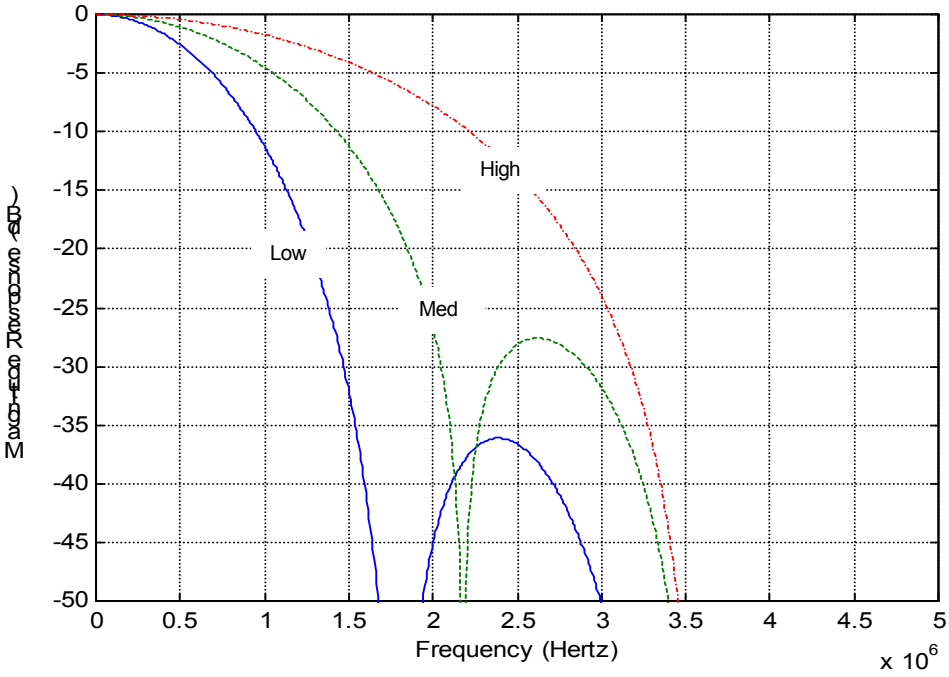
Chroma Band Pass Filter Curves



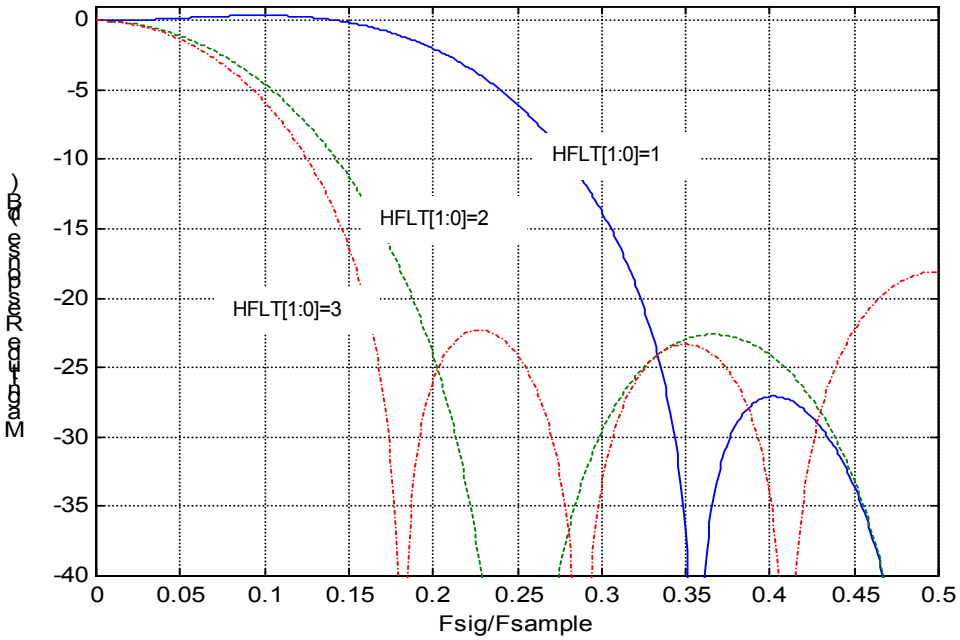
Luma Notch Filter Curve for NTSC and PAL/SECAM



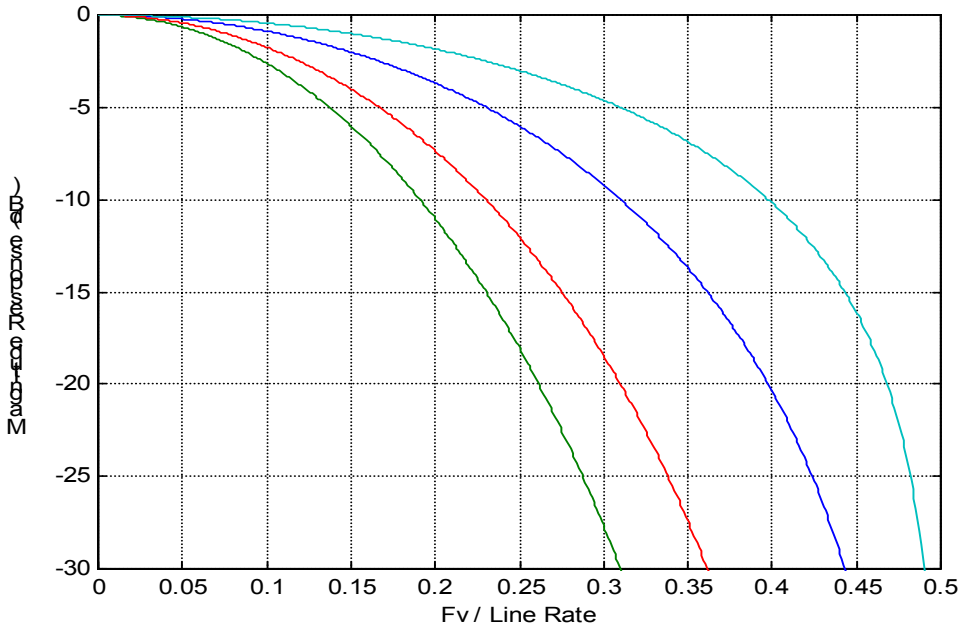
Chrominance Low-Pass Filter Curve



Horizontal Scaler Pre- Filter curves

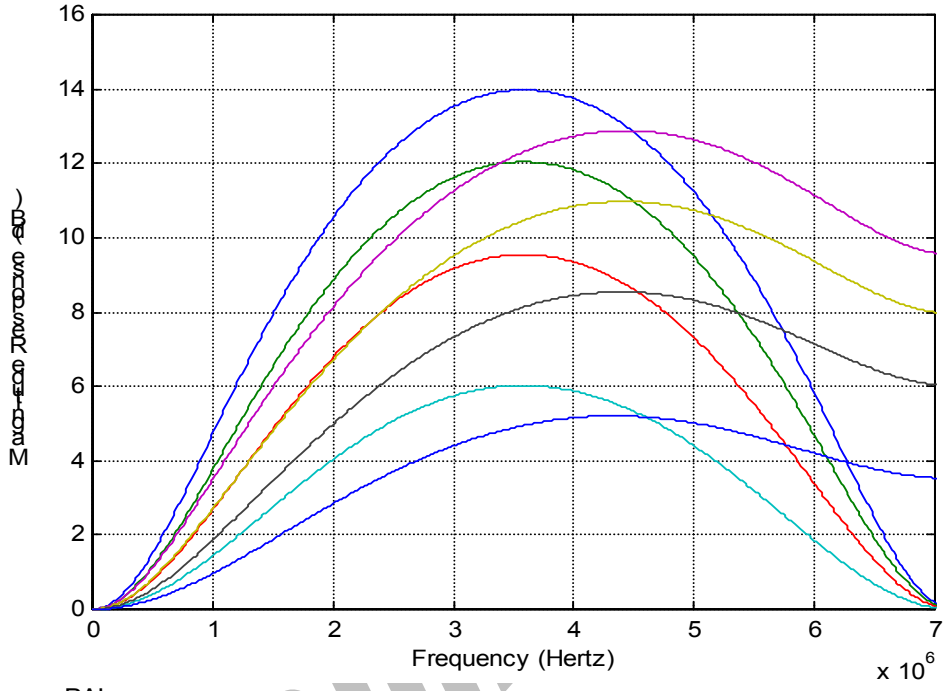


Vertical Interpolation Filter curves

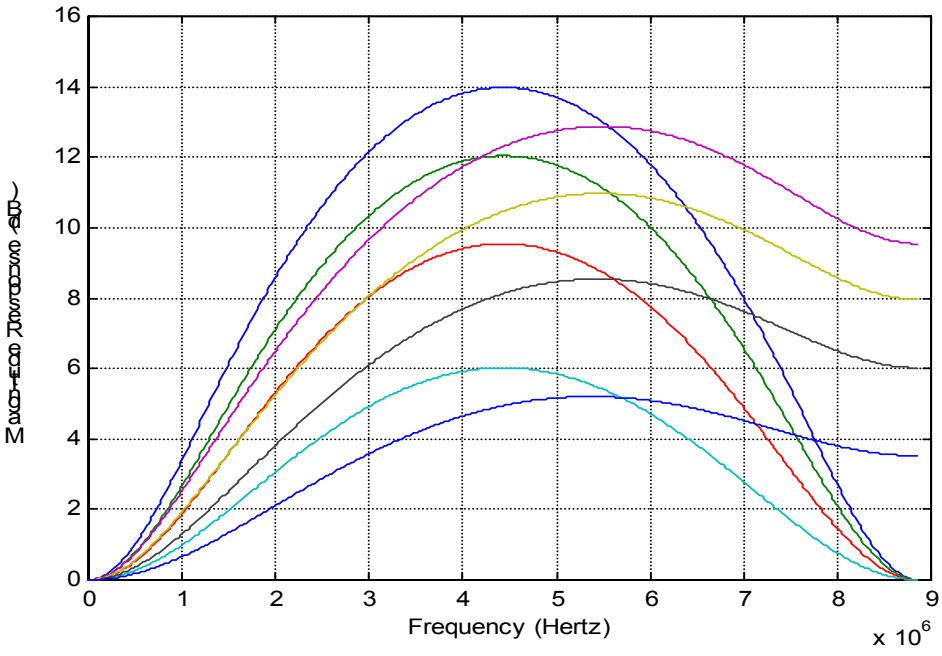


Peaking Filter Curves

NTSC



PAL



Control Register

TW9920 Register SUMMARY

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
00	ID					REV			3A
01	VDLOSS	HLOCK	SLOCK	FIELD	VLOCK		MONO	DET50	00
02	YSEL2	FC27	IFSEL		YSEL		CSEL	SEL	40
03	MODE	LEN	LLCMODE	AINC	VSCTL	OEN	TRI_SEL		04
04	GMEN	CKHY		HSDLY					00
05	VSP	VSSL			HSP	HSSL			00
06	SRESET	IREF	VREF	AGC_EN	CLKPDN	Y_PDN	C_PDN	-	00
07	VDELAY_HI		VACTIVE_HI		HDELAY_HI		HACTIVE_HI		02
08	VDELAY_LO								12
09	VACTIVE_LO								F0
0A	HDELAY_LO								0F
0B	HACTIVE_LO								D0
0C	PBW	DEM	PALSW	SET7	COMB	HCOMP	YCOMB	PDLY	CC
0D	VSCALE_LO								00
0E	VSCALE_HI				HSCALE_HI				11
0F	HSCALE_LO								00
10	BRIGHTNESS								00
11	CONTRAST								5C
12	SCURVE	VSF	CTI		SHARPNESS				51
13	SAT_U								80
14	SAT_V								80
15	HUE								00
16	-				-				53
17	SHCOR				-	VSHP			80
18	CTCOR		CCOR		VCOR		CIF		44
19	VBI_EN	VBI_BYT	VBI_FRAM	HA_EN	CTL656	RTSEL			58
1A	LLCTEST	PLL_PDN	-	-	YFLEN	YSV	CFLEN	CSV	00
1B	CK2S		CK1S		FLP	FLSL			50
1C	DTSTUS	STDNOW			ATREG	STANDARD			07
1D	START	PAL60	PALCN	PALM	NTSC4	SECAM	PALB	NTSC	7F
1E	-	CVSTD			CVFMT				08
1F	TEST								00

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
20	CLPEND				CLPST				50
21	NMGAIN				WPGAIN			Agcgain8	22
22	AGCGAIN[7:0]								F0
23	PEAKWT								F8
24	CLMPLD	CLMPL							BC
25	SYNCTD	SYNCT							B8
26	MISSCNT				HSWIN				44
27	PCLAMP								38
28	VLCKI		VLCKO		VMODE	DETV	AFLD	VINT	00
29	BSHT			VSHT					00
2A	CKILMAX		CKILMIN						78
2B	HTL				VTL				44
2C	CKLM	YDLY			EVCNT	HFLT			30
2D	-	-	PALC	SDET	TBC_EN	BYPASS	SYOUT	HADV	14
2E	HPM		ACCT		SPM		CBW		A5
2F	NKILL	PKILL	SKILL	CBAL	FCS	LCS	CCS	BST	E0
30	sf	pf	ff	kf	CSBAD	MCVSN	CSTRIPE	CTYPE	00
31	VCR	WKAIR	WKAIR1	VSTD	NINTL	WSSDET	EDSDET	CCDET	00
32	HFREF								x
33	FRM		YNR		CLMD		PSP		05
34	IDX		NSEN / SSEN / PSEN / WKTH						1A
35	CTEST	YCLEN	CCLEN	VCLEN	GTEST	VLPF	CKLY	CKLC	00
36	-								
37	-								
38	-								
39	-								
3A	-								
3B	-								
3C	-								
3D	-								
3E	-								
3F	-								
40	ACKI[7:0]								64
41	ACKI[15:8]								85
42	-		ACKI[21:16]						35
43	ACKN[7:0]								BC
44	ACKN[15:8]								DF
45							ACKN[17:16]		02
46	-		SDIV						01
47	-		LRDIV						20
48	-	APZ	APG		-	ACPL	SRPH	LRPH	60
4E	HBLEN								8A
4F			WSS[19:14]						X
50	FILLDATA								A0

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
51	NODAEN	SYRM	SDID						22
52	ANCEN	YCBCR422	VIPCFG	DID					31
53	CRCERR	WSSFLD	WSS[13:8]						X
54	WSS[7:0]								X
55	HA656	EAVSWAP	HAMM84	NTSC656	VVBI				00
56	LCTL6								00
57	LCTL7								00
58	LCTL8								00
59	LCTL9								00
5A	LCTL10								00
5B	LCTL11								00
5C	LCTL12								00
5D	LCTL13								00
5E	LCTL14								00
5F	LCTL15								00
60	LCTL16								00
61	LCTL17								00
62	LCTL18								00
63	LCTL19								00
64	LCTL20								00
65	LCTL21								00
66	LCTL22								00
67	LCTL23								00
68	LCTL24								00
69	LCTL25								00
6A	LCTL26								00
6B	HSBEGIN								2C
6C	HSEND								60
6D	OVSDLY								00
6E	HSPIN	OFDLY			VSMODE	OVSEND			20
6F	PDNSVBI	HASYNC	VBIDELAY						24

Encoder

70	SYS5060	INTERLACE	FSC		-	PHALT	ALTRST	PED	40
71	ENC_IN_ORDER		ENC_VS	ENC_FLD	HSPOL	VSPOL	FLDPOL	ENC_CK	20
72	ENC_VSOFF		ENC_VSDEL						10
73	ENC_HSDEL								45
74	ENC_YBW		ENC_CBW		ENC_BAR	ENC_TCSEL			F0
75	CKILL	DAC_OUT	TEST_MODE						30
76	DBL	ENC_LOOP	ENC_PD	DAC_PD0	DAC_PD1	DAC_PD2	DAC_PD3	DAC_PD4	00
77	DAC_IREF0				DAC_IREF1				FF
78	DAC_IREF2				DAC_IREF3				FF
79	-	-	NONSTA	FRUN	DAC_IREF4				0F
7A	-	-	-	ENC_YDEL					0F
7B	ENC_SYNC_L				ENC_BLK_L				25
7C	ENC_YBRT								00
7D	-	-	-	ENC_CBURST_L					00

0x00 – Product ID Code Register (ID)

Bit	Function	R/W	Description	Reset
7-3	ID	R	The TW9920 Product ID code is 00111.	7
2-0	Revision	R	The revision number.	2

0x01 – Chip Status Register I (STATUS1)

Bit	Function	R/W	Description	Reset
7	VDLOSS	R	1 = Video not present. (sync is not detected in number of consecutive line periods specified by Misscnt register) 0 = Video detected.	0
6	HLOCK	R	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	0
5	SLOCK	R	1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked.	0
4	FIELD	R	0 = Odd field is being decoded. 1 = Even field is being decoded.	0
3	VLOCK	R	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	0
2			Reserved	0
1	MONO	R	1 = No color burst signal detected. 0 = Color burst signal detected.	0
0	DET50	R	0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked.	0

0x02 – Input Format (INFORM)

Bit	Function	R/W	Description	Reset
7	YSEL2	R/W	See YSEL	0
6	FC27	R/W	1 = Input crystal clock frequency is 27MHz. 0 = Square pixel mode. Must use 24.54MHz for 60Hz field rate source or 29.5MHz for 50Hz field rate source.	1
5-4	IFSEL	R/W	01 = S-video decoding 00 = Composite video decoding	0
3-2	YSEL	R/W	YSEL2 together with these two bits control the Y input video selection. 000 = Mux0 selected 001 = Mux1 selected 010 = Mux2 selected 011 = Mux3 selected 100-111 = Invalid	0
1	CSEL	R/W	This bit selects the chroma channel input. 0 = CIN0 1 = CIN1	0
0		R/W	Reserved	0

0x03 – Output Format Control Register (OPFORM)

Bit	Function	R/W	Description	Reset
7	MODE	R/W	0 = CCIR601 compatible YCrCb 4:2:2 format with separate syncs and flags. 1 = ITU-R-656 compatible data sequence format.	0
6	LEN	R/W	0 = 8/10-bit YCrCb 4:2:2 output format. 1 = 16/20-bit YCrCb 4:2:2 output format.	0
5	LLCMODE	R/W	1 = LLC output mode. 0 = free-run output mode	0
4	AINC	R/W	Serial interface indexing control 0 = auto-increment 1 = non-auto	0
3	VSCTL	R/W	1 = Vertical scale-downed output controlled by DVALID only. 0 = Vertical scale-downed output controlled by both HACTIVE and DVALID.	0
2	OEN	R/W	0 = Enable outputs. 1 = Tri-state outputs defined by Tri-state select bits of this register.	1
1-0	TRI_SEL	R/W	These bits select the outputs to be tri-stated when the OEN bit is asserted high. There are three major groups that can be independently tri-stated: timing group (HS, VS, DVALID, MPOUT, FLD), data group (VD[19:0]), and clock group (CLKX1, CLKX2) according to following definition. 00 = Timing and data group only. 01 = Data group only. 10 = All three groups. 11 = Clock and data group only.	0

0x04 – GAMMA and HSYNC Delay Control

Bit	Function	R/W	Description	Reset
7	GMEN	R/W	Reserved for test	0
6-5	CKHY	R/W	Color killer hytheresis 0 – fastest 1 – fast 2 – medium 3 - slow	0
4-0	HSDLY	RW	Reserved for test.	0

0x05 – Output Control I

Bit	Function	R/W	Description	Reset
7	VSP	R/W	0 = VS pin output polarity is active high 1 = VS pin output polarity is active low.	0
6-4	VSSL	R/W	VS pin output control 0 = VSYNC 1 = VACT 2 = HACT 3 = VVALID 4 - 7 = Reserved	0
3	HSP	R/W	0 = HS pin output polarity is active high 1 = HS pin output polarity is active low.	0
2-0	HSSL	R/W	HS pin output control 0 = HACT 1 = HSYNC 2 = VSYNC 3 = Hlock 4 – 7 = Reserved	0

0x06 – Analog Control Register (ACNTL)

Bit	Function	R/W	Description	Reset
7	SRESET	W	An 1 written to this bit resets the device to its default state but all register content remain unchanged. This bit is self-resetting.	0
6	IREF	R/W	0 = Internal current reference 1. 1 = Internal current reference 2.	0
5	VREF	R/W	1 = Internal voltage reference. 0 = external voltage reference using VCOM, VREFP and VREFN.	0
4	AGC_EN	R/W	0 = AGC loop function enabled. 1 = AGC loop function disabled. Gain is set to by AGCGAIN.	0
3	CLK_PDN	R/W	0 = Normal clock operation. 1 = System clock in power down mode, but the MPU INTERFACE module and output clocks (CLKX1 and CLKX2) are still active.	0
2	Y_PDN	R/W	0 = Luma ADC in normal operation. 1 = Luma ADC in power down mode.	0
1	C_PDN	R/W	0 = Chroma ADC in normal operation. 1 = Chroma ADC in power down mode.	0
0		R/W	Reserved for future use	0

0x07 – Cropping Register, High (CROP_HI)

Bit	Function	R/W	Description	Reset
7-6	VDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Vertical Delay register.	0
5-4	VACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit VACTIVE register. Refer to description on Reg09 for its shadow register.	0
3-2	HDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Horizontal Delay register.	0
1-0	HACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit HACTIVE register.	2

0x08 – Vertical Delay Register, Low (VDELAY_LO)

Bit	Function	R/W	Description	Reset
7-0	VDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Delay register. The two MSBs are in the CROP_HI register. It defines the number of lines between the leading edge of VSYNC and the start of the active video.	12

0x09 – Vertical Active Register, Low (VACTIVE_LO)

Bit	Function	R/W	Description	Reset
7-0	VACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Active register. The two MSBs are in the CROP_HI register. It defines the number of active video lines per frame output. The VACTIVE register has a shadow register for use with 50Hz source when Atreg of Reg0x1C is not set. This register can be accessed through the same index address by first changing the format standard to any 50Hz standard.	F0

0x0A – Horizontal Delay Register, Low (HDELAY_LO)

Bit	Function	R/W	Description	Reset
7-0	HDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Delay register. The two MSBs are in the CROP_HI register. It defines the number of pixels between the leading edge of the HSYNC and the start of the image cropping for active video. The HDELAY_LO register has two shadow registers for use with PAL and SECAM sources respectively. These register can be accessed using the same index address by first changing the decoding format to the corresponding standard.	0F

0x0B – Horizontal Active Register, Low (HACTIVE_LO)

Bit	Function	R/W	Description	Reset
7-0	HACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Active register. The two MSBs are in the CROP_HI register. It defines the number of active pixels per line output.	D0

0x0C – Control Register I (CNTRL1)

Bit	Function	R/W	Description	Reset
7	PBW	R/W	1 = Wide Chroma BPF BW 0 = Normal Chroma BPF BW	1
6	DEM	R/W	Secam control 1 = reduction 0 = normal	1
5	PALSW	R/W	1 = PAL switch sensitivity low. 0 = PAL switch sensitivity normal.	0
4	SET7	R/W	1 = The black level is 7.5 IRE above the blank level. 0 = The black level is the same as the blank level.	0
3	COMB	R/W	1 = Adaptive comb filter on for NTSC 0 = Notch filter	1
2	HCOMP	R/W	1 = operation mode 1. (recommended) 0 = mode 0.	1
1	YCOMB	R/W	This bit controls the Y comb. 1 = Y output is the averaging of two adjacent lines. 0 = No comb.	0
0	PDLY	R/W	PAL delay line. 1 = enabled. 0 = disabled.	0

0x0D – Vertical Scaling Register, Low (VSCALE_LO)

Bit	Function	R/W	Description	Reset
7-0	VSCALE_LO	R/W	These bits are bit 7 to 0 of the 12-bit vertical scaling ratio register	00h

0x0E – Scaling Register, High (SCALE_HI)

Bit	Function	R/W	Description	Reset
7-4	VSCALE_HI	R/W	These bits are bit 11 to 8 of the 12-bit vertical scaling ratio register.	1
3-0	HSCALE_HI	R/W	These bits are bit 11 to 8 of the 12-bit horizontal scaling ratio register.	1

0x0F – Horizontal Scaling Register, Low (HSCALE_LO)

Bit	Function	R/W	Description	Reset
7-0	HSCALE_ LO	R/W	These bits are bit 7 to 0 of the 12-bit horizontal scaling ratio register.	00

0x10 – BRIGHTNESS Control Register (BRIGHT)

Bit	Function	R/W	Description	Reset
7-0	BRIGHT	R/W	These bits control the brightness. They have value of –128 to 127 in 2's complement form. Positive value increases brightness. A value 0 has no effect on the data.	00

0x11 – CONTRAST Control Register (CONTRAST)

Bit	Function	R/W	Description	Reset
7-0	CNTRST	R/W	These bits control the contrast. They have value of 0 to 3.98 (FFh). A value of 1 ('100_0000') has no effect on the video data.	5C

0x12 – SHARPNESS Control Register I (SHARPNESS)

Bit	Function	R/W	Description	Reset
7	SCURVE	R/W	This bit controls the sharpness filter center frequency. 0 = Normal 1 = High	0
6	VSF	R/W	This bit is for internal used.	1
5-4	CTI	R/W	CTI level selection. 0 = lowest. 3 = hightest.	1
3-0	SHARP	R/W	These bits control the amount of sharpness enhancement on the luminance signals. There are 16 levels of control with '0' having no effect on the output image. 1 through 7 provides sharpness enhancement with '7' being the strongest. Value 8 through 15 are provided for noise reduction purpose.	1

0x13 – Chroma (U) Gain Register (SAT_U)

Bit	Function	R/W	Description	Reset
7-0	SAT_U	R/W	These bits control the digital gain adjustment to the U (or Cb) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80

0x14 – Chroma (V) Gain Register (SAT_V)

Bit	Function	R/W	Description	Reset
7-0	SAT_V	R/W	These bits control the digital gain adjustment to the V (or Cr) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80

0x15 – Hue Control Register (HUE)

Bit	Function	R/W	Description	Reset
7-0	HUE	R/W	These bits control the color hue as 2's complement number. They have value from +36^o (7Fh) to -36^o (80h) with an increment of 0.28^o. The positive value gives greenish tone and negative value gives purplish tone. The default value is 0^o (00h). This is effective only on NTSC system.	00

0x16 – Sharpness Control II (SHARP2)

Bit	Function	R/W	Description	Reset
7-4		R/W	Reserved for future use.	5
3-0		R/W	Reserved for future use.	3

0x17 – Vertical Sharpness (VSHARP)

Bit	Function	R/W	Description	Reset
7-4	SHCOR	R/W	These bits provide coring function for the sharpness control.	8
3			Reserved	0
2-0	VSHP	R/W	Vertical peaking level. 0 = none. 7 = highest.	0

0x18 – Coring Control Register (CORING)

Bit	Function	R/W	Description	Reset
7-6	CTCOR	R/W	These bits control the coring for CTI.	1
5-4	CCOR	R/W	These bits control the low level coring function for the Cb/Cr output.	0
3-2	VCOR	R/W	These bits control the coring function of vertical peaking.	1
1-0	CIF	R/W	These bits control the IF compensation level. 0 = None 1 = 1.5dB 2 = 3dB 3 = 6dB	0

0x19 – VBI Control Register (VBICNTL)

Bit	Function	R/W	Description	Reset
7	VBI_EN	R/W	0 = VBI capture disabled. 1 = VBI capture enabled.	0
6	VBI Byte Order	R/W	If LEN(Reg0x03[6]) is "1" 0 = Pixel 1, 3, 5 … on the VD[19:12] data bus, and pixel 2, 4, 6, … on the VD[9:2] data bus. 1 = Pixel 1, 3, 5, … on the VD[9:2] data bus, and pixel 2, 4, 6, … on the VD[19:12] data bus. If LEN is "0" 0 = Pixel 2,1,4,3,6,5,…. on the VD[19:12] data bus. 1 = Pixel 1,2,3,4,5,6,…. on the VD[19:12] data bus.	1
5	VBI_ FRAM	R/W	0 = Normal mode 1 = ADC output mode VD[19:12] is Y-ADC data,VD[9:0] pin is C-YADC data	0
4	HA_EN	R/W	0 = HACTIVE output is disabled during vertical blanking period. 1 = HACTIVE output is enabled during vertical blanking period.	1
3	CNTL656	R/W	0 = 0x80 and 0x10 code will be output as invalid data during active video line. 1 = 0x00 code will be output as invalid data during active video line.	1
2-0	RTSEL	R/W	These bits control the real time signal output from the MPOUT pin. 000 = Video loss 001 = H-lock 010 = S-lock 011 = V-lock 100 = MONO 101 = Det50 110 = LVALID 111 = RTCO	0

0x1A – Analog Control II

Bit	Function	R/W	Description	Reset
7	LLCTEST	R/W	LLC test mode	0
6	PLL_PDN	R/W	0 = LLC PLL in normal operation. 1 = PLL in power down mode.	0
5-4			Reserved	0
3	YFLEN	R/W	Y-Ch anti-alias filter control 1 = enable 0 = disable	0
2	YSV	R/W	Y-Ch power saving mode 1 = enable 0 = disable	0
1	CFLEN	R/W	C-Ch anti-alias filter control 1 = enable 0 = disable	0
0	CSV	R/W	C-Ch power saving mode 1 = enable 0 = disable	0

0x1B – Output Control II

Bit	Function	R/W	Description	Reset
7-6	CK2S	R/W	CLKX2 pin output control 0 = CLKX2 1 = VCLK 2 = LLCK 3 = LLCK2	1
5-4	CK1S	R/W	CLKX1 pin output control 0 = VCLK 1 = CLKX1 2 = LLCK 3 = LLCK4	1
3	FLP	R/W	0 = FLD pin output polarity is active high 1 = FLD pin output polarity is active low.	0

2-0	FLSL	R/W	FLD pin output control 0 = FLD 1 = Vlock 2 = Slock 3 = Vdloss 4 – 7 = Reserved	0

0x1C – Standard Selection (SDT)

Bit	Function	R/W	Description	Reset
7	DETSTUS	R	0 = Idle 1 = detection in progress	0
6-4	STDNOW	R	Current standard invoked 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Not valid	0
3	ATREG	R/W	1 = Disable the shadow registers. 0 = Enable VACTIVE and HDELAY shadow registers value depending on standard	0
2-0	STD	R/W	Standard selection 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Auto detection	7

0x1D – Standard Recognition (SDTR)

Bit	Function	R/W	Description	Reset
7	ATSTART	R/W	Writing 1 to this bit will manually initiate the auto format detection process. This bit is a self-resetting bit.	0
6	PAL6_EN	R/W	1 = enable recognition of PAL60. 0 = disable recognition.	1
5	PALN_EN	R/W	1 = enable recognition of PAL (CN). 0 = disable recognition.	1
4	PALM_EN	R/W	1 = enable recognition of PAL (M). 0 = disable recognition.	1
3	NT44_EN	R/W	1 = enable recognition of NTSC 4.43. 0 = disable recognition.	1
2	SEC_EN	R/W	1 = enable recognition of SECAM. 0 = disable recognition.	1
1	PALB_EN	R/W	1 = enable recognition of PAL (B,D,G,H,I). 0 = disable recognition.	1
0	NTSC_EN	R/W	1 = enable recognition of NTSC (M). 0 = disable recognition.	1

0x1E – Component Video Format (CVFMT)

Bit	Function	R/W	Description	Reset
7		R	Reserved	0
6-4	CVSTD	R	Component video input format detection. 0 = 480i, 1 = 576i, 2 = 480p, 3 = 576p	0
3-0	CVFMT	R/W	Component video format selection. 0 = 480i, 1 = 576i, 2 = 480p, 3 = 576p, 8 = Auto	8

0x1F – Test Control Register (TEST)

Bit	Function	R/W	Description	Reset
7-0	TEST	R/W	This register is reserved for testing purpose. In normal operation, only 0 should be written into this register. 1 = Analog test mode. Y and C channel portion of the device can be tested in this mode. The Y channel ADC output can be obtained from VD[19-10]. The C channel ADC output can be obtained from VD[9-0]. 2 = Clamp test mode. Clamp control YU, YUX, YD, YDX, CU, CUX, CD, and CDX are mapped to PD[7-0]. 3 = Reserved 4 = Digital test mode1. This is the CVBS test mode. The 9-bit input corresponds to PD[9-1] in the order of bit 8 to 0. 5 = Digital test mode 2. This is the Y/C test mode. Y input is defined by test mode 1. The C channel data is inputted from VD[9-1]. In this mode, only 8/10-bit output format is allowed. 6 = Digital test mode 3. Encoder output test mode. The 20-bit Encoder output corresponds to VD[19-0]. 7 = Digital test mode 4. Encoder in-out test mode. In this mode. 9-bit data inputted from PD[9-1] to decoder. 20-bit Encoder output corresponds to VD[19-0]. 8 = Reserved 9 = Sync output mode. The 6-bit Sync output corresponds to VD[5-0] in the order of bit 5 to 0. Y and Cb/Cr outputs correspond to VD[19-10] in 422 format A = DAC test mode. In this mode, the 10-bit DAC input corresponds to PD[9:0] bus.	0

0x20 – Clamping Gain (CLMPG)

Bit	Function	R/W	Description	Reset
7-4	CLPEND	R/W	These 4 bits set the end time of the clamping pulse in the increment of 8 system clocks. The clamping time is determined by this together with CLPST.	5
3-0	CLPST	R/W	These 4 bits set the start time of the clamping pulse in the increment of 8 system clocks. It is referenced to PCLAMP position.	0

0x21 – Individual AGC Gain (IAGC)

Bit	Function	R/W	Description	Reset
7-4	NMGAIN	R/W	These bits control the normal AGC loop maximum correction value.	2
3-1	WPGAIN	R/W	Peak AGC loop gain control.	1
0	AGCGAIN 8	R/W	This bit is the MSB of the 9-bit register that controls the AGC gain when AGC loop is disabled.	0

0x22 – AGC Gain (AGCGAIN)

Bit	Function	R/W	Description	Reset
7-0	AGCGAIN	R/W	These bits are the lower 8 bits of the 9-bit register that controls the AGC gain when AGC loop is disabled.	F0

0x23 – White Peak Threshold (PEAKWT)

Bit	Function	R/W	Description	Reset
7-0	PEAKWT	R/W	These bits control the white peak detection threshold. This function can be disabled by setting 'FF'.	F8

0x24– Clamp level (CLMPL)

Bit	Function	R/W	Description	Reset
7	CLMPLD	R/W	0 = Clamping level is set by CLMPL. 1 = Clamping level preset at 60d.	1
6-0	CLMPL	R/W	These bits determine the clamping level of the Y channel.	3C

0x25– Sync Amplitude (SYNCT)

Bit	Function	R/W	Description	Reset
7	SYNCTD	R/W	0 = Reference sync amplitude is set by SYNCT. 1 = Reference sync amplitude is preset to 38h.	1
6-0	SYNCT	R/W	These bits determine the standard sync pulse amplitude for AGC reference.	38

0x26 – Sync Miss Count Register (MISSCNT)

Bit	Function	R/W	Description	Reset
7-4	MISSCNT	R/W	MISSCNT[3] controls the speed of VDLOSS detection with '0' being fast and '1' being slow. MISSCNT[2:0] control the threshold of horizontal sync miss detection per field.	4
3-0	HSWIN	R/W	These bits determine the VCR mode Hsync detection window.	4

0x27 – Clamp Position Register (PCLAMP)

Bit	Function	R/W	Description	Reset
7-0	PCLAMP	R/W	These bits set the clamping position from the PLL sync edge	38

0x28 – Vertical Control I (VCNTL1)

Bit	Function	R/W	Description	Reset
7-6	VLCKI	R/W	Vertical lock in time. 0 = fastest 3 = slowest.	0
5-4	VLCKO	R/W	Vertical lock out time. 0 = fastest 3 = slowest.	0
3	VMODE	R/W	This bit controls the vertical detection window. 1 = search mode. 0 = vertical count down mode.	0
2	DETV	R/W	1 = recommended for special application only. 0 = Normal Vsync logic	0
1	AFLD	R/W	Auto field generation control 0 = Off 1 = On	0
0	VINT	R/W	Vertical integration time control. 1 = long 0 = normal	0

0x29 – Vertical Control II (VCNTL2)

Bit	Function	R/W	Description	Reset
7-5	BSHT	R/W	Burst PLL center frequency control.	0
5-0	VSHT	R/W	Vsync output delay control in the increment of half line length.	00

0x2A – Color Killer Level Control (CKILL)

Bit	Function	R/W	Description	Reset
7-6	CKILMAX	R/W	These bits control the amount of color killer hysteresis. The hysteresis amount is proportional to the value.	1
5-0	CKILMIN	R/W	These bits control the color killer threshold. Larger value gives lower killer level.	28

0x2B – Comb Filter Control (COMB)

Bit	Function	R/W	Description	Reset
7-4	HTL	R/W	Adaptive Comb filter control.	4
3-0	VTL	R/W	Adaptive Comb filter combing strength control. Higher value provides stronger comb filtering.	4

0x2C – Luma Delay and H Filter Control (LDLY)

Bit	Function	R/W	Description	Reset
7	CKLM	R/W	Color Killer mode. 0 = normal 1 = fast (for special application)	0
6-4	YDLY	R/W	Luma delay fine adjustment. This 2's complement number provide –4 to +3 unit delay control.	3
3	EVCNT	R/W	1 = Even field counter in special mode. 0 = Normal operation	0
2-0	HFLT	R/W	Pre-filter selection for horizontal scaler 1** = Bypass 000 = Auto selection based on Horizontal scaling ratio. 001 = Recommended for CIF size image 010 = Recommended for QCIF size image 011 = Recommended for ICON size image	0

0x2D – Miscellaneous Control I (MISC1)

Bit	Function	R/W	Description	Reset
7-6		R/W	Reserved for future use.	0
5	PALC	R/W	Reserved for future use.	0
4	SDET	R/W	ID detection sensitivity. A '1' is recommended.	1
3	TBC_EN	R/W	1:TBC enable in freerun clock mode. 0:Disable	0
2	BYPASS	R/W	It controls the standard detection and should be set to '1' in normal use.	1
1	SYOUT	R/W	1 = Hsync output is disabled when video loss is detected 0 = Hsync output is always enabled	0
0	HADV	R/W	This bit advances the HACTIVE and DVALID pin output by one data clock when set.	0

0x2E – LOOP Control Register (LOOP)

Bit	Function	R/W	Description	Reset
7-6	HPM	R/W	Horizontal PLL acquisition time. 3 = Fast 2 = Auto1 1 = Auto2 0 = Slow	2
5-4	ACCT	R/W	ACC time constant 0 = No ACC 1 = slow 2 = medium 3 = fast	2
3-2	SPM	R/W	Burst PLL control. 0 = Slowest 1 = Slow 2 = Fast 3 = Fastest	1
1-0	CBW	R/W	Chroma low pass filter bandwidth control. Refer to filter curves.	1

0x2F – Miscellaneous Control II (MISC2)

Bit	Function	R/W	Description	Reset
7	NKILL	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL	R/W	0 = Normal output 1 = special output mode.	0
3	FCS	R/W	1 = Force decoder output value determined by CCS. 0 = Disabled.	0
2	LCS	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled.	0
1	CCS	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0x30 – Macrovision Detection (MVSN)

Bit	Function	R/W	Description	Reset
7	SF	R		0
6	PF	R		0
5	FF	R		0
4	KF	R		0
3	CSBAD	R	1 = Macrovision color stripe detection may be un-reliable	0
2	MCVSN	R	1 = Macrovision AGC pulse detected. 0 = Not detected.	0
1	CSTRIPE	R	1 = Macrovision color stripe protection burst detected. 0 = Not detected.	0
0	CTYPE	R	This bit is valid only when color stripe protection is detected, i.e. Cstripe=1. 1 = Type 2 color stripe protection 0 = Type 3 color stripe protection	0

0x31 – Chip STATUS II (STATUS2)

Bit	Function	R/W	Description	Reset
7	VCR	R	VCR signal indicator	0
6	WKAIR	R	Weak signal indicator 2.	0
5	WKAIR1	R	Weak signal indicator controlled by WKTH.	0
4	VSTD	R	1 = Standard signal 0 = Non-standard signal	0
3	NINTL	R	1 = Non-interlaced signal 0 = interlaced signal	0
2	WSSDET	R	1 = WSS data detected. 0 = Not detected.	0
1	EDSDET	R	1 = EDS data detected. 0 = Not detected.	0
0	CCDET	R	1 = CC data detected. 0 = Not detected.	0

0x32 – H monitor (HFREF)

Bit	Function	R/W	Description	Reset
7-0	HFREF	R	Horizontal line frequency indicator	X

0x33 – CLAMP MODE (CLMD)

Bit	Function	R/W	Description	Reset
7-6	FRM	R/W	Free run mode control 0 = Auto 2 = default to 60Hz 3 = default to 50Hz	0
5-4	YNR	R/W	Y HF noise reduction 0 = None 1 = smallest 2 = small 3 = medium	0
3-2	CLMD	R/W	Clamping mode control. 0 = Sync top 1 = Auto 2 = Pedestal 3 = N/A	1
1-0	PSP	R/W	Slice level control 0 = low 1 = medium 2 = high	1

0x34 – ID Detection Control (IDCNTL)

Bit	Function	R/W	Description	Reset
7-6	IDX	R/W	These two bits indicates which of the four lower 6-bit registers is currently be controlled. The write sequence is a two steps process unless the same register is written. A write of {ID,000000} selects one of the four registers to be written. A subsequent write will actually write into the register.	0
5-0	NSEN / SSEN / PSEN / WKTH	R/W	IDX = 0 controls the NTSC ID detection sensitivity (NSEN). IDX = 1 controls the SECAM ID detection sensitivity (SSEN). IDX = 2 controls the PAL ID detection sensitivity (PSEN). IDX = 3 controls the weak signal detection sensitivity (WKTH).	1A / 20 / 1C / 11

0x35 – Clamp Control I (CLCNTL1)

Bit	Function	R/W	Description	Reset
7	CTEST	R/W	Clamping control for debugging use.	0
6	YCLEN	R/W	1 = Y channel clamp disabled 0 = Enabled.	0
5	CCLEN	R/W	1 = C channel clamp disabled 0 = Enabled.	0
4	VCLEN	R/W	Reserved	0
3	GTEST	R/W	1 = Test. 0 = Normal operation.	0
2	VLPF	R/W	Sync filter control.	0
1	CKLY	R/W	Clamping current control 1.	0
0	CKLC	R/W	Clamping current control 2.	0

0x40 – 0x48 AUDIO CLOCK

0x40 – Audio Clock Increment (ACKI)

Bit	Function	R/W	Description	Reset
7-0	ACKI	RW	Bit 7-0 of ACKI	64

0x41 – Audio Clock Increment (ACKI)

Bit	Function	R/W	Description	Reset
7-0	ACKI	RW	Bit 15-8 of ACKI	85

0x42 – Audio Clock Increment (ACKI)

Bit	Function	R/W	Description	Reset
5-0	ACKI	RW	Bit 21-16 of ACKI	35

0x43 – Audio Clock Number (ACKN)

Bit	Function	R/W	Description	Reset
7-0	ACKN	RW	Bit 7-0 of Audio clock number per field	BC

0x44 – Audio Clock Number (ACKN)

Bit	Function	R/W	Description	Reset
7-0	ACKN	RW	Bit 15-8 of ACKN	DF

0x45 – Audio Clock Number (ACKN)

Bit	Function	R/W	Description	Reset
1-0	ACKN	RW	Bit 17-16 of ACKN	2

0x46 – Serial Clock Divider (SDIV)

Bit	Function	R/W	Description	Reset
5-0	SDIV	RW	Serial Clock divider	01

0x47 – Left/Right Clock Divider (LRDIV)

Bit	Function	R/W	Description	Reset
5-0	LRDIV	RW	Left/Right Clock divider	20

0x48 – Audio Clock Control (ACCNTL)

Bit	Function	R/W	Description	Reset
6	APZ	RW	Loop control	1
5-4	APG	RW	Loop control	2
2	ACPL	RW	0 = Loop closed 1 = Loop open	0
1	SPH	RW	ASCLK divider trigger phase	0
0	LRPH	RW	ALRCLK divider trigger phase	0

0x4E – HBLEN

Bit	Function	R/W	Description	Reset
7-0	HBLEN	R/W	These bits are effective when HASYNC bit is set to 1.These bits set up the length of EAV to SAV code when HASYNC bit is 1.	8A

0x4F – WSS3

Bit	Function	R/W	Description	Reset
7-0	WSS[19:14]	R	CGMS(WSS525) Bit19-14 in 525 line video system.These bits show CRC 6bits in CGMS(WSS525). These bits are only valid in 525 line video system.	X

0x50 – FILLDATA

Bit	Function	R/W	Description	Reset
7-0	FILLDATA	R/W	Filled data as dummy data in ANC Dword data packet.	A0

0x51 – SDID

Bit	Function	R/W	Description	Reset
7	NODAEN	R/W	1:Bit7 in 4th byte of EAV/SAV code will be 0 when sync lost(No Video input.) 0: Bit7 in 4th byte of EAV/SAV is always VIPCFG register bit.	0
6	SYRM	R/W	1: Minimum value in raw VBI will be 0x10 for Sync Level remove. 0:none.	0
5-0	SDID	R/W	Secondary data ID in ANC data packet type 2	22

0x52 – DID

Bit	Function	R/W	Description	Reset
7	ANCEN	R/W	1:ANC data packet output enable. 0:disable.	0
6	YCBCR422	R/W	1: Average process YCbCr 4:2:2 output 0:Normal process YCbCr 4:2:2 output	0
5	VIPCFG	R/W	Set up Bit7 in 4th byte of EAV/SAV code.	1
4-0	DID	R/W	Data ID in ANC data packet type 2.	11

0x53 – WSS1

Bit	Function	R/W	Description	Reset
7	CRCERR	R	This bit is only valid in 525 line video system. 1:CGMS(WSS525) CRC error detected in current field. 0:No CRC error	X
6	WSSFLD	R	0:current WSS data is received in Oddfield. 1: current WSS data is received in Even field.	X
5-0	WSS[13:8]	R	CGMS(WSS525) Bit13-8 in 525 line video system. Wide Screen Signaling Bit13-8 in 625 line video system.	X

0x54 – WSS2

Bit	Function	R/W	Description	Reset
7-0	WSS[7:8]	R	CGMS(WSS525) Bit7-0 in 525 line video system. Wide Screen Signaling Bit7-0 in 625 line video system.	X

0x55 – VVBI

Bit	Function	R/W	Description	Reset
7	HA656	R/W	1:HACTIVE signal is same as DVALID signal in H Down scaled video output. 0:HACTIVE signal is always HACTIVE register's length.	0
6	EAVSWAP	R/W	1:EAV-SAV code is swapped. 0:EAV-SAV code is not swapped(standard 656 output mode)	0
5	HAMM84	R/W	1:enable 84 Hamming Code checking BI Slicer.0: disable.	0
4	NTSC656	R/W	1:Number of Even Field Video output line is (the number of Odd field Video output line – 1). This bit is required for ITU-R BT.656 output for 525 line system standard. 0: Number of Even Field Video output line is same as the number of Odd field Video output line.	0
3-0	VVBI	R/W	The number of raw VBI data output line counted from top video active line signal timing.	0

0x56~6A LCTL6~LCTL26

Bit	Function	R/W	Description	Reset
7-4	LCTLn	R/W	Set up VBI Data Slicer Decoding mode on Line-n. Value is set up by upper bit7-4 meaning for Line-n in odd field.	0
3-0		R/W	Value is set up by below bit3-0 meaning for Line-n in even field. 0h:disable decoding. 1h:Teletext-B 2h:Teletext-C 3h:Teletext-D 4h:Closed Captioning and Extended Data service. (EIA-608 type). 5h:CGMS (WSS525) in 525 line system or WSS625 in 625 line system. 6h:VITC 7h:Gemstar 1x 8h:Gemstar 2x 9h:VPS (Line16 VPS type) Ah: Teletext-A Bh~Fh: reserved	0

0x6B – HSGEGIN

Bit	Function	R/W	Description	Reset
7-0	HSBEGIN	R/W	HSYNC Start position.	2C

0x6C – HSEND

Bit	Function	R/W	Description	Reset
7-0	HSEND	R/W	HSYNC End position.	60

0x6D – OVSDLY

Bit	Function	R/W	Description	Reset
7-0	OVSDLY	R/W	VSYNC Start position.	00

0x6E – OVSEND

Bit	Function	R/W	Description	Reset
7	HSPIN	R/W	1:HSYNC output is HACTIVE. 0:HSYNC output is HSYNC.	0
6-4	OFDLY	R/W	FIELD output delay. 0h:0H line delay FIELD output. (601 mode only) 1h-6h: 1H-6H line delay FIELD output. 7h:FIELD output is synchronized to the leading edge of VACTIVE.	2
3	VSMODE	R/W	1:VSYNC output is HACTIVE-VSYNC mode. 0:VSYNC output is HSYNC-VSYNC mode.	0
2-0	OVSEND	R/W	Line delay for VSYNC end position.	0

0x6F – VBIDELAY

Bit	Function	R/W	Description	Reset
7	PDNSVBI	R/W	1:VBI data slicer enable 0: VBI data slicer is in reset and power-down mode	0
6	HASYNC	R/W	1:the length of EAV to SAV is set up and fixed by HBLEN registers. 0:the length of SAV to EAV is set up and fixed by HACTIVE registers.	0
5-0	VBIDELAY	R/W	Raw VBI output delay	24

0x70 – ENCODER CONTROL1

Bit	Function	R/W	Description	Reset
7	SYS5060	R/W	Input/Output Field Rate Selection. 1:50Hz 0:60Hz	0
6	INTERLACE	R/W	Output Scan Format Selection. 1:Interlace 0:Non-Interlace	1
5-4	FSC	R/W	Set color sub-carrier frequency for video encoder. 3: 3.58205625 MHz 2: 3.57561149 MHz 1: 4.43361875 MHz 0: 3.57954545 MHz	0
3		R/W	Reserved for future use.	0
2	PHALT	R/W	Set phase alternation. 1:Enable phase alternation for line-by-line 0:Disable phase alternation for line-by-line	0
1	ALTRST	R/W	Reset phase alternation for every 8 fields 1:Enable phase alternation reset for every 8 fields 0:Disable phase alternation reset for every 8 fields	0
0	PED	R/W	Set 7.5 IRE for pedestal level 1:Enable 7.5 IRE for pedestal level 0:Disable 7.5 IRE for pedestal level	0

0x71 – ENCODER CONTROL2

Bit	Function	R/W	Description	Reset
7-6	ENC_IN_ORDER	R/W	Encoder Digital Video Data Input port order selection. 3:Video Input Data [0:7] 2:Video Input Data [7:0] 1:Video Input Data [2:9] 0:Video Input Data [9:2]	0
5	ENC_VS	R/W	Define vertical sync detection type. 1:Detect vertical sync from combination of HSYNC and FIELD information 0:Detect vertical sync from VSYNC information	1
4	ENC_FLD	R/W	Define field polarity detection type. 1:Detect field polarity from combination of HSYNC and VSYNC information 0:Detect field polarity from FIELD information	0
3	HSPOL	R/W	Control horizontal sync polarity. 1:Active high 0:Active low	0
2	VSPOL	R/W	Control vertical sync polarity. 1:Active high 0:Active low	0
1	FLDPOL	R/W	Control field polarity. 1:Odd field is high 0:Even field is high	0
0	ENC_CK	R/W	Encoder Input Clock polarity Control. 1:Invert PDCLK 0:PDCLK	0

0x72 – ENCODER CONTROL3

Bit	Function	R/W	Description	Reset
7-6	ENC_VSOFF	R/W	Compensate field offset for first active video line. 3:Applied ENC_VSDEL for odd and {ENC_VSDEL+2} for even field 2:Applied ENC_VSDEL for odd and {ENC_VSDEL+1} for even field 1:Applied {ENC_VSDEL+1} for odd and ENC_VSDEL for even field 0:Applied same ENC_VSDEL for odd and even field	0
5-0	ENC_VSDEL	R/W	Control vertical delay of active video line from vertical sync by 1 line/step. 63: 63 Lines delayed : : 0: No delayed	10

0x73 – ENCODER CONTROL4

Bit	Function	R/W	Description	Reset
7-0	ENC_HSDEL	R/W	Control horizontal delay of active video pixel from horizontal sync by 2 pixels/step. 255: 510 pixels delayed : : 0: No delayed	45

0x74 – ENCODER CONTROL5

Bit	Function	R/W	Description	Reset
7-6	ENC_YBW	R/W	Control luminance bandwidth of video encoder. 3:Do not use 2:Wide bandwidth 1:Do not use 0:Narrow bandwidth	3
5-4	ENC_CBW	R/W	Control chrominance bandwidth of video encoder. 3:Do not use 2: 1.35 MHz 1: 1.15 MHz 0: 0.8 MHz	3
3	ENC_BAR	R/W	Enable test pattern output. 1:Internal color bar with 100% amplitude 100% saturation 0:Normal operation	0
2-0	ENC_TCSEL	R/W	Test pattern color selection control. 7:Blue color 6: Red color 5:Magenta color 4:Green color 3:Cyan color 2:Black color 1:White color 0:Color bar	0

0x75 – ENCODER CONTROL6

Bit	Function	R/W	Description	Reset
7	CKILL	R/W	Color killer 1:Color is killed 0:Normal operation	0
6	DAC_OUT	R/W	Define analog video format. 1: S-Video output 0: CVBS output	0
5-0	TEST_MODE	R/W	Encoder TEST Mode control	30

0x76 – ENCODER & DAC Power Down

Bit	Function	R/W	Description	Reset
7	DBL	R/W	Double DAC output current control. 1 : 2 mA / 1 step 0 : 1mA / 1 step	0
6	ENC_LOOP	R/W	Decoder to Encoder loop test mode. 1:Decoder output direct connect to Encoder input for Test purpose 0:Normal Decoder & Encoder operation	0
5	ENC_PD	R/W	Encoder Power Down mode. 1:Encoder Power Down mode ON 0:Encoder Power Down mode OFF	0
4	DAC_PD0	R/W	CVBS/Y Output DAC Power Down mode. 1:DAC0 Power Down mode ON 0:DAC0 Power Down mode OFF	0
3	DAC_PD1	R/W	COUT DAC Power Down mode. 1:DAC1 Power Down mode ON 0:DAC1 Power Down mode OFF	0
2	DAC_PD2	R/W	YOUT DAC Power Down mode. 1:DAC2 Power Down mode ON 0:DAC2 Power Down mode OFF	0
1	DAC_PD3	R/W	CBOUT DAC Power Down mode. 1:DAC3 Power Down mode ON 0:DAC3 Power Down mode OFF	0
0	DAC_PD4	R/W	CROUT DAC Power Down mode. 1:DAC4 Power Down mode ON 0:DAC4 Power Down mode OFF	0

0x77 – DAC Control1

Bit	Function	R/W	Description	Reset
7-4	DAC_IREF0	R/W	CVBS/Y Output DAC IREF control. (1mA or 2mA / 1 step decrease, please see DBL.) 15: 1mA : : 0: Full Scale = 16mA	F
3-0	DAC_IREF1	R/W	COUT DAC IREF control. (1mA or 2mA / 1 step decrease, please see DBL.) 15: 1mA : : 0: Full Scale = 16 mA	F

0x78 – DAC Control12

Bit	Function	R/W	Description	Reset
7-4	DAC_IREF2	R/W	YOUT DAC IREF control. (1mA or 2mA / 1 step decrease, please see DBL.) 15: 1mA : : 0: Full Scale = 16 mA	F
3-0	DAC_IREF3	R/W	CBOUT DAC IREF control . (1mA or 2mA / 1 step decrease, please see DBL.) 15: 1mA : : 0: Full Scale = 16 mA	F

0x79 – DAC Control13

Bit	Function	R/W	Description	Reset
7-6		R/W	Reserved for future use.	0
5	NONSTA	R/W	Horizontal Range Change for Non-standard input (1: Enable)	0
4	FRUN	R/W	Free Run mode for Encoder (1: Free Run Mode)	0
3-0	DAC_IREF4	R/W	CROUT DAC IREF control. (1mA or 2mA / 1 step decrease, please see DBL.) 15: 1mA : : 0: Full Scale = 16 mA	F

0x7a – Encoder YDEL

Bit	Function	R/W	Description	Reset
7-5		R/W	Reserved for future use.	0
4-0	ENC_YDEL	R/W	Encoder Y Output delay control (27MHz 1-clock / step) 31: 16 clocks delayed : : 15: 0 clock delayed : : 0: -15 clocks delayed	0F

0x7b – Encoder SYNC_L & BLK_L

Bit	Function	R/W	Description	Reset
7-4	ENC_SYNC_L	R/W	Encoder DAC Output Sync Level control 15: Sync Level : 10'd181 : : 6: Sync Level : 10'd63 : : 3: Sync Level : 10'd26 2: Sync Level : 10'd11 : : 0: Sync Level : 10'd0	2
3-0	ENC_BLK_L	R/W	Encoder DAC Output Blank Level control 15: Blank Level : 10'd318 : : 5: Blank Level : 10'd240 : : 1: Blank Level : 10'd212 0: Blank Level : 10'd198	5

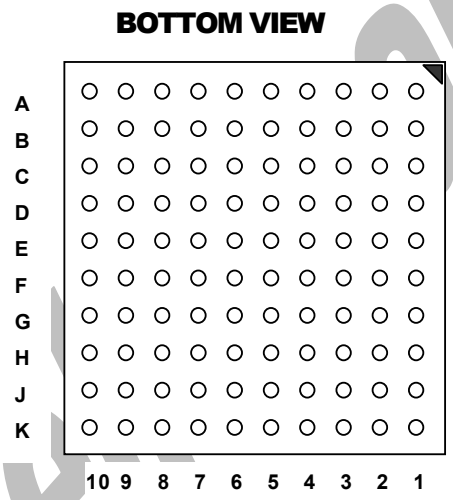
0x7c – Encoder YBRT

Bit	Function	R/W	Description	Reset
7-0	ENC_YBRT	R/W	Encoder Y Data Brightness Control FF: Brightness Control Level : -8'd127 : : 00: Brightness Control Level : 8'd0 : : 7F: Brightness Control Level : +8'd127	00

0x7d – Encoder CBURST

Bit	Function	R/W	Description	Reset
7-5		R/W	Reserved for future use.	0
4-0	ENC_CBURST_L	R/W	Encoder Color Burst Level control (0x70 : Bit2==0 → 1.2% / step) (0x70 : Bit2==1 → 1.25% / step) 0Fh : Increase of Color Burst Level : : 00h : Standard Color Burst Level 10h : Standard Color Burst Level : : 1Fh : Decrease of Color Burst Level	0F

Pin Diagram



Pin Description

Pin#	I/O	Pin Name	Description
Analog video signals			
J8	I	MUX0	Analog CVBS or Y input. Connect used input to AGND through 0.1uF capacitor.
K9	I	MUX1	Analog CVBS or Y input. Connect used input to AGND through 0.1uF capacitor.
K10	I	MUX2	Analog CVBS or Y input. Connect used input to AGND through 0.1uF capacitor.
J10	I	MUX3	Analog CVBS or Y input. Connect used input to AGND through 0.1uF capacitor.
K7	I	CIN0	Analog chroma input. Connect unused input to AGND through 0.1uF capacitor.
K8	I	CIN1	Analog chroma input. Connect unused input to AGND through 0.1uF capacitor.
H9	O	VREFP	The positive reference for the ADC. It should be connected to AVSS through 0.1uF capacitor. NC pin.
H10	O	VREFN	The negative reference for the ADC. It should be connected to AVSS through a 0.1uF capacitor. NC pin.
G9	O	VCOM	The common mode node. It should be connected to analog VSS through a 0.1uF capacitor. NC pin.
J9	I	AVSY	Y signal return.
J7	I	AVSC	C signal return.
Clock Signals			
G1	I	XTI	External clock input
H1	O	XTO	External clock output
Host Interface			
J1	I	SCLK	The MPU Serial interface Clock Line.
H2	I/O	SDAT	The MPU Serial interface Data Line.
J2	I	SIAD0	The MPU interface address select pin 0. This pin is used to select one of the two addresses that chip will respond. It is internally pulled down to ground.
General signals			
G3	I	RSTB	Reset input. Low active.
G2	I	PDN	Power down control pin. It is high active.
K1	I	TMODE	Test pin. It should be low for normal operation.
H3	-	TEST2	NC pin.
C3, C7, H6	-	NC	NC pin.
Video output Signals			
B4	O	HS	Horizontal sync and multi-purpose output pin. See register for control
A3	O	VS	Vertical Sync and multi-purpose output. See register for control information.
B3	O	FLD	Field indicator and multi-purpose output pin. See register for control information.
C4	O	DVALID	Data valid flag and multi-purpose output pin. See register for control information.
A2	O	MPOUT	Multi-purpose output pin.

B2	O	CLKX1	Multi-function clock output pin.
A1	O	CLKX2	Multi-function clock output pin.
B1	O	VD[19]	Digitized Video Data Outputs of Y/YCbCr. VD[10] is the LSB and VD[19] is the MSB.
C2	O	VD[18]	Digitized Video Data Outputs of Y/YCbCr.
D3	O	VD[17]	Digitized Video Data Outputs of Y/YCbCr.
C1	O	VD[16]	Digitized Video Data Outputs of Y/YCbCr.
D2	O	VD[15]	Digitized Video Data Outputs of Y/YCbCr.
D1	O	VD[14]	Digitized Video Data Outputs of Y/YCbCr.
E2	O	VD[13]	Digitized Video Data Outputs of Y/YCbCr.
E1	O	VD[12]	Digitized Video Data Outputs of Y/YcbCr.
F1	O	VD[11]	Digitized Video Data Outputs of Y/YcbCr.
F2	O	VD[10]	Digitized Video Data Outputs of Y/YcbCr.
K2	I/O	VD[9]	Digitized video data output of CbCr. VD[9] is the MSB and VD[0] is the LSB.
J3	I/O	VD[8]	Digitized video data output of CbCr.
H4	I/O	VD[7]	Digitized video data output of CbCr.
K3	I/O	VD[6]	Digitized video data output of CbCr.
J4	I/O	VD[5]	Digitized video data output of CbCr.
K4	I/O	VD[4]	Digitized video data output of CbCr.
J5	I/O	VD[3]	Digitized video data output of CbCr.
K5	I/O	VD[2]	Digitized video data output of CbCr.
K6	I/O	VD[1]	Digitized video data output of CbCr.
J6	I/O	VD[0]	Digitized video data output of CbCr.
Audio Clock Signals			
A4	I	AMXCLK	Audio clock input. It should be connected to AMCLK in normal operation.
A5	O	AMCLK	Field locked audio clock output
B5	O	ASCLK	Audio bit serial clock
A6	O	ALRCLK	Audio frame clock

Encoder

Pin#	I/O	Pin Name	Description
Analog output Signals			
G10	O	CVBS	CVBS/Y output pin. A load resistor is required.
F9	O	COUT	Chroma output pin. A load resistor is required.
F10	O	YOUT	Y output pin. A load resistor is required.
E10	O	CBOUT	Cb output pin. A load resistor is required.
E9	O	CROUT	Cr output pin. A load resistor is required.

Pin#	I/O	Pin Name	Description
D10	I	RSET	DAC current setting resistor pin. NC pin.
Digital Video Input			
C10	I	PD[9]	Encoder data input bus. PD[9] is MSB and PD[0] is LSB.
C9	I	PD[8]	Encoder data input bus
B10	I	PD[7]	Encoder data input bus
B9	I	PD[6]	Encoder data input bus
A10	I	PD[5]	Encoder data input bus
A9	I	PD[4]	Encoder data input bus
B8	I	PD[3]	Encoder data input bus
A8	I	PD[2]	Encoder data input bus
B7	I	PD[1]	Encoder data input bus
A7	I	PD[0]	Encoder data input bus
B6	I	PDCLK	Encoder data input clock.

Power and Ground Pins

Pin#	I/O	Pin Name	Description
E3, G4, G6, C6	I	VDD	2.5V digital core power.
E4, F5, F6, E6, D6	I	VSS	2.5V digital core return
F3, H5, C5. D4	I	VDDE	3.3V digital I/O power.
E5, F4, G5, D5	I	VSSE	3.3V digital I/O return
H7, G8,	I	AVDD	2.5V analog ADC supply
G7, H8	I	AVSS	2.5V analog ADC return
D7, D8	I	AVDDC	2.5V analog DAC supply
E7, D9	I	AVSSC	2.5V analog DAC return
E8, C8	I	AVSSC	2.5V analog DAC return
F8	I	DVDD	2.5V digital ADC and DAC supply
F7	I	DVSS	2.5V digital ADC and DAC return

Parametric Information

AC/DC Electrical Parameters

Table 21. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
AVDD (measured to AVSS)	V_{DDAM}	-	-	2.7	V
V_{DD} (measured to DVSS)	V_{DDM}		-	2.7	V
Voltage on any signal pin (See the note below)	-	DVSS – 0.5	-	V_{DDAM} + 0.5	V
Analog Input Voltage	-	AVSS – 0.5	-	V_{DDM} + 0.5	V
Storage Temperature	T_S	–65	-	+150	°C
Junction Temperature	T_J	-	-	+125	°C
Vapor Phase Soldering(15 Seconds)	T_{VSOL}	-	-	+220	°C

NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device employs high-impedance CMOS devices on all signal pins. It must be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V or drops below ground by more than 0.5 V can induce destructive latchup.

Table 22. characteristics

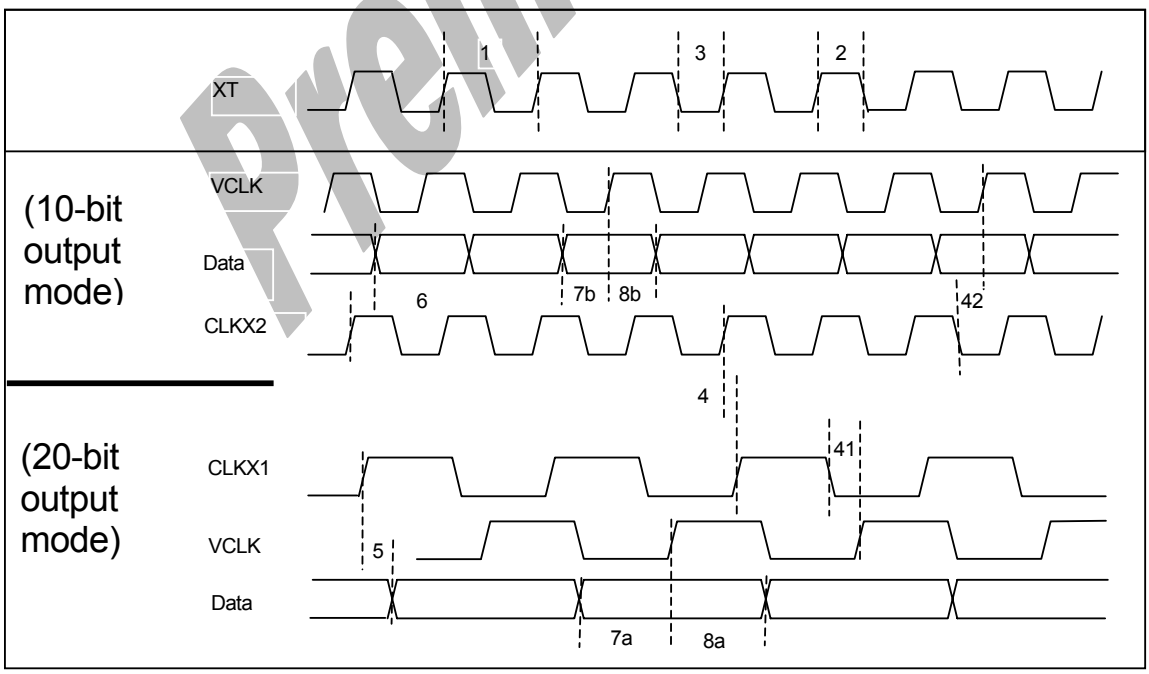
Parameter	Symbol	Min	Typ	Max	Units
Supply					
Power Supply — IO	V_{DDE}	3.15	3.3	3.6	V
Power Supply — Analog	V_{DDA}	2.4	2.5	2.8	V
Power Supply — Digital	V_{DD}	2.3	2.5	2.6	V
Maximum $\|V_{DD} - AVDD\|$		-	-	0.3	V
MUX0, MUX1 , MUX2 and MUX3 Input Range (AC coupling required)		0.5	1.00	2.00	V
CIN0 and CIN1 Amplitude Range (AC coupling required)		0.5	1.00	2.00	V
Ambient Operating Temperature	T_A	0		+70	°C
Analog Supply current	Iaa	-	176	-	mA
		-			MA
Digital Supply current	Idd	-	15	-	MA
Digital Core Supply Current		-	52	-	MA
Digital Inputs					
Input High Voltage (TTL)	V_{IH}	2.0	-	V_{DDM} + 0.5	V
Input Low Voltage (TTL)	V_{IL}	-	-	0.8	V
Input High Voltage (XTI)	V_{IH}	2.0	-	V_{DDM} + 0.5	V
Input Low Voltage (XTI)	V_{IL}	VSS -0.5	-	1.0	V

Input High Current (V_{IN} =V_{DD})	I_{IH}	-	-	10	μA
Input Low Current (V_{IN} =VSS)	I_{IL}	-	-	–10	μA
Input Capacitance (f=1 MHz, V_{IN} =2.4 V)	C_{IN}	-	5	-	pF

Parameter	Symbol	Min	Typ	Max	Units
Digital Outputs					
Output High Voltage (I_{OH} = –4 mA)	V_{OH}	2.4	-	V_{DD}	V
Output Low Voltage (I_{OL} = 4 mA)	V_{OL}	-	0.2	0.4	V
3-State Current	I_{OZ}	-	-	10	μA
Output Capacitance	C_O	-	5	-	pF
Analog Input					
Analog Pin Input voltage	Vi	-	1	-	Vpp
Analog Pin Input Capacitance	C_A	-	7	-	pF
ADCs					
ADC resolution	ADCR	-	10	-	bits
ADC integral Non-linearity	AINL	-	±1	-	LSB
ADC differential non-linearity	ADNL	-	±1	-	LSB
ADC clock rate	f_{ADC}	24	27	30	MHz
Video bandwidth (-3db)	BW	-	10	-	MHz
Horizontal PLL					
Line frequency (50Hz)	f_{LN}	-	15.625	-	KHz
Line frequency (60Hz)	f_{LN}	-	15.734	-	KHz
static deviation	Δf_H	-	-	6.2	%
Subcarrier PLL					
subcarrier frequency (NTSC-M)	f_{SC}	-	3579545	-	Hz
subcarrier frequency (PAL-BDGHI)	f_{SC}	-	4433619	-	Hz
subcarrier frequency (PAL-M)	f_{SC}	-	3575612	-	Hz
subcarrier frequency (PAL-N)	f_{SC}	-	3582056	-	Hz
lock in range	Δf_H	±450	-	-	Hz
Crystal spec					
nominal frequency (fundamental)		-	27	-	MHz
deviation		-	-	±50	ppm
Temperature range	Ta	0	-	70	°C
load capacitance	CL	-	20	-	pF
series resistor	RS	-	80	-	Ohm
Oscillator Input					
nominal frequency		-	27	-	MHz
deviation		-	-	±25	ppm
duty cycle		-	-	55	%

Parameter	Symbol	Min	Typ	Max	Units
Output CLK					
CLKX1		12	13.5	15	MHz
CLKX2		24	27	30	MHz
CLKX1 Duty Cycle		-	-	55	%
CLKX2 Duty Cycle		-	-	55	%
CLKX2 to CLKX1 Delay	4	-	-	2	ns
CLKX1 to Data Delay	5	-	5	-	ns
CLKX2 to Data Delay	6	-	5	-	ns
CLKX1 (Falling Edge) to VCLK (Rising Edge)	41	-	0	-	ns
CLKX2 (Falling Edge) to VCLK (Rising Edge)	42	-	0	-	ns
Output Video Data					
10-bit Mode (1)					
Data to VCLK (Rising Edge) Delay	7b	-	18	-	ns
VCLK (Rising Edge) to Data Delay	8b	-	18	-	ns
20-bit Mode (1)					
Data to VCLK (Rising Edge) Delay	7a	-	37	-	ns
VCLK (Rising Edge) to Data Delay	8a	-	37	-	ns

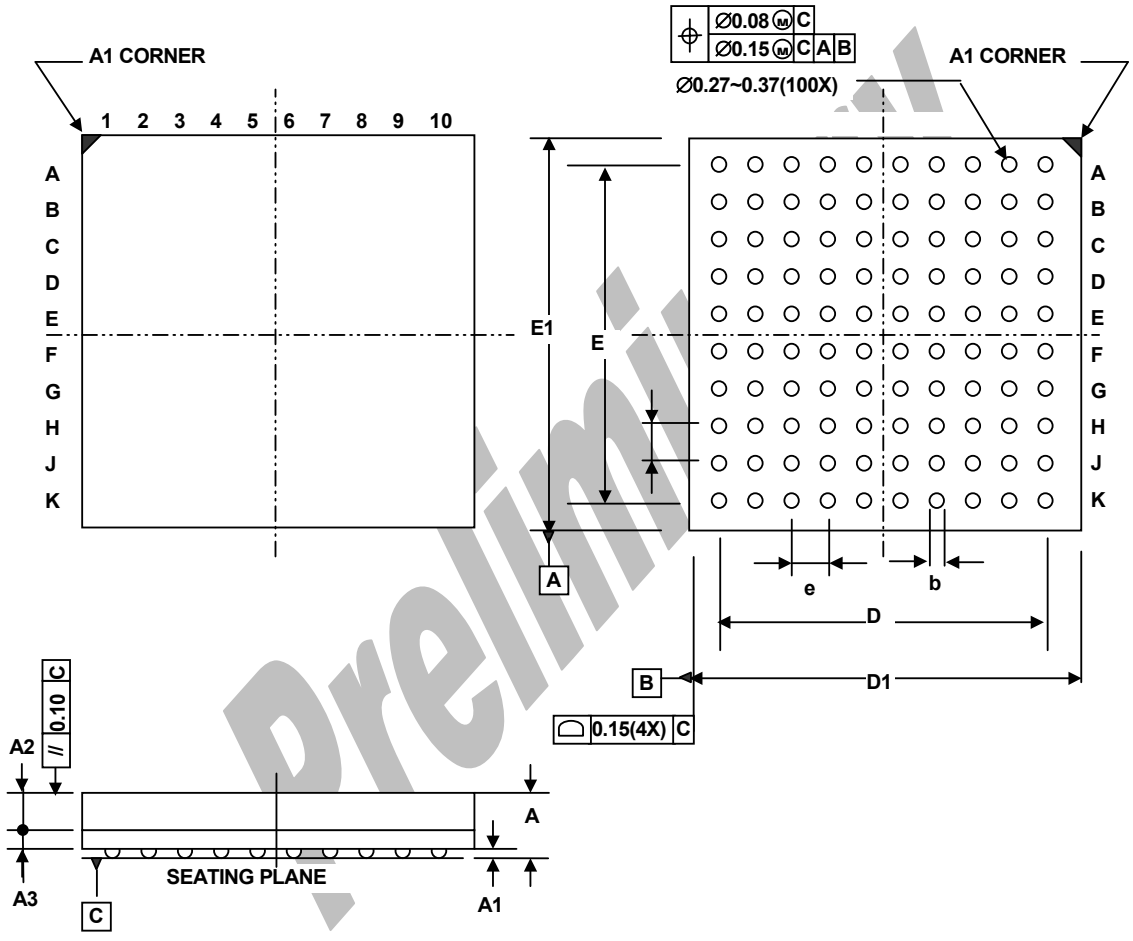
Clock Timing Diagram



Mechanical Data

100L VFBGA Package Mechanical Drawing: Package Size: 8x8x1.0 mm

TOP VIEW **BOTTOM VIEW**



UNIT	D1	D	E1	E	A	A1	A2	A3	b	e
mm	8±0.05	6.75	8±0.05	6.75	1.0 MAX	0.18~0.28	0.45	0.21	0.3	0.75

Copyright Notice

Disclaimer

This document provides technical information for the user. Techwell, Inc. reserves the right to modify the information in this document as necessary. The customer should make sure that they have the most recent data sheet version. Techwell, Inc. holds no responsibility for any errors that may appear in this document. Customers should take appropriate action to ensure their use of the products does not infringe upon any patents. Techwell, Inc. respects valid patent rights of third parties and does not infringe upon or assist others to infringe upon such rights.

Life Support Policy

Techwell, Inc. products are not authorized for use as critical components in life support devices or systems.

Revision history

Revision	Date	File name	
REV. C1	4/08/2005	TW9920CSPEC0408.PDF	Supply Currents are added.
REV.D	08/02/2005		Revision D