Features

- **Module Interface**
  - **2 full independent module capability**
  - **Common Interface Standard compliant**
    - **DVB_CI (CENELEC EN-50221)**
    - **NRSS-B (SCTE IS-679 Part B)**
    - **DAVIC v1.2 (CA0 interface)**
  - **Memory PCMCIA compliance (R2)**
    - **8-bit data access**
    - **26-bit address Memory Card**
  - **Attribute Memory access (CIS, Tupple)**
  - **High speed capability**
    - **Up to 20Mbits/s on Command Interface**
    - **Up to 100Mbits/s on Transport Stream**
  - **Polling and Interrupt modes**
  - **Hot Insertion (Automatic and Reset VCC handling)**
  - **3.3V or 5V I/O buffers**
- **PQFP 128 package**
- **Host microprocessor Interface**
  - **Universal Control Signal Generator (UCSG)**
  - **PC Card control signals generation**
  - **Supports PowerPC, ARM, ST20, 68xxx, TMS, LSI 64008, TC81220F, IDTR3041 host microprocessors**
  - **I2C port**
    - **CIMaX™ Set-up**
    - **Slot selection**
  - **Cascade mode management (up to 4 CIMaX™)**
  - **Chip Select bank and Interrupt facilities**
  - **3.3V or 5V I/O buffers**
- **Digital Video Stream Interface**
  - **MPEG II Transport Stream compliant**
  - **3.3V or 5V I/O buffer for direct interface with FEC and DEMUX ICs**

Description

The T90FJR, also called CIMaX™ controller is the hardware extension of SCM Microsystems' second generation Common Interface integration package (CI Pack+™). It enables CI Driver software to directly address two complete independent Common Interface modules.

As such, it contributes to offer an optimized, homogeneous and complete solution for digital TV receiver manufacturer that wants quickly to implement the Common Interface.

CIMaX™ includes the necessary I/Os to interface the MPEG Transport stream generated by the receiver demodulator and to daisy chain it through two modules and back it to the demultiplexer. Voltage level translators allow to avoid any additional component.

CIMaX™ interfaces with major digital TV receiver microprocessors. An I2C bus is used for initialization and module selection, while a Universal Control Signal Generator (UCSG)maps CPU control bus into Command Interface control signals. To minimize pin count, host address and data buses transit through external buffers that are driven by CIMaX™.

CIMaX™ includes a memory mode that allows to use any of the two Common interface slots to read/write a 8-bit PC Card Memory card. This feature gives the receiver memory extension capability for software upgrade or better performance.

ATMEL WIRELESS & µC

Dual Common Interface Hardware Controller-CIMax™

T90FJR

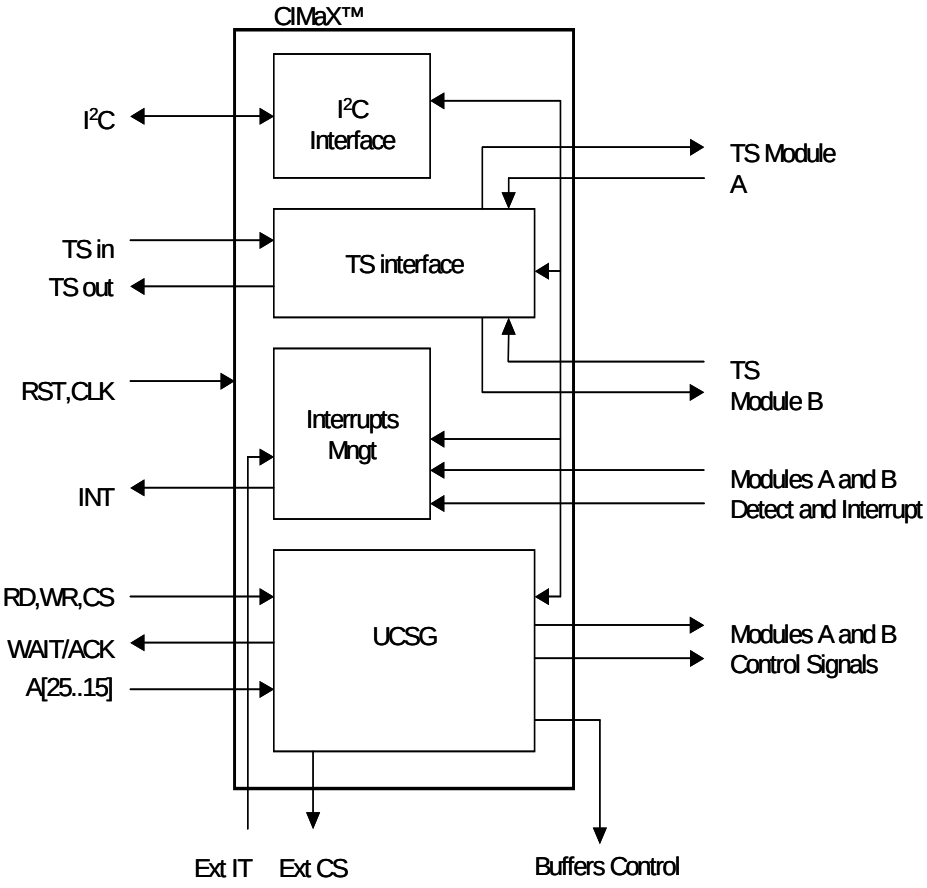
Rev. A – 7-Sep-01

In case of modules order is significant, CIMaX™ may virtually swap them (SCM' Patent Pending) after identifying which module must be in front of the transport stream.

CI Pack+™ includes hardware, software and qualification tools and is suitable for Set Top box, Digital TV set or PC board.

Block Diagram

Figure 1. Block Diagram



Pin description

Name	I/O	Type	RST	Function
RESET	I	TTL		CIMaX™ reset
CLK	I	TTL		27MHz clock input
SA1	I	CMOS		I^2C address bit 2
SA0	I	CMOS		I^2C address bit 1
SCL	I	trig		I^2C clock
SDA	I/O	trig	Z	I^2C data
A25	I	TTL		Host microprocessor address bit 25
A24	I	TTL		Host microprocessor address bit 24
A23	I	TTL		Host microprocessor address bit 23
A22	I	TTL		Host microprocessor address bit 22
A21	I	TTL		Host microprocessor address bit 21
A20	I	TTL		Host microprocessor address bit 20
A19	I	TTL		Host microprocessor address bit 19
A18	I	TTL		Host microprocessor address bit 18
A17	I	TTL		Host microprocessor address bit 17
A16	I	TTL		Host microprocessor address bit 16
A15	I	TTL		Host microprocessor address bit 15
CS	I	TTL		CIMaX™ chip select input
RD/DIR	I	TTL		Read strobe / transfer direction input
WR/STR	I	TTL		Write strobe / transfer strobe
WAIT/ACK	O	CMOS / TS	Z	WAIT / transfer acknowledge
INT	O	CMOS / TS	Z	Interrupt output to host microprocessor
EXTCS	O	CMOS / TS	Z	External device chip select
EXTINT	I	TTL		External device interrupt input

Name	I/O	Type	RST	Function
MICLK	I	TTL		MPEG clock input from front-end
MISTRT	I	TTL		MPEG packet start input
MIVAL	I	TTL		MPEG valid data input
MDI7	I	TTL		MPEG data input bit 7
MDI6	I	TTL		MPEG data input bit 6
MDI5	I	TTL		MPEG data input bit 5
MDI4	I	TTL		MPEG data input bit 4
MDI3	I	TTL		MPEG data input bit 3

Name	I/O	Type	RST	Function
MDI2	I	TTL		MPEG data input bit 2
MDI1	I	TTL		MPEG data input bit 1
MDI0	I	TTL		MPEG data input bit 0
MOCLK	O	CMOS	0	MPEG clock output to MPEG decoder
MOSTRT	O	CMOS	0	MPEG packet start output
MOVAL	O	CMOS	0	MPEG valid data output
MDO7	O	CMOS	0	MPEG data output bit 7
MDO6	O	CMOS	0	MPEG data output bit 6
MDO5	O	CMOS	0	MPEG data output bit 5
MDO4	O	CMOS	0	MPEG data output bit 4
MDO3	O	CMOS	0	MPEG data output bit 3
MDO2	O	CMOS	0	MPEG data output bit 2
MDO1	O	CMOS	0	MPEG data output bit 1
MDO0	O	CMOS	0	MPEG data output bit 0

Name	I/O	Type	RST	Function
MICLKA	O	CMOS / TS	Z	Module A MPEG clock input
MISTRTA	O	CMOS / TS	Z	Module A MPEG packet start input
MIVALA	O	CMOS / TS	Z	Module A MPEG valid data input
MDIA7	O	CMOS / TS	Z	Module A MPEG data input bit 7
MDIA6	O	CMOS / TS	Z	Module A MPEG data input bit 6
MDIA5	O	CMOS / TS	Z	Module A MPEG data input bit 5
MDIA4	O	CMOS / TS	Z	Module A MPEG data input bit 4
MDIA3	O	CMOS / TS	Z	Module A MPEG data input bit 3
MDIA2	O	CMOS / TS	Z	Module A MPEG data input bit 2
MDIA1	O	CMOS / TS	Z	Module A MPEG data input bit 1
MDIA0	O	CMOS / TS	Z	Module A MPEG data input bit 0
MOCLKA	I	TTL down		Module A MPEG clock output to MPEG decoder
MOSTRTA	I	TTL down		Module A MPEG packet start output
MOVALA	I	TTL down		Module A MPEG valid data output
MDOA7	I	TTL down		Module A MPEG data output bit 7
MDOA6	I	TTL down		Module A MPEG data output bit 6
MDOA5	I	TTL down		Module A MPEG data output bit 5
MDOA4	I	TTL down		Module A MPEG data output bit 4
MDOA3	I	TTL down		Module A MPEG data output bit 3

Name	I/O	Type	RST	Function
MDOA2	I	TTL down		Module A MPEG data output bit 2
MDOA1	I	TTL down		Module A MPEG data output bit 1
MDOA0	I	TTL down		Module A MPEG data output bit 0
MICLKB	O	CMOS / TS	Z	Module B MPEG clock input
MISTRTB	O	CMOS / TS	Z	Module B MPEG packet start input
MIVALB	O	CMOS / TS	Z	Module B MPEG valid data input
MDIB7	O	CMOS / TS	Z	Module B MPEG data input bit 7
MDIB6	O	CMOS / TS	Z	Module B MPEG data input bit 6
MDIB5	O	CMOS / TS	Z	Module B MPEG data input bit 5
MDIB4	O	CMOS / TS	Z	Module B MPEG data input bit 4
MDIB3	O	CMOS / TS	Z	Module B MPEG data input bit 3
MDIB2	O	CMOS / TS	Z	Module B MPEG data input bit 2
MDIB1	O	CMOS / TS	Z	Module B MPEG data input bit 1
MDIB0	O	CMOS / TS	Z	Module B MPEG data input bit 0
MOCLKB	I	TTL down		Module B MPEG clock output to MPEG decoder
MOSTRTB	I	TTL down		Module B MPEG packet start output
MOVALB	I	TTL down		Module B MPEG valid data output
MDOB7	I	TTL down		Module B MPEG data output bit 7
MDOB6	I	TTL down		Module B MPEG data output bit 6
MDOB5	I	TTL down		Module B MPEG data output bit 5
MDOB4	I	TTL down		Module B MPEG data output bit 4
MDOB3	I	TTL down		Module B MPEG data output bit 3
MDOB2	I	TTL down		Module B MPEG data output bit 2
MDOB1	I	TTL down		Module B MPEG data output bit 1
MDOB0	I	TTL down		Module B MPEG data output bit 0

Name	I/O	Type	RST	Function
RSTA	O	CMOS / TS	Z	Module A reset
CD1A#	I	CMOS trig up		Module A card detect 1
CD2A#	I	CMOS trig up		Module A card detect 2
CE1A#	O	CMOS / TS	Z	Module A card enable 1
CE2A#	O	CMOS / TS	Z	Module A card enable 2
RDY/IRQA#	I	TTL		Module A Ready / IRQ signal
WAITA#	I	TTL		Module A WAIT# signal
RSTB	O	CMOS / TS	Z	Module B reset
CD1B#	I	CMOS trig up		Module B card detect 1
CD2B#	I	CMOS trig up		Module B card detect 2
CE1B#	O	CMOS / TS	Z	Module B card enable 1
CE2B#	O	CMOS / TS	Z	Module B card enable 2
RDY/IRQB#	I	TTL		Module B Ready / IRQ signal
WAITB#	I	TTL		Module B WAIT# signal
REG#	O	CMOS / TS	Z	Modules REG# signal
OE#	O	CMOS / TS	Z	Modules output enable
WE#	O	CMOS / TS	Z	Modules write enable
IORD#	O	CMOS / TS	Z	Modules I/O read
IOWR#	O	CMOS / TS	Z	Modules I/O write
VCCEN	O	CMOS	Z	Modules VCC switch control
DATOE#	O	CMOS	1	External data buffers output enable
DATDIR	O	CMOS	0	External data buffer direction
ADOE#	O	CMOS	1	External address buffer output enable
ADLE	O	CMOS	1	External address buffer latch enable

Name	I/O	Type	Function
VCC_DVB1		Power	DVB CI modules buffers power
VCC_DVB2		Power	DVB CI modules buffers power
VCC_CORE		Power	Core power
VCC_TSI		Power	MPEG input buffers power
VCC_TSO		Power	MPEG output buffers power
VCC_PROC		Power	Host microprocessor control signals buffers power
GND_DVB1		Power	DVB CI modules buffers ground
GND_DVB2		Power	DVB CI modules buffers ground

Name	I/O	Type	Function
GND_CORE		Power	Core ground
GND_TSI		Power	MPEG input buffers ground
GND_TSO		Power	MPEG output buffers ground
GND_PROC		Power	Host microprocessor control signals buffers ground

Note: RST column indicates the output pin status after a reset issued by asserting RESET pin or RST bit in the CIMaX™ Control Register.

Notations:

TTL:TTL level
CMOS:CMOS level
TS:Tristate
trig:Schmitt Trigger
up:internal pull-up
down:internal pull-down

Host microprocessor interface

Configuration interface

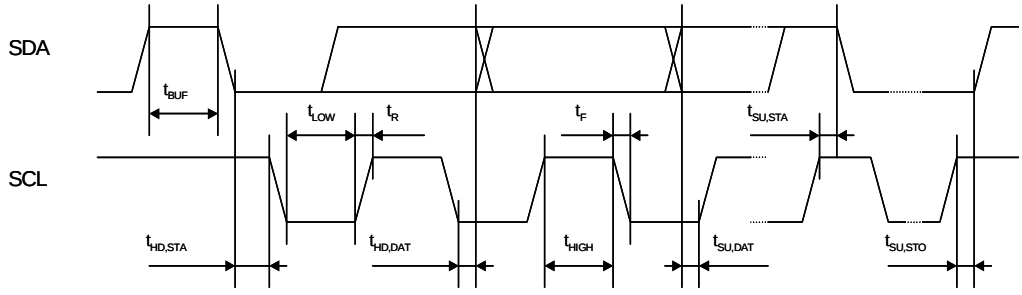
The CIMaX™ needs a clock source at 27MHz frequency with a duty cycle comprised between 33% and 67%. This frequency is commonly available in any digital video system.

A RESET input pin (active high) is available to reset the CIMaX™ at any time when power is on (e.g. : power monitor, watchdog…). The clock must be activated before the end of the reset. The reset signal must be active during at least 16 clock cycles (600ns @ 27MHz), before CIMaX™ reset. The CIMaX™ is operational 8 cycles after reset deactivation.

CIMaX™ includes an input high order address bus A[25:15] to achieve address decoding for automatic destination select or to be rerouted to the modules when using a memory PC Card with HAD=1 and TSIEN=0 and TSOEN=0, in the Module Control Register.

The CIMaX™ configuration is achieved by accessing the various registers through a standard I^2C interface. The I^2C device address can be chosen among four values by connecting SA1 and SA0 to VCC or GND. The binary address is 1 0 0 0 0 SA1 SA0 R/W. Though, the base address can be chosen between 80h, 82h, 84h or 86h allowing the connection of up to four CIMaX™ on the same bus.

Figure 2. Chronograms



Parameter	Symbol	Min	Max	Unit
SCL frequency	f_{SCL}		400	KHz
Bus free time between stop and start	t_{BUF}	1.3		µs
Hold time start condition	$t_{HD,STA}$	0.6		µs
SCL low period	t_{LOW}	1.3		µs
SCL high period	t_{HIGH}	0.6		µs
Setup time before a repeated start	$t_{SU,STA}$	0.6		µs
Data hold time	$t_{HD,DAT}$	0	0.9	µs
Data setup time	$t_{SU,DAT}$	100		ns
Rise time for both SDA and SCL signals	t_R	20	300	ns
Fall time for both SDA and SCL signals	t_F	20	300	ns

Parameter	Symbol	Min	Max	Unit
Setup time before a stop condition	$t_{SU,STO}$	0.6		µs
Capacitive load for each bus line	C_b		400	pF

Universal Control Signal Generator (UCSG)

CIMaX™ can be connected to various CPUs, each of them having a different external bus control structure with different signals and timings. To interface with a large number of different microprocessors, the host microprocessor interface includes a fully configurable UCSG block that generates the right PCMCIA control signals.

At reset, the host microprocessor interface is disabled ; CS, RD/DIR and WR/STR inputs are inactive and WAIT/ACK and INT are in high impedance state. The only available access is the configuration interface (I2C) which permits to set up the CIMaX™. Once the proper parameters have been entered in the CIMaX™, the interface is enabled by setting the LOCK bit in the CIMaX™ Control Register (@1Fh). The access to the modules is then possible and some parameters related to the host microprocessor interface are impossible to modify.

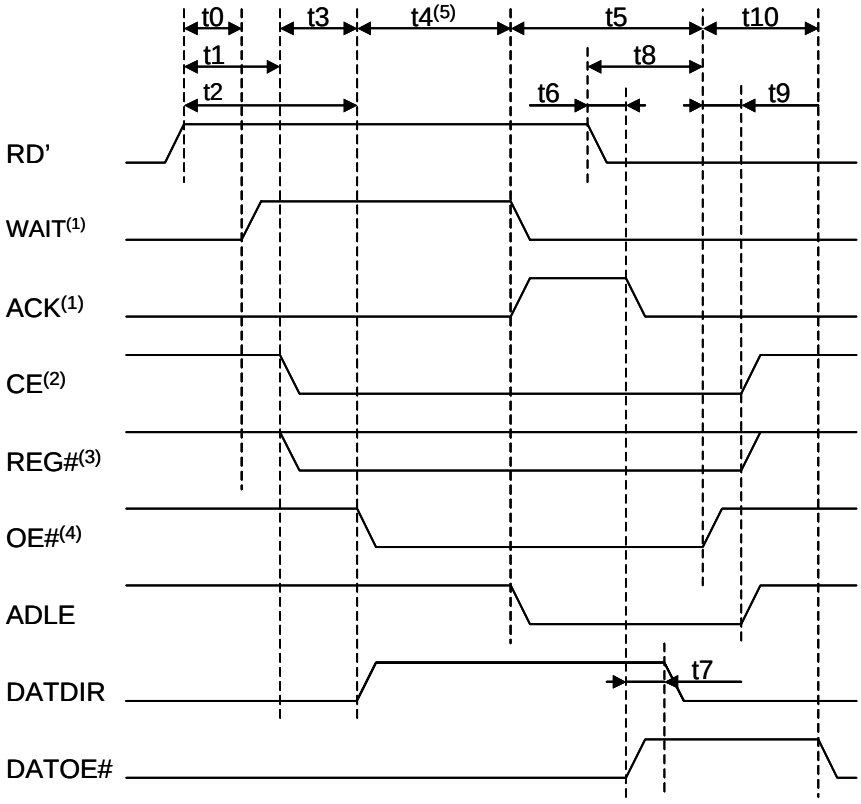
Host microprocessor input control signals are CS, RD/DIR, WR/STR and output signals are WAIT/ACK and INT. Input and output active levels can be individually set up by configuration bits. In addition, the output buffer structure is also configurable to be either open-drain (allowing wired-or) or push-pull, in the UCSG1 and UCSG2 registers.

- CS: Chip select signal indicates to the CIMaX™ that the current bus cycle is addressed to one of the modules (or external device)
- RD/DIR: Read strobe or direction signal. This signal function can be chosen with the RDIR bit. Read strobe indicates a valid read bus cycle or direction signal indicates the bus transfer direction when a valid bus transfer is indicated by the transfer strobe signal
- WR/STR: Write strobe or transfer strobe. This signal function can be adjusted with the WSTR bit. Write strobe indicates a valid write bus cycle or transfer strobe indicates a valid bus transfer in direction indicated by RD/DIR state.
- WAIT/ACK: Wait or Acknowledge transfer. In WAIT mode, this signal inserts wait cycles in the bus read or write operation in process. In ACK mode, this signal indicates the completion of the bus cycle.
- INT: Interrupt output to the host microprocessor.

The UCSG (universal control signals generator) inputs the RD / DIR, WR / STR and CS signals from host microprocessor, WAITA# and WAITB# from the modules and generates all the control signals to modules, host microprocessor, buffers and external device : CE1A#, CE2A#, CE1B#, CE2B#, REG#, OE#, WE#, IORD#, IOWR#, WAIT, ACK, ADLE, ADOE#, DATDIR, DATOE#.

The input signals from the host microprocessor are combined, depending on the host microprocessor configuration, to form a read and write signal RD' and WR'. These signals indicate an active read or write cycle in process.

Figure 3. Read access



Notes:
1. The WAIT/ACK output is either WAIT or ACK formatted according to the WAIT/ACK pin settings (active level, driving structure).
2. Depending on the read access type, CE can be either CE1A# or CE1B# for access to memory or IO to module A or B, CE2A# or CE2B# for access in EC (Extended Channel) mode, or even EXTCS for access to external device in regenerate mode.
3. REG# signal is not asserted during a common memory or external access.
4. OE# signal is asserted during a memory access (attribute or common). It is replaced by IORD# during an IO read cycle, an EC (Extended Channel) read cycle (using CE2A# or CE2B#) or an external access in regenerate mode.
5. t4 can be lengthened by the insertion of wait cycles. When the destination module asserts WAIT# signal, the t4 cycles counter stops until WAIT# becomes inactive anew.

Memory read timings are given for various cycle duration. In attribute memory mode, only 600ns and 300ns cycles are available. In common memory mode, 300ns doesn't exist. IO and external device in regenerate mode share the same timing specifications as they all use IORD# and IOWR# signals. Timings are given in CIMaX™ clock cycles. They are calculated to comply with PCMCIA specifications when 27MHz clock is used.

	Memory read						IO, EC, Ext
	600ns	300 ns	250ns	200ns	150 ns	100 ns	
t0 max(1)	26 ns						
t1 max	1.5 cycle + 26 ns (2)						
t2 min	3	1	1	1	1	1	2
t3	3	1	1	1	1	1	2
t4	14	8	7	5	4	3	3
t5 min	0						2
t6 max(1)	26 ns						
t7 min	0 ns						
t7 max	70 ns						
t8 max	1.5 cycle + 26 ns						
t9	1	1	1	1	1	1	1
t10 min	5	3	3	3	3	2	2

(1) these timings are given for a load of 50 pF on WAIT/ACK pin.

(1) 1.5 cycle corresponds to the start cycle detection time. t1 depends actually on the previous cycle completion which depends on t8 and t10 read timings. So t1 ranges from 3.5 to 6.5 cycles.

Note: t0: delay between start of a read cycle and activation of WAIT

t1: delay between start of a read cycle and falling edge of CE and REG# (if required for the current cycle)

t2: delay between start of a read cycle and falling edge of OE# (and switching of the data buffer direction control)

t3: delay between falling edge of CE and falling edge of OE# (and switching of the data buffer direction control)

t4: read cycle length. This time is the necessary delay for the module to present the read data on the data output bus. After t4 delay is expired, WAIT is deasserted and ACK asserted thus enabling the processor to read the data on the bus. At the same time, ADLE is reset to latch the address presented to the module so that the data is not changed while the processor is reading. t4 can be lengthened by the module if the module requires extra wait cycles by asserting its WAIT# pin low.

t5: delay to deassertion of module read signal (OE# or IORD#) after minimum delay after t4.

t6: delay between end of read cycle indicated by the processor and data bus isolation (DATOE# asserted)

t7: delay between data bus isolation and switching back of the data bus direction

t8: delay to deassertion of module read signal (OE# or IORD#) after end of a read cycle by the processor.

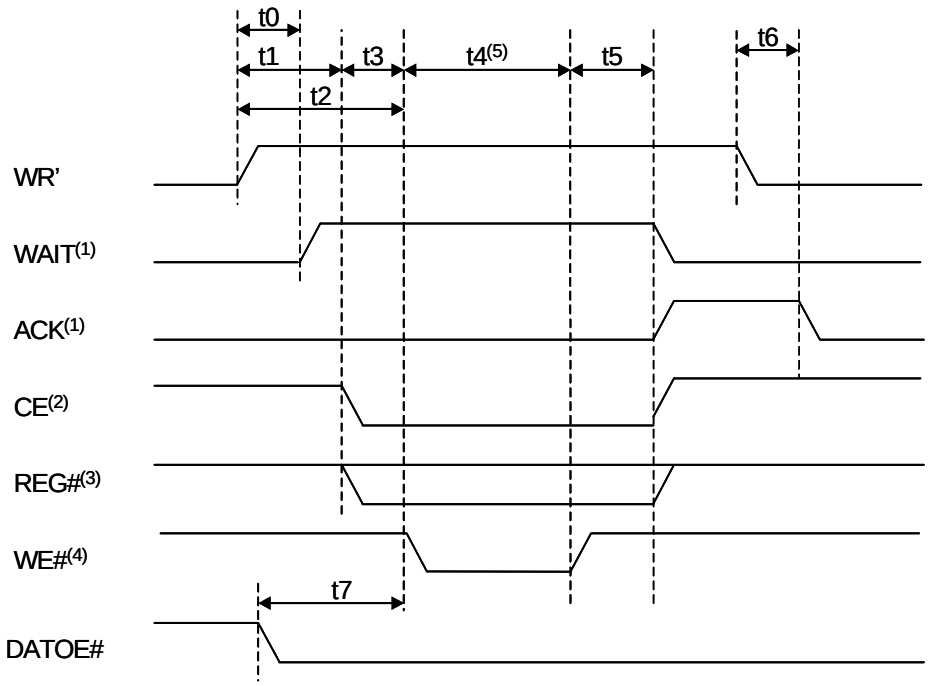
t9: delay between deassertion of the module read signal and deassertion of CE, REG# and ADLE (releasing the address bus)

t10: delay between deassertion of the module read signal and re-enabling of the data bus (see t7 on write cycle)

The corresponding timings are given below for a 27 MHz clock:

	Memory read						
	600ns	**300 ns**	**250ns**	**200ns**	**150 ns**	**100 ns**	**IO, EC, Ext**
t0 max	26 ns						
t1 max	80 ns (from start cycle detection – see note in table above)						
t2 min	111 ns	37 ns	37 ns	37 ns	37 ns	37 ns	75 ns
t3	111 ns	37 ns	37 ns	37 ns	37 ns	37 ns	75 ns
t4	530 ns	297 ns	260 ns	185 ns	150 ns	111 ns	111 ns
t5 min	0 ns						75 ns
t6 max	26 ns						
t7 min	0 ns						
t7 max	70 ns						
t8 max	80 ns						
t9	37 ns	37 ns	37 ns	37 ns	37 ns	37 ns	37 ns
t10 min	185 ns	111 ns	111 ns	111 ns	111 ns	75 ns	75 ns

Write access



Note: (1): The WAIT / ACK output is either WAIT or ACK formatted according to the WAIT / ACK pin settings (active level, driving structure).
(2): Depending on the write access type, CE can be either CE1A# or CE1B# for access to memory or IO to module A or B, CE2A# or CE2B# for access in EC (Extended Channel) mode or even EXTCS for access to external device in regenerate mode
(3): REG# signal is not asserted during a common memory or external access.
(4): WE# signal is asserted during a memory access (attribute or common). It is replaced by IOWR# during an IO write cycle, an EC (Extended Channel) write cycle (using CE2A# or CE2B#) or an external access in regenerate mode.
(5): t4 can be lengthened by the insertion of wait cycles. When the destination module asserts WAIT# signal, the t4 cycles counter stops until WAIT# becomes inactive anew.

Memory write is valid for both attribute and common memory access. Timings are given in CIMaX™ clock cycles. They are calculated to comply with PCMCIA specifications when 27MHz clock is used.

	Memory write					IO, EC, Ext
	600ns	250ns	200ns	150ns	100ns	
t0 max(1)	26 ns					
t1 max	1.5 cycle + 26 ns (2)					
t2 min	2	1	1	1	1	2
t3	2	1	1	1	1	2
t4	9	5	4	3	2	5
t5	2	1	1	1	1	1
t6 max(1)	26 ns					
t7 min	1	1	1	1	1	2

Note: 1. these timings are given for a load of 50 pF on WAIT/ACK pin.

2. 1.5 cycle corresponds to the start cycle detection time. t1 depends actually on the previous cycle completion which depends on t8 and t10 read timings. So t1 ranges from 3.5 to 6.5 cycles.

Note: t0: delay between start of a write cycle and activation of WAIT
t1: delay between start of a write cycle and assertion of CE and REG# (if necessary for the current cycle)
t2: delay to assertion of the write signal (WE# or IOWR#) after the start of the write cycle
t3: delay to assertion of the write signal (WE# or IOWR#) after the assertion of CE
t4: write cycle duration. This delay can be lengthened by the assertion of the module WAIT# pin
t5: delay between deassertion of the write signal and deassertion of CE, REG# and WAIT and assertion of ACK indicating to the processor the end of its write cycle
t6: delay between end of the write cycle and deassertion of ACK
t7: delay between enabling of the data bus and write signal assertion. This delay is necessary when a write cycle is immediately following a read cycle (see t10 in read cycle)

The corresponding timings are given below for a 27 MHz clock:

	Memory write					IO, EC, Ext
	600ns	250ns	200ns	150ns	100ns	
t0 max	24 ns					
t1 max	80 ns (from start cycle detection – see note in table above)					
t2 min	75 ns	37 ns	37 ns	37 ns	37 ns	75 ns
t3	75 ns	37 ns	37 ns	37 ns	37 ns	75 ns
t4	334 ns	185 ns	150 ns	111 ns	75 ns	185 ns
t5	75 ns	37 ns	37 ns	37 ns	37 ns	37 ns
t6 max	26 ns					

	Memory write					IO, EC, Ext
	600ns	250ns	200ns	150ns	100ns	
t7 min	37 ns	37 ns	37 ns	37 ns	37 ns	75 ns

External peripheral control signals

CIMaX™ outputs a chip select EXTCS. This output is fully configurable through the Destination Select register to be open-drain or push-pull output driver and active high or low.

The activation of this output can be programmed to be automatically the default selection when none of the modules is selected (bit DEF = 1 in the external access auto select mask low register) and CS input is asserted or when address match the external access auto select mask and pattern registers on the same basis as for the modules auto selection when DEF = 0.

The EXTCS output can also be manually chosen to be the destination when AUTOSEL bit is 0 in the Destination Select Register and when SEL = 11.

In addition, the EXTCS output can work in two ways :transmit mode or regenerate mode selected by the XCSMOD in the Destination Select Register.

The EXTCS output reproduces the CS input whenever the external device selection conditions are met in the CIMaX™, regardless of the selection mode (automatic / manual, default / pattern match). This mode permits to insert the CIMaX™ in an existing hardware architecture by replacing an existing peripheral by the CIMaX™ on the address decoder and connecting this peripheral to the CIMaX™. The address decoding must then be set up properly on the address decoder and in the CIMaX™ to match the new hardware architecture but no extra CS is needed on the address decoder ; the CIMaX™ provides a new one in replacement of the one it needs. The following table gives the maximum propagation delay according to different conditions (70 °C):

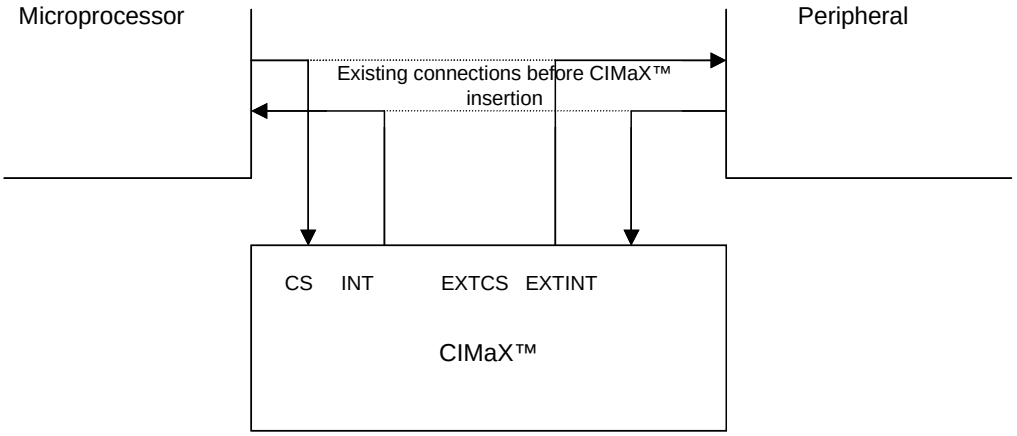
Conditions		CS to EXTCS maximum time
Vcc	EXTCS Load	
4.5 V	10 pF	9 ns
4.5 V	50 pF	13 ns
3.0 V	10 pF	13 ns
3.0 V	50 pF	16 ns

In regenerate mode, the EXTCS output acts as CEx# outputs to the modules as it is generated by the internal CIMaX™ state machine in conjunction with assertion of IORD# or IOWR#. This mode permits to access to any 8-bit peripheral accessed with a RD, a WR and a CS input such as a static RAM or an UART for example with programmable access time provided by the CIMaX™.

The CIMaX™ also provides an interrupt input. This input is rerouted to the INT output connected to the host microprocessor through the interrupt manager of the CIMaX™. EXTINT pin is programmable to be either active-high or active-low with the EXTLVL bit in the Interrupt Config Register and is maskable with the EXTM bit in the Interrupt Mask Register. The EXTINT input status can be monitored by reading the EXT bit in the Inter-

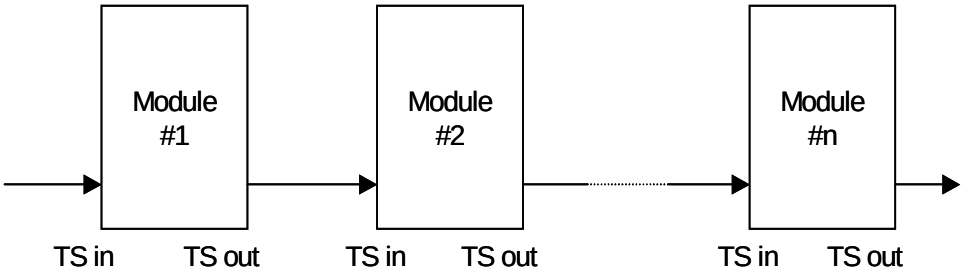
rupt Status Register. This feature can be used to insert the CIMaX™ in an existing environment by using an interrupt input of the host microprocessor already used by a peripheral for the CIMaX™ interrupt and connecting this peripheral's interrupt to the CIMaX™.

Using EXTCS and EXTINT enables to insert the CIMaX™ in an existing design where all the chip selects and interrupts are already affected as it virtually does not use any chip select nor interrupt.



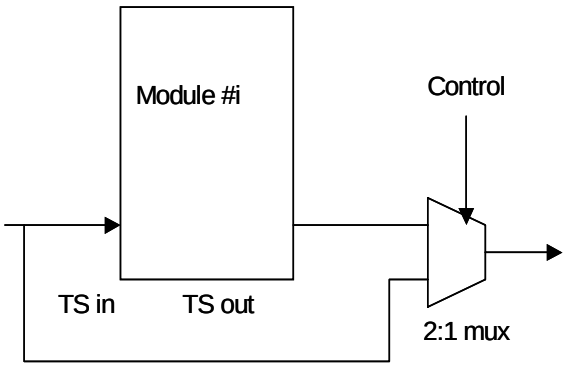
TS Daisy Chain

In the DVB Common Interface, each module has an MPEG input port constituted by MPEG clock, MPEG packet start, MPEG valid data and MPEG data bus and an MPEG output port composed of the same signals. The MPEG transport stream transits through the modules on a daisy chain basis.



Hot plug and bypass

As a module can be inserted or removed at any time, in order not to break the daisy chain, the CIMaX™ handles one MPEG transport stream bypass for each module. This bypass is enabled as long as a valid DVB CI module is not recognized to be inserted and activated in the corresponding slot or automatically as soon as the module is removed from a slot. The disabling of the bypass is controlled by the TSOEN bit in each Module Control Register. The bypass can be switched at any time, regardless of the MPEG stream synchronization.



TS swap (SCM Patent Pending)

With standard conditional access modules, the order in which the transport stream passes through has no influence. However, in some particular cases, it can be useful to choose which module is first in the TS daisy chain. The TSWAP bit in the Destination Select Register when set, virtually swaps the two modules so that the MPEG stream passes first in the B module and then in the A module.

TS / Addresses input signals

The MPEG input stream pins on the module are shared with the high order addresses specified by the PC Card standard. When a module is inserted, before initialization, all these pins are forced to logical 0 state. If a memory module is recognized, the high order addresses A[25..15] can be applied to the module by setting the HAD bit in the Module Control Register. If a DVB module is recognized, the MPEG stream is applied to the module by setting the TSIEN bit in the Module Control Register. Those two bits cannot be set at the same time and are reset when the module is extracted

When HAD is set, the maximum propagation delay between A[25..15] inputs and TS outputs to the modules is 25 ns with a load of 50 pF on the outputs.

The TSOEN bit (TS bypass control bit) can only be set when TSIEN has previously been set.

Resetting TSIEN also resets TSOEN.

Invert mask

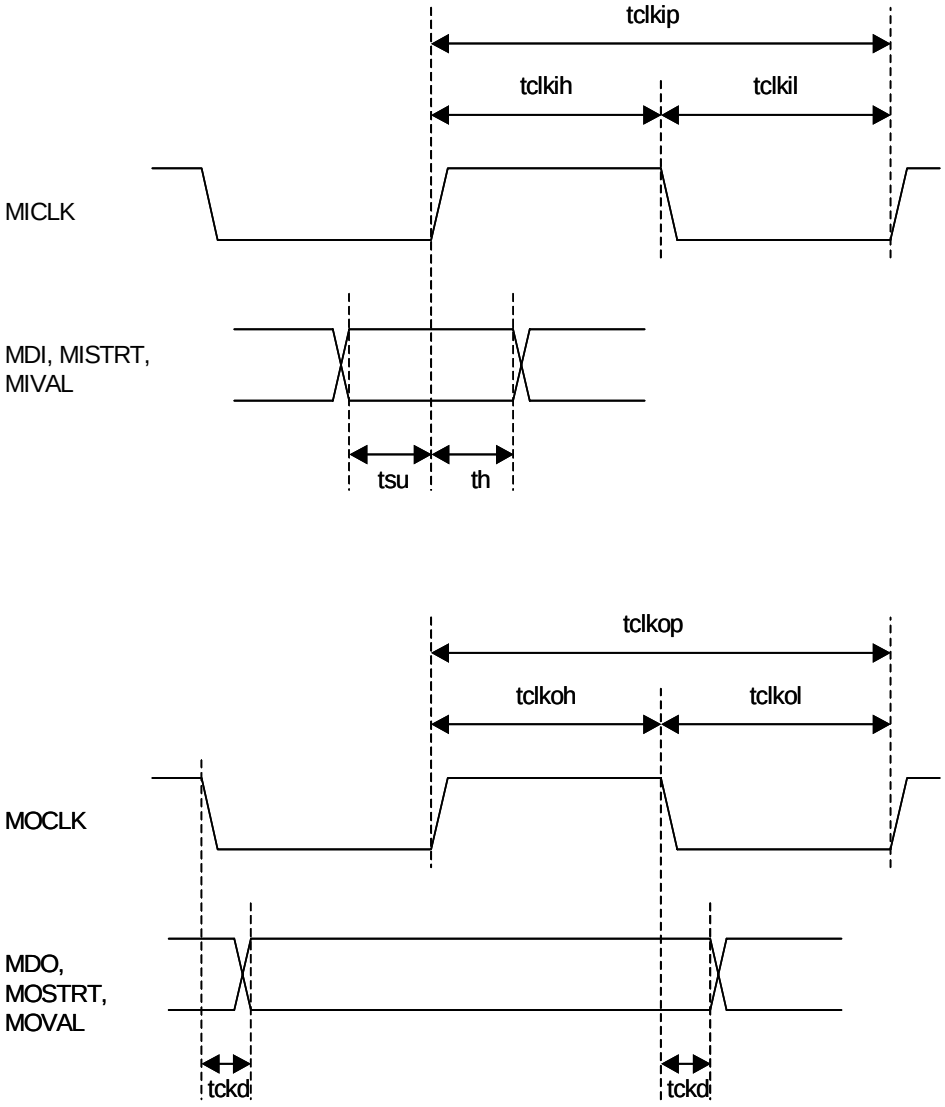
Some modules can output an MPEG stream with inverted bits in the MPEG data bus. The CIMaX™ is able to re-invert those bits to restore the correct data on the bus. This is achieved by setting the appropriate bits in the Invert Mask Register.

IO characteristics

The CIMaX™ ensures that the MPEG stream output signals applied to the modules and to the MPEG decoder (or chained CIMaX™) meets the AC and DC electrical characteristics defined in the PC Card standard [1], the DVB CI standard [2] and Guidelines for implementation [3]. Moreover, the CIMaX™ MPEG inputs from MPEG source (e.g. front-end receiver) and from the modules comply with the same requirements. In order to fulfil the timing requirements, the MPEG stream is re-synchronized at each step

in the daisy chain, thus introducing a few MPEG clock cycles delay (1 to 3) on the data stream between the input and output depending on the number of active modules.

TS signals chronograms



Note: According to Errata in EN 50221 and the Cenelec report Guidelines for implementation and use of the common interface for DVB decoder applications– CIT057 – rev6., delays for MICLK, MDI, MIVAL, MISTRT are also applicable to MOCLKA, MOCLKB, MDOA, MDOB, MOVALA, MOVALB, MOSTRTA, MOSTRB except for clock high and low times. Delays for MOCLK, MDO, MOSTRT, MOVAL are also applicable to MICLKA, MICLKB, MDIA, MDIB, MIVALA, MIVALB, MISTRTA, MISTRTB.

AC Electrical characteristics

VCC = 5V, T = 25°C

Parameter		Min	Max	Unit
tclkip	MPEG input clock period	111		ns
tclkih	MICLK input clock high time MOCLKA/B input clock high time	24 44	97(1) 67	ns
tclkil	MICLK input clock low time MOCLKA/B input clock low time	24 44	97(1) 67	ns
tclkop	MPEG output clock period	111		ns
tclkoh	output clock high time	24	91(1)	ns
tclkol	output clock low time	24	91(1)	ns
tsu	input data setup	10		ns
th	input data hold	10		ns
tckd	clock to data delay	0	15	ns

Note: (1) for a clock period of 111 ns

Command interface

The command interface is directly issued from PC Card standard [1] restricted to 8 bits access and 15 bits addressing. The command interface of a CI module is described in detail in the PC Card standard [1] and the restrictions applied to this standard for the command interface are described in the DVB CI standard [2].

Command interface signals

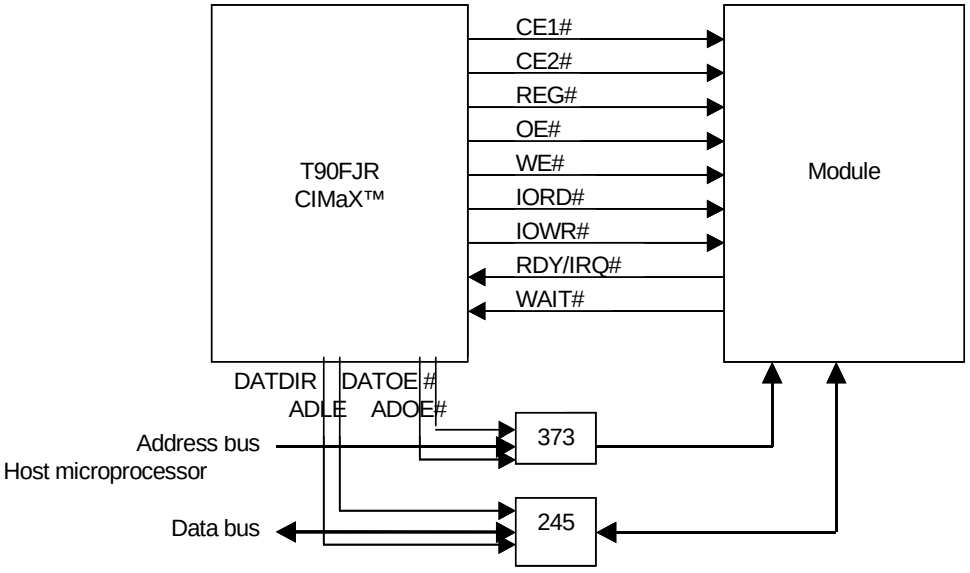
The 15 address bits and 8 data bits of the CI module are connected to the host microprocessor bus through buffers (type 373 and 245) which are controlled by the CIMaX™. The CIMaX™ provides the buffers control signals:

- DATOE#Data Output enable (active low)
- ADOE# Address Output enable (active low)
- DATDIR Data direction according to the read/write current cycle
- ADLE Address Latch enable to latch the address bus until the end of the read/write cycle.

(see application note for connection of the buffers)

The buffers should be powered by the same source (voltage) as the modules.

The CI control signals are the same as the PC Card control signals : CE1#, CE2#, REG#, OE#, WE#, IORD#, IOWR#, RDY/IRQ#, WAIT#. The CIMaX™ generates those signals so that they fit the PC Card standard whenever the host microprocessor accesses one of the modules. The control signals activated depend on the access type chosen in the Module Control Register with ACS[1..0]. The read and write signals active level duration is configured in the memory access cycle time registers. The CIMaX™ receives RDY/IRQ# from the module and retransmits the interruption to the host microprocessor. The module can also send a WAIT# request that is also transmitted to the host microprocessor in addition to the wait states already generated due to the read and write duration.



Registers description

CIMaX™ includes several internal registers as depicted below, and described into the following sections.

Address	Description
00	Module A Control Register
01	Module A auto select mask high Register
02	Module A auto select mask low Register
03	Module A auto select pattern high Register
04	Module A auto select pattern low Register
05	Memory access A cycle time Register
06	Invert Input Mask A Register
07	RFU
08	RFU
09	Module B Control Register
0A	Module B auto select mask high Register
0B	Module B auto select mask low Register
0C	Module B auto select pattern high Register
0D	Module B auto select pattern low Register
0E	Memory access B cycle time Register
0F	Invert Input Mask B Register
10	RFU
11	RFU
12	External access auto select mask high Register
13	External access auto select mask low Register
14	External access auto select pattern high Register
15	External access auto select pattern low Register
16	RFU
17	Destination select Register
18	Power control Register
19	RFU
1A	Interrupt Status Register
1B	Interrupt Mask Register
1C	Interrupt Config Register
1D	UCSG1 : Microprocessor interface config Register
1E	UCSG2 : Microprocessor wait/ack config Register
1F	CIMaX™ control Register

Note: All registers are reset to 00h. Register bits marked **X** should not be set. They are read as 0.
RFU = Reserved for Future Use

CIMaX™ Control Register

This register is used to control the basic functions of CIMaX™.

CIMaX™ control: (@1Fh)

RST	X	X	X	X	X	X	LOCK

LOCK validates and locks the chip setup

0 chip is not configured. Microprocessor inputs and outputs are inactive

1 chip is configured. Configuration bits are locked and CIMaX™ IOs are active

RST reset chip

equivalent to asserting the RESET pin. CIMaX™ is reset to its initial state this bit is automatically reset; no need to write 0 in italways reads as 0

1 reset

Modules Control Registers

This register is available for each module A and B to control the initialization and access to them.

Module control : (@00h mod A, @09h mod B)

RST	TSOEN	TSIEN	HAD	ACS1	ACS0	AUTO	DET

DET module detection

read only, write has no effect

0 no module present

1 module inserted

AUTO module auto activation on detection

0 no auto activation procedure
Interrupt is generated immediately when DET = 1

1 start module auto activation when DET = 1 if VCC = 1
Interrupt is generated at the end of auto activation

ACS[1:0] module access type

automatically forced to 00 when DET = 0

writing those bits is only allowed when DET = 1

00 access to attribute memory
01 access to I/O space
10 access to common memory
11 access to Extended Channel using CE2# signal

HAD source selection applied to the module

automatically forced to 0 when DET = 0

setting this bit is only allowed when DET = 1 and TSIEN = 0 and TSOEN = 0

0 apply MPEG stream

1 apply A[25:15] for memory access

TSIEN MPEG transport stream input control

automatically forced to 0 when DET = 0

setting this bit is only allowed when DET = 1 and HAD = 0

0 no MPEG stream (all signals forced to 0)

1 MPEG stream enabled

TSOEN MPEG transport stream bypass control

automatically forced to 0 when DET = 0 or TSIEN = 0

setting this bit is only allowed when DET = 1 and HAD = 0 and TSIEN = 1

0 bypass enabled

1 bypass disabled (TS through module enabled)

RST module RST pin control

automatically forced to 0 when DET = 0

setting this bit is only allowed when DET = 1

The state of this bit is reproduced on the RST (A or B) pin of the module.

Invert Input Mask Register

The Invert Input Mask Register is used to complement selected bits on the incoming MPEG data stream from modules.

Invert input mask: (@06h mod A, @0Fh mod B)

INV7	INV6	INV5	INV4	INV3	INV2	INV1	INV0

INV[7:0] Invert mask

0 corresponding bit is not complemented

1 corresponding bit is complemented

Destination Select Register

The Destination Select Register is used to choose which peripheral will be accessed by the microprocessor when selecting the CIMaX™. The three available destinations are the two modules and the external device selected by the EXTCS output signal from the CIMaX™. For each module, the access mode (memory / IO) is chosen in the Module Control Register.

The destination select can be achieved either manually when AUTOSEL bit is 0 using SEL bits or automatically by configuring the select masks and patterns registers.

Destination select: (@17h)

X	TSWAP	XCSDRV	XCSLVL	XCSMOD	SEL1	SEL0	AUTOSEL

AUTOSEL

automatic module selection

uses high order addresses to choose module or external device (using EXTCS)

0 manual selection

1 automatic selection

SEL[1:0]

module select

relevant only when AUTOSEL = 0

00 no destination selected

01 select module A

10 select module B

11 select external device using EXTCS

XCSMOD

EXTCS signal mode

changing this bit is only allowed when LOCK = 0

retransmit CS signal input from processor when external device is selected or regenerate EXTCS as done for CE# signal and simultaneously generate IORD# or IOWR#

0 transmit mode

1 regenerate mode

XCSLVL

EXTCS output pin active level

changing this bit is only allowed when LOCK = 0

0 EXTCS pin is active-low

1 EXTCS pin is active-high

XCSDRV

EXTCS output pin structure

changing this bit is only allowed when LOCK = 0

0 EXTCS buffer is open drain

1 EXTCS buffer is push-pull

TSWAP

TS daisy chain order swap (SCM Patent Pending)

0 module A before module B

1 module B before module A

Power Control Register

This register is used to control the power of the modules if the power switch is implemented (optional, see application note). When the VCC bit is 0, no VCC is supposed to be applied to the modules so all the outputs to the modules are in high impedance state. When VCC = 0, ADOE# and DATOE# are also high to put the address and data buffers outputs in high impedance. This implies that when no VCC switch is used, the VCC bit should anyway be set to enable the control signals to be applied to the modules.

Power control : (@18h)

VCDRV	VCLVL	X	X	X	X	X	VCC

VCC

module power supply switch control

changing this bit is only allowed when LOCK = 1

0 power off

1 power on

VCLVL

module VCC output pin active level

changing this bit is only allowed when LOCK = 0

0 VCC pin is active-low

1 VCC pin is active-high

VCDRV

module VCC output pin structure

changing this bit is only allowed when LOCK = 0

0 VCC buffer is open drain

1 VCC buffer is push-pull

Module Auto Select Registers

When automatic destination selection is used, the module auto select mask indicates the high order address bits used for decoding the address windows for each module and the module auto select pattern register determines the address at which the module is addressed.

Auto select mask high : (@01h mod A, @0Ah mod B)

X	X	X	X	X	MA25	MA24	MA23

Auto select mask low : (@02h mod A, @0Bh mod B)

MA22	MA21	MA20	MA19	MA18	MA17	MA16	MA15

MA[25:15]

address mask for decoding

0 address bit doesn't care

1 address bit should match programmed address bit in module auto select pattern register

Auto select mask high external : (@12h)

DEF	X	X	X	X	MA25	MA24	MA23

Auto select mask low external : (@13h)

MA22	MA21	MA20	MA19	MA18	MA17	MA16	MA15

MA[25:15] address mask for decoding

relevant only when DEF = 0. Doesn't care if DEF = 1.

0 address bit doesn't care

1 address bit should match programmed address bit in module auto select pattern register

DEF external device default addressing

0 EXTCS asserted when address match mask and pattern

1 EXTCS asserted when neither module A nor module B is selected while CS input active

Auto select pattern high : (@03h mod A, @0Ch mod B, @14h Ext)

X	X	X	X	X	PA25	PA24	PA23

Auto select pattern low : (@04h mod A, @0Dh mod B, @15h Ext)

PA22	PA21	PA20	PA19	PA18	PA17	PA16	PA15

PA[25:15] address pattern to match in accordance with address mask to select the corresponding module. Relevant only when DEF = 0 in external auto select mask. Doesn't care if DEF=1.

Access Time Registers

When accessing a module, the CIMaX™ regenerates the module control signals and in the meantime controls the host microprocessor by inserting wait states in the microprocessor cycle or delaying the transfer acknowledge. The read or write cycle time generated by the CIMaX™ to the module can be adjusted individually for each module,

each access type and each direction with different standard timings (refer to PC Card standard for details about timings).

Memory access cycle time : (@05h mod A, @0Eh mod B)

X	AM2	AM1	AM0	X	CM2	CM1	CM0

AM[2:0] attribute memory cycle time used :

000	100ns
001	150ns
010	200ns
011	250ns
100	600ns
101 to 111	reserved. Do not use

This timing is valid for write access. During read access, if AM = 100, 600 ns cycles will be used, if AM = 0XX, 300ns will be used.

CM[2:0] common memory cycle time used:

000	100ns
001	150ns
010	200ns
011	250ns
100	600ns
101 to 111	reserved. Do not use

Interrupt Registers

The CIMaX™ handles five interrupt sources issued from modules detection, modules IRQ and external device. Each interrupt is latched in the Interrupt Status Register. Each bit in this register can generate an interrupt to the microprocessor when set and when the corresponding mask bit in the interrupt mask register is set.

In addition, the interrupt output pin structure and level can be configured to match the host hardware requirements.

Interrupt status: (@1Ah) (read only)

X	X	X	EXT	IRQB	IRQA	DETB	DETA

DETA slot A module detection

reset on read

0 no change

1 a module has been inserted or extracted in slot A

DETB slot B module detection

reset on read

0 no change

1 a module has been inserted or extracted in slot B

IRQA slot A inverted IRQ# line state

0 IRQ# on slot A is high (inactive)

1 IRQ# on slot A is low (active)

IRQB slot B inverted IRQ# line state

0 IRQ# on slot B is high (inactive)

1 IRQ# on slot B is low (active)

EXT EXTINT status

0 EXTINT is inactive

1 EXTINT is active

Interrupt mask register: (@1Bh)

X	X	X	EXTM	IRQBM	IRQAM	DETBM	DETAM

DETAM slot A module detection mask

0 masked

1 unmasked : a module movement in slot A will generate an interrupt

DETBM slot B module detection mask

0 masked

1 unmasked : a module movement in slot B will generate an interrupt

IRQAM slot A IRQ# mask

0 masked

1 unmasked : an interrupt request from module A will be transmitted to the microprocessor

IRQBM slot B IRQ# mask

0 masked

1 unmasked : an interrupt request from module B will be transmitted to the microprocessor

EXTM external interrupt mask

0 masked

1 unmasked : an interrupt from external source will be transmitted to the microprocessor

Interrupt config register: (@1Ch)

X	X	X	X	X	ITDRV	ITLVL	EXTLVL

EXTLVL

EXTINT input pin active level

changing this bit is only allowed when LOCK = 0

0 EXTINT pin is active-low

1 EXTINT pin is active-high

ITLVL

INT output pin active level

changing this bit is only allowed when LOCK = 0

0 INT pin is active-low

1 INT pin is active-high

ITDRV

INT output pin structure

changing this bit is only allowed when LOCK = 0

0 INT buffer is open drain

1 INT buffer is push-pull

UCSG1 and UCSG2 Registers

The UCSG1 and UCSG2 Registers generate PC Card control signals (REG#, OE#, WE#, IORD#, IOWR#, CE1/2A#, CE1/2B#) from microprocessor control signals (RD/DIR, WR/STR, WAIT/ACK, CS, A[25..15]).

UCSG1 Register : (@1Dh)

X	X	X	X	CSLVL	WSTRLVL	RDIRLVL	RDIR

RDIR

RD/DIR and WR/STR inputs function

changing this bit is only allowed when LOCK = 0

0 RD/WR mode

1 DIR/STR mode

RDIRLVL

RD/DIR input active level (for read strobe or read direction)

changing this bit is only allowed when LOCK = 0

0 RD is active-low or RD/DIR input is low during read transfer and high during write

1 RD is active-high or RD/DIR input is high during read transfer and low during write

WSTRLVL

WR/STR input active level

changing this bit is only allowed when LOCK = 0

0 WR/STR is active-low

1 WR/STR is active-high

CSLVL CS input active level

changing this bit is only allowed when LOCK = 0

0 CS is active-low

1 CS is active-high

UCSG2 Register : (@1Eh)

X	**X**	**X**	**X**	**X**	**WACK**	**WDRV**	**WLVL**

WLVL WAIT/ACK output pin active level

changing this bit is only allowed when LOCK = 0

0 WAIT/ACK pin is active-low

1 WAIT/ACK pin is active-high

WDRV WAIT / ACK output pin structure

changing this bit is only allowed when LOCK = 0

0 WAIT/ACK buffer is open drain (or open source to VCC if active high)

1 WAIT/ACK buffer is push-pull

WACK WAIT/ACK pin function

changing this bit is only allowed when LOCK = 0

0 WAIT mode

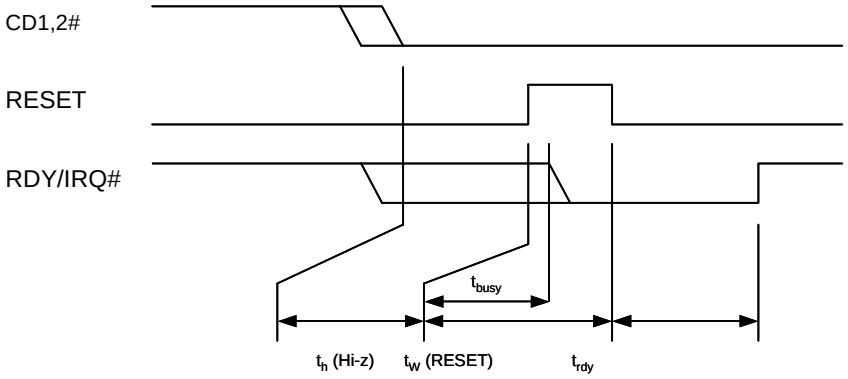
1 ACK mode

Module Detection & Activation

Common Interface modules are hot-plugable. In order to achieve this function, the CIMaX™ automatically detects the insertion and removal of a module and acts as programmed whenever this occurs.

In order to detect a module, the PC Card standard defines two reserved pins on the connector: CD1# and CD2#. They must be simultaneously asserted (grounded) to ensure a module is inserted. When a module is inserted, the CIMaX™ can automatically activate the module if programmed so when AUTO bit is asserted in the Module Control Register and VCC bit is set in the Power Control Register (modules VCC is on). The activation can also be handled manually by the host microprocessor by sequentially asserting the right bits in the Module Control Register. If both modules are inserted simultaneously, autoactivation procedure is performed sequentially on one module after the other.

The module activation consists in resetting the module and waiting for RDY signal to go high with respect to the PC Card standard timings.



Symbol		Min	Max	Unit
t_h (Hi-z)	Card detect to reset driven	300		ms
t_w (RESET)	Reset pulse width	11		µs
t_{busy} (informative)	Reset asserted to ready negated		10	µs
t_{rdy} (informative)	Reset negated to module ready		5	s

Interrupts

Interrupts are managed by CIMaX™ and one interrupt output is available for connecting CIMaX™ to the main microprocessor interrupt controller. Five interrupt sources are available : modules detection (2) modules IRQ (2) and one external device interrupt applied to the CIMaX™ by using the external interrupt input pin. Modules detection interrupts are latched inside the CIMaX™ and are acknowledged on the reading of the Interrupt Status Register. Each interrupt source can be individually masked. When masked, an incoming interrupt is visible in the Interrupt Status Register but does not generate an interrupt to the host microprocessor. The INT output to the host microprocessor can be configured to be active high or low and driven by a push-pull or an open drain.

Power

The CIMaX™ has 6 power pairs (VCC – GND):

Block	Pins	Description
Module interface	VCC_DVB1, VCC_DVB2, GND_DVB1, GND_DVB2	Two pairs of power supplies to drive all inputs and outputs from/to the two modules
Core logic	VCC_CORE, GND_CORE	One pair for core logic
Demod interface	VCC_TSI, GND_TSI	One pair for interfacing the TS input
Demux interface	VCC_TSO, GND_TSO	One pair for interfacing the TS output
Host microprocessor interface	VCC_PROC GND_PROC	One pair for interfacing host microprocessor control signals

The core power pair must be connected to a 3.3V power source.

The other pairs can be either connected to a 3.3V or 5V power source depending on the voltage required by the device connected to it.

The DVB1 and DVB2 pairs must be connected to the same power source.

Electrical Characteristics

Absolute Maximum Ratings

Symbol	Description	Min Value	Max Value	Unit
	Storage Ambient temperature	- 50	150	°C
T_A	Operating Ambient temperature	0	70	°C
V_{DD5}	5V Supply voltage	-0.5	5.5	V
V_{DD3}	Core Supply voltage	-0.5	3.6	V
	I/O voltage	-0.5	V_{DD} + 0.5	V

Notice: Stresses beyond those listed values may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended period may affect device reliability

DC Characteristics

Specified at V_{DD} = 5.0V (+/- 10%):

Symbol	Parameter	Min	Type	Max	Unit
V_{IL}	Input low voltage			0.8	V
V_{IH}	Input high voltage	2.0			V
V_{OL}	Output low voltage I_{OL} = 1.7 mA			0.5	V
V_{OH}	Output high voltage I_{OH} = -1.7 mA	$0.7 \times V_{DD}$			V
V_{T+}	Schmitt trigger positive threshold			1.74	V
V_{T-}	Schmitt trigger negative threshold	0.88			V
V_{HYST}	Schmitt trigger hysteresis		0.68		V
I_L	Input leakage current	-10		10	µA
I_{OZ}	Tristate output leakage current	-10		10	µA

Specified at V_{DD} = 3.3V (+/- 10%):

Symbol	Parameter	Min	Type	Max	Unit
V_{IL}	Input low voltage			0.8	V
V_{IH}	Input high voltage	2.0			V
V_{OL}	Output low voltage I_{OL} = -2 mA			0.4	V
V_{OH}	Output high voltage I_{OH} = -2 mA	$0.7 \times V_{DD}$			V
V_{T+}	Schmitt trigger positive threshold			1.74	V
V_{T-}	Schmitt trigger negative threshold	0.88			V

Symbol	Parameter	Min	Type	Max	Unit
V_{HYST}	Schmitt trigger hysteresis		0.68		V
I_L	Input leakage current	-10		10	µA
I_{OZ}	Tristate output leakage current	-10		10	µA

Power consumption

Some typical power consumptions are given below in the following conditions and limitations.

The power consumption due to the USCG module isn't available because depending on the application.

Temperature: ..... 25°C

CIMaX clock frequency: ..... 27 MHz

TS clock frequency: ..... 2.75 MHz

VCC core: 3.3V

VCC Padring: 5V

Capacitance on TS pins: ..... 30 pF max

Core power consumption:

Icore ..... 6.8 mA

Padring power consumption:

no TS activity, no module connected ..... 0.0 mA

TS bypassed TSin ÆTSout, VCC off ..... 0.67 mA

TS bypassed TSin ÆTSout, VCC on ..... 0.75 mA

TS through module A ..... 0.79 mA

TS through modules A and B ..... 0.83 mA

Input/Output Capacitances

The following table provides the Input and Output capacitance:

Symbol	Description	Test condition	Min	Type	Max	Unit
Cin	Inputs capacitance	3.3V		5.4		pF
Cout	Outputs capacitance	3.3V		8.6		pF
Cbid	Bi-directional buffers capacitance	3.3V		9.6		pF

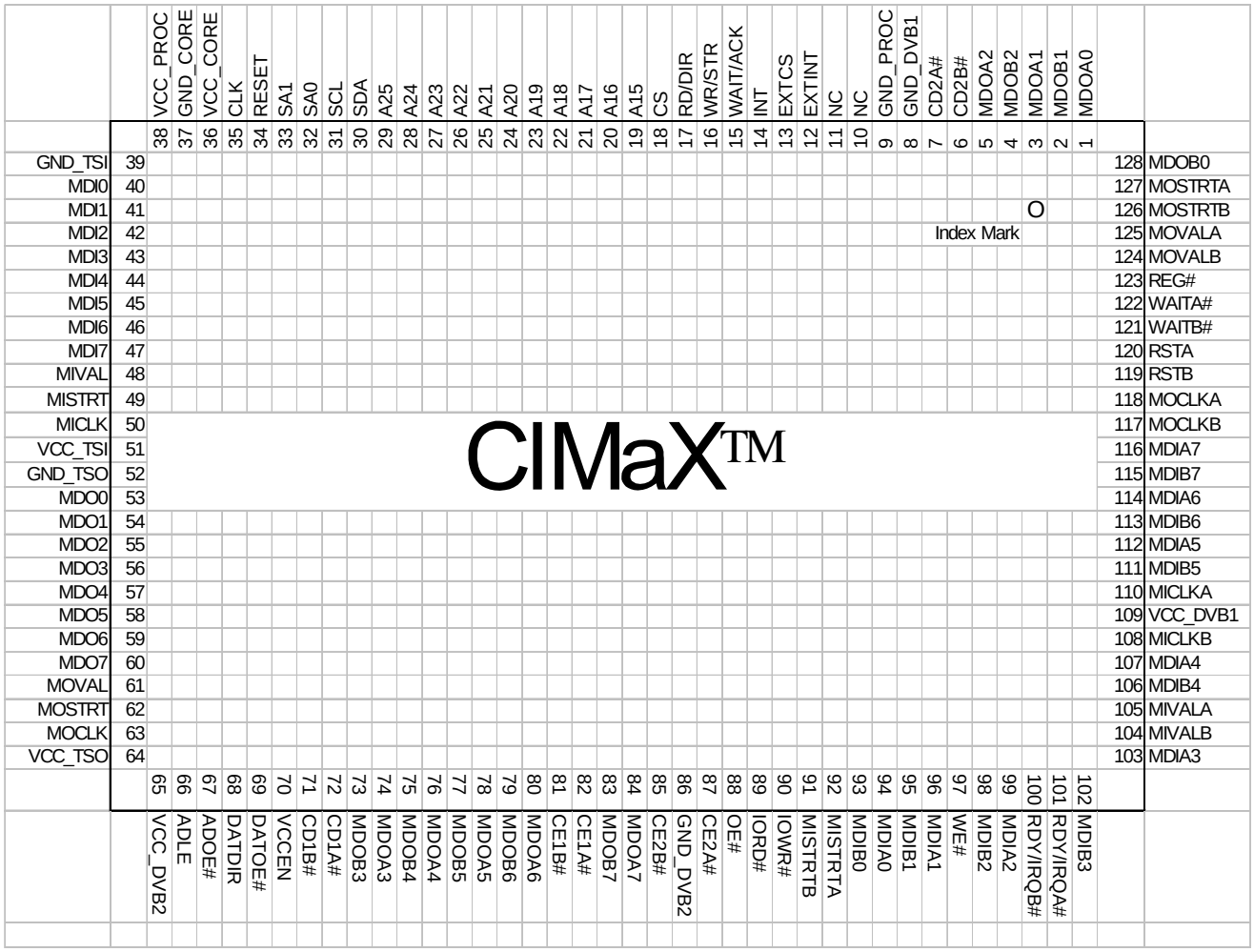
Pull-up/pull-down

The following table provides the internal pull-up and pull-down resistor values:

Symbol	Description	Min	Type	Max	Unit
up	pull-up resistor value		40		KΩ
down	pull-down resistor value		120		KΩ

Package

PQFP 128 pin configuration



Pinning

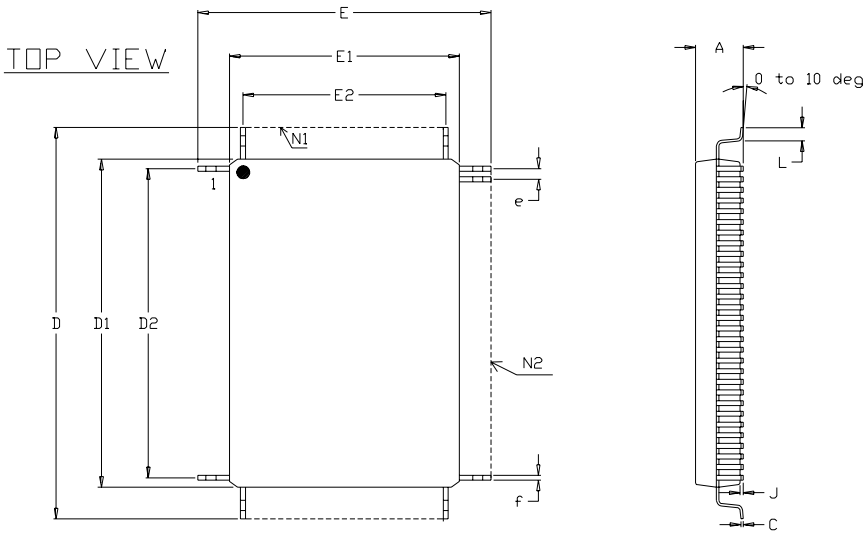
Name	Pin Nb
MDOA0	1
MDOB1	2
MDOA1	3
MDOB2	4
MDOA2	5
CD2B#	6
CD2A#	7
GND_DVB1	8
GND_PROC	9
NC	10
NC	11
EXTINT	12
EXTCS	13
INT	14
WAIT/ACK	15
WR/STR	16
RD/DIR	17
CS	18
A15	19
A16	20
A17	21
A18	22
A19	23
A20	24
A21	25
A22	26
A23	27
A24	28
A25	29
SDA	30
SCL	31
SA0	32
SA1	33
RESET	34

Name	Pin Nb
CLK	35
VCC_CORE	36
GND_CORE	37
VCC_PROC	38
GND_TSI	39
MDI0	40
MDI1	41
MDI2	42
MDI3	43
MDI4	44
MDI5	45
MDI6	46
MDI7	47
MIVAL	48
MISTRT	49
MICLK	50
VCC_TSI	51
GND_TSO	52
MDO0	53
MDO1	54
MDO2	55
MDO3	56
MDO4	57
MDO5	58
MDO6	59
MDO7	60
MOVAL	61
MOSTRT	62
MOCLK	63
VCC_TSO	64
VCC_DVB2	65
ADLE	66
ADOE#	67
DATDIR	68
DATOE#	69

Name	Pin Nb
VCCEN	70
CD1B#	71
CD1A#	72
MDOB3	73
MDOA3	74
MDOB4	75
MDOA4	76
MDOB5	77
MDOA5	78
MDOB6	79
MDOA6	80
CE1B#	81
CE1A#	82
MDOB7	83
MDOA7	84
CE2B#	85
GND_DVB2	86
CE2A#	87
OE#	88
IORD#	89
IOWR#	90
MISTRTB	91
MISTRTA	92
MDIB0	93
MDIA0	94
MDIB1	95
MDIA1	96
WE#	97
MDIB2	98
MDIA2	99
RDY/IRQB#	100
RDY/IRQA#	101
MDIB3	102
MDIA3	103
MIVALB	104

Name	Pin Nb
MIVALA	105
MDIB4	106
MDIA4	107
MICLKB	108
VCC_DVB1	109
MICLKA	110
MDIB5	111
MDIA5	112
MDIB6	113
MDIA6	114
MDIB7	115
MDIA7	116
MOCLKB	117
MOCLKA	118
RSTB	119
RSTA	120
WAITB#	121
WAITA#	122
REG#	123
MOVALB	124
MOVALA	125
MOSTRTB	126
MOSTRTA	127
MDOB0	128

Package outlines PQFP L 128 pin



	MM			INCH		
	min	nom	max	min	nom	max
A			3.400			.134
C	0.130		0.230	.005		.009
D	22.95	23.20	23.45	.904	.913	.923
D1	19.90	20.00	20.10	.783	.787	.791
D2	18.50 REF			.728 REF		
E	16.95	17.20	17.45	.667	.677	.687
E1	13.90	14.00	14.10	.547	.551	.555
E2	12.50 REF			.492 REF		
L	0.730		1.030	.029		.041
J	0.250	0.330		.010	.013	
e	0.500 BSC			.020 BSC		
f	0.130		0.280	.005		.011
N1	26			26		
N2	38			38		

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