



3.3V CMOS 18-BIT READ/WRITE BUFFER WITH 5 VOLT TOLERANT I/O AND BUS-HOLD

IDT74LVCH16701A

FEATURES:

- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{cc} = 3.3V \pm 0.3V$, Normal Range
- $V_{cc} = 2.7V$ to $3.6V$, Extended Range
- CMOS power levels (0.4 μ W typ. static)
- All inputs, outputs, and I/O are 5V tolerant
- Supports hot insertion
- Available in SSOP, TSSOP, and TVSOP packages

DRIVE FEATURES:

- High Output Drivers: $\pm 24mA$
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

DESCRIPTION:

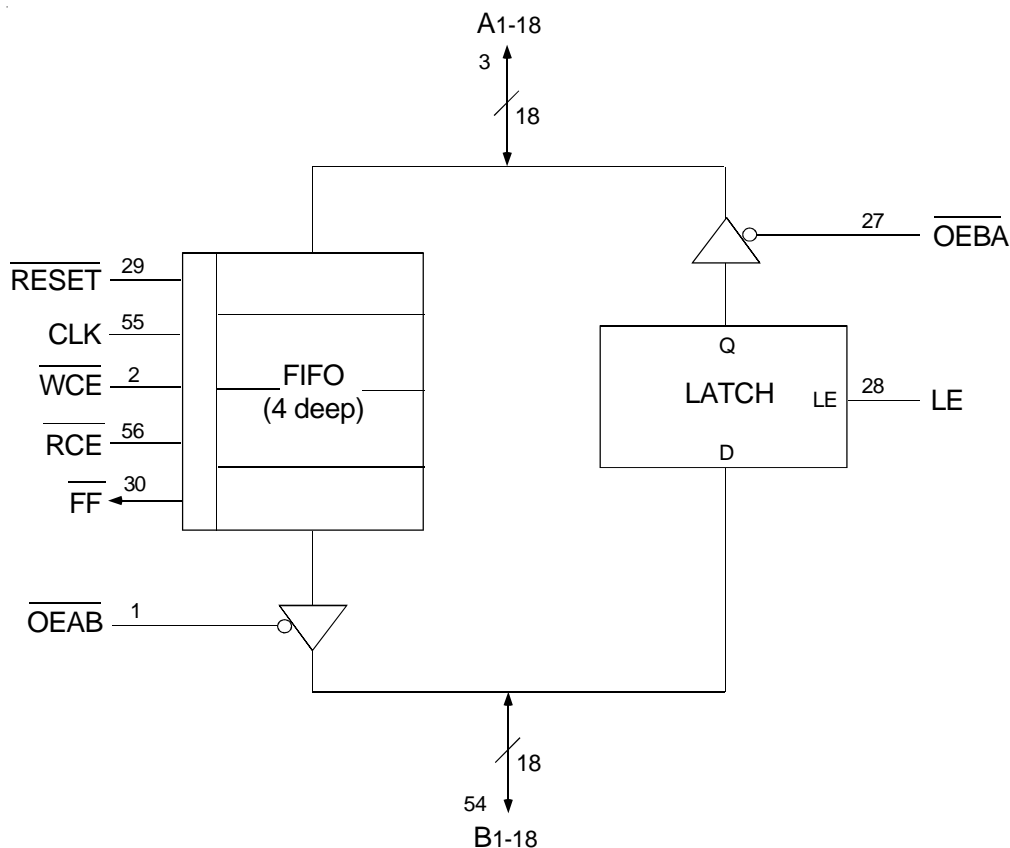
The LVCH16701A 18-bit read/write buffer is built using advanced dual metal CMOS technology. The device is designed as an 18-bit read/write buffer with a four deep FIFO and a read-back latch. It can be used as a read/write buffer between a CPU and a memory or to interface a high-speed bus and a slow peripheral. The A-to-B (write) path has a four deep FIFO for pipelined operations. The FIFO can be reset and a FIFO full condition is indicated by the full flag (\overline{FF}). The B-to-A (read) path has a latch.

All pins can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVCH16701A has been designed with a $\pm 24mA$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The LVCH16701A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM

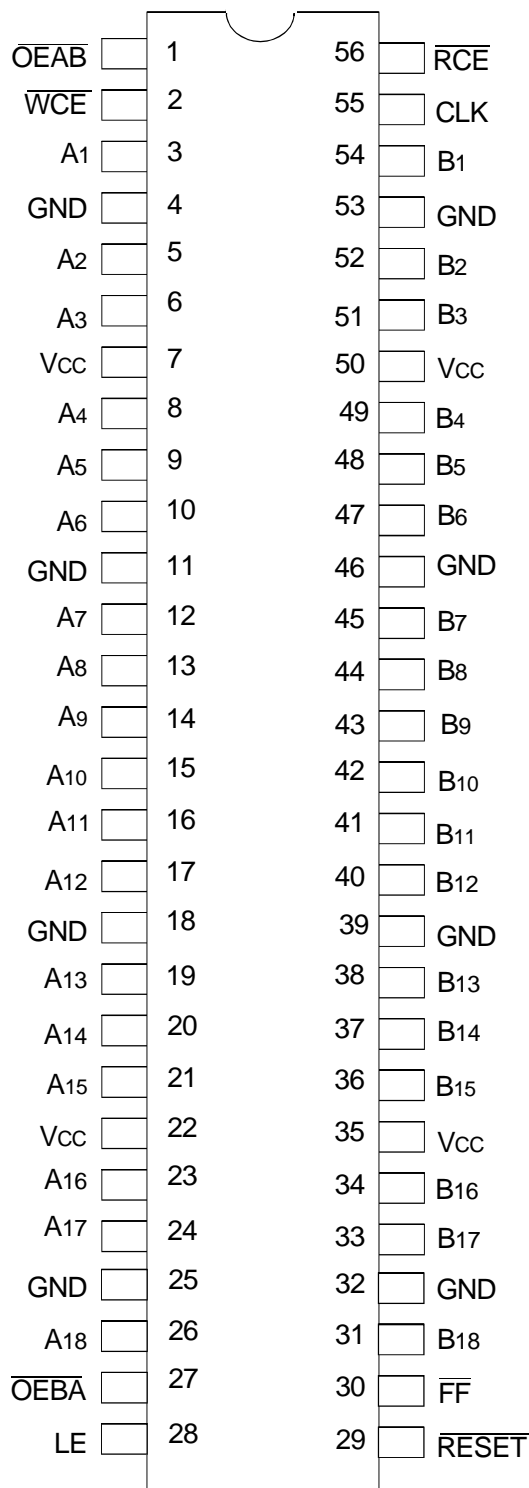


The IDT logo is a registered trademark of Integrated Device Technology, Inc.

INDUSTRIAL TEMPERATURE RANGE

OCTOBER 1999

PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +6.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-50 to +50	mA
I _{IK} I _{OK}	Continuous Clamp Current, V _I < 0 or V _O < 0	-50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	6.5	8	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	6.5	8	pF

NOTE:

1. As applicable to the device type.

PIN DESCRIPTION

Pin Names	I/O	Description
A1-18	I/O	18 bit I/O port ⁽¹⁾
B1-18	I/O	18 bit I/O port ⁽¹⁾
CLK	I	Clock for write path FIFO. Clocks data into FIFO when \overline{WCE} is low, clocks data out of FIFO when \overline{RCE} is low. When FIFO is full all further writes to the FIFO are inhibited. When FIFO is empty all reads from the FIFO are inhibited. CLK also resets the FIFO when \overline{RESET} is low.
\overline{WCE}	I	Enable pin for FIFO input clock (Active LOW)
\overline{RCE}	I	Enable pin for FIFO output clock (Active LOW)
\overline{FF}	O	Write path FIFO full flag. Goes low when FIFO is full.
\overline{RESET}	I	Synchronous FIFO reset - when low CLK resets the FIFO. The FIFO pointers are initialized to the "empty" condition and FIFO output is forced high (all ones). The FIFO full flag (\overline{FF}) will be high immediately after reset. (Active LOW)
\overline{OEAB}	I	Output Enable pin for B port (Active LOW)
\overline{OEBA}	I	Output Enable pin for A port (Active LOW)
LE	I	Read path latch enable pin. When high, data flows transparently from B port to A port, B data is latched on the falling edge of LE. (Note: LE is independent of CLK and data)

NOTE:

1. These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE⁽¹⁾

Inputs					Outputs		Notes
\overline{OEBA}	\overline{OEAB}	LE	\overline{RESET}	CLK	Ax	Bx	
H	H	H	H	↑	Q ⁽²⁾ (B) Bus Hold	Q ⁽²⁾ (A) -4CLKS Bus Hold	
L	H	H	H	↑	B to A		Transparent Mode
L	H	L	H	↑	Q ₀ (B)		
H	H	X	H	↑	Q ⁽²⁾ (A) Bus Hold	Q ⁽²⁾ (B) Bus Hold	
H	L	X	H	↑		A to B - 4 CLKS	
L	L	L	H	↑	Q ⁽²⁾ (B) Bus Hold	Q ⁽²⁾ (B) - 4 CLKS Bus Hold	Case not recommended

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition
- Level of Q before the indicated steady-state input conditions were established.

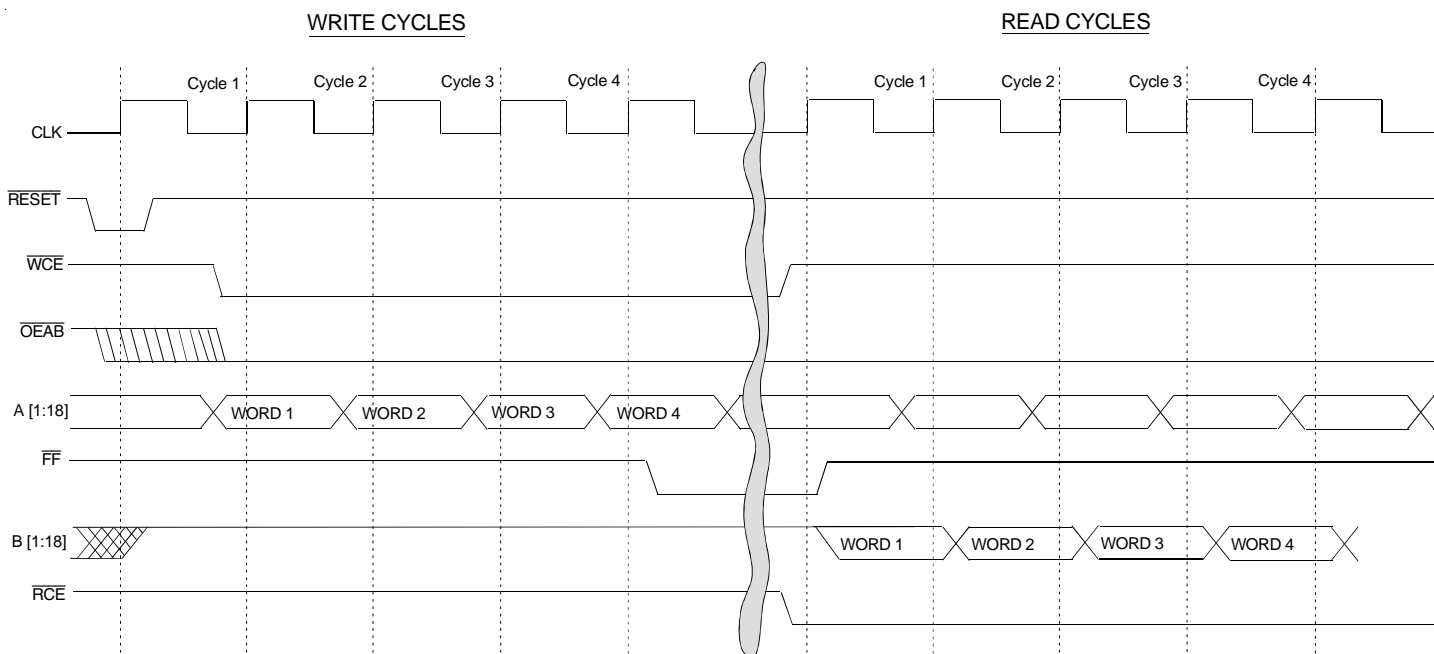
FUNCTIONAL DESCRIPTION

This device is useful as a read/write buffer for modular high end designs. It provides multi-level buffering in the write path and single deep buffering in the read path, and is suited to write back cache implementation. The read path provides a transparent latch.

The four deep FIFO uses one clock with two clock enable pins, \overline{WCE} and \overline{RCE} to clock data in and out. The FIFO has an external full flag which goes LOW when the FIFO is full. Internal read and write pointers keep track of the words stored in the FIFO. A write attempt to a full FIFO is ignored. An attempt to read from an empty FIFO will have no effect and the last read data

remains at the output of the FIFO. The FIFO may be reset by the synchronous \overline{RESET} input. This resets the read and write pointers to the original "empty" condition and also sets all B outputs = 1. Simultaneous read and write attempts (clock data into FIFO as well as clock data out of FIFO) are possible except on FIFO empty and full boundaries. When the FIFO is empty, and a simultaneous read and write is attempted, the read is ignored while the write is executed. If the same is attempted when the FIFO is full, the write is ignored while the read is executed. Normal operation of the four deep FIFO in the write path is independent of the read path operation.

TIMING DIAGRAM



DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to 5.5V	—	—	± 5	μA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = 0$ to 5.5V	—	—	± 10	μA
I_{OFF}	Input/Output Power Off Leakage	$V_{CC} = 0\text{V}$, V_{IN} or $V_O \leq 5.5\text{V}$		—	—	± 50	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$	$V_{IN} = \text{GND}$ or V_{CC}	—	—	10	μA
			$3.6 \leq V_{IN} \leq 5.5\text{V}^{(2)}$	—	—	10	
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$, other inputs at V_{CC} or GND		—	—	500	μA

NOTES:

- Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.
- This applies in the disabled state only.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
IBHH IBHL	Bus-Hold Input Sustain Current	V _{CC} = 3V	V _I = 2V	-75	—	—	μA
			V _I = 0.8V	75	—	—	
IBHH IBHL	Bus-Hold Input Sustain Current	V _{CC} = 2.3V	V _I = 1.7V	—	—	—	μA
			V _I = 0.7V	—	—	—	
IBHHO IBHLO	Bus-Hold Input Overdrive Current	V _{CC} = 3.6V	V _I = 0 to 3.6V	—	—	±500	μA

NOTES:

1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = -0.1mA	V _{CC} - 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = -6mA	2	—	
		V _{CC} = 2.3V	I _{OH} = -12mA	1.7	—	
		V _{CC} = 2.7V		2.2	—	
		V _{CC} = 3V		2.4	—	
		V _{CC} = 3V	I _{OH} = -24mA	2	—	
VOL	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 6mA	—	0.4	
			I _{OL} = 12mA	—	0.7	
		V _{CC} = 2.7V	I _{OL} = 12mA	—	0.4	
		V _{CC} = 3V	I _{OL} = 24mA	—	0.55	

NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = -40°C to +85°C.

OPERATING CHARACTERISTICS, V_{CC} = 3.3V ± 0.3V, T_A = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation \overline{WCE} Mode, $\overline{OEAB} = 0$	C _L = 0pF, f = 10Mhz		pF
CPD	Power Dissipation \overline{RCE} Mode, $\overline{OEBA} = 0$			
CPD	Registered Channel (B to A) Power Dissipation $\overline{OEBA} = 0$; $\overline{CE} = 0$			
CPD	Registered Channel Power Dissipation $\overline{OEBA} = 0$; $\overline{CE} = 1$			

SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	Test Conditions	V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Unit
			Min.	Max.	Min.	Max.	
PROPAGATION DELAYS							
1	B1-18 to A1-18	Read path/latch			2	4.5	ns
2	LE (LOW to HIGH) to A1-18	Read path/latch			2	4.8	ns
3	CLK to \overline{FF}	Write path			1.5	6	ns
4	CLK to B1-18	Write path			1.5	6	ns
5	Output Skew ⁽²⁾	Write path			—	1	ns
SETUP & HOLD TIMES							
6	A1-18 to CLK (LOW to HIGH) Setup	Write path			1.5	—	ns
7	A1-18 to CLK (LOW to HIGH) Hold	Write path			0.9	—	ns
8	B1-18 to LE (HIGH to LOW) Setup	Read path/latch			1.2	—	ns
9	B1-18 to LE (HIGH to LOW) Hold	Read path/latch			1	—	ns
10	\overline{WCE} , \overline{RCE} (LOW) to CLK Setup	Write path			3.5	—	ns
11	\overline{WCE} , \overline{RCE} (LOW) to CLK Hold	Write path			0	—	ns
12	\overline{RESET} (LOW) to CLK Setup	Write path			1.8	—	ns
13	\overline{RESET} (LOW) to CLK Hold	Write path			0.6	—	ns
ENABLE & DISABLE TIMES							
14	\overline{OEBA} LOW to A1-18 Enable	Write path			1.5	6	ns
15	\overline{OEBA} HIGH to A1-18 Disable	Write path			1.5	5.7	ns
16	\overline{OEBA} LOW to B1-18 Enable	Read path			1.5	6	ns
17	\overline{OEBA} HIGH to B1-18 Disable	Read path			1.5	5.7	ns
MINIMUM PULSE WIDTHS							
18	CLK HIGH or LOW Pulse Width	Write path			5	—	ns
19	LE HIGH Pulse Width	Read path/latch			5	—	ns
19	Clock Frequency					83	MHz
20	Clock Cycle Time				12		ns

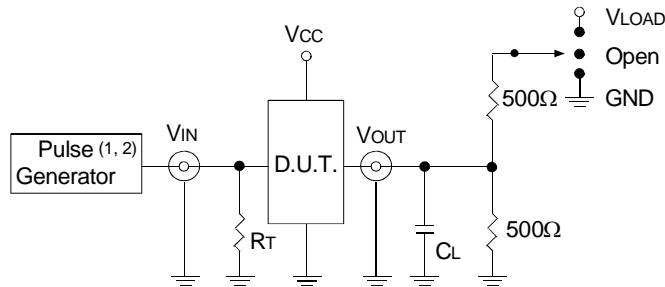
NOTES:

1. See TEST CIRCUITS AND WAVEFORMS. T_A = - 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} ⁽¹⁾ =3.3V±0.3V	V _{CC} ⁽¹⁾ =2.7V	V _{CC} ⁽²⁾ =2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF



LVC Link

Test Circuit for All Outputs

DEFINITIONS:

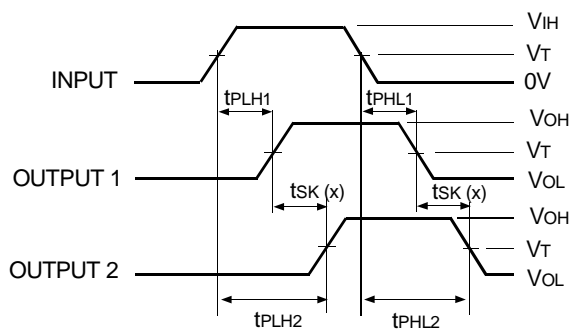
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other Tests	Open



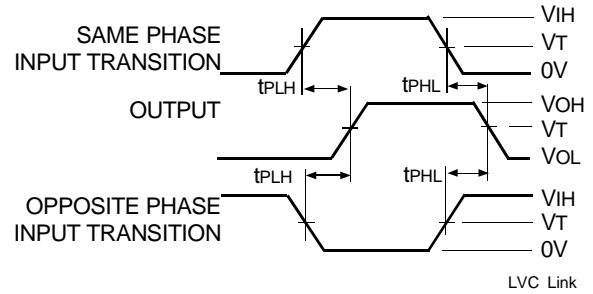
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

LVC Link

Output Skew - t_{SK}(x)

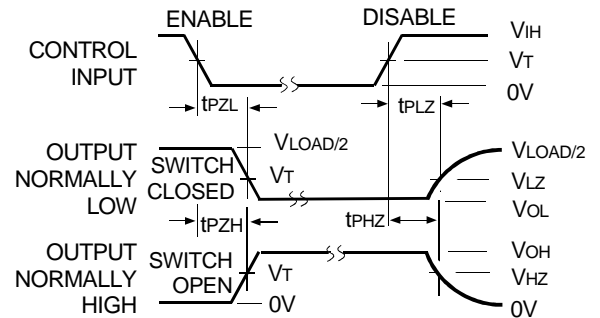
NOTES:

1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.



LVC Link

Propagation Delay

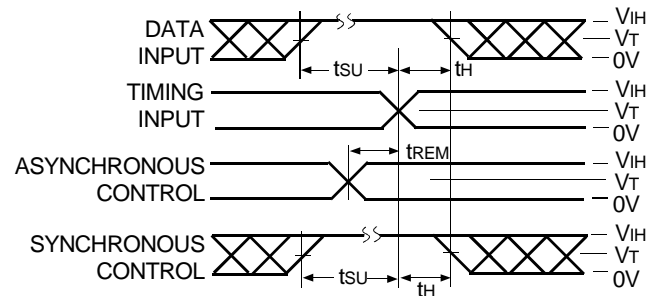


LVC Link

Enable and Disable Times

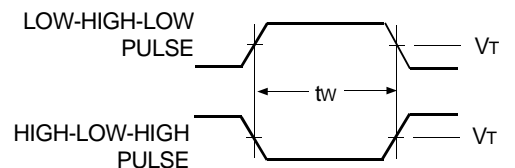
NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



LVC Link

Set-up, Hold, and Release Times



LVC Link

Pulse Width

