FEATURES

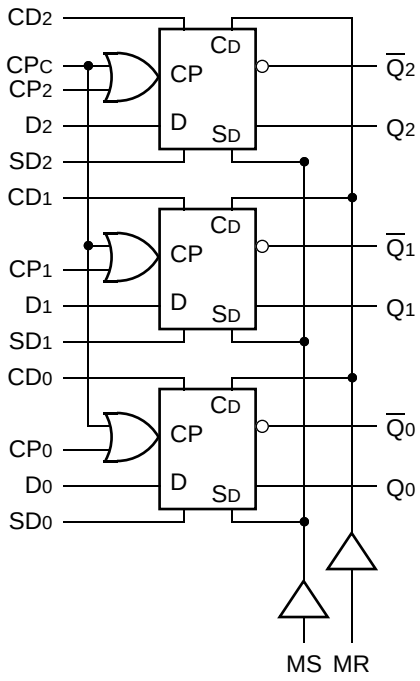
- **Max. toggle frequency of 800MHz**
- **Differential outputs**
- **I_{EE} min. of –80mA**
- **Industry standard 100K ECL levels**
- **Extended supply voltage option: V_{EE} = –4.2V to –5.5V**
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **150% faster than Fairchild**
- **40% lower power than Fairchild**
- **Function and pinout compatible with Fairchild F100K**
- **Available in 24-pin CERPACK and 28-pin PLCC packages**

DESCRIPTION

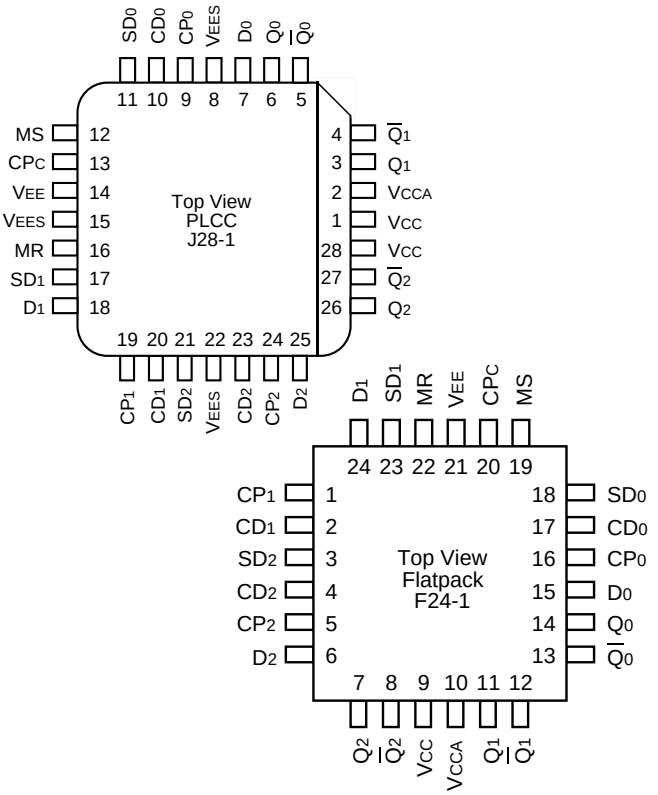
The SY100S331 offers three D-type, edge-triggered master/slave flip-flops with true and complement outputs, designed for use in high-performance ECL systems. Each flip-flop is controlled by a common clock (CP_C), as well as its own clock pulse (CP_n). The resultant clock signal controlling the flip-flop is the logical OR operation of these two clock signals. Data enters the master when both CP_C and CP_n are LOW and enters the slave on the rising edge of either CP_C or CP_n (or both).

Additional control signals include Master Set (MS) and Master Reset (MR) inputs. Each flip-flop also has its own Direct Set (SD_n) and Direct Clear (CD_n) signals. The MR, MS, SD_n and DC_n signals override the clock signals. The inputs on this device have 75KΩ pull-down resistors.

BLOCK DIAGRAM



PIN CONFIGURATIONS



Rev.: G Amendment: /0
Issue Date: July, 1999

PIN NAMES

Pin	Function
$CP_0 – CP_2$	Individual Clock Inputs
CP_C	Common Clock Input
$D_0 – D_2$	Data Inputs
$CD_0 – CD_2$	Individual Direct Clear Inputs
SD_n	Individual Direct Set Inputs
MR	Master Reset Input
MS	Master Set Input
$Q_0 – Q_2$	Data Outputs
$\overline{Q}_0 – \overline{Q}_2$	Complementary Data Outputs
V_{EES}	V_{EE} Substrate
V_{CCA}	V_{CCO} for ECL Outputs

TRUTH TABLES

Asynchronous Operation[1]					
Inputs					Outputs
D_n	CP_n	CP_C	MS SD_n	MR DC_n	Q_n (t+1)
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

NOTE:

1. H = High Voltage Level, L = Low Voltage Level, X = Don't Care, U = Undefined, t = Time before CP Positive Transition, t+1 = Time after CP Positive Transition, u = Low-to-High Transition

Synchronous Operation[1]					
Inputs					Outputs
D_n	CP_n	CP_C	MS SD_n	MR DC_n	Q_n
L	u	L	L	L	L
H	u	L	L	L	H
L	L	u	L	L	L
H	L	u	L	L	H
X	L	L	L	L	Q_n (t)
X	H	X	L	L	Q_n (t)
X	X	H	L	L	Q_n (t)

NOTE:

1. H = High Voltage Level, L = Low Voltage Level, X = Don't Care, U = Undefined, t = Time before CP Positive Transition, t+1 = Time after CP Positive Transition, u = Low-to-High Transition

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current, All Inputs	—	—	200	µA	V_{IN} = V_{IH} (Max.)
I_{EE}	Power Supply Current	–80	–65	–35	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERPACK

V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND

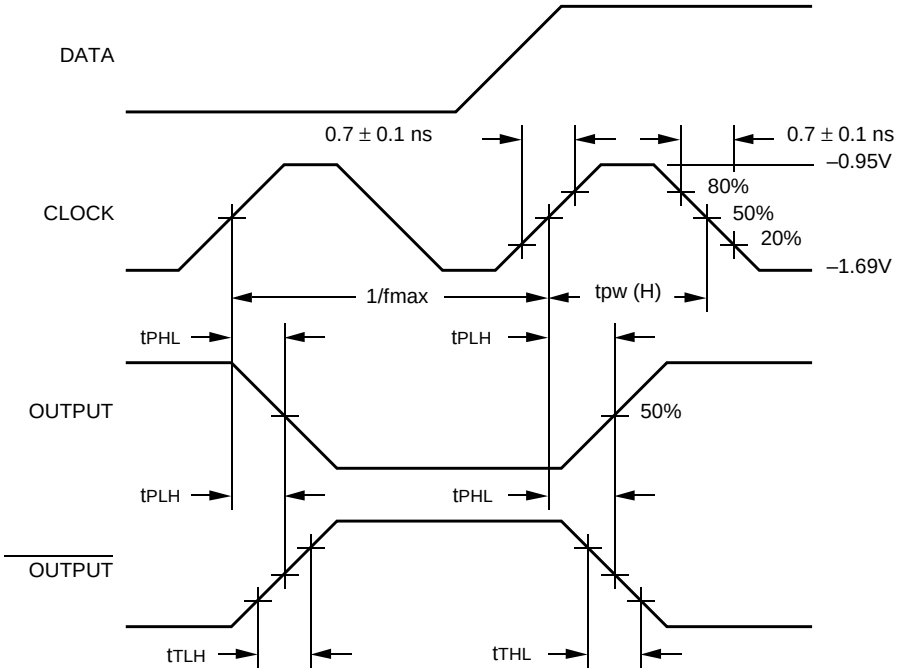
Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{max}	Toggle Frequency	800	—	800	—	800	—	MHz	
t_{PLH} t_{PHL}	Propagation Delay CP_c to Output	300	800	300	800	300	800	ps	
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	300	800	300	800	300	800	ps	
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n to Output	300	900	300	900	300	900	ps	
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	300	1000	300	1000	300	1000	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t_S	Set-up Time D_n CD_n, SD_n (Release Time) MS, MR (Release Time)	 400 500 800	 — — —	 400 500 800	 — — —	 400 500 800	 — — —	ps	
t_H	Hold Time D_n	300	—	300	—	300	—	ps	
t_{pw} (H)	Pulse Width HIGH CP_n, CP_c, DC_n SD_n, MR, MS	800	—	800	—	800	—	ps	

PLCC

V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{max}	Toggle Frequency	800	—	800	—	800	—	MHz	
t_{PLH} t_{PHL}	Propagation Delay CP_c to Output	300	700	300	700	300	700	ps	
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	300	700	300	700	300	700	ps	
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n to Output	300	800	300	800	300	800	ps	
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	300	900	300	900	300	900	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t_S	Set-up Time D_n CD_n, SD_n (Release Time) MS, MR (Release Time)	 400 500 800	 — — —	 400 500 800	 — — —	 400 500 800	 — — —	ps	
t_H	Hold Time D_n	300	—	300	—	300	—	ps	
t_{pw} (H)	Pulse Width HIGH CP_n, CP_c, DC_n SD_n, MR, MS	800	—	800	—	800	—	ps	

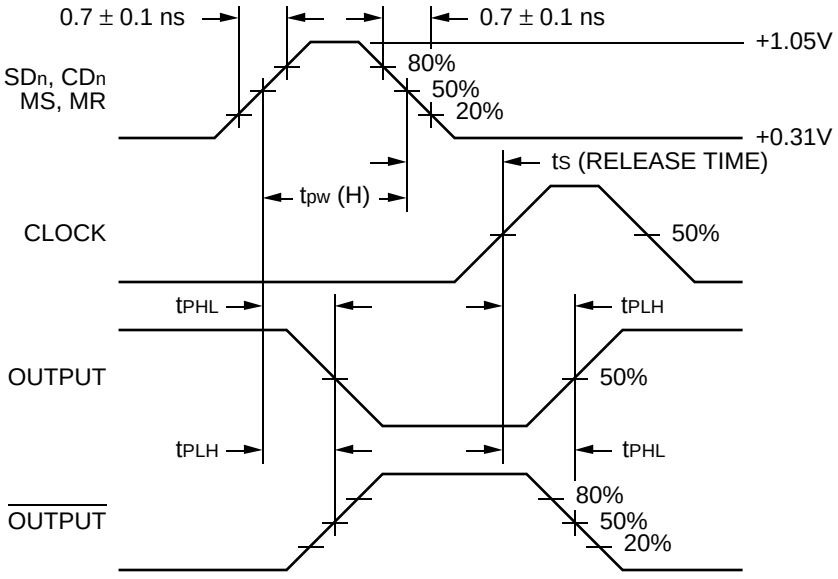
TIMING DIAGRAMS



Propagation Delay (Clock) and Transition Times

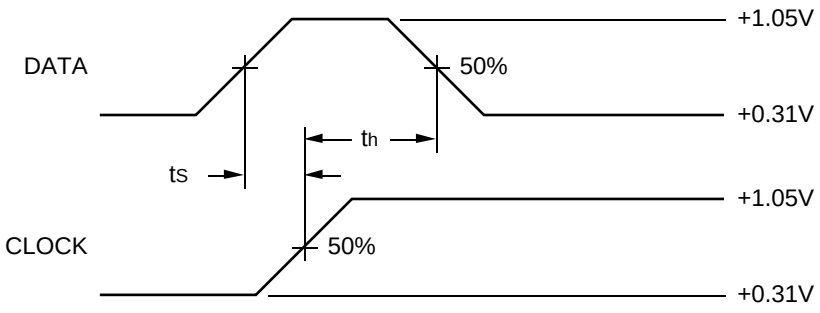
NOTE:

V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND



Propagation Delay (Sets and Resets)

TIMING DIAGRAMS



Data Setup and Hold Time

NOTES:

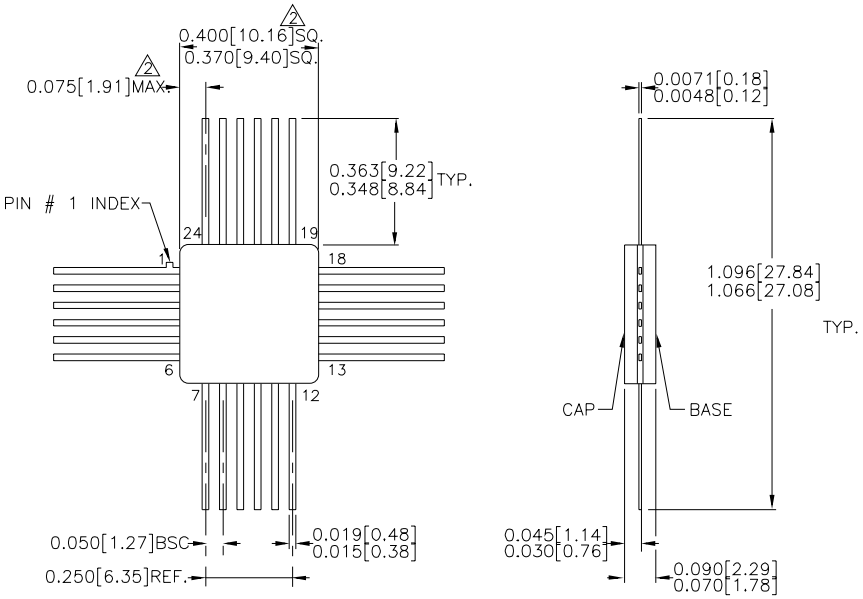
t_s is the minimum time before the transition of the clock that information must be present at the data input.

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S331FC	F24-1	Commercial
SY100S331JC	J28-1	Commercial
SY100S331JCTR	J28-1	Commercial

24 LEAD CERPACK (F24-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

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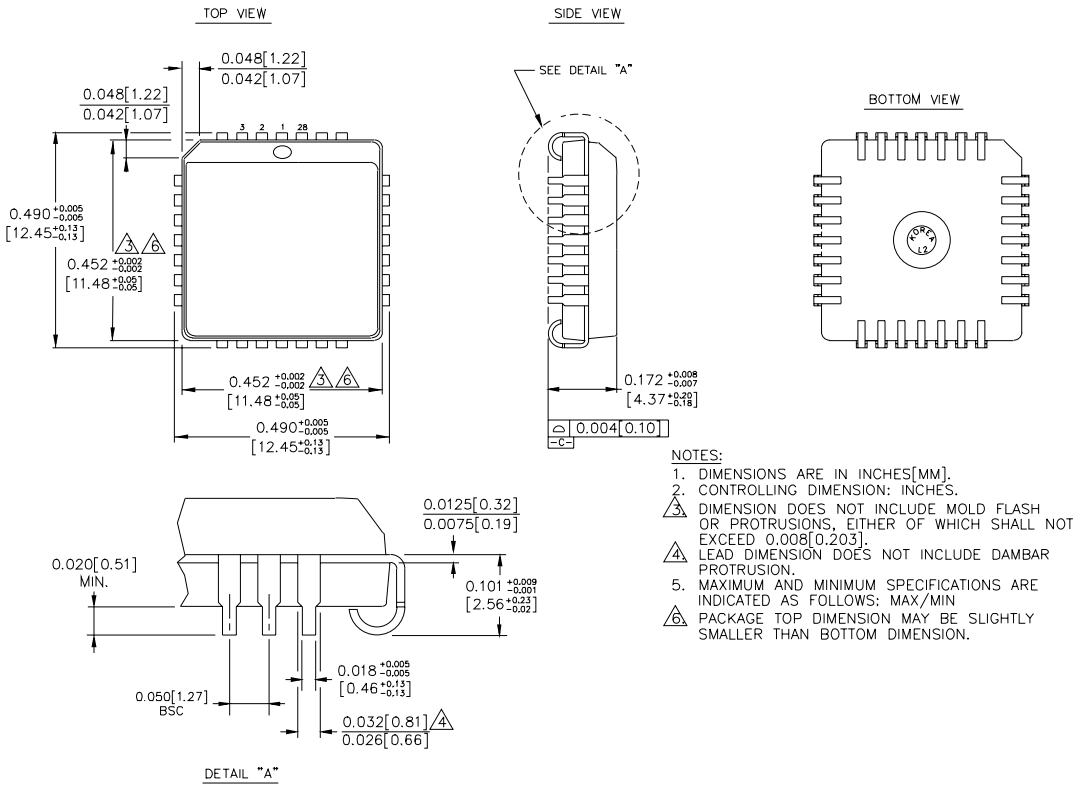
28 LEAD PLCC (J28-1)



Rev. 03

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