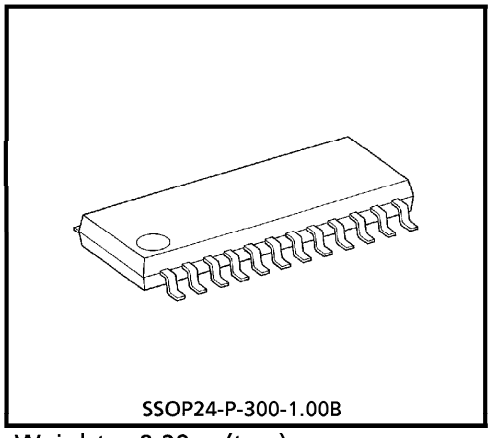
TENTATIVE

TOSHIBA INTELLIGENT POWER DEVICE
SILICON MONOLITHIC POWER MOS INTEGRATED CIRCUIT

TPD7201F

POWER MOSFET GATE DRIVER FOR 3-PHASE DC MOTOR

TPD7201F is a power MOSFET Gate Driver for 3-Phase full-bridge circuit using charge pump system. Because this IC contains a charge pump circuit for high-side drive, it allows you to configure 3-phase full-bridge circuit.



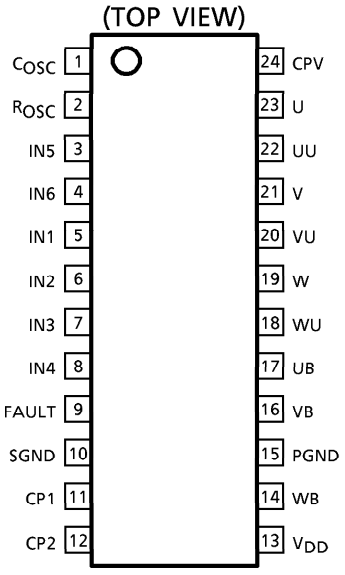
SSOP24-P-300-1.00B

Weight : 0.29 g (typ.)

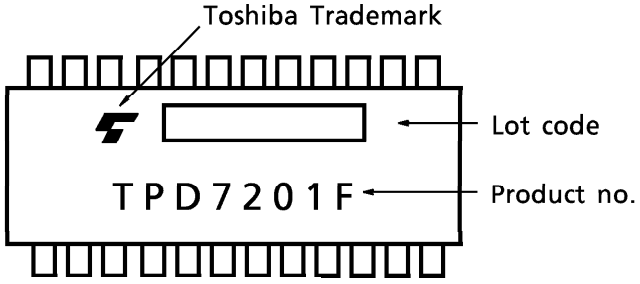
FEATURES

- Power MOSFET Gate Driver for 3-Phase DC Motor
- Built-in power MOSFET protection and diagnosis functions: overvoltage and low-voltage protection
- Built-in a charge pump circuit
- Package: SSOP-24 (300 mil) with embossed-tape packing

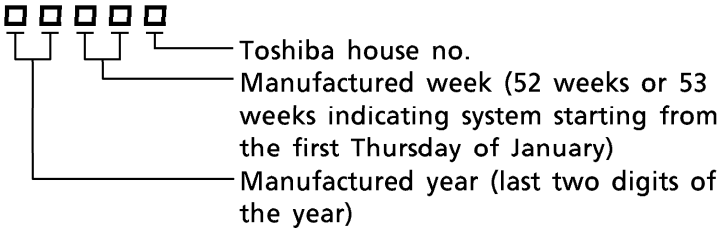
PIN ASSIGNMENT



MARKING



Lot code naming system

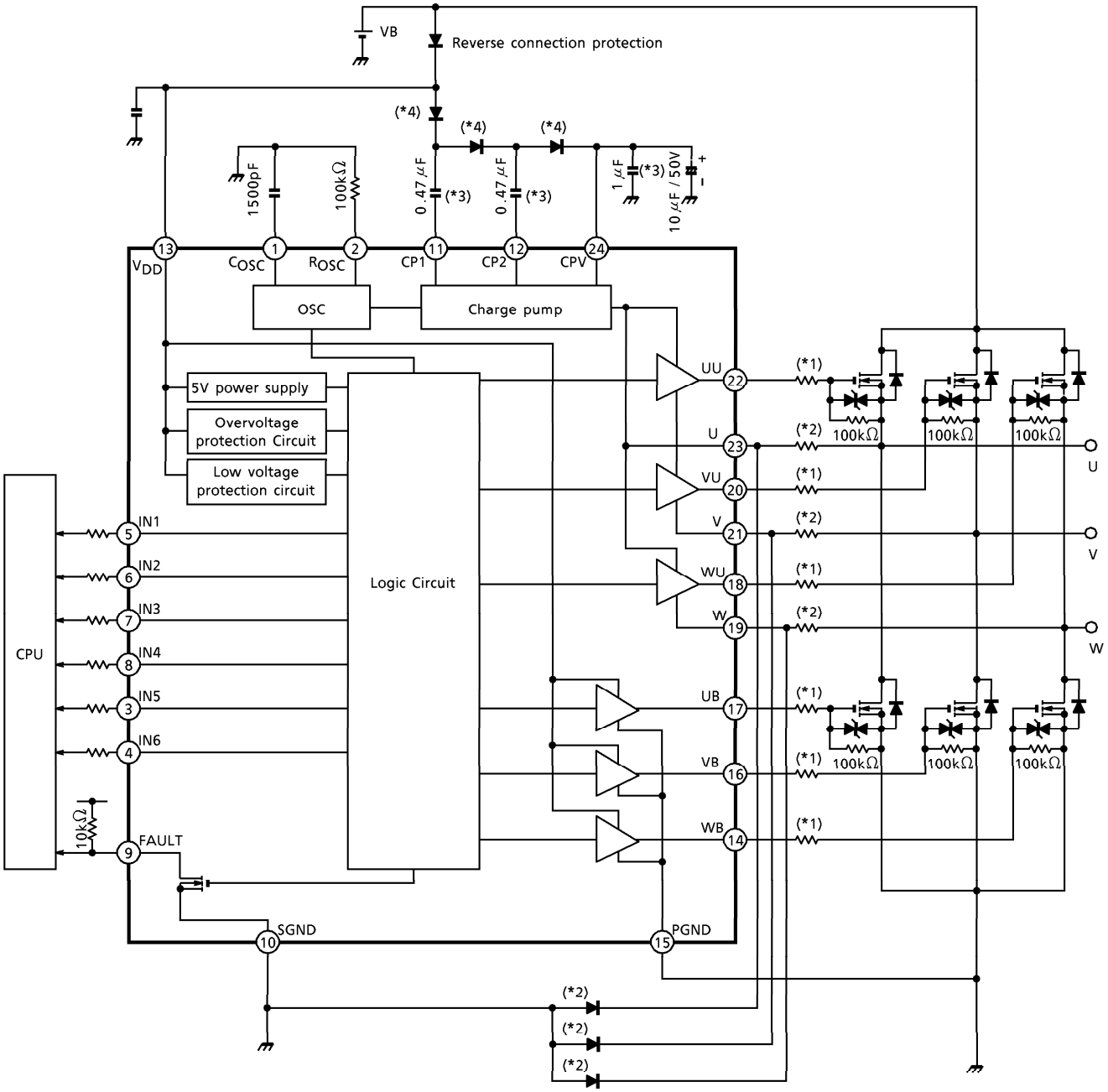


Because this product uses MOS structure, must take special care with electrostatic when handling.

980910EBA2

TENTATIVE

BLOCK DIAGRAM / APPLICATION CIRCUIT



(*1) : Optimum conditions depend on switching loss, EMI, etc. of external MOSFET.
(*2) : SBD V_F = 0.5 V max (Recommended : CRS03)
This is need when the U, V and W pin is biased to the negative side by more than 0.5 V.
(*3) : This is a laminated ceramic capacitor.
(*4) : High-speed diode t_{rr} = 100 ns max (Recommended : CRH01)

(Note) : When selecting external parts, please read "Method for selecting external parts" described later.

TENTATIVE

PIN DESCRIPTION

PIN No.	SYMBOL	PIN DESCRIPTION
1	C_{OSC}	This pin sets the oscillation frequency for charge pump drive. Connect a 1500 pF (recommended) capacitor.
2	R_{OSC}	This pin sets the oscillation frequency for charge pump drive. Connect a 100 kΩ (recommended) resistor.
3	IN5	Input pin: it controls the power MOSFET connected to VB and built-in pull-down resistor (100 kΩ typ.)
4	IN6	Input pin: it controls the power MOSFET connected to WB and built-in pull-down resistor (100 kΩ typ.)
5	IN1	Input pin: it controls the power MOSFET connected to UU and built-in pull-down resistor (100 kΩ typ.)
6	IN2	Input pin: it controls the power MOSFET connected to VU and built-in pull-down resistor (100 kΩ typ.)
7	IN3	Input pin: it controls the power MOSFET connected to WU and built-in pull-down resistor (100 kΩ typ.)
8	IN4	Input pin: it controls the power MOSFET connected to UB and built-in pull-down resistor (100 kΩ typ.)
9	FAULT	Diagnosis output pin: when low-voltage 6 V (typ.) or overvoltage 22 V (typ.) is detected, output "H". Circuit configuration is N-ch open drain.
10	SGND	Signal block GND pin
11	CP1	Capacitor pin for charge pump Connect a 0.47 μF (recommended) laminated ceramic capacitor.
12	CP2	Capacitor pin for charge pump Connect a 0.47 μF (recommended) laminated ceramic capacitor.
13	V_{DD}	Power supply pin: when low voltage (6 V typ.) or overvoltage (22 V typ.) is detected, all outputs are shut down.
14	WB	Drives the power MOSFET connected to the low side of W phase.
15	PGND	Power block GND pin
16	VB	Drives the power MOSFET connected to the low side of V phase.
17	UB	Drives the power MOSFET connected to the low side of U phase.
18	WU	Drives the power MOSFET connected to the high side of W phase.
19	W	W phase output pin
20	VU	Drives the power MOSFET connected to the high side of V phase.
21	V	V phase output pin
22	UU	Drives the power MOSFET connected to the high side of U phase.
23	U	U phase output pin
24	CPV	Final stage capacitor for the charge pump Connect 1 μF (recommended) laminated ceramic capacitor and 10 μF (recommended) aluminum electrolytic capacitor in parallel.

TENTATIVE

TRUTH TABLE (All outputs go low for input in High side / Low side arm shorting mode)

MODE No.	INPUT						OUTPUT						REMARKS
	IN1 (UU)	IN2 (VU)	IN3 (WU)	IN4 (UB)	IN5 (VB)	IN6 (WB)	OUT UU	OUT VU	OUT WU	OUT UB	OUT VB	OUT WB	
01	L	L	L	L	L	L	L	L	L	L	L	L	
02	H	L	L	L	L	L	H	L	L	L	L	L	
03	L	H	L	L	L	L	L	H	L	L	L	L	
04	L	L	H	L	L	L	L	L	H	L	L	L	
05	L	L	L	H	L	L	L	L	L	H	L	L	
06	L	L	L	L	H	L	L	L	L	L	H	L	
07	L	L	L	L	L	H	L	L	L	L	L	H	
08	H	L	L	H	L	L	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
09	H	L	L	L	H	L	H	L	L	L	H	L	120 ° square wave conducting normal mode
10	H	L	L	L	L	H	H	L	L	L	L	H	120 ° square wave conducting normal mode
11	L	H	L	H	L	L	L	H	L	H	L	L	120 ° square wave conducting normal mode
12	L	H	L	L	H	L	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
13	L	H	L	L	L	H	L	H	L	L	L	H	120 ° square wave conducting normal mode
14	L	L	H	H	L	L	L	L	H	H	L	L	120 ° square wave conducting normal mode
15	L	L	H	L	H	L	L	L	H	L	H	L	120 ° square wave conducting normal mode
16	L	L	H	L	L	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
17	H	H	L	L	L	L	H	H	L	L	L	L	
18	L	H	H	L	L	L	L	H	H	L	L	L	
19	H	L	H	L	L	L	H	L	H	L	L	L	
20	L	L	L	H	H	L	L	L	L	H	H	L	
21	L	L	L	L	H	H	L	L	L	L	H	H	
22	L	L	L	H	L	H	L	L	L	H	L	H	
23	H	H	L	H	L	L	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
24	H	H	L	L	H	L	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
25	H	H	L	L	L	H	H	H	L	L	L	H	
26	L	H	H	H	L	L	L	H	H	H	L	L	
27	L	H	H	L	H	L	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
28	L	H	H	L	L	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
29	H	L	H	H	L	L	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
30	H	L	H	L	H	L	H	L	H	L	H	L	

(*) : High side / Low side arm shorting mode is disabled by the internal logic. (FAULT is kept low.) When undervoltage (6 V typ.) or overvoltage (22 V typ.) is detected, all outputs are pulled low regardless of input signals. At this time, FAULT output goes high (open-drain, high-impedance).

TENTATIVE

TRUTH TABLE (All outputs go low for input in High side / Low side arm shorting mode)

MODE No.	INPUT						OUTPUT						REMARKS
	IN1 (UU)	IN2 (VU)	IN3 (WU)	IN4 (UB)	IN5 (VB)	IN6 (WB)	OUT UU	OUT VU	OUT WU	OUT UB	OUT VB	OUT WB	
31	H	L	H	L	L	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
32	H	L	L	H	H	L	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
33	H	L	L	L	H	H	H	L	L	L	H	H	
34	H	L	L	H	L	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
35	L	H	L	H	H	L	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
36	L	H	L	L	H	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
37	L	H	L	H	L	H	L	H	L	H	L	H	
38	L	L	H	H	H	L	L	L	H	H	H	L	
39	L	L	H	L	H	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
40	L	L	H	H	L	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
41	H	H	H	L	L	L	H	H	H	L	L	L	
42	L	L	L	H	H	H	L	L	L	H	H	H	
43	H	H	L	H	H	L	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
44	H	H	L	L	H	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
45	H	H	L	H	L	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
46	L	H	H	H	H	L	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
47	L	H	H	L	H	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
48	L	H	H	H	L	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
49	H	L	H	H	H	L	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
50	H	L	H	L	H	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
51	H	L	H	H	L	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
52	H	H	H	H	L	L	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
53	H	H	H	L	H	L	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
54	H	H	H	L	L	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
55	H	L	L	H	H	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
56	L	H	L	H	H	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
57	L	L	H	H	H	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
58	H	H	H	H	H	L	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
59	H	H	H	L	H	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
60	H	H	H	H	L	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
61	H	H	L	H	H	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
62	L	H	H	H	H	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
63	H	L	H	H	H	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
64	H	H	H	H	H	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)

(*) : High side / Low side arm shorting mode is disabled by the internal logic. (FAULT is kept low.) When undervoltage (6 V typ.) or overvoltage (22 V typ.) is detected, all outputs are pulled low regardless of input signals. At this time, FAULT output goes high (open-drain, high-impedance).

TENTATIVE

MAXIMUM RATING (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT	REMARKS
Power Supply Voltage	V_{DD}	−0.5~30	V	
Output Current	I_{SOURCE}	1	A	Pulse width ≦ 10 μs
	I_{SINK}	1		
Input Voltage	V_{IN}	−0.5~7.0	V	
FAULT Pin Voltage	V_{FAULT}	30	V	
U, V and W Pin Negative Voltage	U (−) V (−) W (−)	−0.5	V	Negative voltage that can be applied to U, V and W pins (reference to SGND pin)
PGND Pin Negative Voltage	PGND (−)	−0.5	V	Negative voltage that can be applied to PGND pin (reference to SGND pin)
Fault Pin Current	I_{FAULT}	5	mA	
Power Dissipation	P_D	0.8	W	
		1.5 (Note)		
Operating Temperature	T_{opr}	−40~125	°C	
Storage Temperature	T_{stg}	−40~150	°C	

THERMAL RESISTANCE

CHARACTERISTIC	SYMBOL	RATING	UNIT
Junction to Ambient Thermal Resistance	$R_{th\ (j\text{-}a)}$	156.3	°C / W
		83.4 (Note)	

(Note) : When a device mounted on 60 mm × 60 mm × 1.6 t glass epoxy PCB.

TENTATIVE

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = −40~125°C)

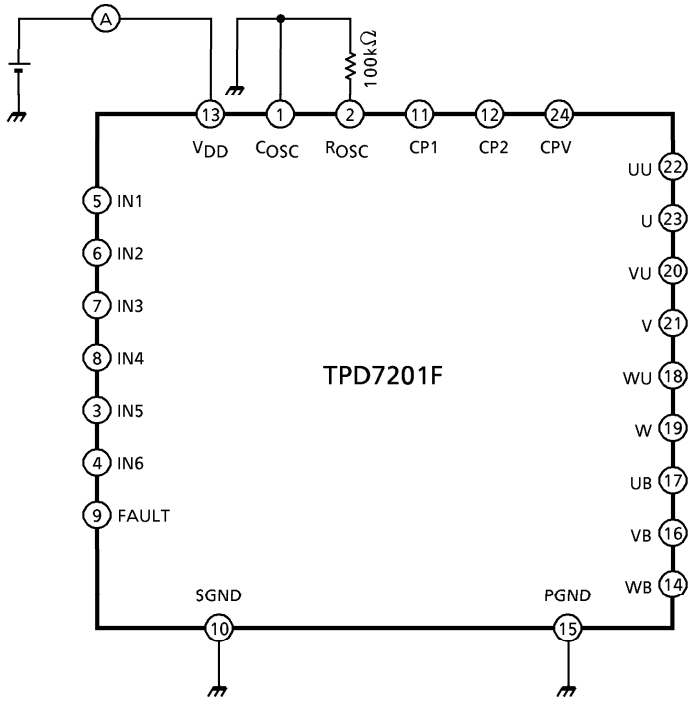
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARKS
Operating Supply Voltage		V_{DD}	—	—	7	13.5	18	V	
Supply Current		I_{DD} (1)	1	V_{DD} = 13.5 V	—	—	10	mA	Oscillation circuit stops
		I_{DD} (2)	2	V_{DD} = 13.5 V, V_{IN1}~V_{IN6} = 0 V	—	—	100		When oscillation circuit is operating f = 20 kHz, mean current
Input Voltage		V_{IH}	2	V_{DD} = 7~18 V, I_O = 0 A	3.5	—	—	V	IN1-IN6 high-level input voltage
		V_{IL}			—	—	1.5		IIN1-IN6 low-level input voltage
Input Current		I_{IH}	2	V_{DD} = 7~18 V, V_{IN} = 5 V, I_O = 0 A	—	—	1	mA	IN1-IN6 input current
		I_{IL}		V_{DD} = 7~18 V, VIN = 0 V, I_O = 0 A	− 10	—	10	μA	
Output Voltage	High side	V_{OH}	2	V_{DD} = 13.5 V, V_{IN} = 5 V, I_O = 0 A	V_{CPV} − 2	—	V_{CPV}	V	UU pin voltage (reference to U pin) VU pin voltage (reference to V pin) WU pin voltage (reference to W pin) V_{CPV} denotes CPV pin voltage.
		V_{OL}		V_{DD} = 13.5 V, V_{IN} = 0 V, I_O = 0 A	—	—	0.1		
	Low side	V_{OH}		V_{DD} = 13.5 V, V_{IN} = 5 V, I_O = 0 A	11.5	—	13.5		UB pin voltage (reference to PGND pin) VB pin voltage (reference to PGND pin) WB pin voltage (reference to PGND pin)
		V_{OL}		V_{DD} = 13.5 V, V_{IN} = 0 V, I_O = 0 A	—	—	0.1		
Charge Pump Voltage		V_{CPV}	2	V_{DD} = 13.5 V	23.5	—	34	V	CPV pin voltage (reference to SGND pin)
Active Clamp Voltage	High side	V_{CLAMP}	—	V_{IN} = 5 V, I_O = 10 mA	14	—	20	V	Clamp voltage between UU and U pins Clamp voltage between VU and V pins Clamp voltage between WU and W pins
	Low side			V_{IN} = 5 V, I_O = 10 mA	—	18	—		UB, VB and WB pins clamp voltage (reference to PGND pin)

TENTATIVE

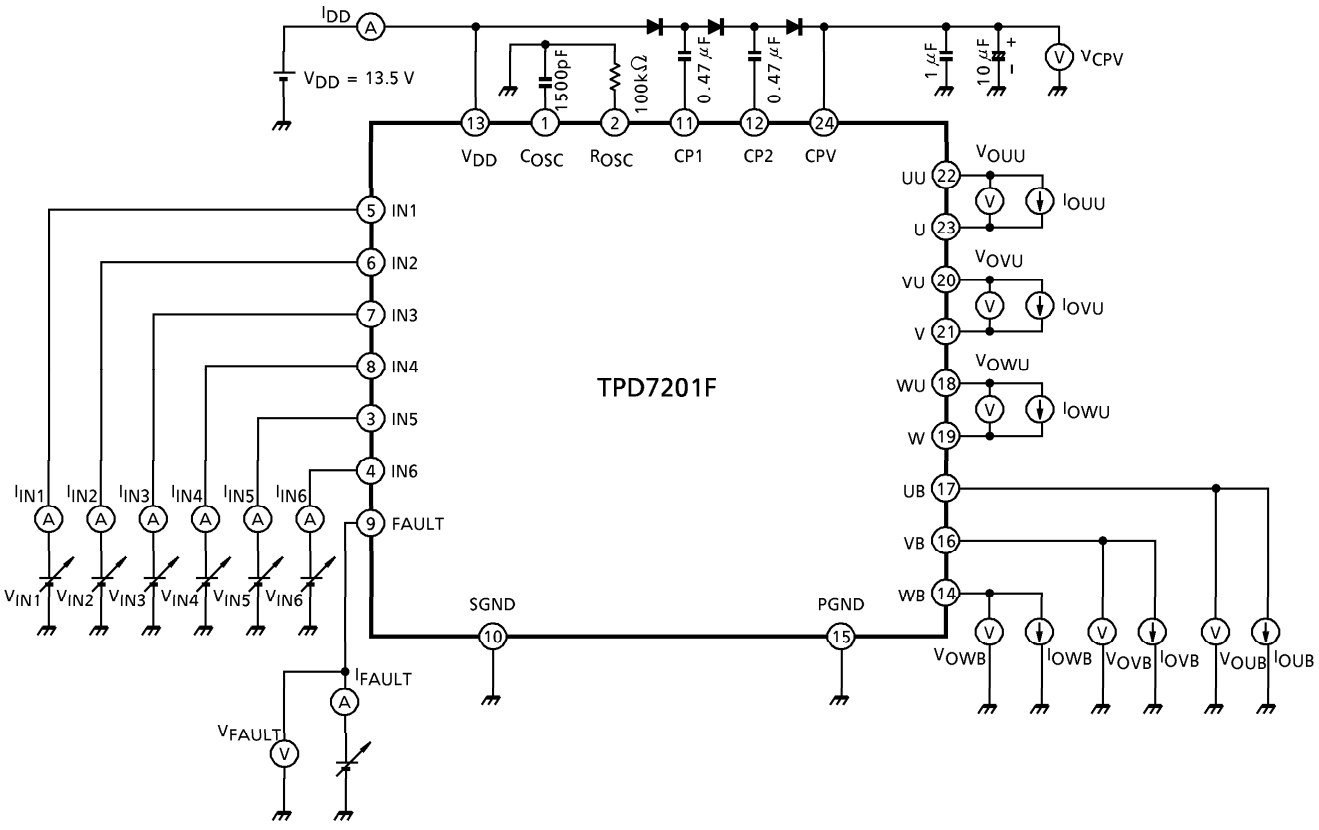
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARKS
Output Resistance		R_{SOURCE}	2	V_{DD} = 13.5 V, V_{IN} = 5 V, I_O = 0.5 A	—	7	10	Ω	UU, VU, WU, UB, VB and WB output resistance pulse width ≦ 10 μs
		R_{SINK}		V_{DD} = 13.5 V, V_{IN} = 0 V, I_O = −0.5 A	—	4.5	10		
Low-Voltage Protection	Detection	V_{SD} (L)	3	—	5.5	6	6.5	V	Low-voltage detection voltage and hysteresis (V_{DD} voltage detected)
	Hysteresis	ΔV_{SD} (L)			—	0.5	—		
Over-Voltage Protection	Detection	V_{SD} (H)	3	—	20	22	24	V	Overvoltage detection voltage and hysteresis (V_{DD} voltage detected)
	Hysteresis	ΔV_{SD} (H)			—	2	—		
Swithcing Time	Turn-on delay time	t_{d} (ON)	4	V_{DD} = 7~18 V, C_{OUT} = 0.047 μF, R_G = 47 Ω	—	—	4	μs	UU, VU, WU, UB, VB and WB switching time
	Turn-on time	t_{ON}			—	—	6		
	Turn-off delay time	t_{d} (OFF)			—	—	4		
	Turn-off time	t_{OFF}			—	—	6		
Oscillating Frequency		f_{OSC}	2	V_{DD} = 7~18 V, R_{OSC} = 100 kΩ, C_{OSC} = 1500 pF	—	20	—	kHz	f_{OSC} calculation formula $f_{OSC} = 3 / \{C_{OSC} (R_{OSC} + 2\ k)\}$ (Hz)
FAULT Pin Voltage		V_{FAULT}	2	I_{FAULT} = 1 mA	—	—	0.8	V	FAULT pin low-level voltage (open-drain)
FAULT Delay Time		t_{ON}	3	R_{FAULT} = 5.1 kΩ, V_{FAULT} = 5 V (External power supply)	—	1	—	μs	Time from low voltage / overvoltage detection or restoration to FAULT output inversion
		t_{OFF}			—	1	—		

TENTATIVE

TESTING CIRCUIT 1 I_{DD} (1)

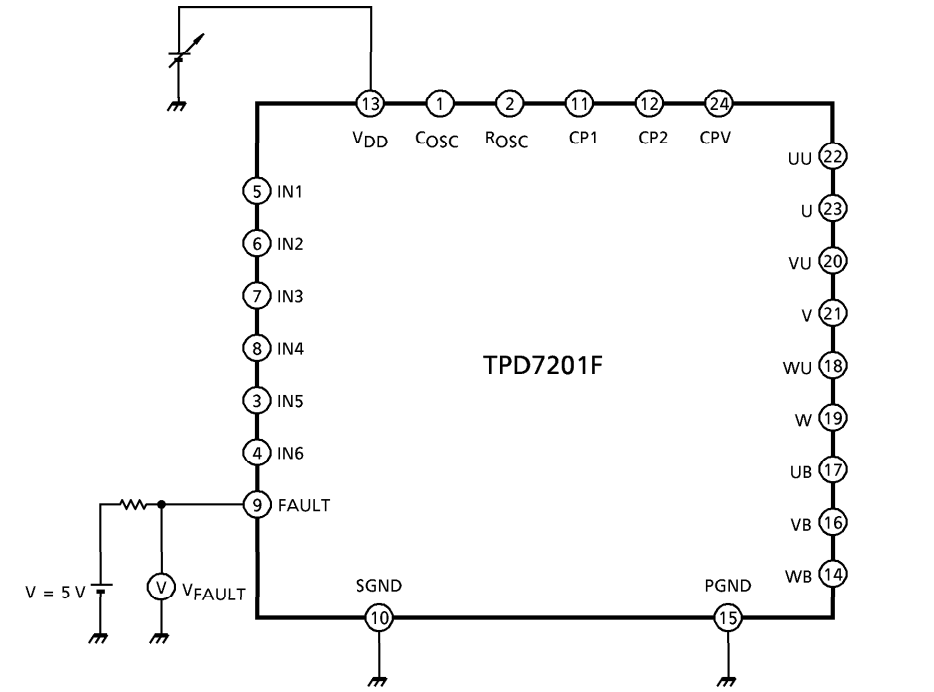


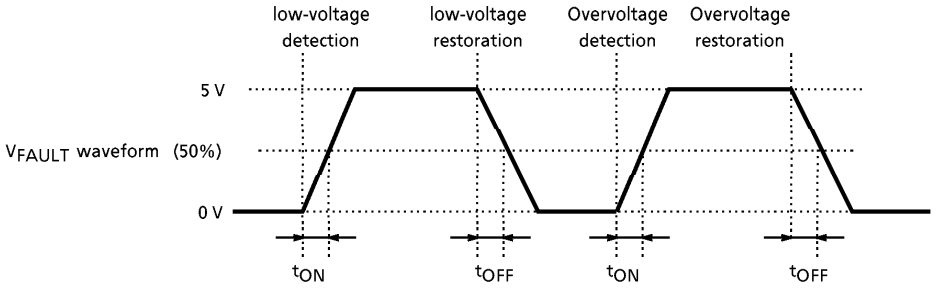
TESTING CIRCUIT 2 I_{DD} (2), V_{IH}, V_{IL}, I_{IH}, I_{IL}, V_{OH}, V_{OL}, V_{CPV}, V_{FAULT}



TENTATIVE

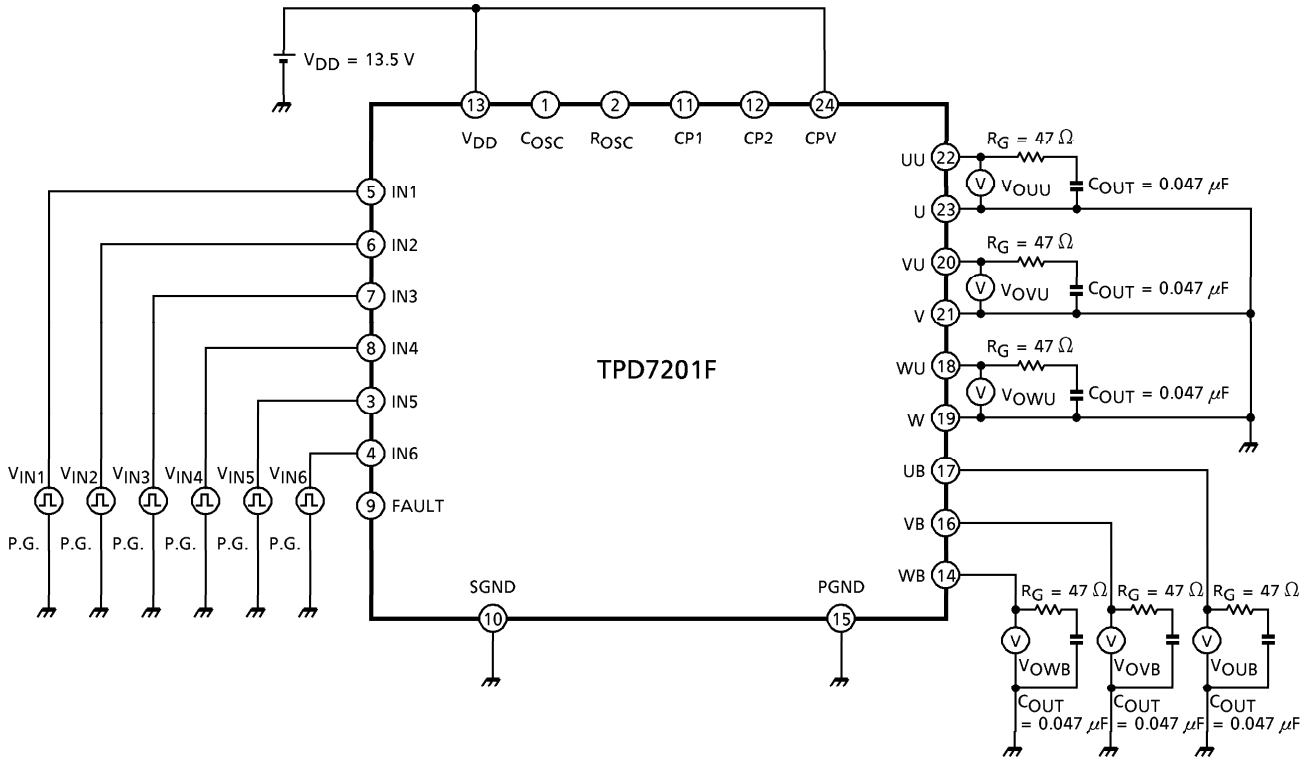
TESTING CIRCUIT 3 $V_{SD\,(L)}$, $\Delta V_{SD\,(L)}$, $V_{SD\,(H)}$, $\Delta V_{SD\,(H)}$, FAULT delay time t_{ON}, t_{OFF}

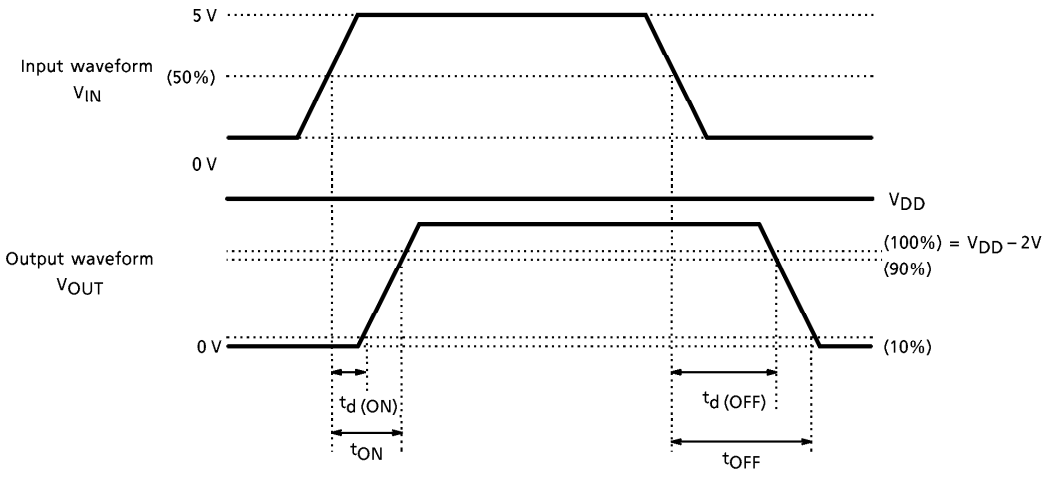




TENTATIVE

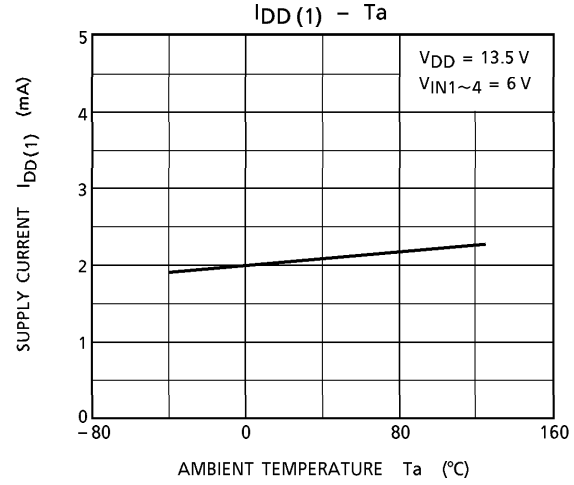
TESTING CIRCUIT 4 $t_{d\,(ON)}$, t_{ON}, $t_{d\,(OFF)}$, t_{OFF}



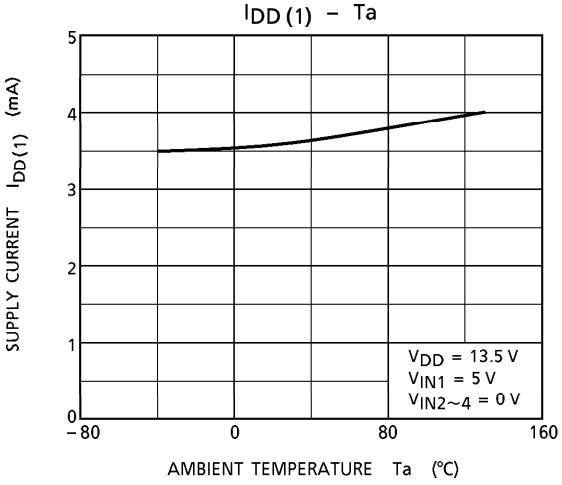


TENTATIVE

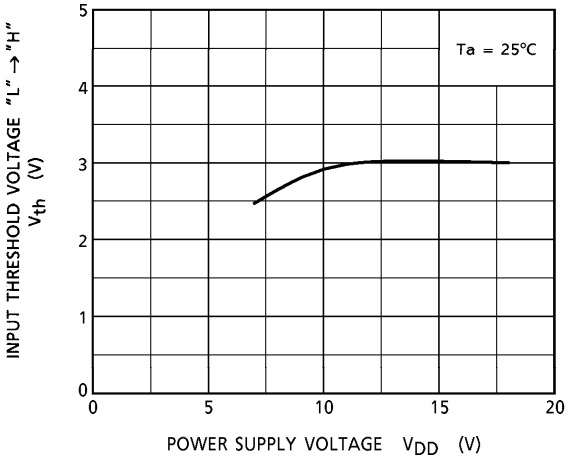
I_{DD} (1) – Ta



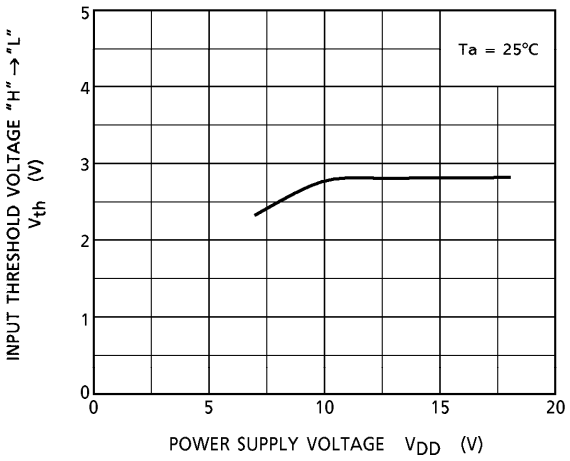
I_{DD} (1) – Ta



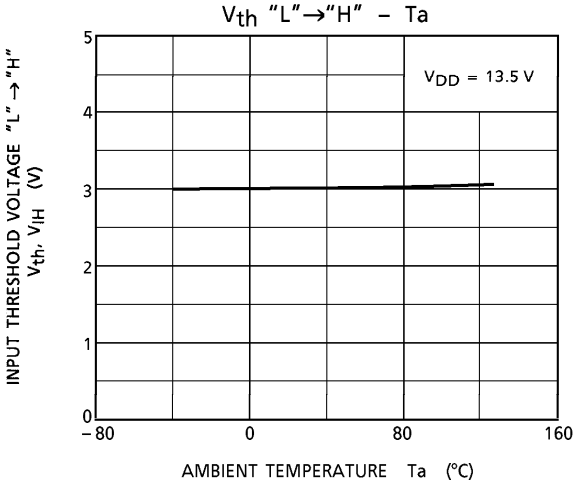
V_{th} "L"→"H" – V_{DD}



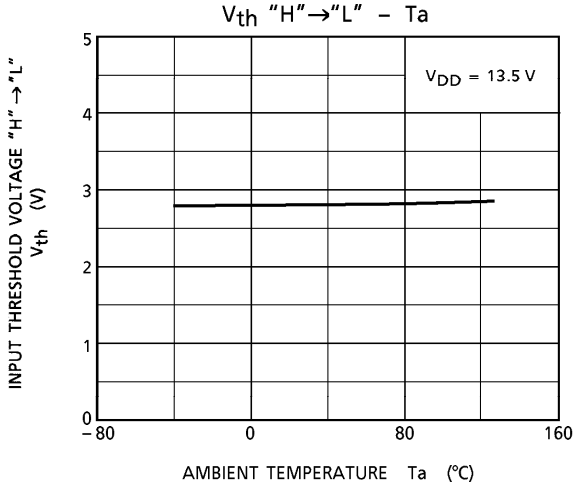
V_{th} "H"→"L" – V_{DD}



V_{th} "L"→"H" – Ta

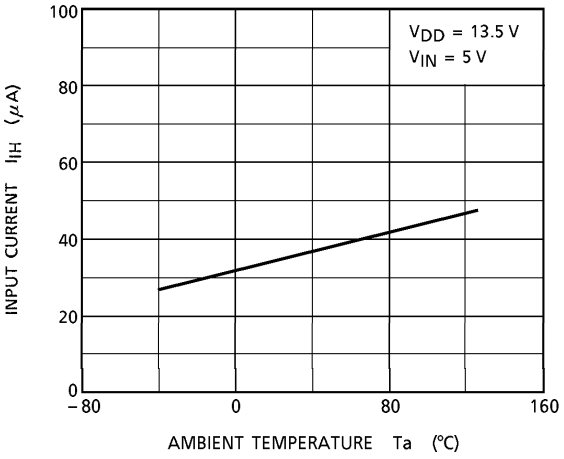


V_{th} "H"→"L" – Ta

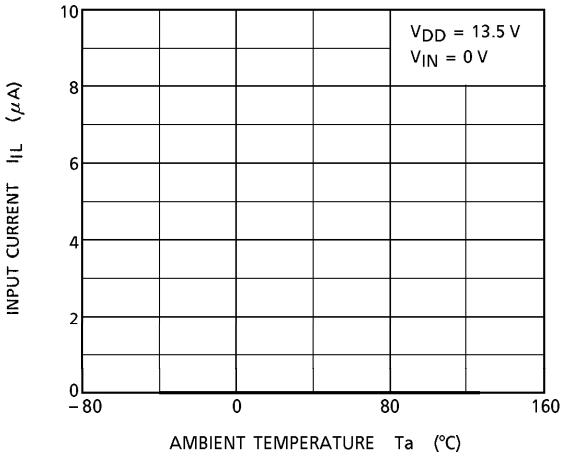


TENTATIVE

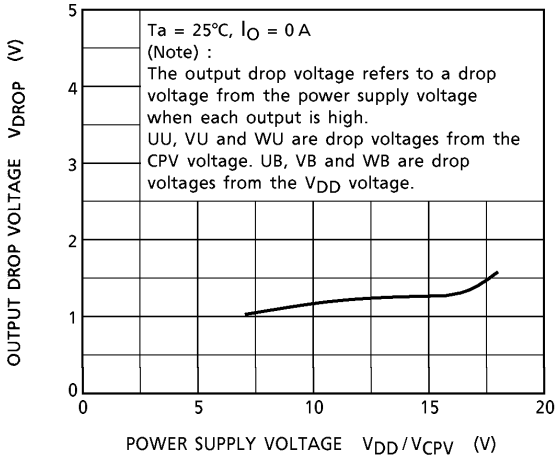
I_{IH} – Ta



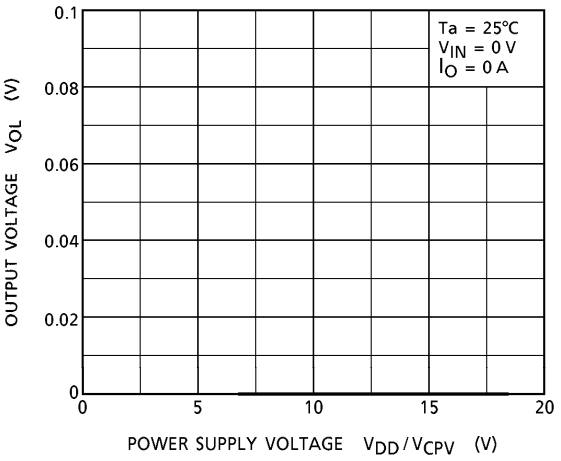
I_{IL} – Ta



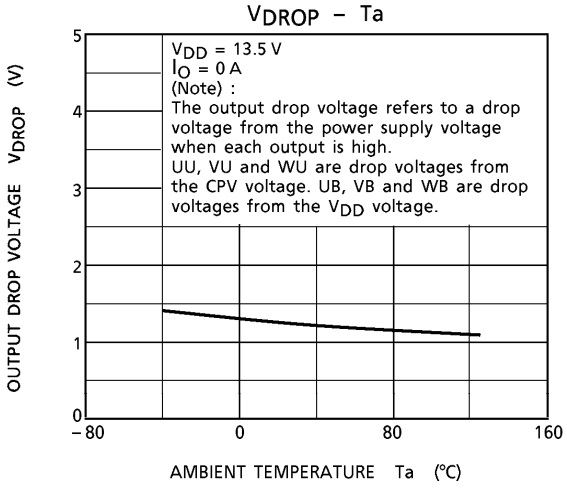
V_{DROP} – POWER SUPPLY VOLTAGE



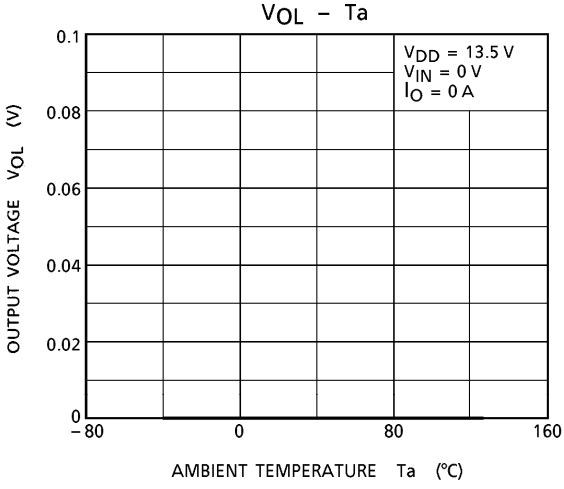
V_{OL} – POWER SUPPLY VOLTAGE



V_{DROP} – Ta

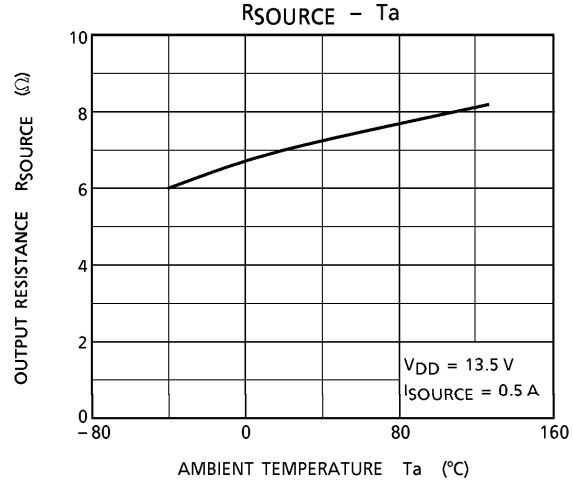


V_{OL} – Ta

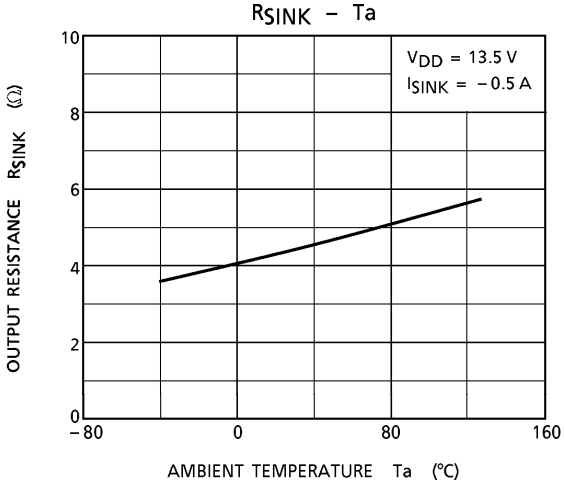


TENTATIVE

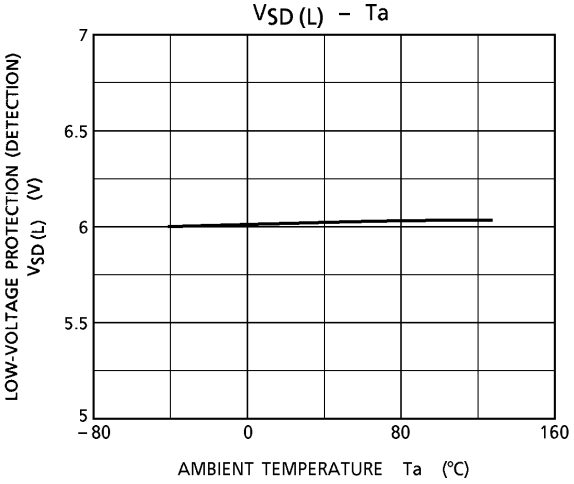
R_{SOURCE} – Ta



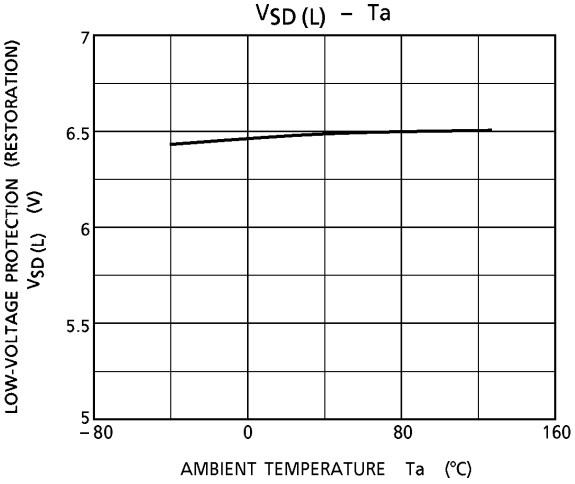
R_{SINK} – Ta



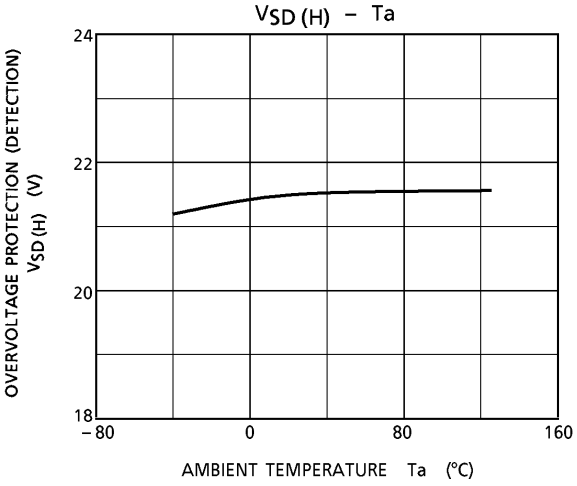
$V_{SD\,(L)}$ – Ta



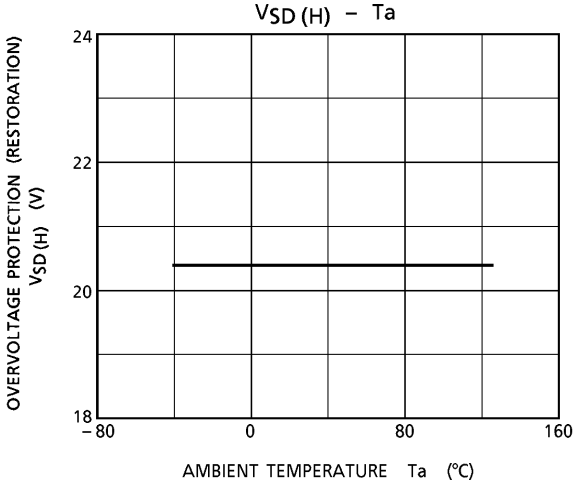
$V_{SD\,(L)}$ – Ta



$V_{SD\,(H)}$ – Ta

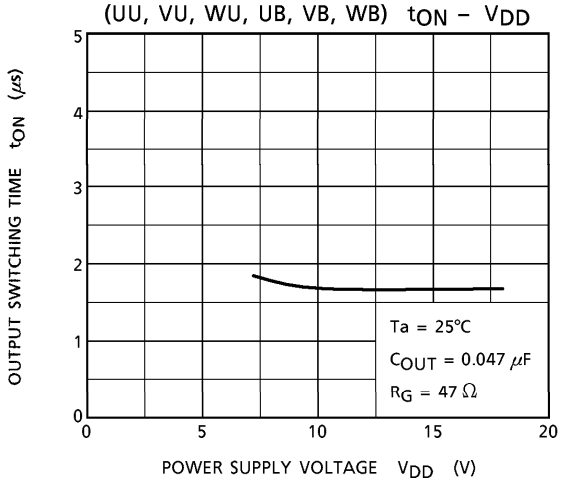


$V_{SD\,(H)}$ – Ta

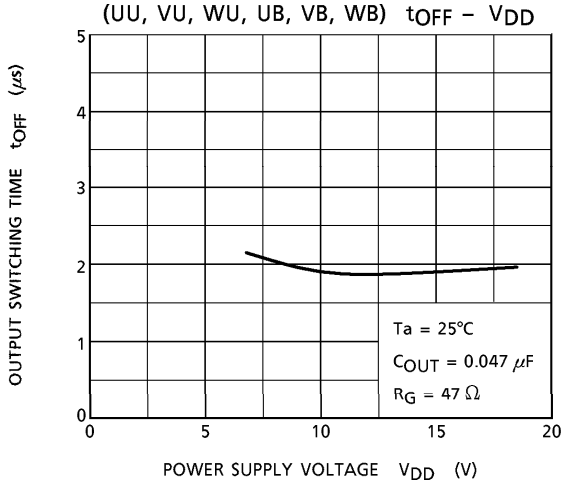


TENTATIVE

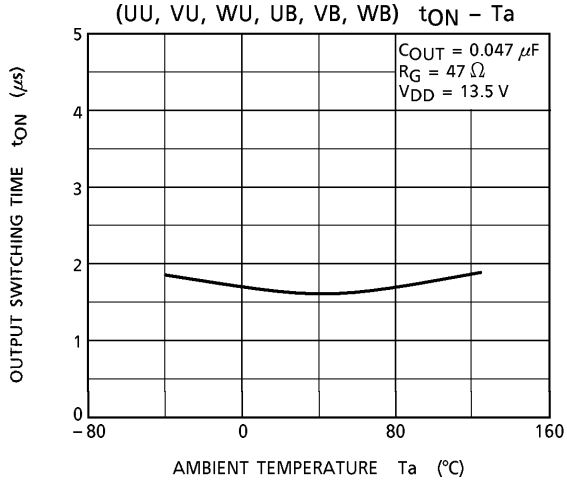
OUTPUT SWITCHING TIME
(UU, VU, WU, UB, VB, WB) t_{ON} – V_{DD}



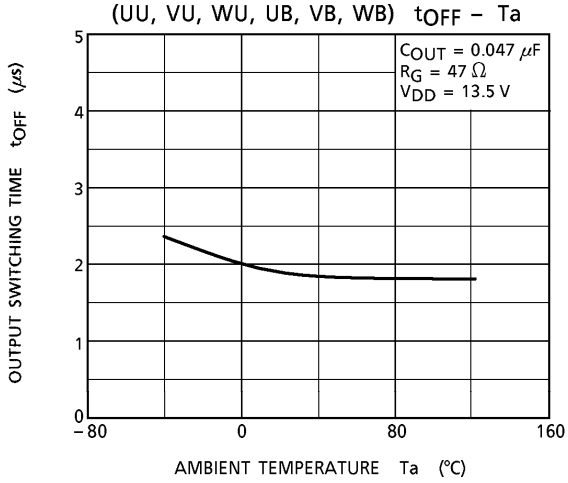
OUTPUT SWITCHING TIME
(UU, VU, WU, UB, VB, WB) t_{OFF} – V_{DD}



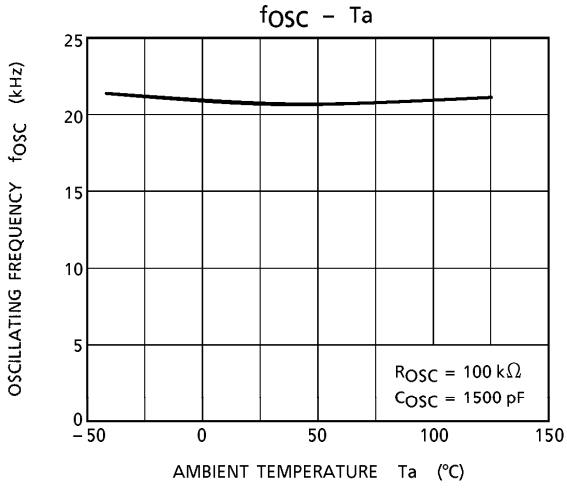
OUTPUT SWITCHING TIME
(UU, VU, WU, UB, VB, WB) t_{ON} – Ta

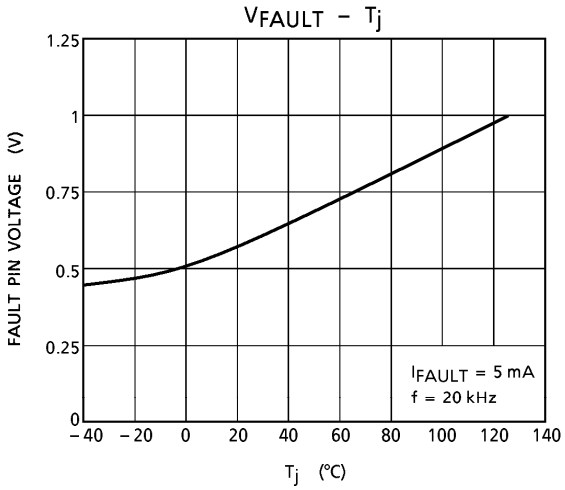


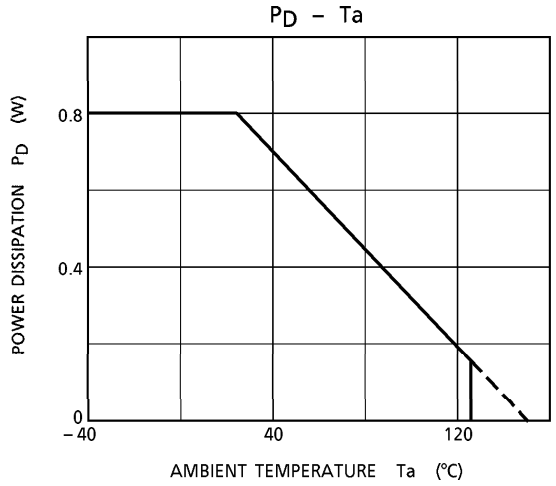
OUTPUT SWITCHING TIME
(UU, VU, WU, UB, VB, WB) t_{OFF} – Ta



TENTATIVE


fOSC – Ta
OSCILLATING FREQUENCY fOSC (kHz)
25
20
15
10
5
0
– 50
0
50
100
150
ROSC = 100 kΩ
COSC = 1500 pF
AMBIENT TEMPERATURE Ta (°C)


VFAULT – Tj
FAULT PIN VOLTAGE (V)
1.25
1
0.75
0.5
0.25
0
– 40
– 20
0
20
40
60
80
100
120
140
IFAULT = 5 mA
f = 20 kHz
Tj (°C)


PD – Ta
POWER DISSIPATION PD (W)
0.8
0.4
0
– 40
40
120
AMBIENT TEMPERATURE Ta (°C)

TENTATIVE

Method for selecting external parts

PIN No.	PIN NAME	TYPE	RECOMMENDED VALUE / RECOMMENDED PRODUCT	DESCRIPTION
1	C_{OSC}	Capacitor	1500 pF (ceramic)	Sets charge pump's oscillation frequency.
2	ROSC	Resistor	100 kΩ	Sets charge pump's oscillation frequency.
11 12	CP1 CP2	Capacitor	0.47 μF (laminated ceramic)	Capacitor for the charge pump. Greater this capacitance larger the charging current to the capacitor, so there is a greater loss in the IC.
24	CPV	Capacitor	1 μF (laminated ceramic) and 10 μF (aluminum electrolytic) connected in parallel	Greater this capacitance, larger the charge pump (CPV pin)'s current supply capacity, so there is a greater loss in the IC. Therefore, be careful not to exceed the allowable loss.
11 12 24	CP1 CP2 CPV	High-speed diode	t_{rr} = 100 ns (max.) CRH01 (t_{rr} = 35 ns max.) recommended	Diode for the charge pump. An electric charge equal to the diode's Q_{rr} component goes out of the capacitor's charged electricity. Therefore, use a high-speed diode.
22 20 18 17 16 14	UU VU WU UB VB WB	Resistor	—	Gate resistor for external power MOSFET. Choose the optimum value by considering the switching loss and EMI of the power MOSFET.
10 23 21 19	SGND U V W	SBD	V_F = 0.5 V (max.) CRS03 (V_F = 0.45 V max. @0.7 A) recommended	This is needed when the U, V or W pin is biased to the negative side by more than 0.5 V from the SGND voltage. Because this IC operates relative to SGND, a parasitic diode exists toward each pin. When the U, V or W pin is biased to the negative side by more than 0.5 V from SGND, the parasitic diode conducts, causing the IC to operate erratically or generate abnormal heat.
23 21 19	U V W	Resistor	—	This is needed when the U, V or W pin is biased to the negative side by more than 0.5 V from the SGND voltage. This is used to limit current for external SBD.

TENTATIVE

USAGE PRECAUTIONS

(Note 1) : About taking the charge pump voltage to external devices

Current can be taken out of the charge pump's final stage (CPV pin) to external devices without causing any problem. In this case, because the charge pump voltage drops, increase the capacitance of the capacitor connected to the CPV pin. However, this may cause the charging current to the capacitor and, hence, loss in the IC to increase. So be careful not to exceed the allowable loss.

(Note 2) : About heat sink design

Because this IC contains a charge pump function, loss in it affects external capacitor capacitance and diode characteristics. It is recommended that the junction temperature, T_j, be judged from the on-voltage of the FAULT pin (open-drain). When V_{DD} is within the range of operating power supply voltages, the FAULT pin outputs a low. For details about on-voltage characteristics, see T_j-V_{FAULT} characteristic curves.

(Note 3) : About dead time setting

For arm-shorting input logic, all outputs (UU, VU, WU, UB, VB and WB) are pulled low. When operating in forward or reverse mode, consider the IC output switching time and the switching time (including temperature characteristic) of the external power MOSFET as you set the dead time. The dead time required for only the IC, not including the external power MOSFET, is 4 μs (within all operating power supply voltages and all operating temperatures).

(Note 4) : Shorting between outputs, Shortcircuit of outputs and V_{DD} pin or shortcircuit of outputs GND pin may cause the IC to break down. Therefore, pay careful attention to the design of output lines and V_{DD} and GND lines.

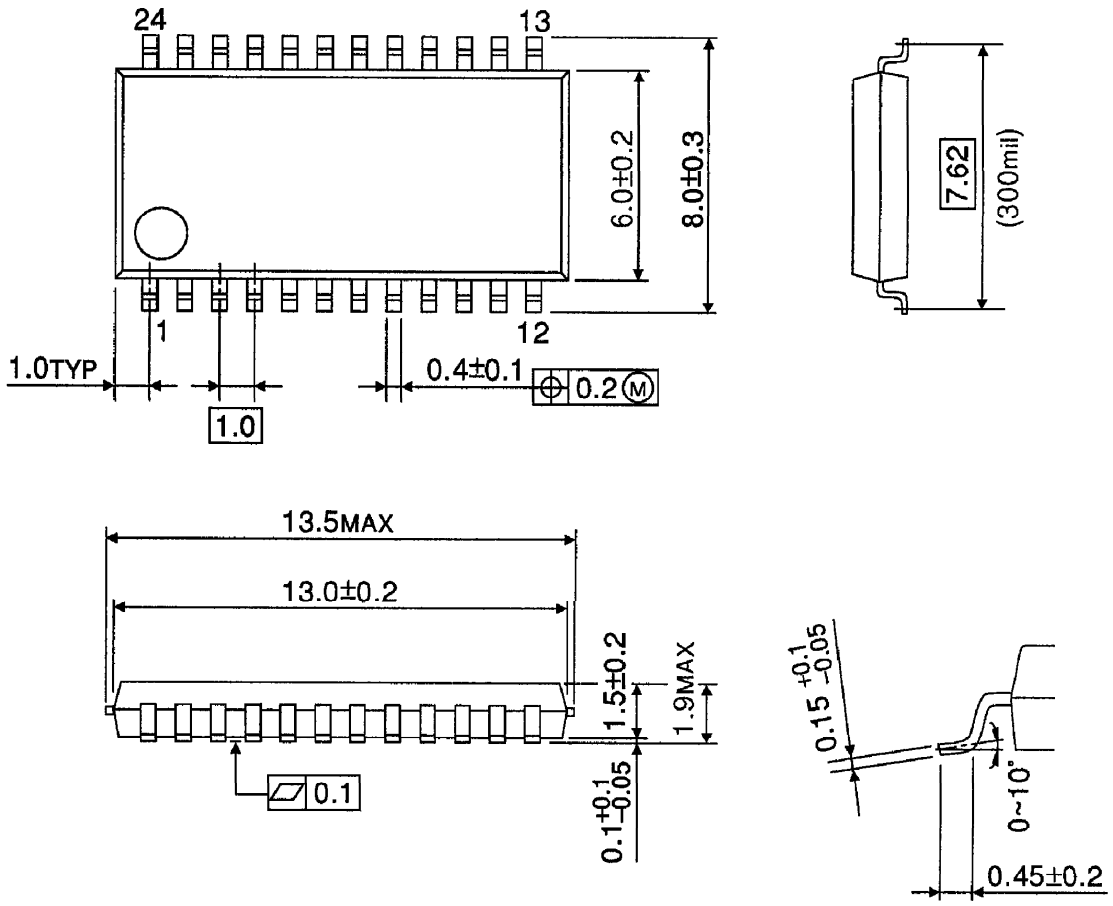
(Note 5) : Precautions on dry packing

After unpacking dry or moistureproof packing, please make sure the device is mounted in place within 48 hours at temperature and humidity of 30°C and 60% RH or less. Because the device is emboss-taped and cannot be processed by baking, always be sure to use it within said allowable time after unpacking.
Tape packing quantity: 500 devices / reel (EL) or 2000 devices / reel (EL1)

TENTATIVE

PACKAGE DIMENSIONS

SSOP24-P-300-1.00B Unit : mm



Weight : 0.29 g (typ.)