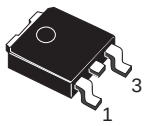
STD150NH02L
STD150NH02L-1

N-CHANNEL 24V - 0.003Ω - 150A - ClipPAK™/IPAK
STripFET™ III MOSFET FOR DC-DC CONVERSION

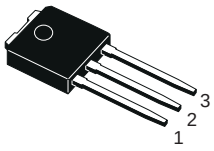
PRELIMINARY DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STD150NH02L	24 V	< 0.0035 Ω	150 A
STD150NH02L-1	24 V	< 0.0035 Ω	150 A

- TYPICAL R_{DS}(on) = 0.003Ω @ 10V
- TYPICAL R_{DS}(on) = 0.005Ω @ 5V
- $R_{DS(ON)}$ * Q_g INDUSTRY's BENCHMARK
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- LOW THRESHOLD DEVICE
- SURFACE MOUNTING POWER PACKAGE IN TAPE & REEL (SUFFIX "T4")

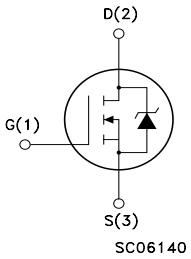


ClipPAK™
Suffix "T4"



IPAK
Suffix "-1"

INTERNAL SCHEMATIC DIAGRAM



DESCRIPTION

The **STD150NH02L** utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This novel 0.6µ process utilizes also unique metallization techniques that coupled to a "bondless" assembly technique result in outstanding performance with standard DPAK outline. It is therefore ideal in high performance DC-DC converter applications where efficiency is to be achieved at very high output currents.

APPLICATIONS

- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY DC/DC CONVERTERS

ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STD150NH02LT4	D150NH02L	DPAK	TAPE & REEL
STD150NH02L-1	D150NH02L	IPAK	TUBE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{spike}(1)	Drain-source Voltage Rating	30	V
V_{DS}	Drain-source Voltage (V_{GS} = 0)	24	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	24	V
V_{GS}	Gate-source Voltage	± 20	V
I_D	Drain Current (continuous) at T_C = 25°C	150	A
I_D	Drain Current (continuous) at T_C = 100°C	95	A
I_{DM} (2)	Drain Current (pulsed)	600	A
P_{TOT}	Total Dissipation at T_C = 25°C	125	W
	Derating Factor	0.83	W/°C
E_{AS} (3)	Single Pulse Avalanche Energy	900	mJ
T_{stg}	Storage Temperature	-55 to 175	°C
T_j	Max. Operating Junction Temperature		

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	1.2	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	100	°C/W
T_l	Maximum Lead Temperature for Soldering Purpose	275	°C

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 mA, V_{GS} = 0	24			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = 20 V			1	µA
		V_{DS} = 20 V, T_C = 125 °C			10	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20V			±100	nA

ON (4)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	1	1.8		V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 75 A		0.003	0.0035	Ω
		V_{GS} = 5 V, I_D = 75 A		0.005	0.0065	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (4)	Forward Transconductance	V_{DS} = 10V , I_D = 40A		52		S
C_{iss}	Input Capacitance	V_{DS} = 15V, f = 1 MHz, V_{GS} = 0		4450		pF
C_{oss}	Output Capacitance			1126		pF
C_{rss}	Reverse Transfer Capacitance			141		pF
R_g	Gate Input Resistance	f=1 MHz Gate DC Bias=0 Test Signal Level=20mV Open Drain		1.6		Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 10 V, I_D = 75 A		14		ns
t_r	Rise Time	R_G = 4.7 Ω V_{GS} = 10 V (see test circuit, Figure 3)		224		ns
Q_g	Total Gate Charge	V_{DD} = 16 V, I_D = 150 A,		69	93	nC
Q_{gs}	Gate-Source Charge	V_{GS} = 10 V		13		nC
Q_{gd}	Gate-Drain Charge			9		nC
Q_{oss} (5)	Output Charge	V_{DS} = 16 V, V_{GS} = 0 V		27		nC
Q_{gls} (6)	Third-Quadrant Gate Charge	V_{DS} = 0 V, V_{GS} = 10 V		64		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	V_{DD} = 10 V, I_D = 75 A,		69		ns
t_f	Fall Time	R_G = 4.7Ω, V_{GS} = 10 V (see test circuit, Figure 3)		40	54	ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				150	A
I_{SDM} (2)	Source-drain Current (pulsed)				600	A
V_{SD} (4)	Forward On Voltage	I_{SD} = 75 A, V_{GS} = 0			1.3	V
t_{rr}	Reverse Recovery Time	I_{SD} = 150 A, di/dt = 100A/µs,		47		ns
Q_{rr}	Reverse Recovery Charge	V_{DD} = 15 V, T_j = 150°C		58		nC
I_{RRM}	Reverse Recovery Current	(see test circuit, Figure 5)		2.5		A

1. Garanted when external R_g = 4.7 Ω and $t_f < t_f$ max
2. Pulse width limited by safe operating area
3. Starting T_j = 25°C, I_D = 40A, V_{DD} = 15V
4. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
5. $Q_{oss} = C_{oss}*\Delta V_{in}$, $C_{oss} = C_{gd}+C_{ds}$. See Appendix A
6. Gate charge for Syncronous Operation

Fig. 1: Unclamped Inductive Load Test Circuit

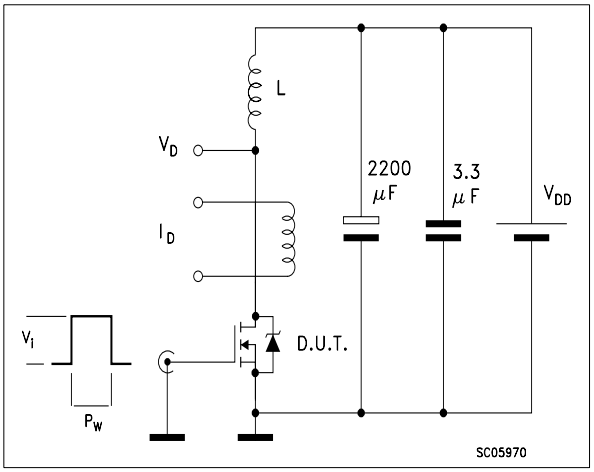


Fig. 2: Unclamped Inductive Waveform

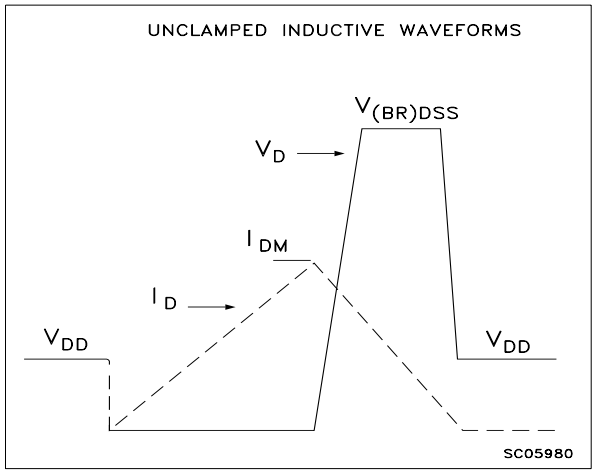


Fig. 3: Switching Times Test Circuit For Resistive Load

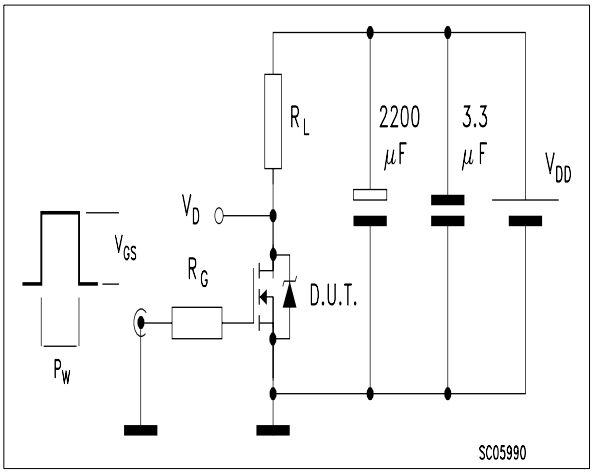


Fig. 4: Gate Charge test Circuit

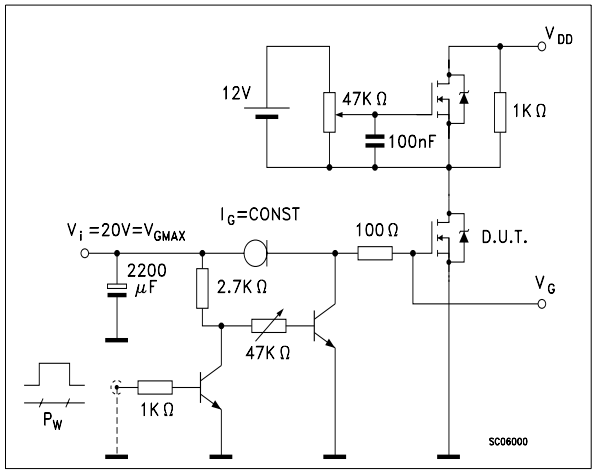
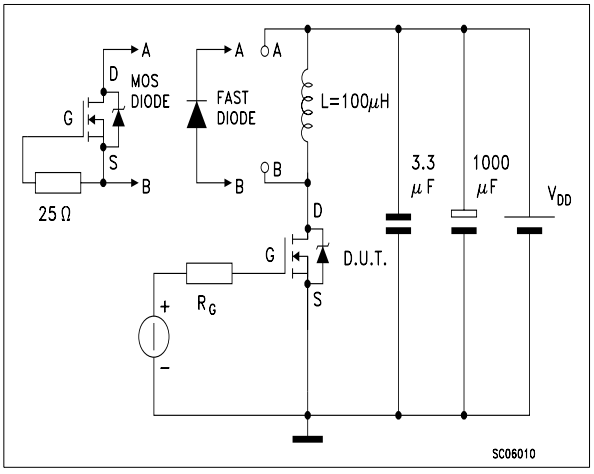
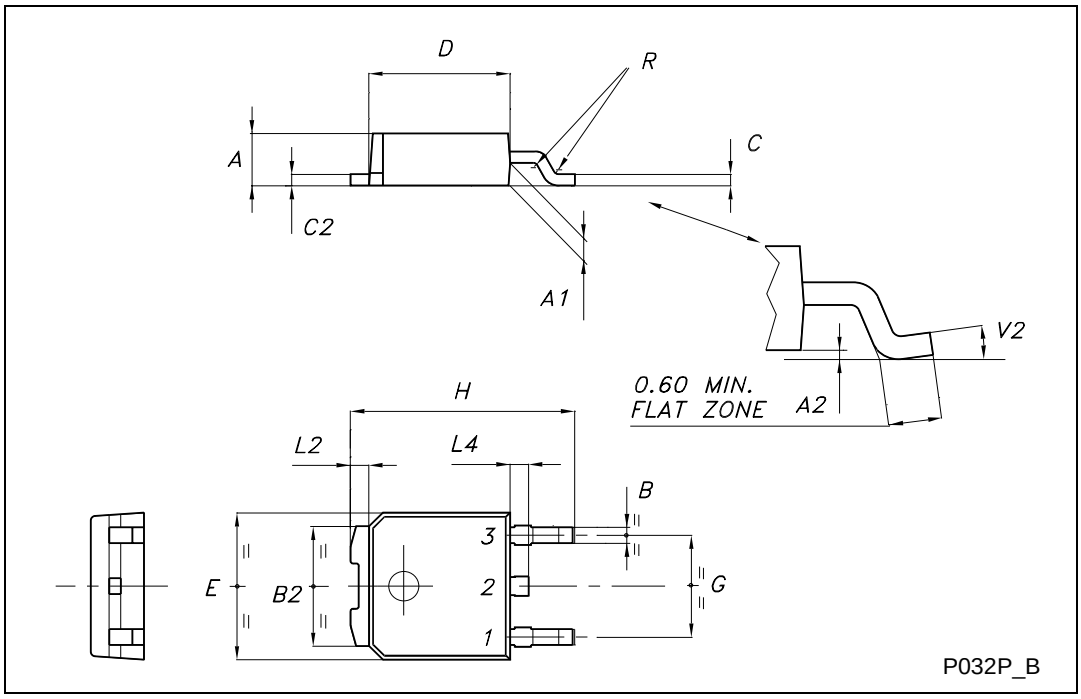


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



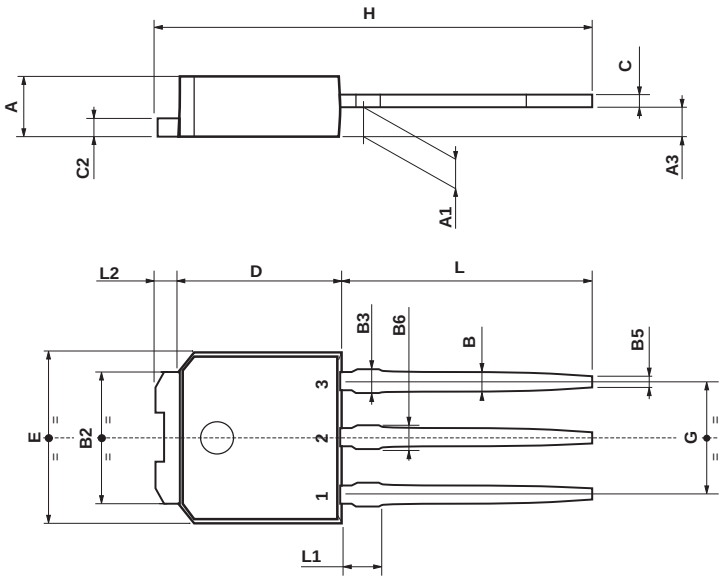
TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0^o		8^o	0^o		0^o



TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



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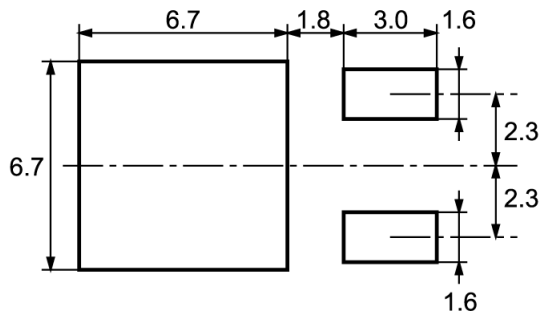
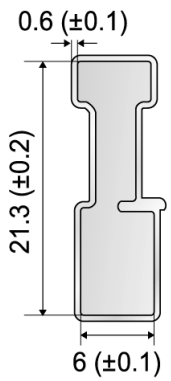
DPAK FOOTPRINT



All dimensions are in millimeters

TUBE SHIPMENT (no suffix)*



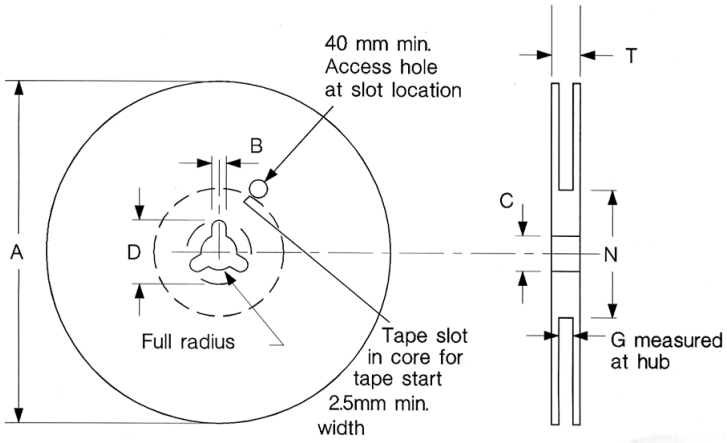
BASE QTY
75

BULK QTY
3000

Tube length 532 (±0.5)

All dimensions are in millimeters

TAPE AND REEL SHIPMENT (suffix "T4")*



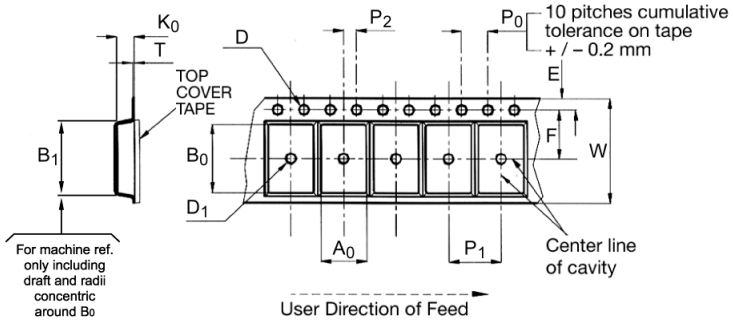
REEL MECHANICAL DATA

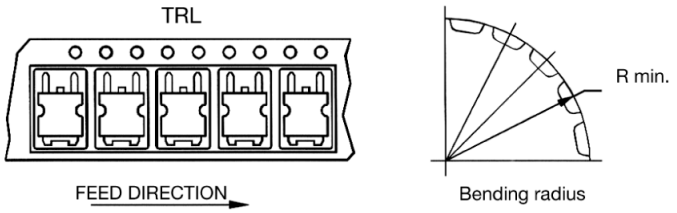
DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641



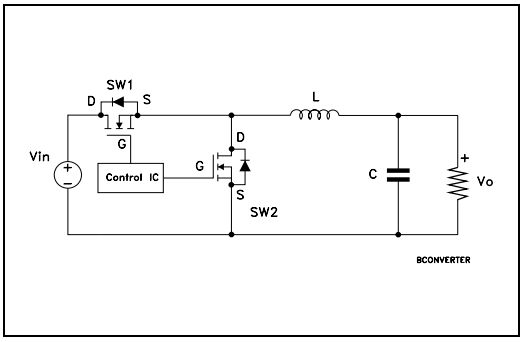


* on sales type

Appendix A: Buck Converter Power Losses Estimation

DESCRIPTION

The power losses associated with the FETs in a Synchronous Buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.



The low side (SW2) device requires:

- Very low RDS(on) to reduce conduction losses
- Small Q_{gls} to reduce the gate charge losses
- Small C_{oss} to reduce losses due to output capaci tance
- Small Q_{rr} to reduce losses on SW1 during its turn-on
- The C_{gd}/C_{gs} ratio lower than V_{th}/V_{GG} ratio especially with low drain to source voltage to avoid the cross conduction phenomenon

The high side (SW1) device requires:

- Small R_g and L_s to allow higher gate current peak and to limit the voltage feedback on the gate
- Small Q_g to have a faster commutation and to reduce gate charge losses
- Low $R_{DS(on)}$ to reduce the conduction losses

		High Side Switch (SW1)	Low Side Switch (SW2)
$P_{conduction}$		$R_{DS(on)SW1} * I_L^2 * \delta$	$R_{DS(on)SW2} * I_L^2 * (1-\delta)$
$P_{switching}$		$V_{in} * (Q_{gsth(SW1)} + Q_{gd(SW1)}) * f * \frac{I_L}{I_g}$	Zero Voltage Switching
P_{diode}	Recovery	Not Applicable	[1] $V_{in} * Q_{rr(SW2)} * f$
	Conduction	Not Applicable	$V_{f(SW2)} * I_L * t_{deadtime} * f$
$P_{gate(Q_t)}$		$Q_{g(SW1)} * V_{gg} * f$	$\mathbf{Q_{gls(SW2)} * V_{gg} * f}$
P_{Qoss}		$\frac{V_{in} * Q_{oss(SW1)} * f}{2}$	$\frac{V_{in} * Q_{oss(SW2)} * f}{2}$

Parameter	Meaning
δ	Duty-Cycle
Q_{gsth}	Post Threshold Gate Charge
Q_{gls}	Third Quadrant Gate Charge
Pconduction	On State Losses
Pswitching	On-off Transition Losses
Pdiode	Conduction and Reverse Recovery Diode Losses
Pdiode	Gate Drive Losses
P_{Qoss}	Output Capacitance Losses

[1] Dissipated by SW1 during turn-on