PM6541

E1XC-EVBD

E1XC EVALUATION DAUGHTERBOARD

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CONTENTS

1 OVERVIEW

The PM6541 E1XC EVBD evaluation daughterboard allows for the test, evaluation and demonstration of the PMC PM6341 E1XC device. It is also compatible with the PM4341 T1XC device. This daughterboard can be used standalone with up to two E1XC devices but has been especially designed to mate with the PMC PM1501 EVMB evaluation motherboard to form a complete evaluation system. All required decoding logic is provided on the E1XC EVBD daughterboard to give the EVMB direct access to all registers of both E1XC devices.

All of the principal connections to both devices have been brought out to header strips for convenient test access. E-1 digital interfaces are provided on a header strip and BNC or mini-bantam connectors are provided for E-1 analog signals. Both 75 Ω and 120 Ω interfaces are provided. The backplane interfaces of each device are accessible through header strips and the devices can be interconnected back to back, effectively creating a jitter-attenuating format converter by dropping in shorting connectors into specific DIP sockets.

Clocks for the backplane are provided by a T1/CEPT digital trunk DPLL which provides a synchronized 1.544 MHz, 2.048 MHz, or 4.096 MHz signal. The PLL can be easily bypassed to allow direct drive of the backplane with an appropriate oscillator. A prototype area has been provided for breadboarding more complex applications.

The E1XC EVBD evaluation daughterboard is configured, monitored, and powered through an edge connector that is designed to mate with the EVMB evaluation motherboard

2 FUNCTIONAL DESCRIPTION

2.1 Block Diagram

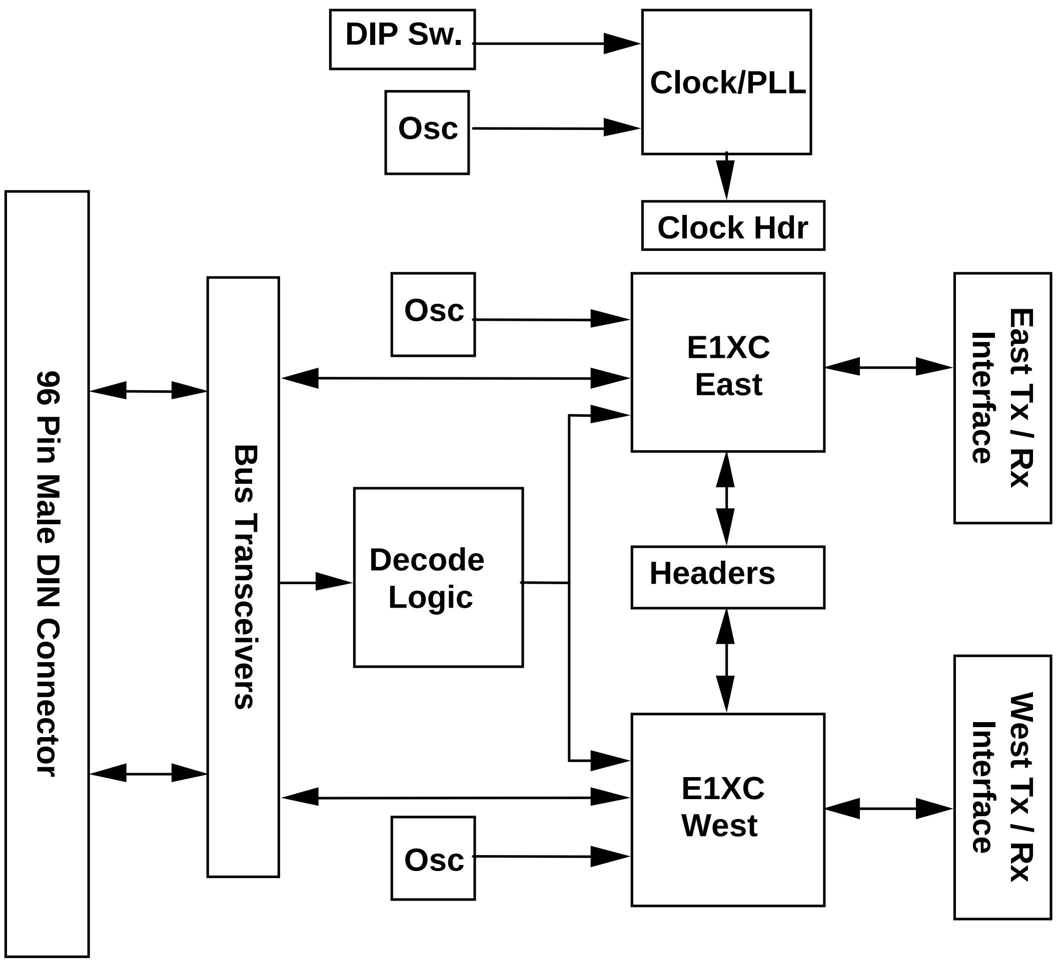

Figure 1: Block Diagram

2.2 Bus Transceivers

Bus transceivers are provided at the connector interface to prevent excessive loading of the 68HC11 on the EVMB evaluation motherboard. In addition they provide some measure of isolation for the daughterboard and protection for other external signals such as the EXTCLK and EXTFP inputs.

2.3 Decode Logic

Decode logic is provided on the daughterboard to give memory mapped access to all of the registers within both E1XCs. Registers within the "east" E1XC are accessible starting at address C000H. Registers within the "west" E1XC are accessible starting at address C100H. Additional chip selects are provided for addresses C200H-C2FFH and C300H-C3FFH for use on the prototype area.

2.4 DIP Switches

The DIP switch settings control the operational modes of the MT8940 DPLL device that is used to generate the backplane clock. Access to the enable inputs for the various clock outputs is also provided through these switches.

2.5 Clock DPLL

The MT8940 T1/CEPT Digital Trunk DPLL can provide a number of different clocks with different methods of synchronization, depending upon its mode setting, which can be used to drive the backplane interface of the E1XCs. The device can output 1.544 MHz, 2.048 MHz, and 4.096 MHz clocks in true or complement format. The DPLL can be allowed to free-run or it can be synchronized to the receive frame pulses of either E1XC. PLL control is accomplished with the DIP switches connected to the inputs.

2.6 Oscillators

Up to four oscillators can be used on the E1XC EVBD daughterboard depending upon the choice of configuration. The E1XC devices require a 49.152 MHz clock if all of the device's features are to be utilized. Although two oscillator sockets are provided, only a single oscillator is necessary if two E1XC devices are used. The insertion of a jumper (J25) will join the two E1XC XCLK inputs together to allow the single clock to drive both devices. If a T1XC device is used in place of one of the E1XC devices then the jumper must be removed to isolate each clock line and a 37.056 MHz oscillator is used to drive the T1XC XCLK input.

The MT8940 DPLL device requires two oscillators to drive internal DPLLs, one at 12.355 MHz, and the other at 16.384 MHz. If the MT8940 is removed from the daughterboard, then these oscillators can be replaced with ones directly compatible with the backplane rate. Each oscillator output is directly accessible at header pins, allowing connections to be made by connecting jumpers to the E1XC devices.

2.7 E1XC Devices

Up to two E1XC devices can be placed on the daughterboard at a time. Each device runs independent of the other, except when explicit connections are made through the header strips (i.e. when configured as a jitter attenuating format converter). All internal registers are individually accessible and each device has been set up with individual receiver, transmitter and backplane access through headers and connectors. A full description of the E1XC device is beyond the scope of this document. For more information, refer to the PM6341 E1XC datasheet.

2.8 "CSU" Connection Blocks

While the main purpose of the evaluation daughterboard is to provide unrestricted access to all of the features of the E1XC device, one application is conveniently provided which allows easy evaluation of most of the features of the device. By plugging in shorting jumpers into the two 16 pin CSU DIP sockets (U5 and U6) on the daughterboard, the two E1XCs are connected back to back to implement a jitter-attenuating format converter (a function often implemented within a CSU) as described in the E1XC datasheet. These CSU DIP socket jumpers make almost all of the necessary connections except for the signals BRCLK, BRFPI, and BTCLK. Connections for these signals are made through E-W and W-E jumper blocks J19, J20, J21, J22, J23, and J24. By installing jumper connections between pin 1 and pin 2 of jumper blocks J19 and J20, between pin 3 and pin 4 of each of jumper blocks J21, J22, J23, J24, and between pin 2 and 3 of jumper block J30, a "CSU" like application can be implemented where the 2.048 MHz clock for the backplane between the two E1XC devices is provided by the MT8940, which in turn is locked to the recovered clock provided by E1XC #1. Variations of this application can be explored by using the other options provided on the jumper blocks. Connections are provided for 2.048 MHz and externally supplied backplane clock rates.

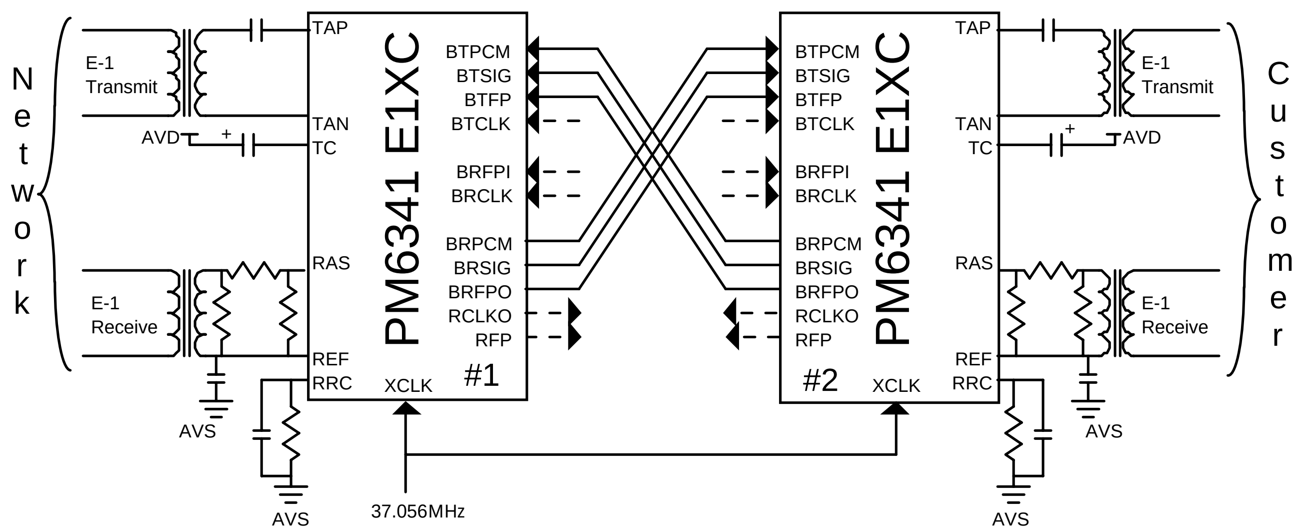

Figure 2: Jitter Attenuating "CSU" Application Hookup

2.9 Transmit/Receive Interface

The daughterboard provides three different types of interfaces for the transmit and receive signals. The two standard analog interfaces provided are a 120 ohm mini-bantam interface and a 75 ohm BNC interface. The transmit mini-bantams are terminated with a 200 ohm resistor on the TN/RN pins to prevent an excessive voltage kick when mini-bantam plugs are inserted or removed. The BNC connector barrel can optionally be terminated with a resistor to ground, or grounded directly, by stuffing a resistor or shorting strap in locations R15, R16, R17, and R18. The daughterboard is shipped with these 4 locations empty, thereby providing a 75• BNC interface. The third interface provided is strictly digital and brings out all of the E1XC's digital E-1 signals to header pins for easy test access. When the digital interface is used each E1XC's analog receiver can be powered down by moving the jumper on jumper block J31 or J32.

3 INTERFACE DESCRIPTION

3.1 Edge Connector Interface

The Edge Connector Interface is made up of a male 96 pin DIN of which 64 pins are actually used. It consists of signals appropriate to read and write to the registers of the devices on the daughterboard, and it provides the necessary power and ground. The connections have been specially designed to mate with PMC's PM1501 EVMB evaluation motherboard. TTL signal levels are used on this interface.

Signal Name	Type	Pin	Function
ALE	O	C1	Address latch enable. When high, identifies that address is valid on AD[7:0].
E	O	C2	Microprocessor Clock
RWB	O	C3	Active low write, active high read enable
RSTB	O	C4	Active low H/W reset
A[15]	O	C5	Address bus bit 15
A[14]	O	C6	Address bus bit 14
A[13]	O	C7	Address bus bit 13
A[12]	O	C8	Address bus bit 12
A[11]	O	C9	Address bus bit 11
A[10]	O	C10	Address bus bit 10
A[9]	O	C11	Address bus bit 9
A[8]	O	C12	Address bus bit 8
AD[7]	I/O	C13	Multiplexed address/data bus bit 7
AD[6]	I/O	C14	Multiplexed address/data bus bit 6
AD[5]	I/O	C15	Multiplexed address/data bus bit 5
AD[4]	I/O	C16	Multiplexed address/data bus bit 4
AD[3]	I/O	C17	Multiplexed address/data bus bit 3
AD[2]	I/O	C18	Multiplexed address/data bus bit 2

AD[1]	I/O	C19	Multiplexed address/data bus bit 1
AD[0]	I/O	C20	Multiplexed address/data bus bit 0
PA3	O	C21	68HC11 Processor Port A bit 3
PA4	O	C22	68HC11 Processor Port A bit 4
PA5	O	C23	68HC11 Processor Port A bit 5
PA6	O	C24	68HC11 Processor Port A bit 6
PD2	I	C25	MISO. Master In Slave Out of Port D acting as SPI. Pulled up on motherboard.
PD3	O	C26	MOSI. Master Out Slave In of Port D acting as SPI. Pulled up on motherboard.
PD4	O	C27	SCK. Serial clock of Port D acting as SPI. Pulled up on motherboard.
PD5	O	C28	SS. Slave Select of Port D acting as SPI active low. Pulled up on motherboard.
IRQ	I	C29	Maskable interrupt
XIRQ	I	C30	Non Maskable Interrupt
DISB	I	C31	EVMB memory disable. Pulling this signal low will disable MPU access to the EVMB's on-board RAM and EPROM.
SP	O	C32	SPARE
GND	O	A1-A28	Ground
+5V	O	A29-A32	+5 Volts

3.2 Header Connections

All E1XC functional pins are connected to male header strips to provide as much access as possible. These headers may be used as probe points or as a means to build sample applications by making appropriate connections between points. Each E1XC can run in isolation of the other, thus any application, other than the default sample "CSU", will require header connections to be made.

3.2.1 External Signal Header

This header is provided to accept an external clock and framing pulse source. These inputs are then buffered for use on the board. External clock sources must be buffered through this header to avoid possible damage to the E1XCs or DPLL.

Signal	Type	Ref.	Description
EXTFP	I	J26-2	External Framing Pulse Input
EXTCLK	I	J26-4	External Clock Input
BEXTFP	O	J27-1	Buffered External Framing Pulse
BEXTCLK	O	J27-2	Buffered External Clock

3.2.2 DPLL Header

This header is provided to give access to the clock generating MT8940 DPLL chip as well as provide direct oscillator access. All of the major DPLL outputs are brought out to this header even though they may be of limited use with the E1XC (e.g. the 4.096 MHz clock).

Signal	Type	Ref.	Description
FPIN	I	J29-2	1.544 MHz Framing pulse input to MT8940.
C8KB	I/O	J29-1	2.048 MHz Framing pulse in/out (mode dependent).
GFP	I/O	J29-3	8 kHz Framing pulse output from the MT8940. Note that this active low output signal is derived from the 16.388 MHz clock and has a 244ns pulse width.
C1M5	O	J29-4	1.544 MHz Output clock from MT8940.
C1M5B	O	J29-5	Inverted C1M5 clock.
C2M	O	J29-6	2.048 MHz output clock from MT8940.
C2MB	O	J29-7	Inverted C2M clock.
C4M	O	J29-8	4.096 MHz Output clock from MT8940.
C4MB	O	J29-9	Inverted C4M clock.

C16M	O	J29-10	Direct access to 16.388 MHz clock driving the MT8940. This pin is mainly provided for direct oscillator access. If the MT8940 is not used the 16.388 MHz clock can be replaced by a 2.048 MHz clock with access to the clock signal provided by this pin.
C12M	O	J29-11	Direct access to 12.355 MHz clock driving the MT8940. This pin is mainly provided for direct oscillator access. If the MT8940 is not used the 12.355 MHz clock can be replaced by a 1.544 MHz clock with access to the clock signal provided by this pin.
GND	G	J29-12	MT8940 DPLL header ground reference.

3.2.3 E1XC Headers

A number of headers are provided which give direct access to the main functional pins on the E1XCs. Both devices on the daughterboard have the same pins brought out to headers and every effort has been made to insure that all headers are symmetrical with both devices. The E1XCs are uniquely identified by an east/west designation. The following table gives a brief description of the E1XC signals. For a more detailed description of the E1XC device, refer to the E1XC datasheet.

Signal	Type	Ref (E)	Ref (W)	Description
TAP	O	J9-1	J10-1	Transmit Analog Positive Pulse
TAN	O	J9-2	J10-2	Transmit Analog Negative Pulse
RAS	I	J9-3	J10-3	Receive Analog Signal
REF	I/O	J9-4	J10-4	Receive Reference
GND	G	J9-5	J10-5	E1XC Analog Ground Reference
TCLKI	I	J15-1	J16-1	Transmit Clock Input
TCLKO	O	J15-2	J16-2	Transmit Clock Output
TDP/TDD	O	J15-3	J16-3	Transmit Digital Positive Line Pulse/ Transmit Digital DS-1 Signal
TDN/TFLG	O	J15-4	J16-4	Transmit Digital Negative Line Pulse/ Transmit FIFO Flag
TDLCLK/ TDLUDR	O	J15-5	J16-5	Transmit Data Link Clock/ Transmit Data Link Underrun
TDLSIG/ TDLINT	I/O	J15-6	J16-6	Transmit Data Link Signal/ Transmit Data Link Interrupt
GND	G	J15-7	J16-7	E1XC Digital Transmit Ground Reference

RDLCLK/ RDLEOM	O	J13-1	J14-1	Receive Data Link Clock/ Receive Data Link End of Message
RDLSIG/ RDLINT	O	J13-2	J14-2	Receive Data Link Signal/ Receive Data Link Interrupt
RCLKI	I	J13-3	J14-3	Receive Line Clock Input
RDP/ RDD/ SDP	I/O	J13-4	J14-4	Receive Digital Positive Line Pulse/ Receive Digital DS-1 Signal/ Sliced Positive Line Pulse
RDN/ RLCV/ SDN	I/O	J13-5	J14-5	Receive Digital Negative Line Pulse/ Receive Line Code Violation Indication/ Sliced Negative Line Pulse
GND	G	J13-6	J14-6	
BTPCM/ BTDP	I	J11-4	J12-4	Backplane Transmit PCM/ Backplane Transmit Positive Line Pulse
BTSIG/ BTDN	I	J11-3	J12-3	Backplane Transmit Signaling/ Backplane Transmit Negative Line Pulse
BTFP	I	J11-2	J12-2	Backplane Transmit Frame Pulse
BTCLK	I	J11-1	J12-1	Backplane Transmit Clock
GND	G	J11-5	J12-5	Backplane Transmit Header Ground Reference
BRCLK	I	J17-1	J18-1	Backplane Receive Clock
BRFPI	I	J17-2	J18-2	Backplane Frame Pulse Input
BRPCM/ BRDP	O	J17-3	J18-3	Backplane Receive PCM/ Backplane Receive Positive Line Pulse
BRSIG/ BRDN	O	J17-4	J18-4	Backplane Receive Signaling/ Backplane Receive Negative Line Pulse
BRFPO	O	J17-5	J18-5	Backplane Frame Pulse Output
RDPCM/ RPCM	O	J17-6	J18-6	Recovered Decoded PCM/ Recovered PCM
RCLKO	O	J17-7	J18-7	Recovered PCM Clock Output
RFP	O	J17-8	J18-8	Receive Frame Pulse
GND	G	J17-9	J18-9	Backplane Receive Ground Reference

3.2.4 Prototype Chip Select Header

Two unused chip selects from the decoding logic are provided on a header near the prototype area.

Signal	Type	Ref.	Description
Spare1_CSB	O	J28-1	Spare CSB pin address (C2XX)
Spare2_CSB	O	J28-2	Spare CSB pin address (C3XX)

3.3 DIP Switches

One 8 bit dip switch is provided on the daughterboard. This switch controls the operating modes of MT8940 PLL chip and the output enables for the various clock outputs. When open, each bit line is pulled high. When closed, the bit lines are individually pulled to ground. For a brief description of the MT8940 operating modes, consult the tables in the Clock PLL implementation description section.

Switch ID	Mapping
Clock 1	MS0
Clock 2	MS1
Clock 3	MS2
Clock 4	MS3
Clock 5	ENC2O
Clock 6	ENCV
Clock 7	ENC4O
Clock 8	Unused

4 PHYSICAL DESCRIPTION

4.1 Characteristics

The E1XC EVBD is an evaluation board that allows the E1XC device to be feature tested and evaluated for various applications. While the daughterboard can be used standalone with a limited feature set, it has been especially designed to link with PMC's EVMB (Evaluation Motherboard). The EVMB controller board provides a microprocessor to read and write to all of the E1XC's internal registers allowing configuration, control and set-up of the various modes of E1XC operation.

The E1XC EVBD is laid out for convenient bench top use for test or demonstration purposes. It is provided with rubber feet that are placed to avoid PCB flexing. Pin headers provide easy access to all signals necessary during device testing. A T1/CEPT Digital PLL is installed to provide the necessary 2.048 MHz backplane rate. External pins allow access when using an externally generated backplane clock. Ground pins for scope probes are conveniently provided and distributed. Simple configuration into the example CSU application is provided. The DIP switches, pin headers, and interface connections are labeled on the silkscreen for easy identification and ample prototype area is provided. The size of the E1XC EVBD is constrained to 8.5 x 6.5 inches and, when mated with the EVMB card, will fit into a standard three ring binder.

4.2 Layout

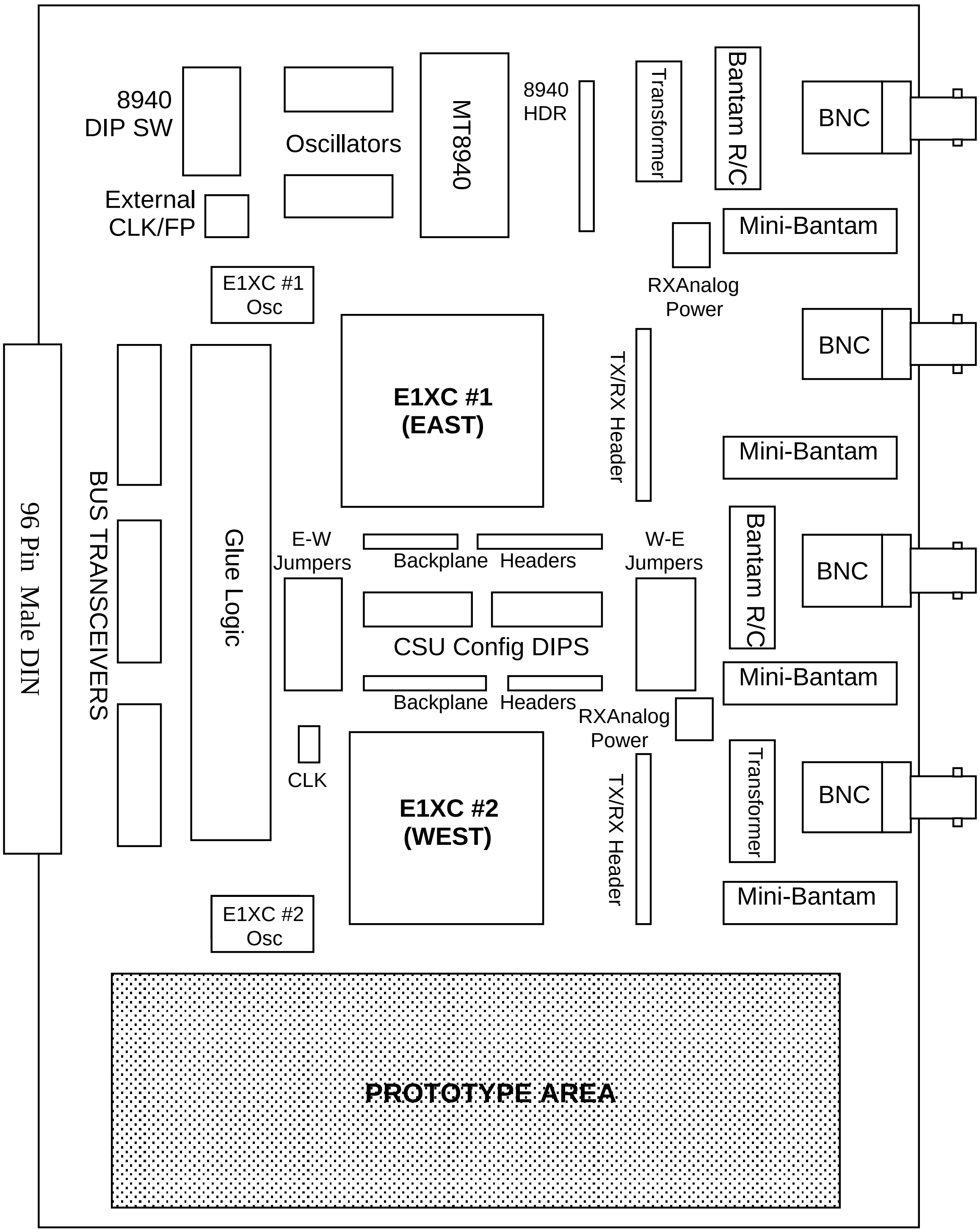

Figure 3: Board Layout

5 D.C. CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{5DC}	+5V DC Power Supply Voltage	4.5	5.5	V	
I_{5DC}	+5V DC Power Supply Current		3	A	V_{5DC} = 5.0 V $\pm$ 10%
T_A	Ambient Temperature	0	50	°C	V_{DC} = 5.0 V $\pm$ 10%

6 IMPLEMENTATION DESCRIPTION

The E1XC EVBD (PM6541) is the T1XC EVBD (PM4541) with different stuffing options. The following are the differences between the two products:

1.) Two PM6341s are stuffed instead of two PM4341s.

2.) Oscillator U1 is not stuffed.

3.) Socket U2 is stuffed with a 49.152 MHz oscillator.

4.) Several resistor values are changed:

R4 = R9 = 523 Ω (1%)

R3 = R8 = 4.53 kΩ (1%)

R20 = R22 = 1 kΩ (5%)

5.) Stuff C1 and C4 with a 1 nF capacitor and a 47 Ω resistor in series.

The E1XC EVBD should be shipped with header shunts between the following pins:

J25 - pins 1 and 2
J19 - pins 3 and 4
J20 - pins 3 and 4

J21 - pins 5 and 6
J22 - pins 5 and 6
J23 - pins 5 and 6
J24 - pins 5 and 6
J22 - pins 5 and 6
J30 - pins 1 and 2
J31 - pins 1 and 2
J32 - pins 1 and 2

6.1 Bus Transceivers

Bus Transceivers have been used on the daughterboard to minimize the loading presented to the motherboard microprocessor. Two 74HCT244's buffer all eight upper address bits, the microprocessor control signals, and the external clock and framing pulse inputs. A single 74HCT245 provides the bi-directional buffering of the multiplexed address/data bus. All motherboard signals from the 96-pin DIN connector have been tied through SIPs to insure proper standalone operation. The standard techniques outlined in the EVMB datasheet for implementing the decoding and buffering has been followed.

6.2 Decode Logic

The decode logic provides the address mapping of all internal registers of both E1XC's as well as providing generation of the required RDB and WRB signals. Again the implementation of the decode logic has followed the techniques outlined in the EVMB datasheet. E1XC #1 (EAST) is mapped starting at address C000H and E1XC #2 (WEST) is mapped starting at address C100H. Two unused chip selects, active for address ranges C200-C2FFH and C300-C3FFH, are available for use on the prototype section. The full register map is given below:

East E1XC	West E1XC	Description
C000H	C100H	E1XC Receive Options
C001H	C101H	E1XC Receive Backplane Options
C002H	C102H	E1XC Datalink Options
C003H	C103H	E1XC Receive Interface Configuration
C004H	C104H	E1XC Transmit Interface Configuration
C005H	C105H	E1XC Transmit Backplane Options
C006H	C106H	E1XC Transmit Framing Options
C007H	C107H	E1XC Transmit Timing Options
C008H	C108H	E1XC Master Interrupt Source
C009H	C109H	E1XC Receive TS0 Data Link Enables
C00AH	C10AH	E1XC Master Diagnostics
C00BH	C10BH	E1XC Master Test
C00CH	C10CH	E1XC Revision/Chip ID
C00DH	C10DH	E1XC Master Reset
C00EH	C10EH	E1XC Phase Status Word (LSB)
C00FH	C10FH	E1XC Phase Status Word (MSB)
C010H	C110H	CDRC TSB Configuration
C011H	C111H	CDRC TSB Interrupt Enable
C012H	C112H	CDRC TSB Interrupt Status
C013H	C113H	Alternate Loss of Signal
C014H	C114H	XPLS TSB Line Length Configuration
C015H	C115H	XPLS TSB Control/Status
C016H	C116H	XPLS TSB CODE Indirect Address
C017H	C117H	XPLS TSB CODE Indirect Data
C018H	C118H	DJAT TSB Interrupt Status

C019H	C119H	DJAT TSB Reference Clock Divisor (N1) Control
C01AH	C11AH	DJAT TSB Output Clock Divisor (N2) Control
C01BH	C11BH	DJAT TSB Configuration
C01CH	C11CH	ELST TSB Configuration
C01DH	C11DH	ELST TSB Interrupt Enable/Status
C020H	C120H	FRMR TSB Framing Alignment Options
C021H	C121H	FRMR TSB Maintenance Mode Options
C022H	C122H	FRMR TSB Framing Status Interrupt Enable
C023H	C123H	FRMR TSB Maintenance/Alarm Status Interrupt
C024H	C124H	FRMR TSB Framing Status Interrupt Indication
C025H	C125H	FRMR TSB Maintenance/Alarm Status Interrupt Indication
C026H	C126H	FRMR TSB Framing Status
C027H	C127H	FRMR TSB Maintenance /Alarm Status
C028H	C128H	FRMR TSB International/National Bits
C029H	C129H	FRMR TSB Extra Bits
C02AH	C12AH	FRMR TSB CRC Error Count - LSB
C02BH	C12BH	FRMR TSB CRC Error Count - MSB
C02CH	C12CH	TS16 AIS Alarm Status
C030H	C130H	TPSC TSB Configuration
C031H	C131H	TPSC TSB µP Access Status
C032H	C132H	TPSC TSB Channel Indirect Address/Control
C033H	C133H	TPSC TSB Channel Indirect Data Buffer
C034H	C134H	XFDL TSB Configuration
C035H	C135H	XFDL TSB Interrupt Status
C036H	C136H	XFDL TSB Transmit Data
C038H	C138H	RFDL TSB Configuration
C039H	C139H	RFDL TSB Interrupt Status/Control
C03AH	C13AH	RFDL TSB Status
C03BH	C13BH	RFDL TSB Receive Data
C040H	C140H	SIGX TSB Configuration
C041H	C141H	SIGX TSB µP Access Status
C042H	C142H	SIGX TSB Channel Indirect Address/Control
C043H	C143H	SIGX TSB Channel Indirect Data Buffer
C044H	C144H	TRAN TSB Configuration
C045H	C145H	TRAN TSB Transmit Alarm/Diagnostic Control
C046H	C146H	TRAN TSB International/National Control
C047H	C147H	TRAN TSB Extra Bits Control

C048H	C148H	PMON TSB Control/Status
C049H	C149H	PMON TSB FER Count
C04AH	C14AH	PMON TSB FEBE Count (LSB)
C04BH	C14BH	PMON TSB FEBE Count (MSB)
C04CH	C14CH	PMON TSB CRC Count (LSB)
C04DH	C14DH	PMON TSB CRC Count (MSB)
C04EH	C14EH	PMON TSB LCV Count (LSB)
C04FH	C14FH	PMON TSB LCV Count (MSB)
C059H	C159H	RSLC TSB Configuration
C05DH	C15DH	RSLC TSB Interrupt Enable/Status

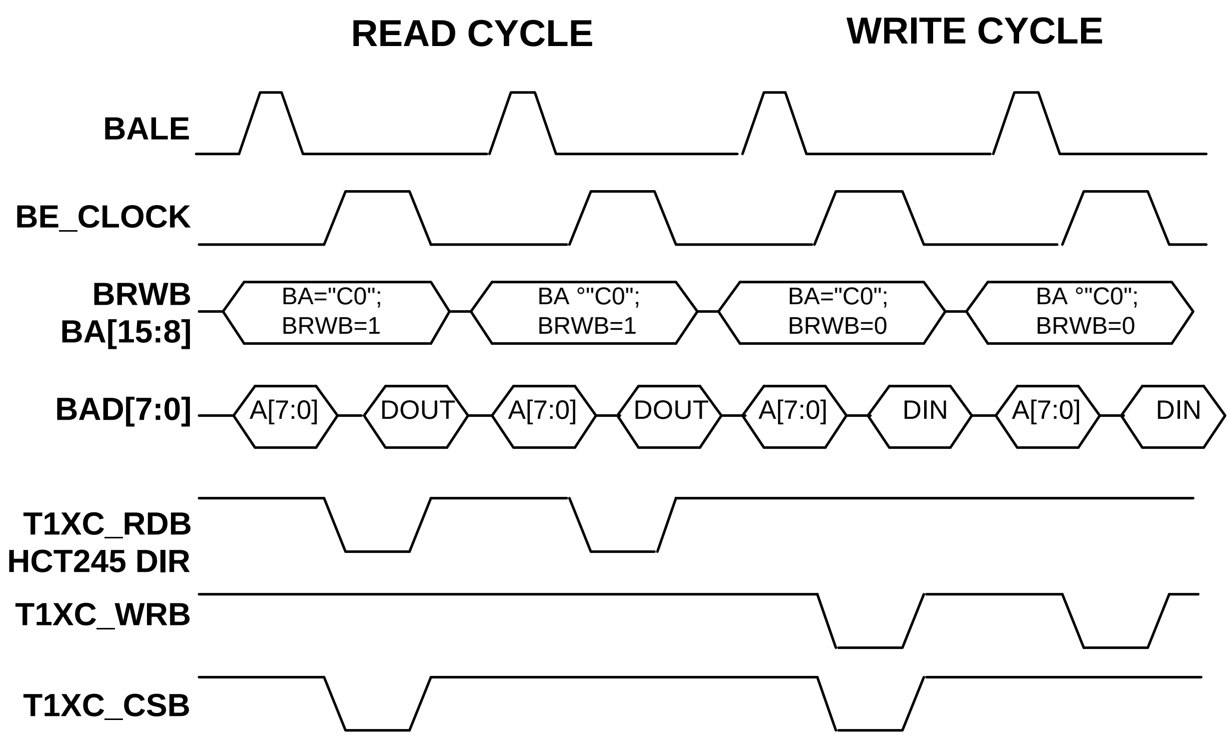

Figure 4: Decode Logic Waveforms

6.3 Clock PLL and DIP Switches

One Mitel MT8940 provides all clocks necessary to drive the 2048 kbit/s backplane rate supported by the E1XC. The MT8940 is a dual digital PLL which can provide timing and synchronization signals for T1 or CEPT transmission links and the ST-BUS . The first PLL provides the T1 clock (1.544 MHz) synchronized to an input framing pulse. The second PLL provides CEPT or ST-BUS timing signals synchronized to an internal or external framing pulse signal. For a more detailed description of the device, refer to the datasheet on the MT8940 in the Mitel Semiconductor Databook.

All outputs of the MT8940 are either brought out to header blocks or routed to the CSU connector DIP sockets. A single 8-position DIP switch provides control over the mode of the MT8940 device as well as control over the output clock enables. If the MT8940 is not used, it can be removed from the daughterboard and its oscillators can be replaced with 1.544 MHz and 2.048 MHz devices. The PLL oscillator clock outputs are conveniently brought out to the header strip for use on the daughterboard.

The mapping of the DIP switches to the MT8940 ports is as follows:

Switch ID	Label	Mapping
SW1-1	MS0	MS0 (Mode Select '0')
SW1-2	MS1	MS1 (Mode Select '1')
SW1-3	MS2	MS2 (Mode Select '2')
SW1-4	MS3	MS3 (Mode Select '3')
SW1-5	ENC2	ENC20 (Active high enable control for pins C2O and C2OB)
SW1-6	ENCV	ENCV (Active high enable control for pins CV and CVB)
SW1-7	ENC4	ENC40 (Active high enable control for pins C4O and C4OB)
SW1-8		Unused

Setting these switches selects the operating mode for the MT8940, as described below:

Mode #	MS[0:3]	DPLL #1 Operating Mode	DPLL #2 Operating Mode
0	0000	Normal Mode: Generates the 1.544 MHz T1 clock synchronized to the falling edge of the input framing pulse.	Externally applied 4.096 MHz. clock and 8 kHz. frame pulse, properly phase related, are used to generate the 2.048 MHz output clock.
1	0001	Normal Mode Operates as above.	Normal Mode: Generates the CEPT (ST-BUS) timing signals locked to the 8 kHz input signal (C8KB)

2	0010	Normal Mode Operates as above.	Externally applied 4.096 MHz. clock is used to generate the 2.048 MHz output clock and 8 kHz frame pulse.
3	0011 DEFAULT CONFIG	Normal Mode Operates as above.	Normal Mode Generates the CEPT (ST-BUS) timing signals locked to the 8 kHz input signal (C8KB)
4	0100	Divide-1 Mode: Divides the CVB input signal by 193. The divided output is connected to DPLL #2	Externally applied 4.096 MHz. clock and 8 kHz. frame pulse, properly phase related, are used to generate the 2.048 MHz output clock.
5	0101	Divide-1 Mode Operates as above	Single Clock-1 Mode: Provides the CEPT/ST-BUS compatible timing signals locked to an 8 kHz. internal signal provided by DPLL #1.
6	0110	Divide-1 Mode	Same as 'mode 2'
7	0111	Divide-1 Mode	Single Clock-1 Mode
8	1000	Normal Mode	Same as 'mode 0'
9	1001	Normal Mode	F0B becomes an input. DPLL #2 provides the ST-BUS signals locked onto F0B input only if it is 16 kHz.
10	1010	Normal Mode	Same as 'mode 2'
11	1011	Normal Mode	Free Run Mode Provides the CEPT/ST-BUS compatible timing and framing signals with no external inputs other than the master clock.

12	1100	Divide-2 Mode: Divides the CVB input by 256. The divided output is connected to DPLL #2	Same as 'mode 0'
13	1101	Divide-2 Mode	Single Clock-2 Mode: Provides the CEPT/ST-BUS signals locked to the 8 kHz. internal signal provided by DPLL #1
14	1110	Divide-2 Mode	Same as 'mode 2'
15	1111	Divide-2 Mode	Single Clock-2 Mode

6.4 E1XC

Two E1XCs can be socketed into the daughterboard. Each is individually accessible and can run independently of the other. All pins except for the microprocessor interface and power pins are connected to header strips for easy test equipment access. Analog receive power pin RAVD is connected to a jumper to enable tying to either ground or power. Tying this pin to ground will disable the internal RSLC TSB, reducing the power consumed. Tying the RAVD pin to VCC enables the normal operating mode. All other power pins are appropriately decoupled and all inputs are tied high through 10 kΩ resistors SIPs.

For a more detailed description of the E1XC and its features, refer to the E1XC Standard Product datasheet.

6.5 "CSU" DIPs and Jumpers

Normally, the two E1XCs run independently of each other except when explicit connections are made between the two devices. To facilitate testing of a simple application involving two devices appropriate control signals have been wired to two 16 pin DIP sockets and six jumpers to enable hooking up the E1XCs in a "CSU"-like application.

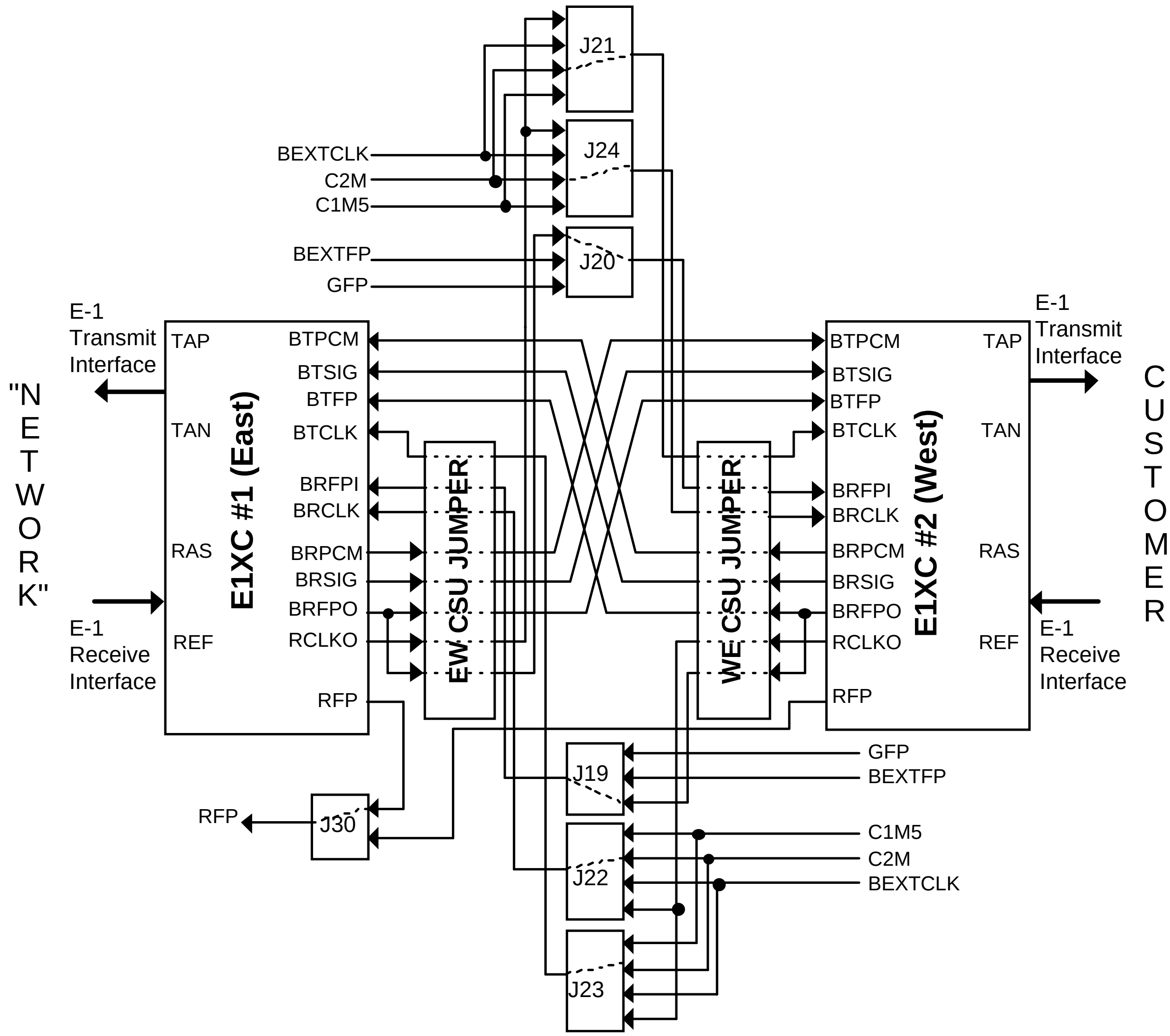

Figure 5: CSU Circuit Overview

Both E1XCs are connected in a symmetrical fashion and most connections are completed by installing shorting bar jumpers into the two 16 pin DIP sockets labeled for the CSU set-up. The remaining unconnected signals are BRCLK, BRFPI, and BTCLK. By installing jumpers across pins 1 and 2 of each of jumper blocks J19 and J20, between pins 3 and 4 of each of the jumper blocks J21, J22, J23, J24, and between pin 2 and 3 of jumper block J30, a "CSU" like application can be implemented where the 2.048 MHz clock for the backplane between the two E1XC devices is provided by the MT8940, which in turn is locked to the recovered clock provided by E1XC #1. Bits 1 and 2 of SW1 must be closed; the remaining bits open. By appropriately making jumper connections to the other available clock options, the backplane can be run at different rates, such 2.048 MHz or at an externally supplied clock rate.

6.6 Transmit/Receive Interfaces

Three different transmit and receive interfaces are provided on the daughterboard. The digital interface can be used by connecting to the two header blocks immediately adjacent to each E1XC. Header blocks J13 and J15 provide the digital interface for the east E1XC while headers J14 and J16 provide the interface for the west E1XC. Before making use of these pins, the analog receiver of each E1XC should be disabled. This is done by moving the jumpers on J31 and J3, which provide power to RAVD, to the grounding position.

Two E-1 analog interfaces are also provided. Both the transmit and receive E-1 interfaces on each E1XC can be connected to either a mini-bantam or BNC connector. The analog transmit and receive interface are passed through a 1:1.36 and 2:1 transformer, respectively, and then connected to either Bantam or BNC connectors. The transmit mini-bantam is terminated with a 100 ohm resistor to prevent "kick-back" when a plug is inserted or removed from the jack. The receive BNC interface is a standard 75 ohm coax with stuffing options for ground or resistor connections across the shield (or barrel).

7 E1XC DAUGHTERBOARD FIRMWARE DESCRIPTION

The EVMB evaluation board provides a serial interface for hooking up a standard "VT100" type terminal. The RF2 SERIAL 25-pin D-type connector on the EVMB is configured as a DCE, 9600 BAUD, 8 bit, NO PARITY, one STOP bit. Connecting a terminal to this port, setting switch 2 on the MODE switch bank to CLOSED and pressing the RESET switch on the EVMB will enable console control.

When the system is started cold or after a hardware reset, the first output to the console will be the Forth kernel identification followed by a prompt:

```
Max-FORTH vX.X
>
```

The first commands that should be downloaded into the system after a cold boot should be (note: each line must be terminated with a "carriage return"; the text within parenthesis are comments and do not have to be typed in):

```
HEX           ( Set up Hex number base )
100 TIB !     ( Relocate text input buffer to eRAM address
100H )
50 TIB 2+ !   ( Define 80 character text input buffer length )
200 DP !      ( Set up Dictionary Pointer )
```

After inputting each of these commands followed by a carriage return, the FORTH interpreter should respond with an "OK" signifying it has accepted it. Any failure to properly input these set-up statements will be characterized by a "?" response from the interpreter and/or by errors when inputting any subsequent data. Further, if an error occurred while entering the commands to relocate the text input buffer or redefine its length, the text buffer will be unable to accept more than the default 16 characters per line input.

The following Forth code was developed for the E1XC daughterboard and presented here as an example. To set-up the E1XC, all that is minimally required is the above EVMB initialization words, the register address CONSTANT definitions, and the RD and WR routines. The remaining words are useful for exercising the more advanced features of the E1XC.

```
VARIABLE DEV
VARIABLE TSB
VARIABLE M
VARIABLE N
VARIABLE T
```

```
( Define base addresses)

C000 CONSTANT EE1XCNORM
C080 CONSTANT EE1XCTEST
C100 CONSTANT WE1XCNORM
C180 CONSTANT WE1XCTEST
10 CONSTANT CDRC
14 CONSTANT XPLS
18 CONSTANT DJAT
1C CONSTANT EELST
20 CONSTANT FRMR
30 CONSTANT PCSC
34 CONSTANT XFDL
40 CONSTANT ESIGX
44 CONSTANT TRAN
48 CONSTANT PMON
5C CONSTANT RSLC
00 CONSTANT RXOPT
01 CONSTANT RXBP
02 CONSTANT RXDL
03 CONSTANT RXIF
04 CONSTANT TXIF
05 CONSTANT TXBP
06 CONSTANT TXFO
07 CONSTANT TXTO
08 CONSTANT INTSTAT
0D CONSTANT MDIAG
0D CONSTANT MRESET

(  ### GENERAL PURPOSE ROUTINES ###  )

: RD        (  addr --- data )
  C@ ;

 : PRT     (  data ---  )
  ." = " U.
  ." HEX" CR ;

: WR        (  addr data --- )
   SWAP C! ;

: EAST
EE1XCNORM DEV !
;
```

```
: WEST
WE1XCNORM DEV !
;

: AD                    ( tsb offset --- addr )
 ( calculate the absolute address of normal register )
 ( assumes DEV has been set to EE1XCNORM or WE1XCNORM )
    + DEV @ + ;

: WRBIT               (  addr data bitpos  --- )
( modify a single bit based upon "bitpos" mask )
    DUP ROT 01 AND * FF ROT -
    2 PICK RD AND OR WR  ;

: WRIND        (  offset base data ---  )
( perform SIGX or PCSC indirect write )
( "offset" is the indirect address )
( "base" is the SIGX or PCSC base address )
( "data" is the value to be written )
   SWAP TSB !            (  store base )
   TSB @ 3 + C!          (  write data )
   TSB @ 2 + SWAP 7F AND WR  (  write offset with R/W low )
    10 0 DO
  TSB @ 1 + RD 80 < IF LEAVE THEN  ( leave if not BUSY )
  I 9 > IF CR ." BUSY STILL HIGH " CR LEAVE THEN
    LOOP ;

: RDIND    (  offset base  --- data  )
( perform SIGX or PCSC indirect read )
( "offset" is the indirect address )
( "base" is the SIGX or PCSC base address )
( "data" is the value to read )

   TSB !        (  store base  )
   TSB @ 2 + SWAP 80 OR WR  (  write addr with R/W high )
    10 0 DO
    TSB @ 1 + RD 80 < IF LEAVE THEN  ( leave if not BUSY )
    I 9 > IF CR ." BUSY STILL HIGH" CR LEAVE THEN
    LOOP
    TSB @ 3 + RD ;          (  read data )


( ### CONFIG ### )
( The "data" value is written to the appropriate bit )

:  SIND              ( data --- )
```

```
    ESIGX 0 AD                    ( calc reg addr )
    SWAP 02 WRBIT ;

:  SPCCE              ( data --- )
    ESIGX 0 AD                    ( calc reg addr )
    SWAP 01 WRBIT ;

: RESET           ( data --- )
    MRESET 0 AD                    ( calc reg addr )
    SWAP 01 WRBIT ;

( ### PCSC CONFIG ### )

: PIND                ( data --- )
    PCSC 0 AD                    ( calc reg addr )
    SWAP 2 WRBIT ;

: PPCCE              ( data --- )
    PCSC 0 AD                    ( calc reg addr )
    SWAP 1 WRBIT ;

( ### TRAN CONFIG ### )

: TXAMI               ( data --- )
    TRAN 0 AD                    ( calc reg addr )
    SWAP 80 WRBIT ;

: TXCCS               ( --- )
    TRAN 0 AD                    ( calc reg addr )
    DUP RD 9F AND WR ;

: TXCAS                ( --- )
    TRAN 0 AD                    ( calc reg addr )
    DUP RD 60 OR  WR ;

: GENCRC               ( data --- )
    TRAN 0 AD                    ( calc reg addr )
    SWAP 10 WRBIT ;

:  CRCEN              ( data --- )
    FRMR 0 AD                    ( calc reg addr )
    SWAP 80 WRBIT ;

:  DDL                ( data --- )
    MDIAG 0 AD                    ( calc reg addr )
    SWAP 4 WRBIT ;
```

```
: DML                ( data --- )
    MDIAG 0 AD                    ( calc reg addr )
    SWAP 8 WRBIT ;

: LL                ( data --- )
    MDIAG 0 AD                    ( calc reg addr )
    SWAP 10 WRBIT ;

: PL                ( data --- )
    MDIAG 0 AD                    ( calc reg addr )
    SWAP 20 WRBIT ;

:   REFR               ( data --- )
    FRMR 0 AD                    ( calc reg addr )
    SWAP 04 WRBIT ;

:  RCRCE               ( data --- )
    FRMR 0 AD                    ( calc reg addr )
    SWAP 02 WRBIT ;

: FDIS               ( data --- )
    TRAN 0 AD                    ( calc reg addr )
    SWAP 08 WRBIT ;

: DUMPSIGX          ( --- )
( print SIGX contents )

   CR
   ESIGX 0 AD  TSB !
   1 SWAP SIND


  8 2 DO
     10 0 DO
        J 10 * I + TSB @
        RDIND 3 .R
      LOOP
      CR
  LOOP
;

: DUMPPCSC          ( --- )
( print PCSC contents )

   CR
```

```
    PCSC 0 AD TSB !
    1 PIND


  6 2 DO
      10 0 DO
         J 10 * I + TSB @
         RDIND 3 .R
       LOOP
       CR
   LOOP
 ;

 ( ### INTERRUPT HANDLING ### )

 :  GETINT  ( data int ---  data/2 int/2 < data mod 2> int mod
 2)
                ( data returned only if int mod 2 = 1 )
    2 /MOD SWAP DUP 0>
    IF ROT 2 /MOD
        3 -ROLL SWAP

    ELSE ROT 2/ 2 -ROLL
    THEN
 ;

 :  INT_HANDLE                 ( --- )

 ( ** FRMR ** )

 FRMR 5 AD DUP RD
 DUP 0>
 IF
    ." TIME = " DECIMAL T @ . HEX CR
    SWAP 2+ RD SWAP
    GETINT  0> IF ." CRCE" CR DROP THEN
    GETINT  0> IF ." FEBE" CR DROP THEN
    GETINT  0> IF ." AIS = " . CR THEN
    GETINT  0> IF ." RED = " . CR THEN
    GETINT  0> IF ." TS16AISD = " . CR THEN
    GETINT  0> IF ." AISD = " . CR THEN
    GETINT  0> IF ." RRMA = " . CR THEN
    GETINT  0> IF ." RRA = " . CR THEN
 THEN
 DROP DROP
```

```
FRMR 4 AD DUP RD 7F AND
DUP 0>
IF
   ." TIME = " DECIMAL T @ U. HEX CR
   SWAP 2+ RD SWAP
   GETINT  0> IF ." CMFER" CR DROP THEN
   GETINT  0> IF ." SMFER" CR DROP THEN
   GETINT  0> IF ." FER"  CR DROP THEN
   GETINT  0> IF ." COFA"  CR DROP THEN
   GETINT  0> IF ." OOCMF = " . CR THEN
   GETINT  0> IF ." OOSMF = " . CR THEN
   GETINT  0> IF ." OOF = " . CR THEN
THEN
DROP DROP

FRMR 1 AD RD
03 AND
?DUP 0>
IF
   DUP 1 AND 0>
   IF ." EXCRCE " CR THEN
   2 AND 0>
   IF ." CMFACT " CR THEN
THEN


( ** ELST ** )

EELST 1 AD RD
2 /MOD SWAP 0>
IF
   ." TIME = " DECIMAL T @ U. HEX CR
   01 AND 0> IF ." FORWARD"
                    ELSE ." BACKWARD"
                    THEN  SPACE ." SLIP" CR
ELSE
   DROP
THEN
;

: IH INT_HANDLE ;

( ## init SIGX Per-chan functions ## )

: SIGX_FILL             ( --- )
```

```
ESIGX 0 AD
80 40 DO
    DUP
    I SWAP 1A WRIND
LOOP
DROP
;

( ## init PCSC ## )

:  PCSCFILLIND           ( --- )
( put incrementing idle code in PCSC )

1 PIND

41 20 DO
    PCSC 0 AD I SWAP
    0 WRIND
LOOP

60 41 DO
    PCSC 0 AD I SWAP
    I F AND 10 OR WRIND
LOOP

PCSC 0 AD
40 SWAP 0 WRIND
PCSC 0 AD 50 SWAP 0 WRIND

;


:  POLLPMON          ( --- error )
( print any non-zero contents )
( "error" = 0 if all zero counts; 1 otherwise )

PMON 0 AD
DUP 1+ RD 7F AND DUP    ( read FER )

2 PICK 2+ @ >< 3FF AND DUP ROT OR  ( two byte read of FEBE )

3 PICK 4 + @ >< 3FF AND DUP ROT OR ( two byte read of CRCE )

4 ROLL 6 + @ >< 1FFF AND DUP ROT OR  ( two byte read of LCV )
```

```
IF                                  ( if non-zero count print
)

  DECIMAL T @ U. SPACE
  ." LCV=" 6 .R SPACE
  ." CRCE=" 5 .R SPACE
  ." FEBE=" 5 .R SPACE
  ." FER=" 5 .R CR HEX SPACE

 1   ( return code )
ELSE                              ( else do nothing )
   DROP DROP DROP DROP 0
THEN
 ;

(  ## MONITOR E1XC ACTIVITY ## )

: POLLE1XC
( check E1XC status continuously and transfer PMON about )
( once per second.  Only error conditions reported. )

03 B026 C! ( INIT PACTL )
40 B025 C! ( CLEAR RTIF )

0 T !
BEGIN
    1F 0 DO
       BEGIN
           INT_HANDLE
           B025 C@ 40 AND 0>
       UNTIL    ( WAIT FOR RTIF )
       40 B025 C! ( CLEAR TOF )
    LOOP
   T 1+!
   PMON 0 AD 0 WR
   POLLPMON DROP

?TERMINAL UNTIL ;

:  MAINTEST

1 PPCCE
1 PIND
1 SIND
1 GENCRC
1 CRCEN
```

```
POLLE1XC
;
```

This document is not intended to give a full tutorial in FORTH, which is better covered in the many FORTH books available. The FORTH kernel on the 68HC11 on the EVMB is based upon the FORTH-83 standard and should be upward compatible from FORTH-79. For a complete, detailed FORTH tutorial, refer to the manuals listed in the references.

8 STOCK LIST

Item	Qty	Reference	Description
1		C1, C4	Not Installed
2	2	C2, C5	0.68 µF ceramic capacitor, 0.3" spacing, 100VDC
3	2	C3, C6	0.1 µF ceramic capacitor, 0.3" spacing, 100VDC
4	2	C7, C8	47 nF ceramic capacitor, 0.2" spacing, 100VDC
5	2	C9, C10	470 nF ceramic capacitor, 0.2" spacing, 100VDC
6	25	C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35	0.01 µF ceramic Capacitor, 0.2" spacing, 100VDC

7	4	J1, J2, J3, J4	ADC PC834 Bantam PCB Jack with cover
8	4	J5, J6, J7, J8	Molex 73136-5001 BNC PCB Mount Jack, 50 ohm impedance
9	1	J9, J10, J11, J12	INDUS 929647-01-36 breakable male straight single row strip headers, 0.1" spacing, tin plated, 36 contacts - CUT INTO LENGTHS OF 5 CONTACTS EACH
10	1	J13, J14	INDUS 929647-01-36 breakable male straight single row strip headers, 0.1" spacing, tin plated, 36 contacts - CUT INTO LENGTHS OF 6 CONTACTS EACH
11	1	J15, J16	INDUS 929647-01-36 breakable male straight single row strip headers, 0.1" spacing, tin plated, 36 contacts - CUT INTO LENGTHS OF 7 CONTACTS EACH
12	1	J17, J18	INDUS 929647-01-36 breakable male straight single row strip headers, 0.1" spacing, tin plated, 36 contacts - CUT INTO LENGTHS OF 9 CONTACTS EACH
13	1	J19, J20	Dual row male header strip, tin plated, 0.1" spacing, straight, 50 contacts total, INDUS 923866 - CUT INTO LENGTHS OF 3 CONTACT PAIRS EACH
14	1	J21, J22, J23, J24	Dual row male header strip, tin plated, 0.1" spacing, straight, 50 contacts total, INDUS 923866 - CUT INTO LENGTHS OF 4 CONTACT PAIRS EACH
15	1	J25, J27, J28	INDUS 929647-01-36 breakable male straight single row strip headers, 0.1" spacing, tin plated, 36 contacts - CUT INTO LENGTHS OF 2 CONTACTS EACH
16	1	J26, J31, J32	Dual row male header strip, tin plated, 0.1" spacing, straight, 50 contacts total, INDUS 923866 - CUT INTO LENGTHS OF 2 CONTACT PAIRS EACH

17	1	J29	INDUS 929647-01-36 breakable male straight single row strip headers, 0.1" spacing, tin plated, 36 contacts - CUT INTO A LENGTH OF 12 CONTACTS
18	1	J30	INDUS 929647-01-36 breakable male straight single row strip headers, 0.1" spacing, tin plated, 36 contacts - CUT INTO A LENGTH OF 3 CONTACTS
19	1	P1	Right angle mount, 96 pin male DIN edge connector, Winchester 96P-6033-0731-0
20	2	R1, R6	1 Ω, 1/4 W, 5% Resistor
21		R2, R7, R11, R12, R13, R14, R15, R16, R17, R18	Not Installed
22	1	R3 R8	4.53 kΩ, 1/4 W, 1% Resistor
23	1	R4 R9	523 Ω, 1/4 W, 1% Resistor
24	2	R5, R10	1.1 kΩ, 1/4 W, 1% Resistor
25	2	R19, R20, R21, R22	200 Ω, 1/4 W, 5%
26	2	R23, R24	316 kΩ, 1/4 W, 5% Resistor
27	2	R25, R26	270 Ω, 1/4 W, 5%
28	2	R27, R28	330 Ω, 1/4 W, 5%

29		R29, R30, R31, R32, R33, R34, R35, R36, R37	Not Used
30	3	R38, R39, R40	10 kΩ, 1/8 W, 5% Resistor
31	8	RN1, RN2, RN3, RN4, RN5, RN6, RN7, RN8,	10 pin 9 resistor SIP – 10kΩ, 5%
32	1	SW1	8 position SPST DIP switch, Grayhill 76SB08
33	6	S_T1, S_T2, S_U1, S_U2, S_U14, S_U15	14 pin DIP Socket
34	2	S_U3, S_U4	68 Pin PLCC Socket, through hole, AMP 821574-1
35	2	S_U5, S_U6	16 pin DIP Socket
36	1	S_U13	24 pin DIP Socket, 0.6" wide
37	2	T1, T2	Dual 1:2CT & 1:1.36 transformer: BH Electronics 500-1777, OR Pulse Engineering PE64952 Q7789-3
38	1	U1	Not Installed
39		U2	FOX 49.152 MHz Oscillator in half inch case, TTL levels.

40	2	U3, U4	E1XC - Single E-1 Transceiver, PM6341
41	2	U5, U6	U-Link - 8 connections
42	2	U7, U8	74HCT244 Bus Transceiver
43	1	U9	74HCT245 Bi-Directional Bus Transceiver
44	1	U10	74HC138 3 to 8 line demux
45	1	U11	74HC139 Dual 2 to 4 line demux
46	1	U12	74HC00 Quad NAND gate
47	1	U13	Mitel MT8940AC T1/CEPT PLL, Ceramic DIP
48	1	U14	FOX 16.388 MHz Oscillator in half inch case, TTL levels
49	1	U15	FOX 12.355 MHz Oscillator in half inch case, TTL levels
50	10	Sh_J19, Sh_J20, Sh_J21, Sh_J22, Sh_J23, Sh_J24, Sh_J25, Sh_J30, Sh_J31, Sh_J32	Header Shunt 0.1" spacing, Textech 41670300-P4

9 REFERENCES

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- PMC-971216, “Evaluation Board Graphical User Interface User’s Guide”. Dec. 1997, Issue 1

APPENDIX 1: COMPONENT PLACEMENT DIAGRAM

APPENDIX 2: SCHEMATICS

NOTES

NOTES

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