



LB1913

FDD Spindle Motor Driver

Overview

The LB1913 is a three-phase disk drive motor driver IC that is optimal for use as a 3.5-inch floppy disk drive spindle motor driver.

Functions and Features

- Three-phase full-wave linear drive
- On-chip digital speed control
- Start and stop circuits (active low)
- Speed switching
High: 300 rpm, Low: 360 rpm
- Current limiter circuit
- Index comparator circuit
- Index delay circuit
- Thermal protection circuit

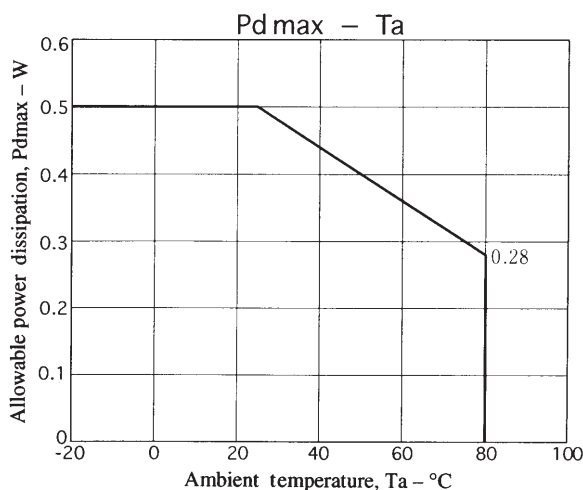
Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max		7.0	V
Maximum output current	I _O max1	t ≤ 0.5 s	1.0	A
Maximum steady-state output current	I _O max2		0.7	A
Allowable power dissipation	Pd max	Independent IC	0.5	W
Operating temperature	T _{opr}		-20 to +80	°C
Storage temperature	T _{stg}		-40 to +150	°C

Allowable Operating Ranges at Ta = 25°C

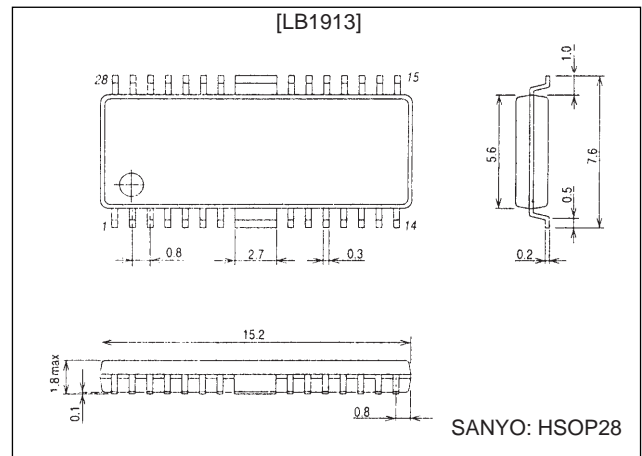
Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V _{CC}		4.2 to 6.5	V



Package Dimensions

unit: mm

3222-HSOP28



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Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I_{CCO}	S/S = 5 V (standby mode)			10	μA
	I_{CC}	S/S = 0 V (normal mode)		12	18	mA
SL bias current	I_{SL}	$V_{SL} = 0\text{ V}$			10	μA
SL input low-level voltage	V_{SLL}		0		1.0	V
SL input high-level voltage	V_{SLH}		3.5		V_{CC}	V
S/S bias current	$I_{S/S}$			180	270	μA
S/S low-level voltage	$V_{S/SL}$		0		0.8	V
S/S high-level voltage	$V_{S/SH}$		3.5		V_{CC}	V
Hall amplifier input bias current	I_{HB}				10	μA
Common-mode input voltage range	V_h		1.5		$V_{CC}-1.0$	V
Differential-mode input voltage range	V_{dif}		50		200	mV_{p-p}
Hall bias output voltage	V_H	$I_H = 5\text{ mA}$		0.8		V
Leakage current	I_{HL}	S/S = 5 V			± 10	μA
Output saturation voltage	V_{sat}	$I_O = 0.7\text{ A}$, sink + source		1.3	1.8	V
Output leakage current	I_{OL}				1.0	mA
Current limiter	V_{lim}		0.27	0.3	0.33	V
Control amplifier voltage gain	G_C			-7		dB
Interphase voltage gain difference	ΔG_C				± 1	dB
V/I converter source current	I^+		9	14	19	μA
V/I converter sink current	I^-		-9	-14	-19	μA
V/I converter current ratio	I^+/I^-		0.8	1.0	1.2	
DSC buffer input current	I_{DSC}				1.0	μA
FG Schmitt hysteresis	ΔV_{sh}	*		50		mV
Number of speed discriminator counts	N			1041.5		
Discriminator operating frequency	F_D	*			1.1	MHz
Oscillator frequency range	F_{OSC}	*			1.1	MHz
Index output low-level voltage	V_{IDL}	$I_O = 2\text{ mA}$			0.4	V
Index output leakage current	I_{IDL}				± 10	μA
FG amplifier voltage gain	G_{FG}	*		48		dB
FG amplifier input offset	V_{FGO}				± 10	mV
FG amplifier internal reference voltage	V_{FGB}		2.2	2.5	2.8	V
Schmitt hysteresis	ΔV_{SH}	*		50		mV
Index input hysteresis	ΔV_{ID}	*		20		mV
Index common-mode input voltage range	V_{ID}		1.0		$V_{CC}-1.0$	V
Thermal shutdown circuit operating temperature	TSD	*	150	180		$^\circ\text{C}$
Hysteresis	ΔTSD	*		40		$^\circ\text{C}$

Note: * These items are design target values and are not tested.

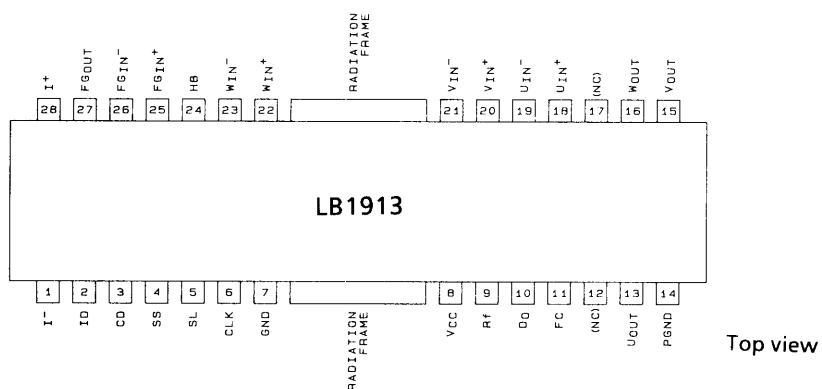
Truth Table

	Source → Sink	Hall input		
		U	V	W
1	V phase → W phase	H	H	L
2	V phase → U phase	L	H	L
3	W phase → U phase	L	H	H
4	W phase → V phase	L	L	H
5	U phase → V phase	H	L	H
6	U phase → W phase	H	L	L

A "high-level" (H) Hall amplifier input means:
 $U_{IN+} > U_{IN-}$
 $V_{IN+} > V_{IN-}$
 $W_{IN+} > W_{IN-}$

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Pin Assignment



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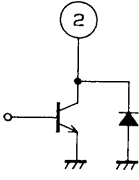
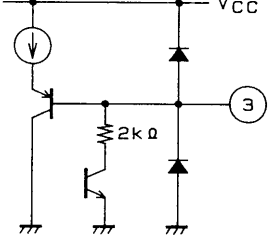
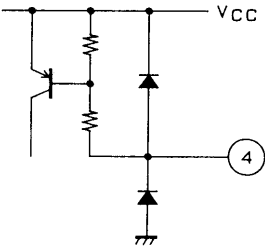
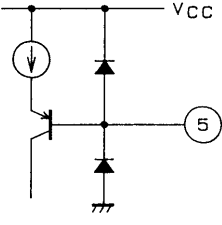
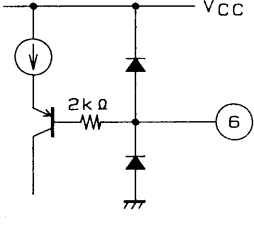
Pin Functions

Pin no.	Pin	Pin voltage	Equivalent circuit	Function
18 19 20 21 22 23	U_{IN+} U_{IN-} V_{IN+} V_{IN-} W_{IN+} W_{IN-}	1.5 V min $V_{CC}-1.0$ V max	<p>A06069</p>	<ul style="list-style-type: none"> • U-phase Hall element input • V-phase Hall element input • W-phase Hall element input
24	HB	0.8 V typ ($I_H = 5$ mA)	<p>A06070</p>	<ul style="list-style-type: none"> • Minus-side pin for applying the Hall bias current This pin goes to the open state in the stopped state and the Hall bias is cut off.
25 26 27	FG_{IN+} FG_{IN-} FG_{OUT}		<p>A06071</p>	<ul style="list-style-type: none"> • FG amplifier plus input A reference voltage of 2.5 V is generated by the IC internally. • FG amplifier minus input • FG amplifier output pin
28 1	I^+ I^-		<p>A06072</p>	<ul style="list-style-type: none"> • Index input

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Pin no.	Pin	Pin voltage	Equivalent circuit	Function
2	ID	Low: 0.4 V max High: 4.5 V min	 <p style="text-align: right;">A06073</p>	<ul style="list-style-type: none"> Index output
3	CD		 <p style="text-align: right;">A06074</p>	<ul style="list-style-type: none"> Connection for external RC time constant circuit.
4	SS	Low: 0.8 V max High: 3.5 V min	 <p style="text-align: right;">A06075</p>	<ul style="list-style-type: none"> Start/stop switching input This is an active-low input.
5	SL	Low: 1.0 V max High: 3.5 V min	 <p style="text-align: right;">A06076</p>	<ul style="list-style-type: none"> Speed switching input
6	CLK	Low: 1.0 V max High: $V_{CC}-1.0$ V min	 <p style="text-align: right;">A06077</p>	<ul style="list-style-type: none"> Reference clock input Use a clock rate of 1 MHz for 300 and 360 rpm speeds.
7	GND			<ul style="list-style-type: none"> Ground connection Connect this pin, pin 14, and the frame to ground.
8	V_{CC}			<ul style="list-style-type: none"> Power supply Provide a well-stabilized power supply so that ripple and noise do not enter the LB1913 from this pin.
9	Rf			<ul style="list-style-type: none"> Used for output current detection. The output current is converted to a voltage and detected by connecting a resistor (Rf) between this pin and V_{CC}. The current limiter operates by detecting the voltage on this pin.

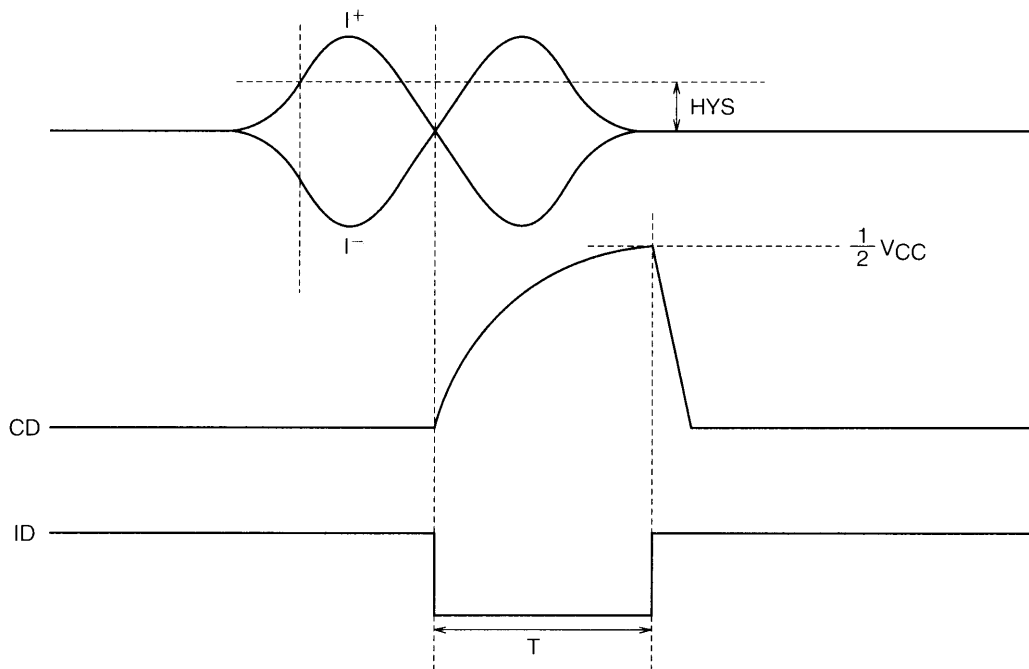
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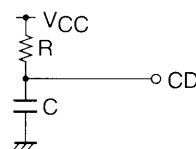
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Pin no.	Pin	Pin voltage	Equivalent circuit	Function
10	D _O			<ul style="list-style-type: none"> • Speed discriminator
11	F _C			<ul style="list-style-type: none"> • Frequency characteristics correction Current control system open loop oscillation can be prevented by inserting a capacitor between this pin and ground.
13 15 16	U _{OUT} V _{OUT} W _{OUT}			<ul style="list-style-type: none"> • U-phase output • V-phase output • W-phase output
14	PGND			<ul style="list-style-type: none"> • Output transistor ground connection

Index Delay Pulse Timing Chart

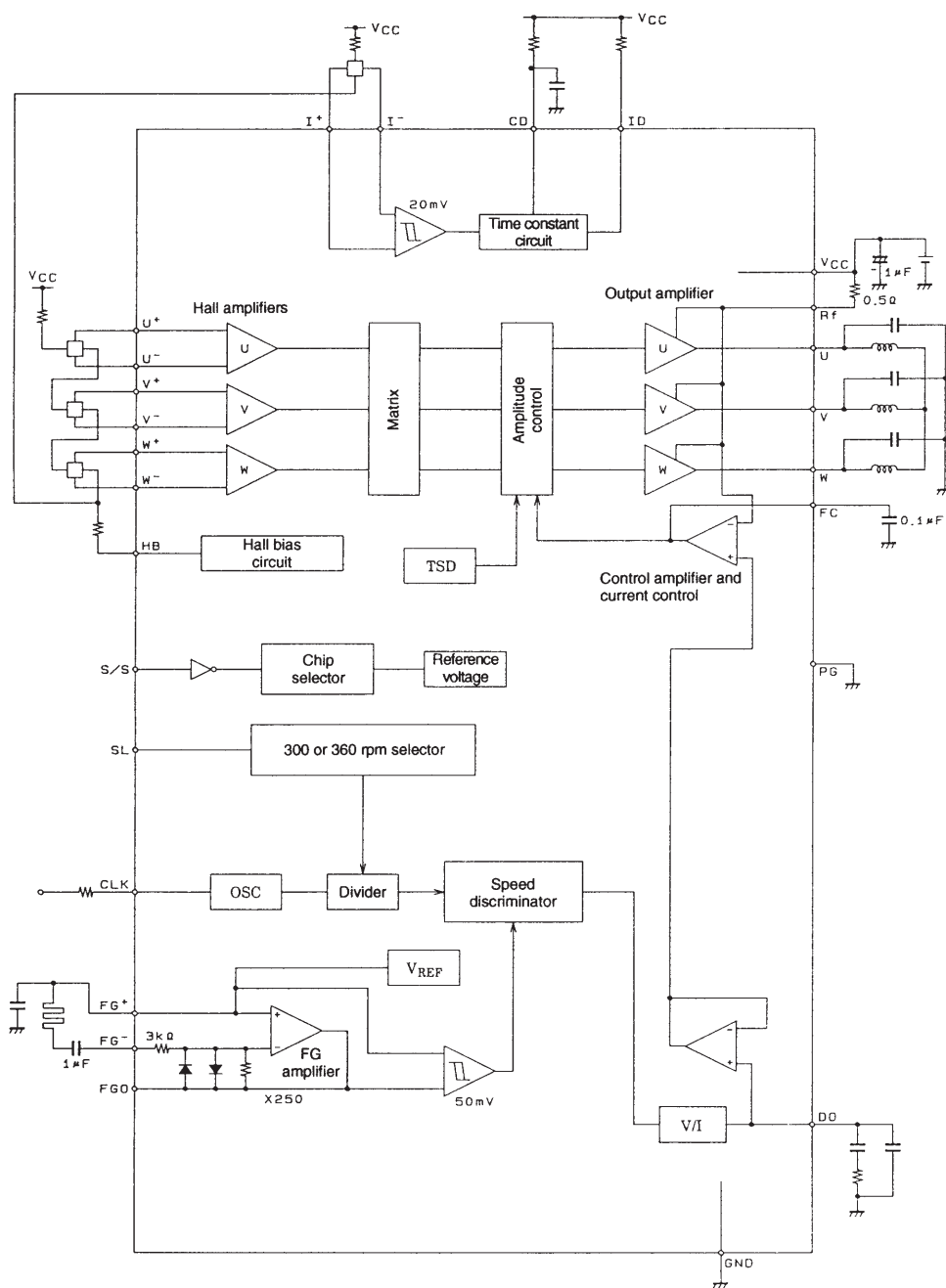


When SL = high $T_{300} \approx 0.693CR$
 When SL = low $T_{360} \approx 0.577CR$



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Block Diagram



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