

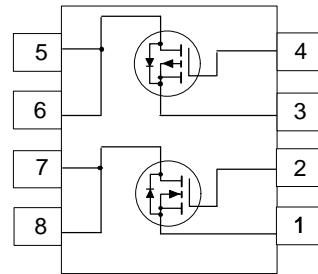
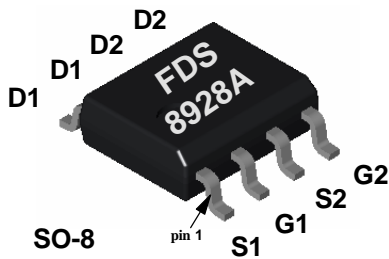
FDS8928A Dual N & P-Channel Enhancement Mode Field Effect Transistor

General Description

These dual N- and P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- N-Channel 5.5 A, 30 V, $R_{DS(ON)}=0.030 \Omega @ V_{GS}=4.5 V$
 $R_{DS(ON)}=0.038 \Omega @ V_{GS}=2.5 V$.
- P-Channel -4 A, -20 V, $R_{DS(ON)}=0.055 \Omega @ V_{GS}=-4.5 V$
 $R_{DS(ON)}=0.072 \Omega @ V_{GS}=-2.5 V$.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual (N & P-Channel) MOSFET in surface mount package.



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage	30	-20	V
V_{GSS}	Gate-Source Voltage	8	-8	V
I_D	Drain Current - Continuous (Note 1a)	5.5	-4	A
	- Pulsed	20	-20	
P_D	Power Dissipation for Dual Operation	2		W
	Power Dissipation for Single Operation (Note 1a)	1.6		
	(Note 1b)	1		
	(Note 1c)	0.9		
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150		$^\circ\text{C}$
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78		$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40		$^\circ\text{C/W}$

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	N-Ch	30			V
		$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	P-Ch	-20			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	N-Ch		32		mV/°C
		$I_D = -250\ \mu\text{A}$, Referenced to 25°C	P-Ch		-23		
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$	N-Ch			1	μA
		$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$	P-Ch			-1	μA
I_{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$	All			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -8\text{ V}, V_{DS} = 0\text{ V}$	All			-100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	N-Ch	0.4	0.67	1	V
		$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	P-Ch	-0.4	-0.6	-1	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	N-Ch		-3		mV/°C
		$I_D = -250\ \mu\text{A}$, Referenced to 25°C	P-Ch		4		
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 4.5\text{ V}, I_D = 5.5\text{ A}$	N-Ch		0.025	0.03	Ω
		$V_{GS} = 2.5\text{ V}, I_D = 4.5\text{ A}$			0.031	0.038	
		$V_{GS} = -4.5\text{ V}, I_D = -4\text{ A}$	P-Ch		0.043	0.055	
		$V_{GS} = -2.5\text{ V}, I_D = -3.4\text{ A}$			0.059	0.072	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	N-Ch	20			A
		$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	P-Ch	-20			
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 5.5\text{ A}$	N-Ch		20		S
		$V_{DS} = -5\text{ V}, I_D = -4\text{ A}$	P-Ch		13		S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	N-Ch		900		pF
			P-Ch		1130		
C_{oss}	Input Capacitance		N-Ch		410		pF
			P-Ch		480		
C_{rss}	Reverse Transfer Capacitance		N-Ch		110		pF
			P-Ch		120		

Electrical Characteristics (continued)

SWITCHING CHARACTERISTICS (Note 2)

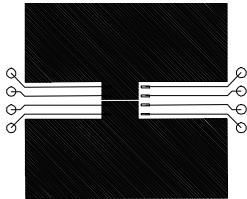
Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
$t_{D(on)}$	Turn - On Delay Time	$V_{DS} = 6\text{ V}$, $I_D = 1\text{ A}$ $V_{GS} = 4.5\text{ V}$, $R_{GEN} = 6\ \Omega$	N-Ch		6	12	ns
			P-Ch		8	16	
t_r	Turn - On Rise Time		N-Ch		19	31	ns
			P-Ch		23	37	
$t_{D(off)}$	Turn - Off Delay Time	$V_{DS} = -10\text{ V}$, $I_D = -1\text{ A}$ $V_{GS} = -4.5\text{ V}$, $R_{GEN} = 6\ \Omega$	N-Ch		42	67	ns
			P-Ch		260	360	
t_f	Turn - Off Fall Time		N-Ch		13	24	ns
			P-Ch		90	125	
Q_g	Total Gate Charge	$V_{DS} = 10\text{ V}$, $I_D = 5.5\text{ A}$, $V_{GS} = 4.5\text{ V}$	N-Ch		19.8	28	nC
			P-Ch		20	28	
Q_{gs}	Gate-Source Charge	$V_{DS} = -5\text{ V}$, $I_D = -4\text{ A}$, $V_{GS} = -5\text{ V}$	N-Ch		2		nC
			P-Ch		2.8		
Q_{gd}	Gate-Drain Charge	$V_{GS} = -5\text{ V}$	N-Ch		6.3		nC
			P-Ch		3.2		

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

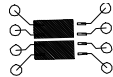
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			1.3	A
			P-Ch			-1.3	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 1.3\text{ A}$ (Note 2)	N-Ch		0.68	1.2	V
		$V_{GS} = 0\text{ V}$, $I_S = -1.3\text{ A}$ (Note 2)	P-Ch		-0.7	-1.2	V

Notes:

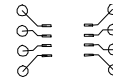
- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 78°C/W on a 0.5 in² pad of 2oz copper.



b. 125°C/W on a 0.02 in² pad of 2oz copper.



c. 135°C/W on a 0.003 in² pad of 2oz copper.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

Typical Electrical Characteristics: N-Channel

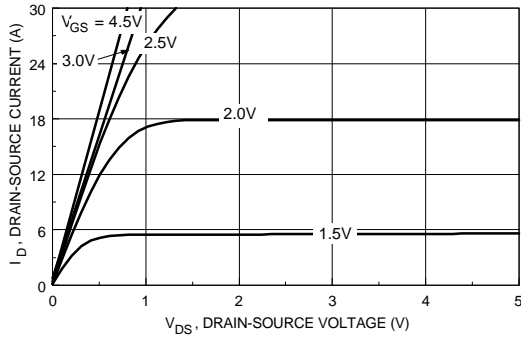


Figure 1. On-Region Characteristics.

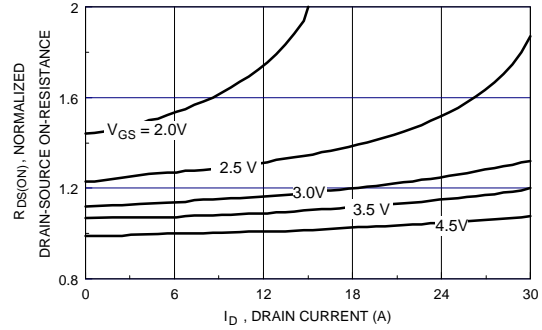


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

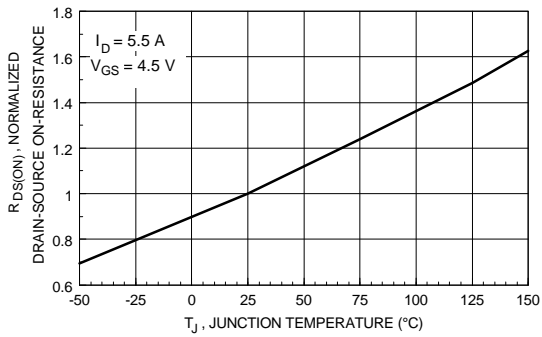


Figure 3. On-Resistance Variation with Temperature.

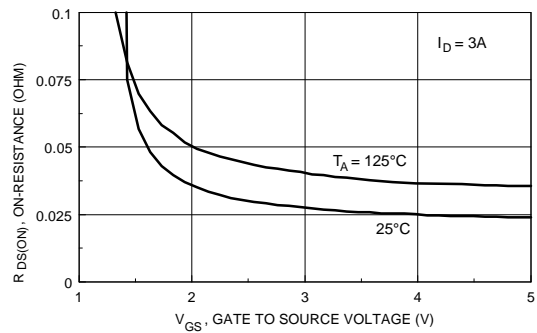


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

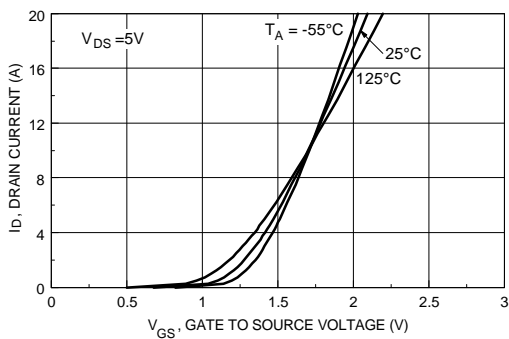


Figure 5. Transfer Characteristics.

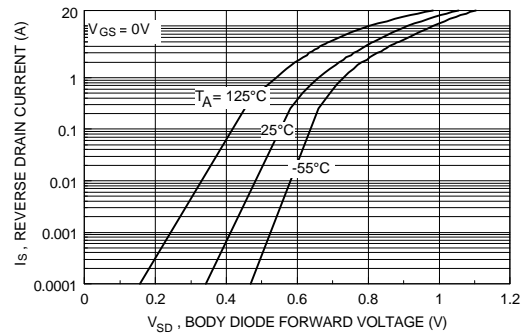


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics: N-Channel (continued)

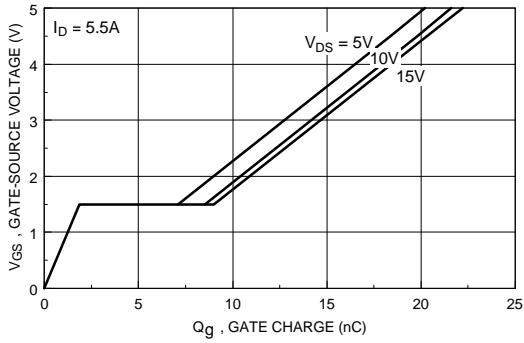


Figure 7. Gate Charge Characteristics.

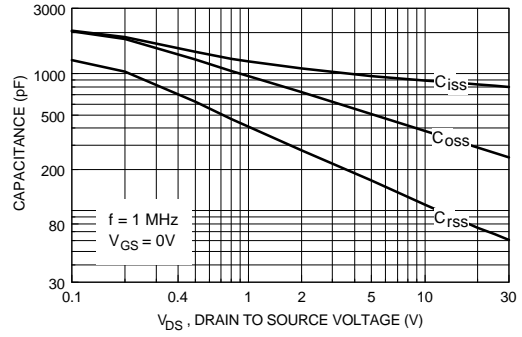


Figure 8. Capacitance Characteristics.

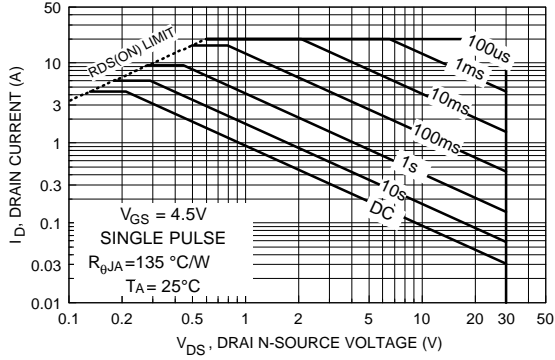


Figure 9. Maximum Safe Operating Area.

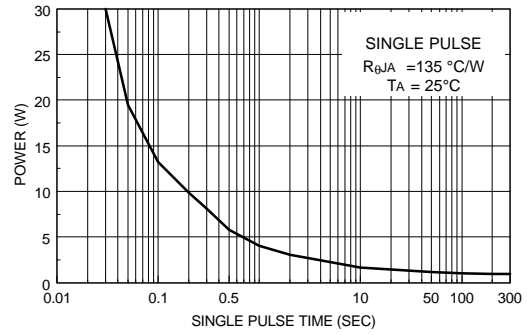


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Electrical Characteristics: P-Channel

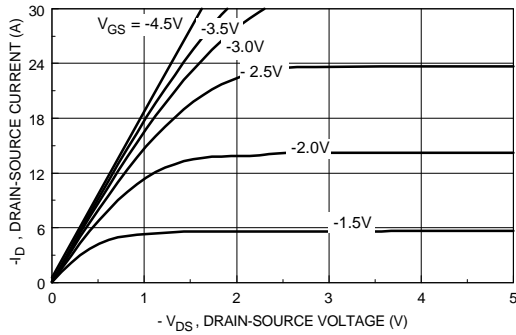


Figure 11. On-Region Characteristics.

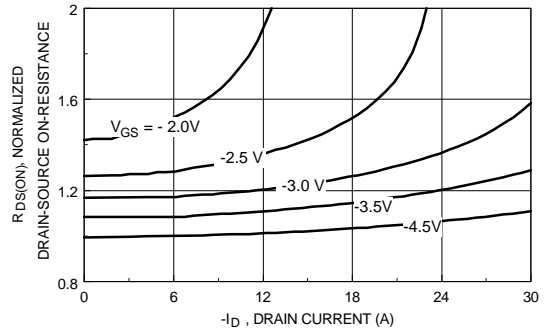


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

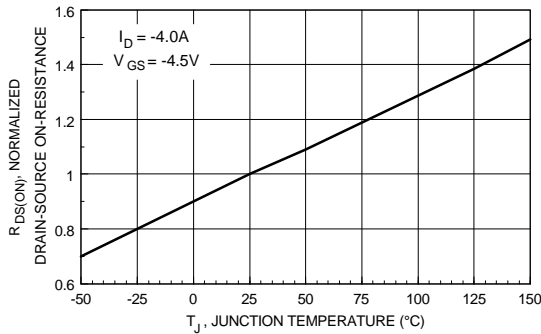


Figure 13. On-Resistance Variation with Temperature.

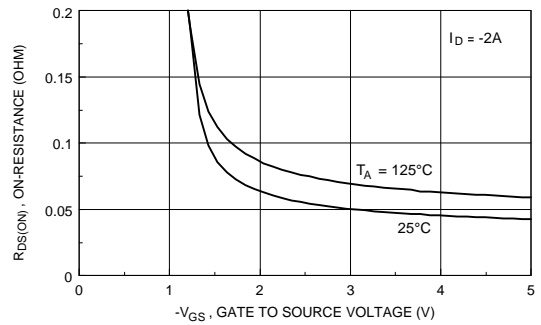


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

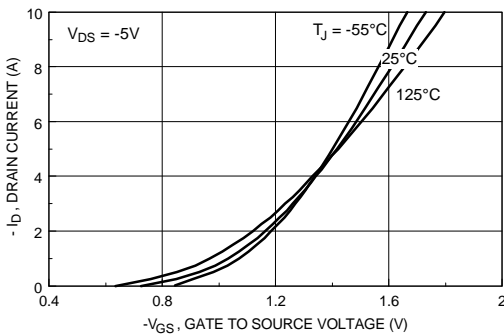


Figure 15. Transfer Characteristics.

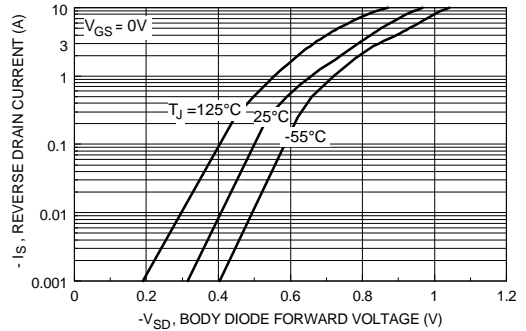


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics: P-Channel (continued)

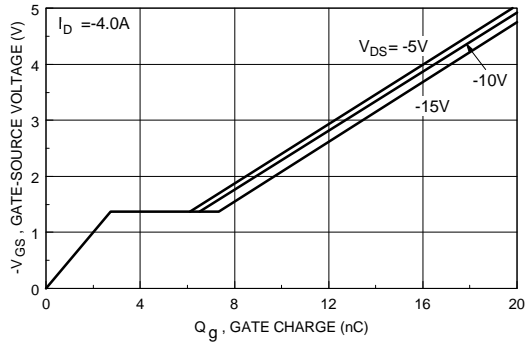


Figure 17. Gate Charge Characteristics.

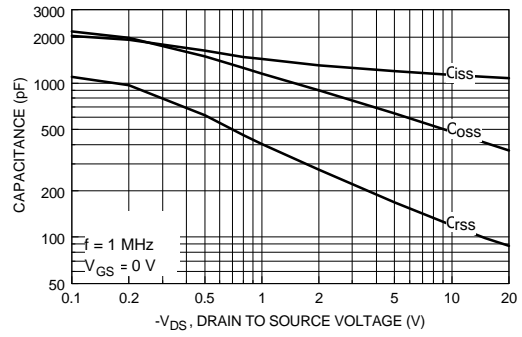


Figure 18. Capacitance Characteristics.

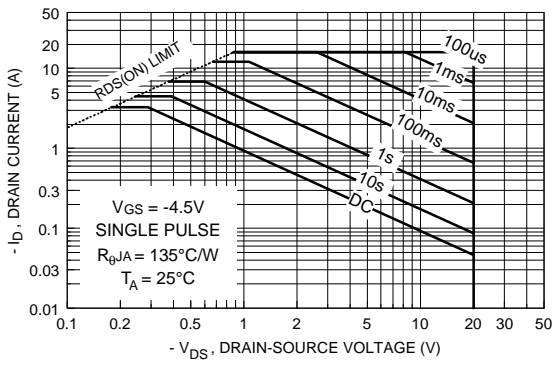


Figure 19. Maximum Safe Operating Area.

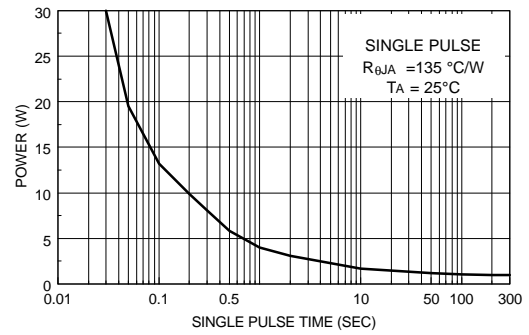


Figure 20. Single Pulse Maximum Power Dissipation.

Typical Thermal Characteristics: N & P-Channel (continued)

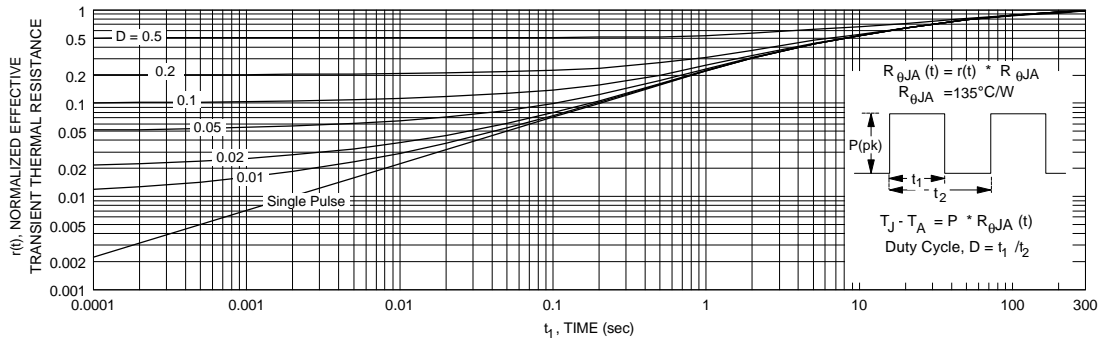


Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in note 1.
Transient thermal response will change depending on the circuit board design.

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