

CD4724BC 8-Bit Addressable Latch

General Description

The CD4724BC is an 8-bit addressable latch with three address inputs (A0–A2), an active low enable (\bar{E}), active high clear input (C_L), a data input (D) and eight outputs (Q0–Q7).

Data is entered into a particular bit in the latch when that is addressed by the address inputs and the enable (\bar{E}) is LOW. Data entry is inhibited when enable (\bar{E}) is HIGH.

When clear (C_L) and enable (\bar{E}) are HIGH, all outputs are LOW. When clear (C_L) is HIGH and enable (\bar{E}) is LOW, the channel demultiplexing occurs. The bit that is addressed has an active output which follows the data input while all unaddressed bits are held LOW. When operating in the addressable latch mode ($\bar{E} = C_L = \text{LOW}$), changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode ($\bar{E} = \text{HIGH}, C_L = \text{LOW}$).

Features

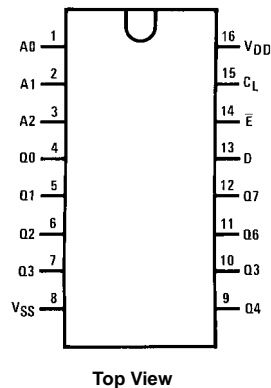
- Wide supply voltage range: 3.0V to 15V
- High noise immunity: $0.45 V_{DD}$ (typ.)
- Low power TTL compatibility: fan out of 2 driving 74L or 1 driving 74LS
- Serial to parallel capability
- Storage register capability
- Random (addressable) data entry
- Active high demultiplexing capability
- Common active high clear

Ordering Code:

Order Number	Package Number	Package Description
CD4724BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4724BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

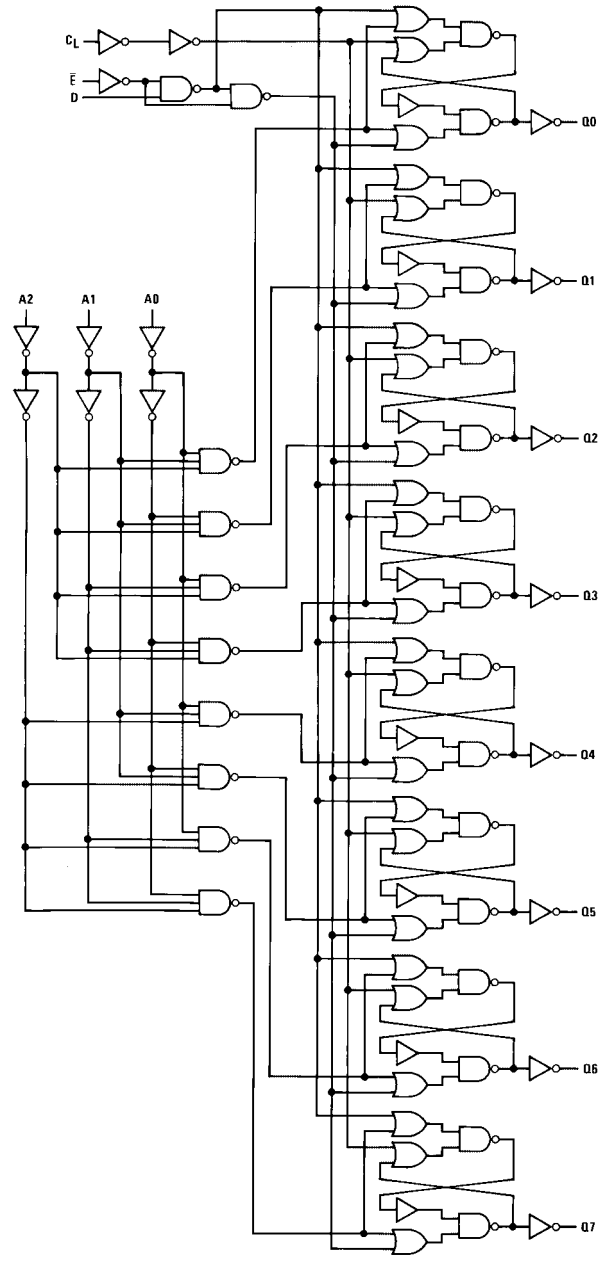
Connection Diagram



Truth Table

Mode Selection				
\bar{E}	C_L	Addressed Latch	Unaddressed Latch	Mode
L	L	Follows Data	Holds Previous Data	Addressable Latch
H	L	Hold Previous Data	Holds Previous Data	Memory
L	H	Follows Data	Reset to "0"	Demultiplexer
H	H	Reset to "0"	Reset to "0"	Clear

Logic Diagram



Absolute Maximum Ratings (Note 1)

(Note 2)

DC Supply Voltage (V_{DD})	-0.5V to +18 V_{DC}
Input Voltage (V_{IN})	-0.5V to $V_{DD} + 0.5 V_{DC}$
Storage Temperature (T_S)	-65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3.0V to 15 V_{DC}
Input Voltage (V_{IN})	0V to $V_{DD} V_{DC}$
Operating Temperature Range (T_A)	-55°C to +125°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	-55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		5 10 20		0.02 0.02 0.02	5 10 20		150 300 600	μA
V_{OL}	LOW Level Output Voltage	$ I_{O} \leq 1 \mu A$ $V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		0.05 0.05 0.05		0 0 0	0.05 0.05 0.05		0.05 0.05 0.05	V
V_{OH}	HIGH Level Output Voltage	$ I_{O} \leq 1 \mu A$ $V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$	4.95 9.95 14.95		4.95 9.95 14.95	5.0 10 15		4.95 9.95 14.95		V
V_{IL}	LOW Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V $V_{DD} = 10V, V_O = 1V$ or 9V $V_{DD} = 15V, V_O = 1.5V$ or 13.5V		1.5 3.0 4.0		2.25 4.5 6.75	1.5 3.0 4.0		1.5 3.0 4.0	V
V_{IH}	HIGH Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V $V_{DD} = 10V, V_O = 1V$ or 9V $V_{DD} = 15V, V_O = 1.5V$ or 13.5V	3.5 7.0 11.0		3.5 7.0 11.0	2.75 5.5 8.25		3.5 7.0 11.0		V
I_{OL}	LOW Level Output Current <small>(Note 3)</small>	$V_{DD} = 5V, V_O = 0.4V$ $V_{DD} = 10V, V_O = 0.5V$ $V_{DD} = 15V, V_O = 1.5V$	0.64 1.6 4.2		0.51 1.3 3.4	0.88 2.25 8.8		0.36 0.9 2.4		mA
I_{OH}	HIGH Level Output Current <small>(Note 3)</small>	$V_{DD} = 5V, V_O = 4.6V$ $V_{DD} = 10V, V_O = 9.5V$ $V_{DD} = 15V, V_O = 13.5V$	-0.64 -1.6 -4.2		-0.51 -1.3 -3.4	-0.88 -2.25 -8.8		-0.36 -0.9 -2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$ $V_{DD} = 15V, V_{IN} = 15V$		-0.1 0.1		-10^{-5} 10^{-5}	-0.1 0.1		-1.0 1.0	μA

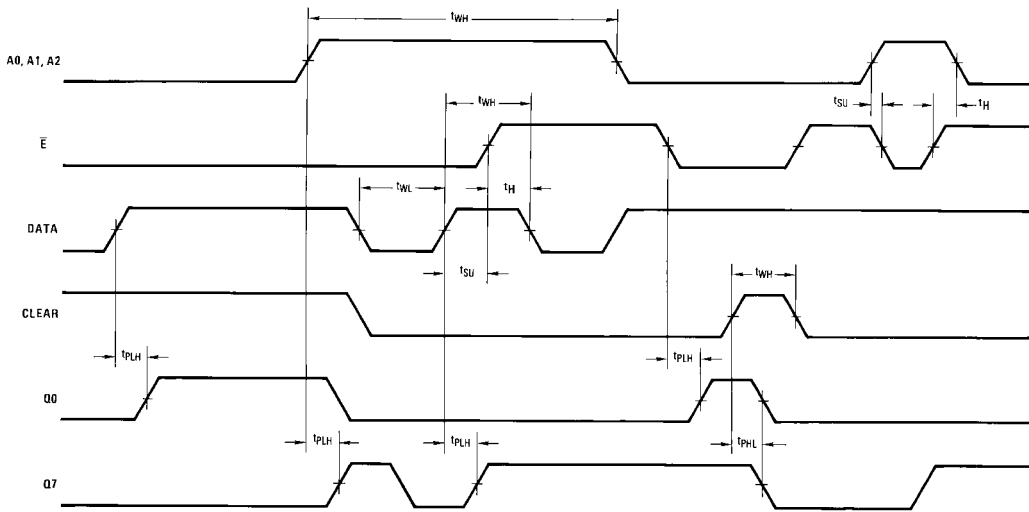
Note 3: I_{OL} and I_{OH} are tested one output at a time.

AC Electrical Characteristics (Note 4)						
T _A = 25°C, C _L = 50 pF, R _L = 200k, Input t _r = t _f = 20 ns, unless otherwise noted						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t _{PHL} , t _{PLH}	Propagation Delay Data to Output	V _{DD} = 5V		200	400	ns
		V _{DD} = 10V		75	150	
		V _{DD} = 15V		50	100	
t _{PLH} , t _{PHL}	Propagation Delay Enable to Output	V _{DD} = 5V		200	400	ns
		V _{DD} = 10V		80	160	
		V _{DD} = 15V		60	120	
t _{PHL}	Propagation Delay Clear to Output	V _{DD} = 5V		175	350	ns
		V _{DD} = 10V		80	160	
		V _{DD} = 15V		65	130	
t _{PLH} , t _{PHL}	Propagation Delay Address to Output	V _{DD} = 5V		225	450	ns
		V _{DD} = 10V		100	200	
		V _{DD} = 15V		75	150	
t _{THL} , t _{TLH}	Transition Time (Any Output)	V _{DD} = 5V		100	200	ns
		V _{DD} = 10V		50	100	
		V _{DD} = 15V		40	80	
T _{WH} , T _{WL}	Minimum Data Pulse Width	V _{DD} = 5V		100	200	ns
		V _{DD} = 10V		50	100	
		V _{DD} = 15V		40	80	
t _{WH} , t _{WL}	Minimum Address Pulse Width	V _{DD} = 5V		200	400	ns
		V _{DD} = 10V		100	200	
		V _{DD} = 15V		65	125	
t _{WH}	Minimum Clear Pulse Width	V _{DD} = 5V		75	150	ns
		V _{DD} = 10V		40	75	
		V _{DD} = 15V		25	50	
t _{SU}	Minimum Setup Time Data to E	V _{DD} = 5V		40	80	ns
		V _{DD} = 10V		20	40	
		V _{DD} = 15V		15	30	
t _H	Minimum Hold Time Data to E	V _{DD} = 5V		60	120	ns
		V _{DD} = 10V		30	60	
		V _{DD} = 15V		25	50	
t _{SU}	Minimum Setup Time Address to E	V _{DD} = 5V		-15	50	ns
		V _{DD} = 10V		0	30	
		V _{DD} = 15V		0	20	
t _H	Minimum Hold Time Address to E	V _{DD} = 5V		-50	15	ns
		V _{DD} = 10V		-20	10	
		V _{DD} = 15V		-15	5	
C _{PD}	Power Dissipation Capacitance	Per Package (Note 5)		100		pF
C _{IN}	Input Capacitance	Any Input		5.0	7.5	pF

Note 4: AC Parameters are guaranteed by DC correlated testing.

Note 5: Dynamic power dissipation (P_D) is given by: P_D = (C_{PD} + C_L) V_{CC}²f + P_Q; where C_L = load capacitance; f = frequency of operation; for further details, see Application Note AN-90, "Family Characteristics".

Switching Time Waveforms

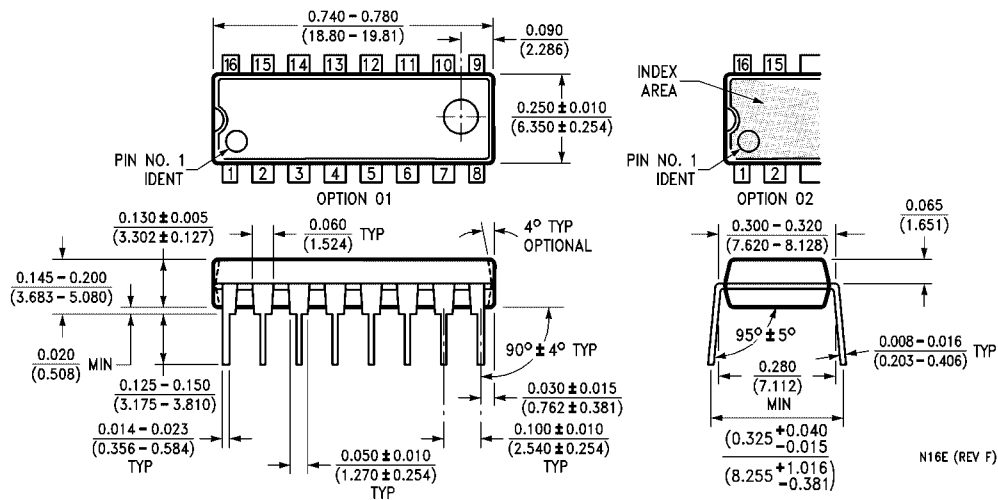


Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E**

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