



Integrated Mixed-Signal Solutions

STIr4200

USB/IrDA Bridge Controller

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OFFICIAL PRODUCT DOCUMENTATION

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STIr4200
USB/IrDA Bridge Controller



1. TABLE OF CONTENTS

1. TABLE OF CONTENTS 2

 1.1. List of Figures 3

 1.2. List of Tables 3

2. PRODUCT OVERVIEW 4

 2.1. Features 4

 2.2. Description 4

 2.3. Ordering Information 4

 2.4. STIr4200 Block Diagram 5

3. CHARACTERISTICS AND SPECIFICATIONS 5

 3.1. Absolute Maximum Ratings 5

 3.2. Recommended Operating Conditions 5

 3.3. Electrical Characteristics 6

4. FUNCTIONAL DESCRIPTION 6

 4.1. Overview 6

 4.2. USB Interface 7

 4.3. Vendor-Specific Device Requests 7

 4.3.1. Write Multiple Registers 7

 4.3.2. Write One Register 7

 4.3.3. Read Multiple Registers 8

 4.3.4. Read ROM 8

 4.3.5. Vendor Clear Stall 8

 4.4. Digital IR Transceiver 9

 4.5. FIFO Contents 9

5. IR FRAMING FORMATS 10

 5.1. Transmit Frame Format 10

 5.1.1. SIR Transmit Frame 10

 5.1.2. FIR Transmit Frame 11

 5.1.3. Receive Frame Format 12

 5.1.3.1. SIR Receive Frame 12

 5.1.3.2. FIR Receive Frame 13

6. DIGITAL IR TRANSCEIVER REGISTERS 14

 6.1. Detailed STIr4200 Register Descriptions 14

 6.1.1. FIFO Data Register 14

 6.1.2. Mode and Baud Rate Registers 15

 6.1.2.1. Mode Register 15

 6.1.2.2. Baud Rate Register 15

 6.1.3. Control Register 16

 6.1.4. Sensitivity Register 17

 6.1.5. Status Register 17

 6.1.6. FIFO Count Registers (LSB,MSB) 18

 6.1.6.1. FIFO Count LSB 18

 6.1.6.2. FIFO Count MSB 18

 6.1.7. DPLL Tune Register 18

 6.1.8. IRDIG Setup Register 19

 6.1.9. Test Register 19

7. PIN DESCRIPTION 20

 7.1. STIr4200S 28-Pin SSOP Pin Description 20

8. PACKAGE DRAWINGS 21



1.1. List of Figures

| | |
|--|----|
| Figure 1. STIr4200 Block Diagram | 5 |
| Figure 2. Typical USB-IR Application | 6 |
| Figure 3. Block Diagram of Digital IR Transceiver | 9 |
| Figure 4. SIR Transmit Frame Format | 10 |
| Figure 5. FIR Transmit Frame Format | 11 |
| Figure 6. SIR Receive Frame Format | 12 |
| Figure 7. FIR Receive Frame Format | 13 |
| Figure 8. STIr4200S 28-Pin SSOP Pin Assignment Drawing | 20 |
| Figure 9. 28-Pin SSOP Package Drawing | 21 |

1.2. List of Tables

| | |
|--|----|
| Table 1. Absolute Maximum Ratings | 5 |
| Table 2. Recommended Operating Conditions | 5 |
| Table 3. Electrical Characteristics | 6 |
| Table 4. Write Multiple Registers | 7 |
| Table 5. Write One Register | 7 |
| Table 6. Read Multiple Registers | 8 |
| Table 7. Read ROM | 8 |
| Table 8. Vendor Clear Stall | 8 |
| Table 9. IrLAP Frame | 9 |
| Table 10. Ir Transceiver Registers | 14 |
| Table 11. FIFO Data Register | 14 |
| Table 12. Mode Register | 15 |
| Table 13. Baud Rate Register | 15 |
| Table 14. Mode and Baud Rate Values for Required IrDA Modes of Operation | 15 |
| Table 15. Control Register | 16 |
| Table 16. Sensitivity Register | 17 |
| Table 17. Status Register | 17 |
| Table 18. FIFO Count LSB | 18 |
| Table 19. FIFO Count MSB | 18 |
| Table 20. DPLL Tune Register | 18 |
| Table 21. IRDIG Setup Register | 19 |
| Table 22. Test Register | 19 |
| Table 23. Pin Descriptions for STIr4200S 28-Pin SSOP Package | 20 |

STIr4200
USB/IrDA Bridge Controller



2. PRODUCT OVERVIEW

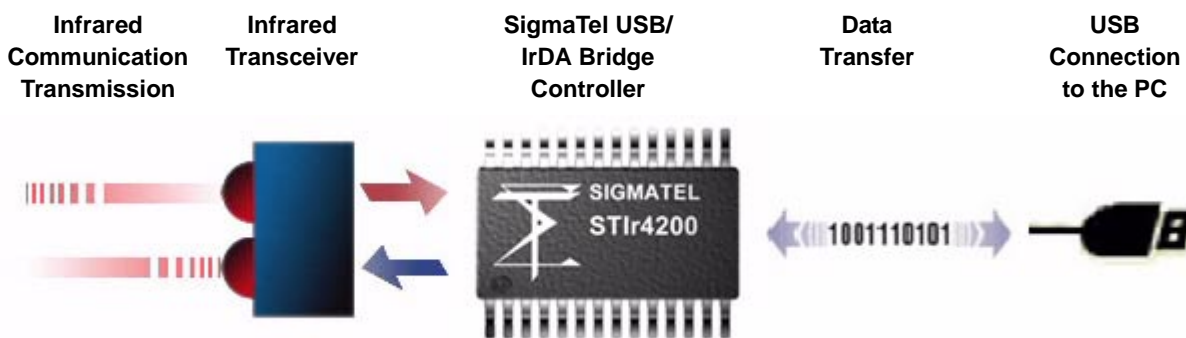
2.1. Features

- Low-power CMOS design
- IrDA data rates from 2.4 Kbps to 4 Mbps
- Obtains power from USB port
- Uses standard IrDA transceivers
- Optional LED driver for additional flexibility
 - LED driver capable of > 650 ma @ 5V, 25% duty cycle
- Full compliance to IrDA 1.3 and USB 1.1 specifications
- 4 Kbyte FIFO buffer memory
- Requires a single 12 Mhz crystal
- Windows 98/98SE/ME/2000/XP™ NDIS/USB driver
- Low-profile 28-Pin SSOP package

2.2. Description

The SigmaTel STIr4200 is a low cost, low power, USB/IrDA Bridge Controller integrated circuit for enabling IrDA wireless data communications through a standard PC USB port. The STIr4200 directly interfaces to both single path and dual path receive IrDA transceiver module architectures and contains a USB controller, IrDA controller, interface logic, and memory buffer for full IrDA 1.3, 4 Mbps data transfer rates. A block diagram is shown in Figure 1.

The STIr4200 is bundled with a Windows 98/98SE/ME/2000/XP™ NDIS/USB driver for enabling the implementation of a cost effective USB/IrDA Adapter solution for wireless data communications.



2.3. Ordering Information

| Part Number | Package | Temp Range | Supply Range |
|-------------|-------------|----------------|------------------|
| STIr4200S | 28-Pin SSOP | 0° C to +70° C | Vdd = 3.1 - 3.6V |



2.4. STIr4200 Block Diagram

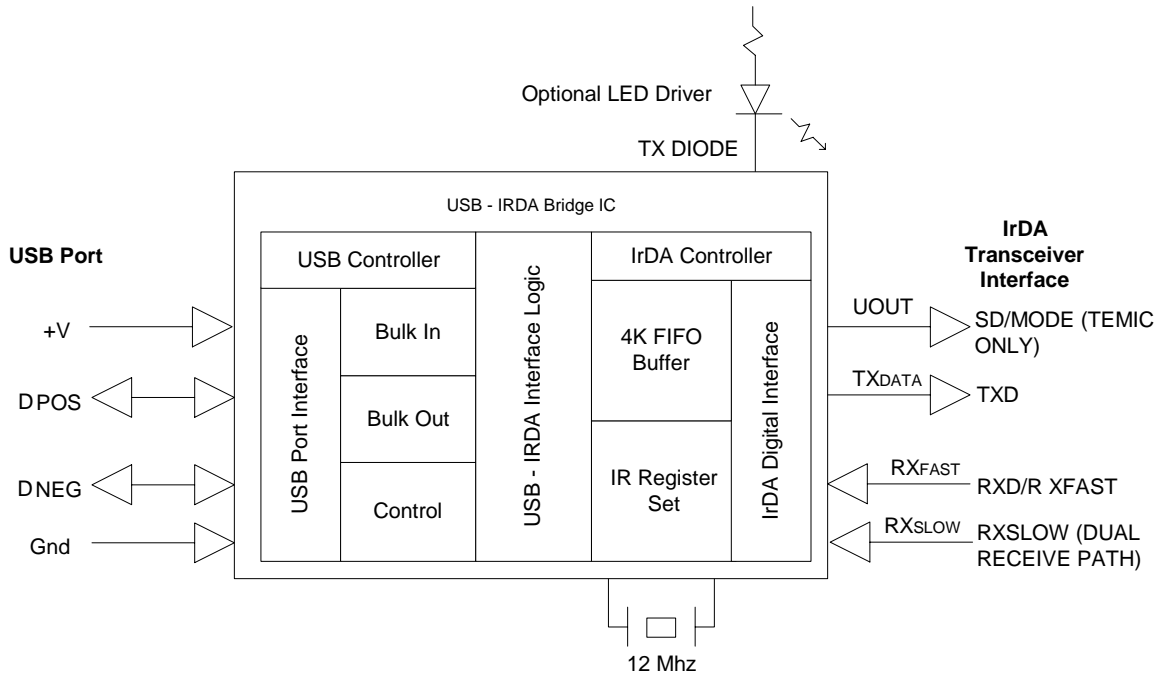


Figure 1. STIr4200 Block Diagram

3. CHARACTERISTICS AND SPECIFICATIONS

3.1. Absolute Maximum Ratings

| Symbol | Parameter | MIN | MAX | UNITS | CONDITIONS |
|------------------|--|--------|------------------------|-------|-----------------|
| PD | Power Dissipation (Package constraint) | | | mW | |
| T _A | Operating Temperature | 0 | 70 | °C | |
| T _J | Lead Solder Temperature | | 260 | °C | for 10 sec max. |
| T _S | Storage Temperature | -55 | 125 | °C | |
| V _{CC} | Supply Voltage | -0.3 V | 6 | V | |
| V _{max} | Voltage at any pin | | V _{DD} + 0.4V | V | |
| ESD | Electrostatic Discharge (ESD) | | +/- 2KV | V | See Note 1 |

Note: 1. The device meets the JESD22-A114-A Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) requirements of +/- 2KV on all pins, except the TXDIODE pin (Pin 2), where the limit is +/-1.5KV.

Table 1. Absolute Maximum Ratings

3.2. Recommended Operating Conditions

| Symbol | Parameter | MIN | TYP | MAX | UNITS | CONDITION |
|-----------------|-----------------------------|-----|-----|-----|-------|-----------|
| V _{DD} | Supply Voltage | 3.1 | 3.3 | 3.6 | V | |
| T _A | Operating Temperature Range | 0 | 25 | 70 | °C | |

Table 2. Recommended Operating Conditions

STIr4200
USB/IrDA Bridge Controller



3.3. Electrical Characteristics

$T_A = 25^{\circ}C_A$ $V_{DD} = 3.3V$ unless otherwise specified. Cap Load = 50pF

| Symbol | Parameter | MIN | TYP | MAX | UNITS | CONDITION |
|------------|--------------------------|---------------------|-----|---------------------|---------|-----------|
| I_{CC} | Active Supply Current | | 12 | 19 | mA | |
| I_{CC} | Suspend Supply Current | | 14 | 50 | μA | |
| V_{RXDH} | Receive Data Logic High | $V_{DD} \times 0.8$ | | | V | |
| V_{RXDL} | Receive Data Logic Low | | | 0.8 | V | |
| V_{TXDH} | Transmit Data Logic High | $V_{DD} \times 0.6$ | | | V | |
| V_{TXDL} | Transmit Data Logic Low | | | $V_{DD} \times 0.4$ | V | |

Table 3. Electrical Characteristics

4. FUNCTIONAL DESCRIPTION

4.1. Overview

The STIr4200 consists of two major functional blocks, the USB controller and the digital IR transceiver. The USB controller provides a Control, Bulk-In, and Bulk- Out endpoints to the USB host. The digital IR transceiver consists of a transmit and receive interface that connects to an analog IR front end. Figure 1 shows a block diagram of the device.

This USB/IrDA Bridge Controller has full interface capability to connect between a USB bus , and an IrDA-compatible infrared transceiver device. A simplified schematic of this arrangement is shown in Figure 2.

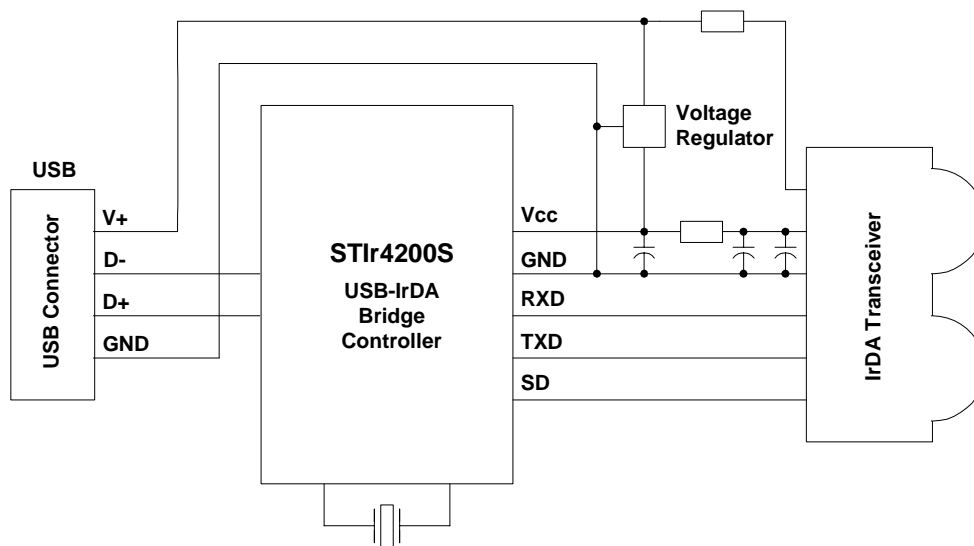


Figure 2. Typical USB-IR Application



4.2. USB Interface

The USB interface to the host controller includes a Control endpoint, a Bulk-In endpoint, and a Bulk-Out endpoint. The USB controller supports the USB 1.1 specification. Hence, it supports all standard functionality associated with device enumeration, standard USB device requests, etc. In addition, there is a set of vendor specific commands provided to allow a USB driver to access registers in the Digital IR Transceiver and ROM in the USB controller.

Note: The STIr4200 device conforms to all of the USB 1.1 specifications with one exception of the "get_interface" command. This command is used only during USB conformance testing, and during that testing, improper operation will be noted on test results. However, the software drivers provided by SigmaTel, Inc. do NOT use that command at all, and this does NOT cause any problem of any kind in operation. A waiver for this command has been obtained from USBIF by SigmaTel, Inc. This command is not used by the software, and therefore has no effect on device and system operation. The only time this "get_interface" command is even accessed is during USB conformance testing.

4.3. Vendor-Specific Device Requests

4.3.1. Write Multiple Registers

The write multiple registers vendor specific command allows the user to write multiple sequential registers to the Digital IR Transceiver. Each register is one byte wide, so the command indicates first register to write, the number of registers to write, and the data phase supplies the data for those registers.

| Offset | Field | Size | Value (hex) | Description |
|--------|---------------|------|-------------------|---|
| 0 | bmRequestType | 1 | 0x40 | Host to device, vendor type, device recipient |
| 1 | Brequest | 1 | 0x00 | Write multiple registers |
| 2 | Wvalue | 2 | Not used (0x0000) | |
| 4 | Windex | 2 | 0x0001–0x000f | First register to write |
| 6 | Wlength | 2 | 0x0001–0x000f | Number of registers to write |

Data phase 1-15 bytes of Register Data

Table 4. Write Multiple Registers

4.3.2. Write One Register

The write one register vendor specific command allows the user to write a single register to the Digital IR Transceiver.

| Offset | Field | Size | Value (hex) | Description |
|--------|---------------|------|-------------------|---|
| 0 | bmRequestType | 1 | 0x40 | Host to device, vendor type, device recipient |
| 1 | Brequest | 1 | 0x03 | Write one register |
| 2 | Wvalue | 2 | LSB contains data | The data to write the register |
| 4 | Windex | 2 | 0x0001 – 0x000f | Register to write |
| 6 | Wlength | 2 | Not used (0x0000) | |

Table 5. Write One Register

STIr4200

USB/IrDA Bridge Controller



4.3.3. Read Multiple Registers

The read multiple registers vendor specific command allows the user to read multiple sequential registers from the Digital IR Transceiver. Each register is one byte wide, so the command indicates the first register to read, the number of registers to read, and the responding data phase supplies the data from those registers. This command is also used for the case of reading only one register.

| Offset | Field | Size | Value (hex) | Description |
|--------|---------------|------|-------------------|---|
| 0 | bmRequestType | 1 | 0xc0 | Device to host, vendor type, device recipient |
| 1 | BRequest | 1 | 0x01 | Read multiple registers |
| 2 | Wvalue | 2 | Not used (0x0000) | |
| 4 | Windex | 2 | 0x0001 – 0x000f | First register to read |
| 6 | Wlength | 2 | 0x0001 – 0x000f | Number of registers to read |

Table 6. Read Multiple Registers

4.3.4. Read ROM

The read ROM vendor specific command allows the user to read the contents of the USB controller endpoint zero ROM. This is primarily a debug feature that allows verification of the endpoint zero ROM contents. Only 64 bytes of ROM data can be requested at a time. The responding data phase supplies the data from the endpoint zero ROM.

| Offset | Field | Size | Value (hex) | Description |
|--------|---------------|------|-------------------|--|
| 0 | BmRequestType | 1 | 0xc0 | Device to host, vendor type, device recipient |
| 1 | Brequest | 1 | 0x02 | Read ROM |
| 2 | Wvalue | 2 | Not used (0x0000) | |
| 4 | Windex | 2 | 0x0000–0x00ff | Base ROM address |
| 6 | Wlength | 2 | 0x01–0x0040 | Number of ROM locations to read (64 bytes max per request) |

Table 7. Read ROM

4.3.5. Vendor Clear Stall

The vendor clear stall command is included as a potential work around for limitations in early versions of the Microsoft™ USB driver stack. Although not a concern with the latest operating systems, the earlier versions could have the possibility that the USB driver stack would not properly clear endpoint stalls. The standard device clear stall request is also supported.

| Offset | Field | Size | Value (hex) | Description |
|--------|---------------|------|-------------------|---|
| 0 | BmRequestType | 1 | 0x42 | Device to host, vendor type, endpoint recipient |
| 1 | Brequest | 1 | 0x01 | Clear endpoint stall |
| 2 | Wvalue | 2 | Not used (0x0000) | |
| 4 | Windex | 2 | 0x0000 – 0x0002 | Endpoint on which to clear stall |
| 6 | Wlength | 2 | Not used (0x0000) | |

Table 8. Vendor Clear Stall



4.4. Digital IR Transceiver

The Digital IR Transceiver is responsible for driving the transmit diode and receiving the digital input from an analog IR front end. The primary components are the transmit modulator, the receive demodulator, the FIFO, the analog transmit section, and the register array. Figure 3 shows a block diagram of the Digital IR Transceiver. By programming the registers in the register array, the device's operation is determined. Various registers are used to specify operations such as the modulation scheme, the baud rate, the current frame size in the FIFO, the RX input selection, etc. The FIFO is 4K bytes in size.

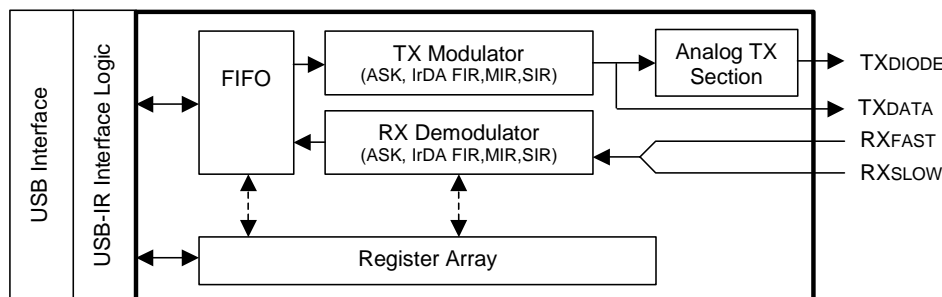


Figure 3. Block Diagram of Digital IR Transceiver

In steady state transmit operation, the USB controller is filling the FIFO with data while the Digital IR Transceiver is emptying it via the transmit modulator. In steady state receive operation, the USB controller is emptying the FIFO while the RX demodulator is filling the FIFO.

4.5. FIFO Contents

Data sent to the USB controller for transmission by the TX modulator must be organized into frames. An IrLAP frame is made up of the following portions:

| | | | | | |
|------------|------------------------------|----------|----------|------------|------------|
| BOF | A | C | I | FCS | EOF |
| BOF | Beginning of frame(s) | | | | |
| A | Address field | | | | |
| C | Control field | | | | |
| I | Information field | | | | |
| FCS | Frame check sequence (CRC) | | | | |
| EOF | End of frame | | | | |

Table 9. IrLAP Frame

The NDIS IR stack only provides the A, C, and I fields to the NDIS mini-port device driver that communicates with the USB/IrDA transceiver. Hence, the mini-port must fill in the BOF, FCS, and EOF fields. Additionally, the driver must add a 2-byte header ID code and a 2-byte frame size to the packet before passing the packet onto the USB stack for delivery to the USB/IrDA transceiver. There are additional special characters and required escape sequences depending upon the rate of transfer. Details on the frame format for each of the support rates is discussed in the following sections.



5. IR FRAMING FORMATS

5.1. Transmit Frame Format

5.1.1. SIR Transmit Frame

The SIR rates include 2.4, 9.6, 19.2, 38.4, 57.6, and 115.2 Kbps. For SIR, the frame presented to the USB bulk transmit interface must be organized in the following fashion as shown in Figure 4.

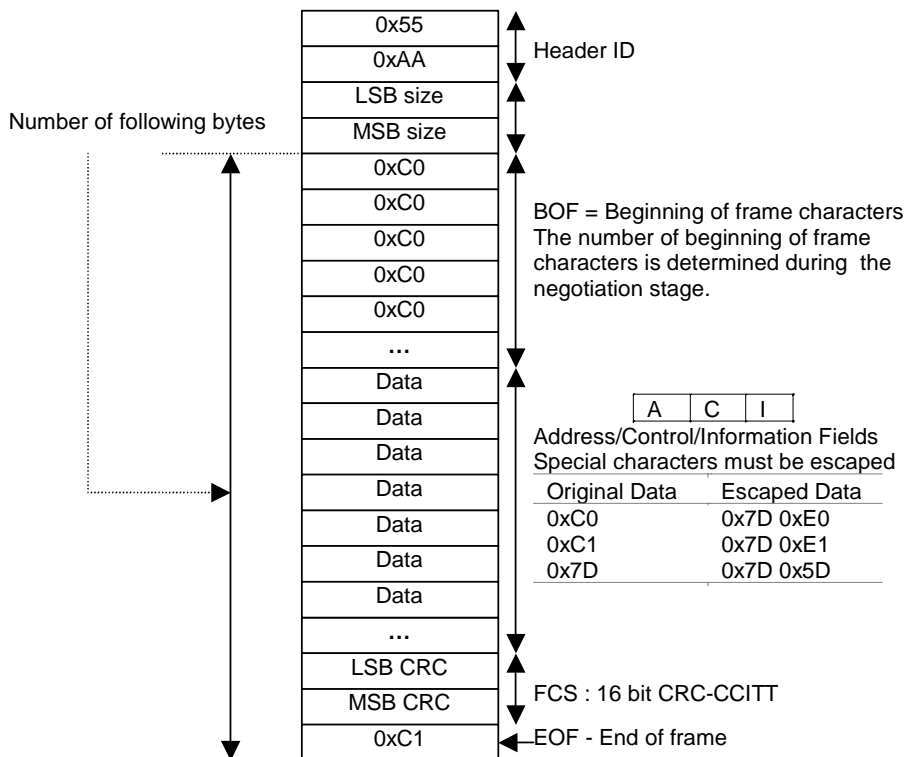
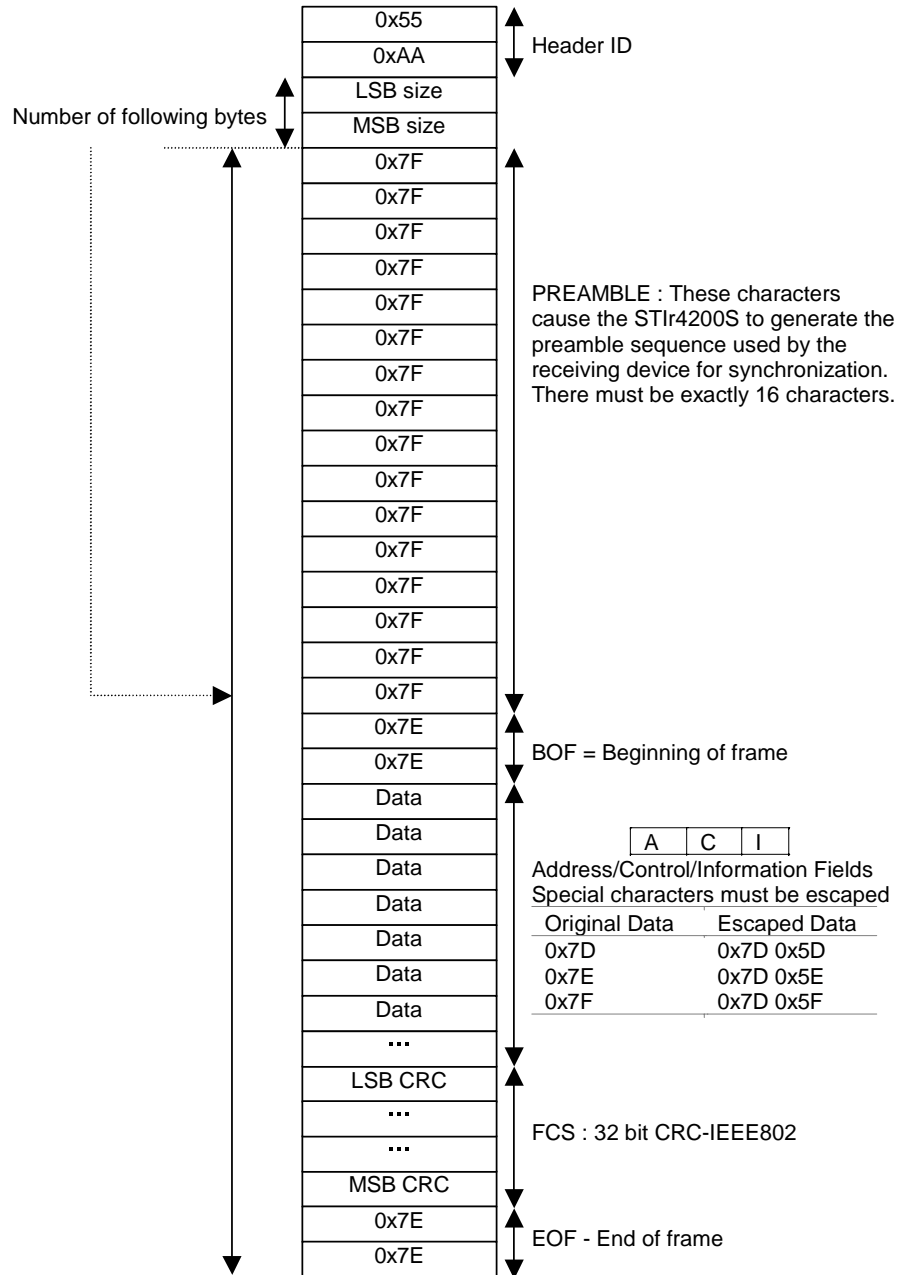


Figure 4. SIR Transmit Frame Format



5.1.2. FIR Transmit Frame

The FIR rate is 4 Mbps The frame organization is detailed in Figure 5.



STIr4200
USB/IrDA Bridge Controller



5.1.3. Receive Frame Format

Data received into the STIr4200 FIFO from the digital infrared interface can be accessed by performing a bulk read on the USB interface. The received data contains the encoded infrared data. The STIr4200 does not perform any frame validation or CRC-Checking. Multiple frames may exist within one bulk read depending upon the size of the bulk read. However, the end of the bulk read buffer may not necessarily coincide with the end of an infrared frame. It is highly likely that the data at the end of a bulk read will be a partial frame. The remaining frame data will be acquired in the next bulk read.

The bulk data thus contains start-of-frame (BOF) characters, end-of-frame (EOF) characters, and escape characters that delineate the actual frame. It is the responsibility of the host software to reconstruct the frame.

5.1.3.1. SIR Receive Frame

The standard SIR encoding scheme provides all information needed to delineate the encoded receive frames. Figure 6 summarizes the SIR receive frame format encoding scheme.

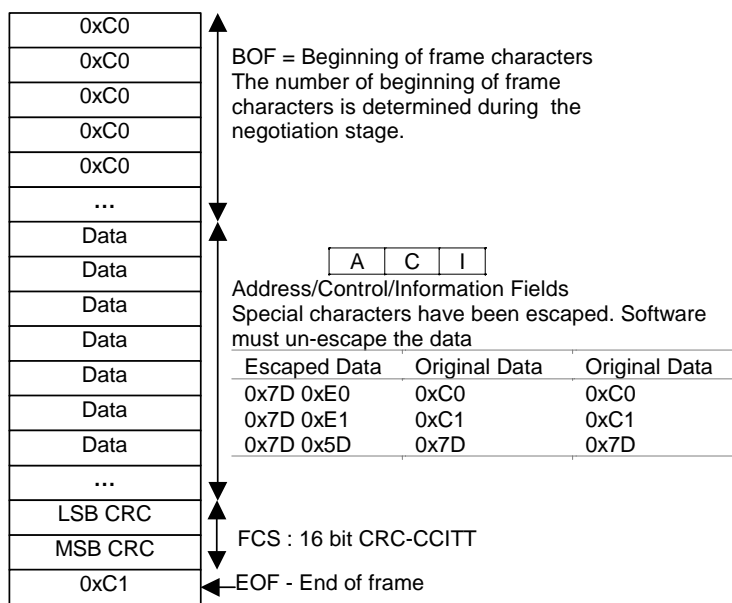


Figure 6. SIR Receive Frame Format



5.1.3.2. *FIR Receive Frame*

The FIR encoding scheme is modified slightly from the standard scheme. The character 0x7E is used to delineate the BOF and EOF. The STIr4200 escapes three characters in the data field on receive, 0x7F, 0x7E and 0x7D, which allows the 0x7E characters used as BOF and EOF to be unique. The 0x7E character can then be used to delineate the infrared frame boundaries. This hardware escaping in the data portion is specific to the STIr4200, and the software must un-escape the data portion of the received frame to restore the original data. Figure 7 summarizes the FIR receive frame format encoding scheme.

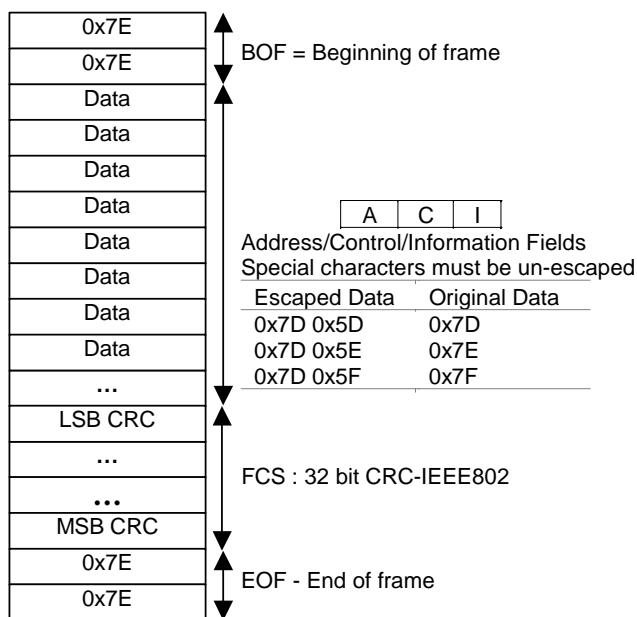


Figure 7. FIR Receive Frame Format

STIr4200
USB/IrDA Bridge Controller



6. DIGITAL IR TRANSCEIVER REGISTERS

| Offset | Description | Access | Bit Position | | | | | | | | |
|--------|------------------------------------|--------|--------------|----------------|---------------|---------------|----------------|---------------|----------------|----------------|--|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0 | FIFO Data | R/W | Reserved | | | | | | | | |
| 1 | Mode Register | R/W | FIR | Reserved | SIR | ASK | FASTRXEN | FFRSTEN | FFSPRST | PDCLK(8) | |
| 2 | Baud Rate Register | R/W | PDCLK(7: 0) | | | | | | | | |
| 3 | Control Register | R/W | SDMODE | RXSLOW | DLOOP1 | TXPWD | RXPWD | TXPWR(1: 0) | | SRESET | |
| 4 | Sensitivity Register | | RXDSNS(2: 0) | | | BSTUFF R/W | SPWIDTH R/W | ID(2) RO | ID(1) RO | ID(0) RO | |
| 5 | Status Register | | EFRAME RO | FFUNDER ROC | FFOVER ROC | FFDIR RO | FFCLR WO | FFEMPTY RO | FFRXERR ROC | FFTXERR ROC | |
| 6 | FIFO Count (Note 1) Register (LSB) | RO | FFCNT(7:0) | | | | | | | | |
| 7 | FIFO Count (Note 1) Register (MSB) | RO | 0 | 0 | 0 | FFCNT(12: 8) | | | | | |
| 8 | DPLL Tune Register | RO | DPCNT(5: 0) | | | | | | LONGP(1: 0) | | |
| 9 | IRDIG Setup Register | R/W | RXHIGH | TXLOW | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | |
| 10 | Reserved | R/W | Reserved | | | | | | | | |
| 11 | Reserved | R/W | Reserved | | | | | | | | |
| 12 | Reserved | R/W | Reserved | | | | | | | | |
| 13 | Reserved | R/W | Reserved | | | | | | | | |
| 14 | Reserved | R/W | Reserved | | | | | | | | |
| 15 | Test Register | R/W | PLLDWN | LOOPIR | LOOPUSB | TSTENA | TSTOSC(3: 0) | | | | |

R/W : Read/Write

RO : Read only

ROC : Read only, clear on read

WO : Write only

Note: 1. Due to double buffering, FFCNT could be off by as much as 3 bytes

Table 10. Ir Transceiver Registers

6.1. Detailed STIr4200 Register Descriptions

6.1.1. FIFO Data Register

Offset 0

| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|--------------|----------|---|--|---|---|---|---|---|
| FIFO Data | | Reserved | | | | | | | |
| Default State | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit Number | Bit Mnemonic | Access | | Function | | | | | |
| 7 – 0 | Reserved | R/W | | The FIFO data register is used internally by the USB interface to access the FIFO data in the digital infrared block. Although this register is accessible through the USB interface, it should never be accessed during normal operation. | | | | | |

Table 11. FIFO Data Register



6.1.2. Mode and Baud Rate Registers

Offset 1 and 2

6.1.2.1. Mode Register

Offset 1

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|----------|-----|-----|----------|---------|---------|----------|
| Mode Register | FIR | Reserved | SIR | ASK | FASTRXEN | FFRSTEN | FFSPRST | PDCLK(8) |
| Default State | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Access | Function |
|------------|--------------|--------|---|
| 7 | FIR | R/W | When set, puts the infrared modulators into fast infrared mode (4PPM). Must be mutually exclusive with the SIR bit. |
| 6 | Reserved | RO | Reserved. Write as zero. |
| 5 | SIR | R/W | When set, puts the infrared modulators into slow infrared mode. Must be mutually exclusive with the FIR bit. |
| 4 | ASK | R/W | When set, puts the infrared modulators into amplitude shift keying infrared mode. |
| 3 | FASTRXEN | R/W | Enables simultaneous reads and writes to/from the FIFO. |
| 2 | FFRSTEN | R/W | Allows the FIFO receive shift register to be automatically reset in FIR mode. |
| 1 | FFSPRST | R/W | Manually resets the FIFO shift register. Must be set to '1' to release the FIFO shift register from reset. |
| 0 | PDCLK(8) | R/W | MSB of baud rate register. |

Table 12. Mode Register

6.1.2.2. Baud Rate Register

Offset 2

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-------------|---|---|---|---|---|---|---|
| Baud Rate Register | PDCLK(7: 0) | | | | | | | |
| Default State | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |

| Bit Number | Bit Mnemonic | Access | Function |
|------------|---------------|--------|--|
| 7:0 | PDCLK (7 : 0) | R/W | Sets the divide ratio of the PLL for the infrared modulator/demodulator. |

Table 13. Baud Rate Register

Below is a table of values to be written to the mode and baud rate registers to set the required IrDA modes of operation:

| Operational Mode | Speed | Mode Register | Baud Rate Register |
|------------------|------------|---------------|--------------------|
| FIR | 4.0 Mbps | 0x80 | 0x02 |
| SIR | 115.2 Kbps | 0x20 | 0x09 |
| | 57.6 Kbps | 0x20 | 0x13 |
| | 38.4 Kbps | 0x20 | 0x1D |
| | 19.2 Kbps | 0x20 | 0x3B |
| | 9.6 Kbps | 0x20 | 0x77 |
| | 2.4 Kbps | 0x21 | 0xDF |

Table 14. Mode and Baud Rate Values for Required IrDA Modes of Operation

STIr4200
USB/IrDA Bridge Controller



6.1.3. Control Register

Offset 3

| | | | | | | | | |
|------------------|--------|--------|----------|-------|-------|-------------|---|--------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Control Register | SDMODE | RXSLOW | Reserved | TXPWD | RXPWD | TXPWR(1: 0) | | SRESET |
| Default State | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Access | Function |
|------------|--------------|--------|---|
| 7 | SD/MODE | R/W | Use this bit only when the STIr4200 is connected to a TEMIC style infrared transceiver. This bit is used to put the infrared transceiver into the power down state or toggle the transceiver between high and low speed. POWER DOWN STATE: Set the SD/MODE bit to enter the power down state. Clear the SD/MODE bit to exit the power down state. SET TEMIC HIGH SPEED: Set the FIR bit (bit 7) in the Mode Register, then set SD/MODE bit, then clear SD/MODE bit. SET TEMIC LOW SPEED: Clear the FIR bit (bit 7) in the Mode Register, then set the SD/MODE bit, then clear the SD/MODE bit. The sequences described above for setting the high or low speed mode enables a state machine in the STIr4200 to automatically toggle the TXDATA and UOUT (SD/MODE) pins on the STIr4200. |
| 6 | RXSLOW | R/W | When set, selects RXSLOW as the receive input. When cleared, selects RXFAST as the receive input. |
| 5 | Reserved | R | Reserved |
| 4 | TXPWD | R/W | When set, powers down the infrared transmitter (modulator). |
| 3 | RXPWD | R/W | When set, powers down the infrared receiver (demodulator). |
| 2-1 | TXPWR(1: 0) | R/W | Sets the internal pull down resistance to control the current presented to the transmit diode. 00 : HIGH (max current) 01 : MED HIGH 10 : MED LOW 11 : LOW (min current) |
| 0 | SRESET | R/W | When set, performs soft reset of the infrared modulator/demodulator. |

Table 15. Control Register



6.1.4. Sensitivity Register

Offset 4

| | | | | | | | | |
|----------------------|--------------|---|---|----------|---------|----------|-------|-------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Sensitivity Register | RXDSNS(2: 0) | | | Reserved | SPWIDTH | ID(2: 0) | | |
| Default State | 0 | 0 | 1 | 0 | 0 | ID(2) | ID(1) | ID(0) |

| Bit Number | Bit Mnemonic | Access | Function | | |
|------------|-------------------|---------|--|---------|-----|
| 7-5 | RXDSNS(2: 0) | R/W | Used to program the sensitivity of the DRS demodulator. The corresponding samples is the number of consecutive samples of an IrDA pulse it takes the digital detector to declare the presence of a valid IrDA pulse. | | |
| | | | Value | FIR | SIR |
| | | | 000 | 1 | 4 |
| | | | 001 | 2 | 8 |
| | | | 010 | 3 | 12 |
| | | | 011 | 4 | 16 |
| | | | 100 | 5 | 20 |
| | | | 101 | Illegal | 24 |
| | | | 110 | Illegal | 28 |
| 111 | Illegal | Illegal | | | |
| 4 | Reserved | RO | Reserved. Write as zero. | | |
| 3 | SPWIDTH | R/W | SIR transmit pulse width. When cleared, the pulse width for SIR mode transmission is 1.6usec. When set, the pulse width is 3/16 th the bit rate. | | |
| 2-0 | ID(2: 0) (Note 1) | RO | Revision ID of the chip. | | |

Note: 1. For LA9 device revision, ID (2::0) = 1 1 1

Table 16. Sensitivity Register

6.1.5. Status Register

Offset 5

| | | | | | | | | |
|-----------------|----------|---|---|-------|-------|---------|----------|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Status Register | Reserved | | | FFDIR | FFCLR | FFEMPTY | Reserved | |
| Default State | 0 | | | 1 | 0 | 1 | 0 | |

| Bit Number | Bit Mnemonic | Access | Function |
|------------|--------------|--------|--|
| 7-5 | Reserved | N/A | Reserved |
| 4 | FFDIR | RO | When set, the FIFO is in transmit mode. When cleared, the FIFO is in receive mode. |
| 3 | FFCLR | WO | When set, clears the FIFO by resetting the pointers to the empty position. This bit must then be cleared to enable operation of the FIFO. Failing to do so, will prohibit operation of the FIFO. The state of the bit can not be read. |
| 2 | FFEMPTY | RO | When set, indicates there is no data in the FIFO. |
| 1-0 | Reserved | N/A | Reserved |

Table 17. Status Register

STIr4200
USB/IrDA Bridge Controller



6.1.6. FIFO Count Registers (LSB,MSB)

Offset 6&7

6.1.6.1. FIFO Count LSB

Offset 6

| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------------------|--------------|--------|---|---|---|---|---|---|---|---|
| FIFO Count Register (LSB) | FFCNT(7: 0) | | | | | | | | | |
| Default State | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit Number | Bit Mnemonic | Access | Function | | | | | | | |
| 7-0 | FFCNT(7:0) | RO | When combined with the FIFO Count Registers (MSB), indicates the number of bytes in the FIFO. | | | | | | | |

Table 18. FIFO Count LSB

6.1.6.2. FIFO Count MSB

Offset 7

| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------------------|--------------|--------|---|---|--------------|---|---|---|---|---|
| FIFO Count Register (MSB) | Reserved | | | | FFCNT(12: 8) | | | | | |
| Default State | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit Number | Bit Mnemonic | Access | Function | | | | | | | |
| 7-5 | Reserved | RO | Write as zeros. | | | | | | | |
| 4-0 | FFCNT(12:8) | RO | When combined with the FIFO Count Registers (LSB), indicates the number of bytes in the FIFO. | | | | | | | |

Table 19. FIFO Count MSB

6.1.7. DPLL Tune Register

Offset 8

| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|--------------|--------|--|---|---|---|---|-------------|---|---|
| DPLL Tune Register | DPCNT(5: 0) | | | | | | | LONGP(1: 0) | | |
| Default State | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| Bit Number | Bit Mnemonic | Access | Function | | | | | | | |
| 7-2 | DPCNT(5: 0) | R/W | Sets the sensitivity of the receiver's digital PLL. This bit should be used for chip debug purposes only. This register setting only affects FIR mode. The default setting is proper for normal operation. | | | | | | | |
| 1-0 | LONGP(1: 0) | R/W | Sets the sensitivity of the pulse detector of the receiver. These bits should be used for chip debug purposes only. | | | | | | | |

Table 20. DPLL Tune Register



6.1.8. IRDIG Setup Register

Offset 9

| | | | | | | | | |
|----------------------|--------|-------|----------|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IRDIG Setup Register | RXHIGH | TXLOW | Reserved | | | | | |
| Default State | 0 | 0 | 0 | | | | | |

| Bit Number | Bit Mnemonic | Read/Write Access | Function |
|------------|--------------|-------------------|--|
| 7 | RXHIGH | R/W | When set, this bit inverts the polarity of the data received by the digital interface on the RXFAST and RXSLOW pins. |
| 6 | TXLOW | R/W | When set, this bits inverts the polarity of the data transmitted by the digital interface on the TXDATA pin. |
| 5-0 | Reserved | R/W | Reserved |

Table 21. IRDIG Setup Register

6.1.9. Test Register

Offset 15

| | | | | | | | | |
|---------------|--------|--------|---------|----------|---------------|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Test Register | PLLDWN | LOOPIR | LOOPUSB | Reserved | TSTOSC(3 : 0) | | | |
| Default State | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Read/Write Access | Function |
|------------|--------------|-------------------|--|
| 7 | PLLDWN | R/W | When set, powers down the secondary infrared transceiver PLL. This bit should be cleared for SIR operation. Two independent PLLs are required in this mode of operation. This bit should be set for FIR operation since the infrared transceiver uses the USB PLL in this mode of operation. |
| 6 | LOOPIR | R/W | When set, puts the infrared transceiver into internal loop back using the FIFO to buffer data. This bit should be used for chip debug purposes only. |
| 5 | LOOPUSB | R/W | When set, puts the USB interface into loop back mode using the FIFO to buffer data. This bit should be used for chip debug purposes only. |
| 4 | TSTENA | R/W | Enables the oscillator to be powered down while in USB Suspend Mode. |
| 3-0 | TSTOSC(3: 0) | R/W | Sets the bias currents for the crystal oscillator circuitry. These bits should be used for chip debug purposes only. |

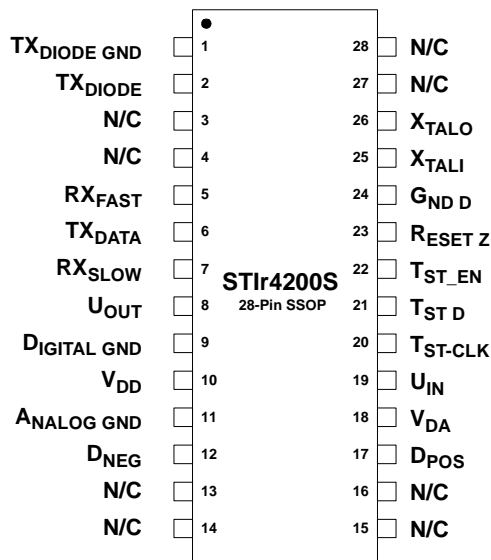
Table 22. Test Register

STIr4200
USB/IrDA Bridge Controller



7. PIN DESCRIPTION

7.1. STIr4200S 28-Pin SSOP Pin Description



Note: "N/C" indicates the pin is "not connected"

Figure 8. STIr4200S 28-Pin SSOP Pin Assignment Drawing

| Pin Number | Signal Name | Type | Description |
|------------|-------------|------|-------------------------------------|
| 1 | TXDIODE GND | PWR | TXDIODE power supply ground |
| 2 | TXDIODE | O | Optional LED driver output |
| 3 | NC | | No connect |
| 4 | NC | | No connect |
| 5 | RXFAST | I | Receive data from IR module (Fast) |
| 6 | TXDATA | O | Transmit data output to IR module |
| 7 | RXSLOW | I | Receive data from IR module (Slow) |
| 8 | UOUT | O | SD/Mode control to IR module |
| 9 | DGND | PWR | Digital power supply ground |
| 10 | VDD | PWR | Digital power supply (+) |
| 11 | AGND | PWR | USB transceiver power supply ground |
| 12 | DNEG | I/O | USB interface negative (-) data |
| 13 | NC | | No connect |
| 14 | NC | | No connect |
| 15 | NC | | No connect |
| 16 | NC | | No connect |
| 17 | DPOS | I/O | USB interface positive (+) data |
| 18 | VDA | PWR | USB transceiver power supply (+) |
| 19 | UIN | I/O | Test |
| 20 | TST-CLK | I | Test clock input |
| 21 | TSTD | I/O | Test data input/output |
| 22 | TST_EN | I | Test enable |
| 23 | RESETZ | I | Master reset, active low |
| 24 | GNDD | PWR | Power supply ground |
| 25 | XTALI | I | 12Mhz crystal/clock input |
| 26 | XTALO | O | 12Mhz crystal/clock output |
| 27 | NC | | No connect |
| 28 | NC | | No connect |

Table 23. Pin Descriptions for STIr4200S 28-Pin SSOP Package



8. PACKAGE DRAWINGS

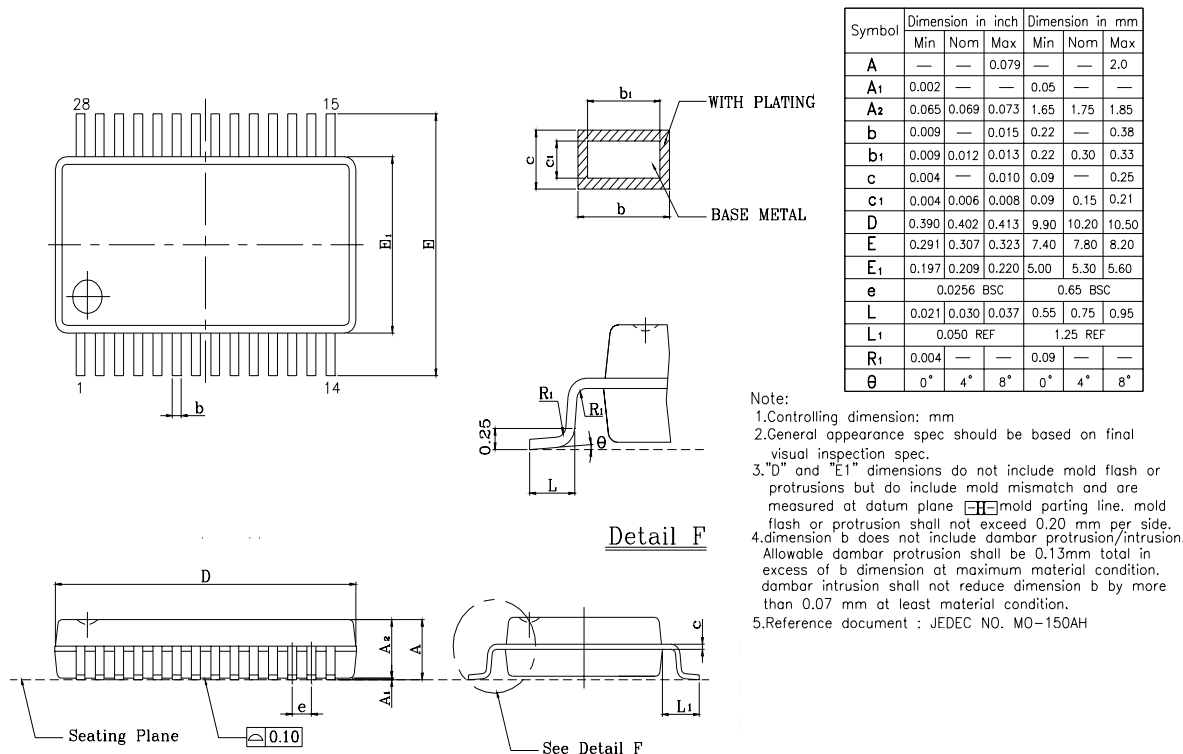


Figure 9. 28-Pin SSOP Package Drawing

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