PM5342

SPECTRA-155

SPECTRA-155 DS3 DESYNCHRONIZATION

APPLICATION NOTE

PRELIMINARY

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1 REFERENCES

1. ITU-T Recommendation G.709 - "Synchronous Multiplexing Structure," Helsinki, March 1993.

2. Bellcore GR-253-CORE , Issue 2, December 1995

3. American National Standards Institute, T1.105.03, 1994

4. RF Micro Devices, AN0001. “Optimization of Quadrature Modulator Performance”

5. RF Micro Devices, TA0019, “Quadrature Modulator/Demodulator IC Covers Baseband to 250 MHz”

2 OVERVIEW

When a DS3 signal is transported through a synchronous network such as SONET/SDH, jitter is introduced through mapping and pointer justifications. Although the SPECTRA-155 accounts partially for mapping jitter, external circuitry is required to smooth the gapped clock from the Spectra-155 to produce a telecom compliant DS3 signal. That external circuitry is the subject of this application note.

3 PROBLEM DESCRIPTION

3.1 Desynchronization in SONET/SDH networks

The desynchronization problem exists in all systems that transport signals not synchronized to the network. In order to minimize jitter and possibility of creating an error, it is necessary to recover the original timing information at the destination. There are two separate processes associated with transporting a digital signal through a synchronous network. First, there is a synchronization process, where the original signal is synchronized to the network. This is done using some sort of bit stuffing mechanism. Second, there is an opposite process called desynchonization. This process removes the effects of bit stuffing and recovers the original clock. In SONET/SDH networks, this problem can be accentuated due to pointer adjustments. A pointer adjustment is the result of a long period of accumulation of the phase difference between two network clocks. This can result in a sudden burst of 8 clock cycles, affecting the instantaneous frequency at the receive end. The desynchonizer circuitry has to average these sudden frequency deviations to provide a smooth, jitter free clock.

3.2 SPECTRA-155 DS3 desynchronizer

The SPECTRA-155 telecom bus can be set to output three DS3 channels consisting of data and clock. These three clocks are formed from a 51.84 MHz or 44.928 MHz system clock. The original system clock is gapped to produce the average frequency of the DS3 signal carried through the network.

The internal desynchonizer in SPECTRA-155 uses a 128 bit long FIFO, and an algorithm called fixed bit leaking. This algorithm will leak 8 bits of buildup in the FIFO over 500 μsec. Table 1 below describes the clock gapping algorithm used by the SPECTRA-155. Under normal conditions, a fixed pattern of gaps is used. To account for frequency variations, a ‘faster’ or ‘slower’ pattern is used. In one SONET row, there should nominally be 621.333 pulses of the 44.736 MHz clock. Under normal conditions, the SPECTRA-155 will output a fixed pattern of 621 or 622 pulses per row, as indicated in Table 1 below in the “Normal or DS3 AIS” column. The nominal average frequency of the 44.736 MHz clock can change due to pointer justifications and changes in the source frequency. When that occurs, the SPECTRA-155 will output a “faster” or “slower” pattern, as indicated in Table 1 below.

Table 1 DS3 Desynchronizer Clock Gapping Algorithm

Row Number	Normal or DS3 AIS	Run Faster	Run Slower
1	621	621	621
2	621	621	621
3	622	622	622
4	621	621	621
5	621	622	621
6	622	622	621
7	621	621	621
8	621	622	621
9	622	622	621

3.3 DS3 Jitter Specifications

Now we shall review related specifications established by bodies that govern data telecommunication. Mainly we will refer to the Bellcore GR-253-CORE, Issue 2, December 1995 section 5.6 “Jitter”.

The requirement **R5-211** for a Category I DS3 interface, the mapping jitter generation shall be less than 0.40 UIp-p. Mapping jitter is the sum of the intrinsic payload mapping jitter and the jitter that is generated as a result of the bit stuffing mechanisms.

Bellcore GR-253-CORE Issue 2, December 1997, section 5.6.2.3.1 “Category I Mapping Jitter” also investigates the pointer adjustment jitter. In that respect there is the requirement specification **R5-212** and an objective specification **O5-213**.

R5-212 Complete data integrity shall be maintained (i.e. no bit error shall occur) through the SONET system during all of the pointer adjustment jitter generation tests where T is either the “required range” given in Table 2 below, or is not applicable.

The objective specification is:

O5-213 Complete data integrity shall be maintained through the SONET system during all of the periodic pointer test sequences where T is in the "objective range" given in Table 2.

Table 2 Pointer Test Sequence Parameters

SPE/Payload	t (for burst and periodic tests)	T (Required range for Periodic tests)	T (Objective range for Periodic tests)
STS-1/DS3	0.5 ms	34 ms < T < 10 s	7.5 ms < T < 34 ms

There are several requirements regarding the pointer justification sequences. Each sequence has three distinctive intervals; an initialization interval, a cool down interval, and a measurement interval. The best description of the payload jitter test procedure is in ANSI T1.105.03 –1994 in Annex C. This information will not be repeated here, but the specifications will be pointed out and comment will be stated regarding specific pointer adjustment test sequence regarding that specific requirement.

GR-253-CORE **R5-214** specifies that allowance for jitter in the case of a single pointer adjustment should be less than 0.3 UIpp plus the mapping jitter generated by the NE under test. During the measurement interval, single pointer adjustments are introduced at intervals larger or equal to 30 sec. It should be not difficult to comply to R5-214 using a narrowband PLL.

GR-253-CORE **R5-215** specifies that jitter in the case of short and fast burst pointer adjustments should be less than 1.3 UIpp. A burst consists of three adjustments in three consecutive superframes. This requirement basically dictates that FIFO size should be able to soak in 3 bytes, as there are no other means to meet the jitter and relieve the FIFO of the excess data.

GR-253-CORE **R5-216** specifies that jitter in the case of long and slow burst pointer adjustments should be less than 1.2 UIpp. A burst consists of seven pointer justifications, first three every 0.25 seconds followed by four every 0.5 seconds. The burst is 2.5 seconds long. There is enough time to drain or fill the FIFO, depending on whether positive or negative pointer justifications were used. It is up to the designer to find a suitable balance between the jitter and FIFO length. This burst pointer adjustment is interesting because it not only tests the capability of the desynchronizer to deal with pointer adjustments, but also tests how the circuit is responding to the starting and stopping of the bursts.

GR-253-CORE **R5-217** specifies that jitter in the case of periodic pointer adjustment sequences should less than 1.0 UIpp or 1.3 UIpp, depending on the specific test sequence identified by GR-253. The pointer adjustments appear after an interval T identified by Table 2. In this case the PLL will reach almost the steady state, treating the pointer adjustments as an increase or decrease in frequency. The different patterns test how the PLL reacts to the changes in the pointer adjustment pattern.

GR-253-CORE **R5-218** specifies that jitter when the timing reference frequency is offset in range from 0 to +/- 4.6 ppm should be less than 1.5 UIpp. In this case the PLL reaches a new steady state. This should be easier to meet than **R5-217**, because there are no random pointer adjustments.

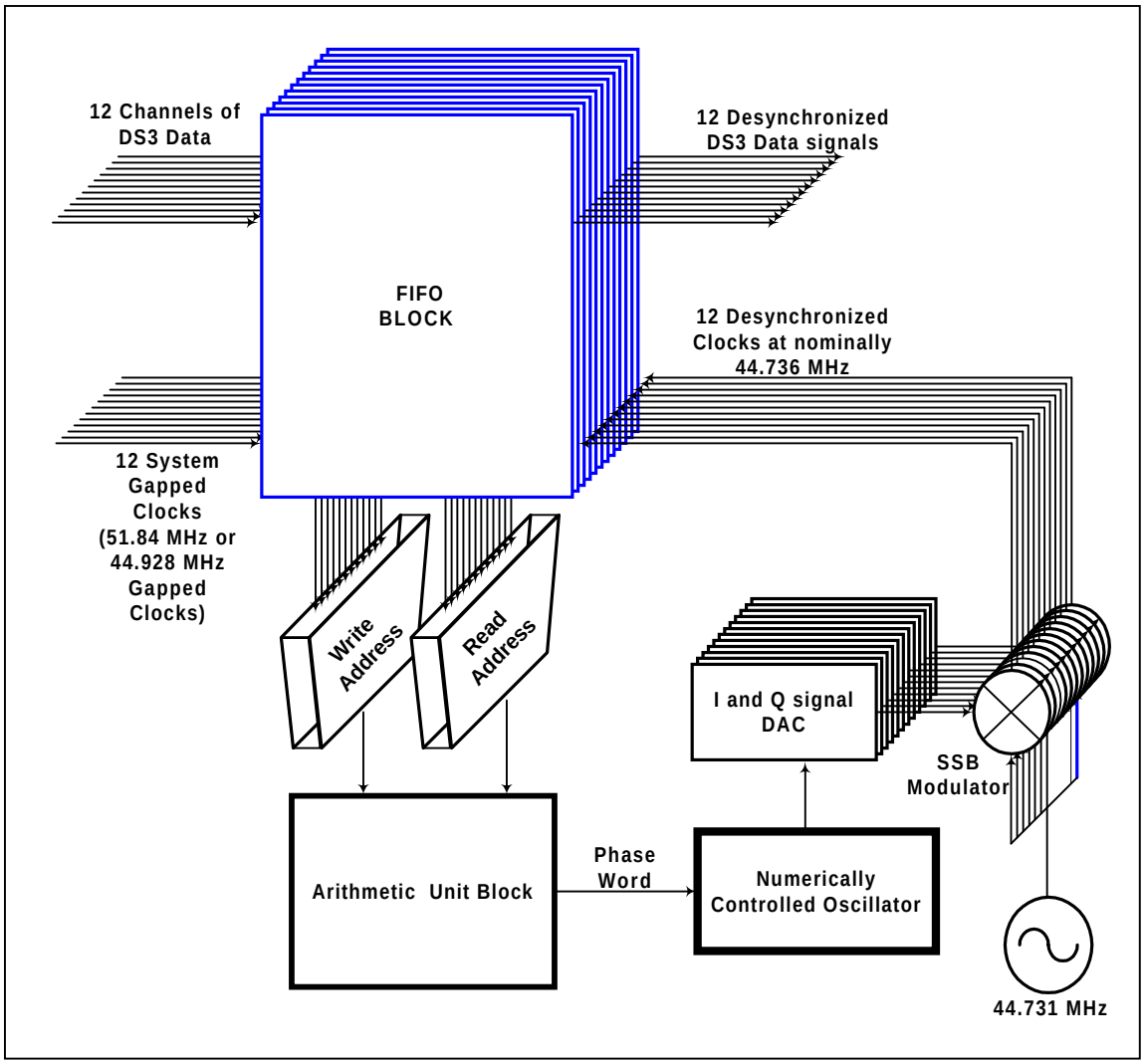
4 FUNCTIONAL DESCRIPTION

This section describes a possible design of an external phase smoothing circuit that will meet all the jitter specifications given in Section 3.3. The DS3 data from the SPECTRA-155 are buffered in a FIFO that allows the clock gaps to be removed. The DS3 data is clocked out of the FIFO using a clock with an average frequency extracted from the gapped system clock. The DS3 clock and data can then be passed to a Interface Unit (LIU).

Smoothing the gaps of the system clock, is a relatively easy task if there are no pointer adjustments. The period of the mapping jitter is 72 KHz and due to the gapping arrangement of the DS3 desynchronizer internal to the SPECTRA-155, the requirement for the FIFO length is only +/- 7 bits. If only smoothing is required than this can be relatively quickly done with a PLL and little FIFO. However, the SPECTRA-155 internal desynchronizer is not adequate to meet the jitter specifications described in Section 3.3. To meet jitter specification of GR-253-CORE a 2048 bit FIFO should be used.

4.1 Block Diagram

Figure 1 - Desynchronizer Block Diagram



The desynchronizer in Figure 1 consists of several modules. The FIFO is 2048 bits organized as 128x16 FIFO. The write clock is system gapped clock from SPECTRA-155. To ease the operations of the PLL, the input data is converted through a SIPO (serial in parallel out) to parallel stream 16 bit wide. The read clock is a variable 44.736 MHz clock generated by the Single Sideband (SSB) modulator. The write and read FIFO address difference is used as an error signal for a second order PLL and Numerically Controlled Oscillator (NCO) that generates an offset frequency. The offset frequency is passed to two Digital to Analog Converters (DACs), which generate a complex offset frequency signal (I

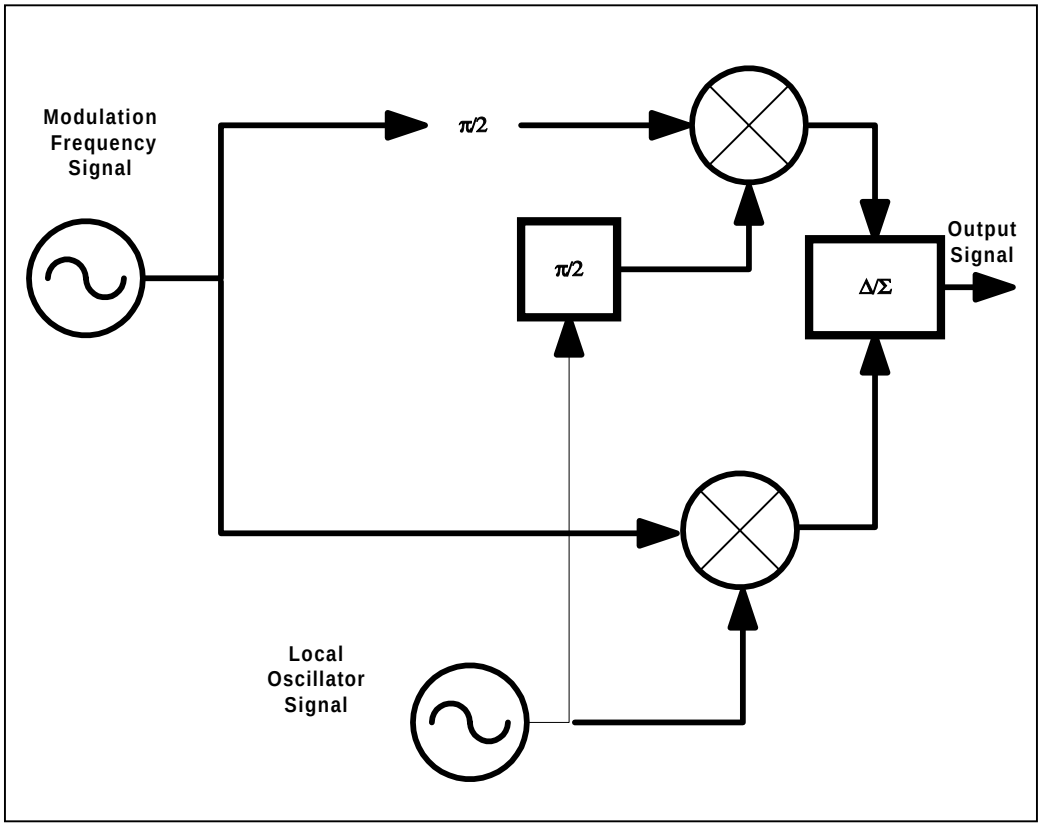
and Q channels). This complex offset frequency is used by the single sideband modulator to generate desired average DS3 frequency.

4.2 Single Sideband Modulator

It is advantageous to implement the FIFO read clock digitally so this clock will not depend on temperature variations and it will be consistent from batch to batch. It is also economical, since the circuitry needs only one crystal oscillator at 44.731 MHz for multiple channels.

The SSB modulator uses two double balanced mixers. The local oscillator signal is split and one copy is shifted 90 degrees. Similarly, the modulation signal is split and a copy of modulation signal is shifted 90 degrees. The two output signals from mixers can form a sum to pick the upper sideband, thus changing the 44.731 MHz clock to the desired frequency.

Figure 2 - SSB Modulator Block Diagram

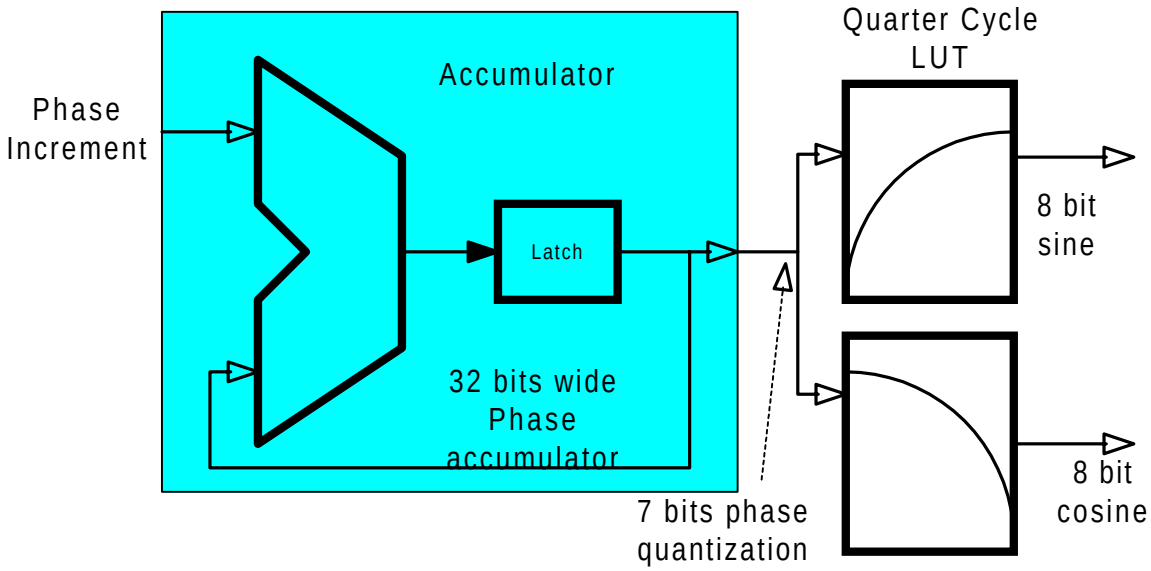


We shall not explain the operation of this circuit. A good treatment of this subject is in RF Micro-Devices application notes AN0001 and TA0019. The RF 2703 from RF Micro Devices is an excellent candidate for the SSB modulator.

4.3 NCO

The SSB modulator requires a local oscillator signal and a modulation signal. The modulation signal is a complex sinusoidal signal with I and Q components (sine and cosine). The NCO block generates these two signals.

Figure 3 - NCO Block Diagram



The NCO can be implemented as an 32 bit wide accumulator with the 7 most significant bits used as a phase representation of modulation signal. This 7 bit phase coding accounts for 128 possible phases that are in fact the 128 possible addresses of an look up table, approximately (90/128= 0.703125) degrees per step. The phase of the modulation signal is converted to amplitude using an 8 bit Look Up Table (LUT). Only one LUT is needed that can be shared among multiple channels. This also applies to the accumulators that can share same adder hardware with 16x16 RAM containing the current value of phase for multiple DS3 channels. In the sine LUT one quarter of the sinusoid is encoded.

Simple manipulation of the addresses of the LUT is used to create the sine and cosine signals.

4.4 Digital to Analog Converter

The DAC circuits generate the I and Q modulation signals for the SSB modulator. An 8 bit DAC with a minimum 160 kHz sampling rate is recommended in order to create the fastest sinusoids of 10 kHz with at least 16 different sampling values. This implementation will limit the intrinsic jitter below 0.1 UIpp.

4.5 FIFO and Write and Read Counters

The FIFO can be implemented using a dual port 4096 bit RAM implying a worst-case delay of 91.559µsec, well within the specification of ANSI T1.506 minimum 4.0msec. The system gapped clock from the SPECTRA-155 is used to write to the FIFO, and the 44.736 MHz clock from the SSB modulator is used to read from the FIFO. Twelve bit synchronous counters can be used for write and read address generation.

4.6 Address Difference and Loop Filter

Figure 4 shows a block diagram of the loop filter.

The fill level of the FIFO is equal to the difference between the read and write FIFO addresses. The fill level determines if the FIFO read clock should be faster or slower. If the FIFO fill level is low, the read frequency should be reduced. If the FIFO fill level is high, the read frequency should be increased. A loop filter prevents the FIFO read clock from changing frequency too quickly, which creates jitter. A loop filter with a perfect integrator should be used because it will eventually reduce phase error to zero in the case of DS3 clock offset with respect to the network clock or sustained pointer adjustment events. Simulations have indicated that the PLL should have a natural frequency of 0.1 Hz and a damping factor of 5. These values result in a closed loop transfer function 3 dB point at 1 Hz. The Scale#1 and Scale#2 values are determined by loop parameters, natural frequency and damping factor, as well as by the rate of the FIFO write and read addresses sampling frequency (72 kHz).

Implementation of the loop filter could be done in an FPGA such as one from the Xilinx Virtex family. The operations that are required to process one DS3 channel are relatively simple and can be sequenced one after other using the same basic circuitry. Operations are:

- Subtract read FIFO address from the write FIFO address and store it for further use in RAM

- Add FIFO address difference to accumulated FIFO address difference that is also stored in RAM, and after the addition store the new value in the RAM for further use.

- Scale the new accumulated (integrated) value of the FIFO address difference by taking only the portion of the accumulated value and adding it to the current FIFO difference.

- Scale the product of the previous operation. This can be done by using a portion of bits that form the value.

- Add obtained value to a phase value that results in 5000 Hz sine waveform to get the new phase increment.

All operations listed above require:

- Add or subtract circuit,

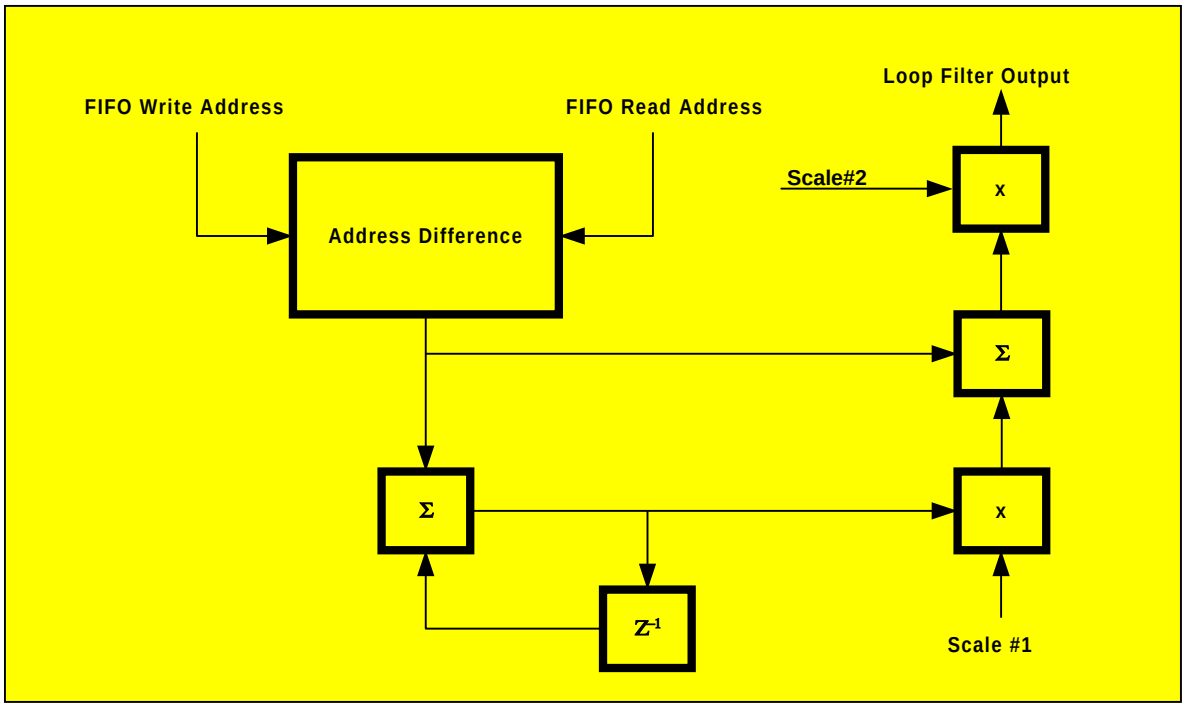
- Memory to store current FIFO read and write address difference,

- Memory to store accumulated FIFO read and write address difference,

- Multiplex circuit to perform two scaling operations (dividing and multiplying by numbers of 2^n value).

A simple structure can used to perform all operations required for the Address Difference and Loop Filter Block.

Figure 4 - Block Diagram of Loop Filter



5 SUMMARY

A low power consumption, compact and low part count design of a 12 DS3 channel desynchronizer that meets GR-253-CORE specifications is presented. This application note gives a brief description how to design the desynchronizer for 12 DS3 channels associated with SPECTRA-155 chip. The design uses the FPGA, twelve quadrature upconverter circuits, one common crystal oscillator. Power consumption should be less than 100 mW per DS3 channel, component count is small and the board space is less than 4”x4”.

NOTES

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