FUJITSU SEMICONDUCTOR
DATA SHEET

DS04–21348–3E

ASSP

Single Serial Input PLL Frequency Synthesizer

On-Chip prescaler

MB15C02

■ DESCRIPTION

The Fujitsu MB15C02 is a serial input Phase Locked Loop (PLL) frequency synthesizer with a prescaler. A 64/65 division is available for the prescaler that enables pulse swallow operation.

This operates with a supply voltage of 1.0 V (min.).

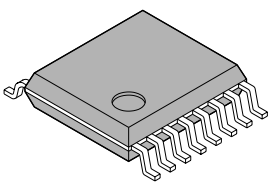
MB15C02 is suitable for mobile communications, such as paging systems.

■ FEATURES

- High frequency operation: 220 MHz max @V_{DD} = 1.0 V to 1.5 V
  330 MHz max @V_{DD} = 1.2 V to 1.5 V
  450 MHz max @V_{DD} = 1.3 V to 1.5 V
- Single power supply : V_{DD} = 1.0 to 1.5 V
- Power saving function
- Pulse swallow function: 64/65
- Serial input 14-bit programmable reference divider: R = 5 to 16,383
- Serial input 18-bit programmable divider consisting of:
  - Binary 6-bit swallow counter: 0 to 63
  - Binary 12-bit programmable counter: 5 to 4,095
- Wide operating temperature: Ta = –20 to 60°C

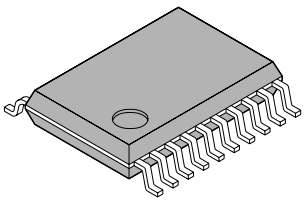
■ PACKAGES

16-pin, Plastic SSOP



(FPT-16P-M05)

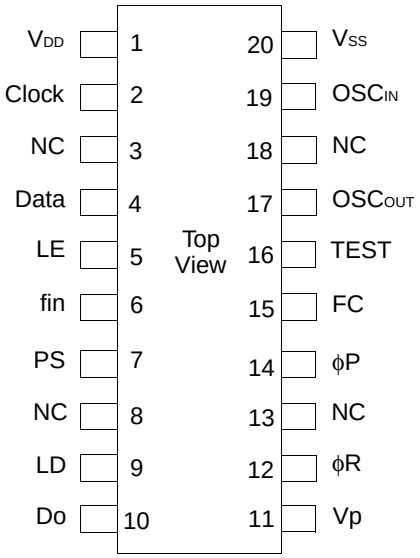
20-pin, Plastic SSOP



(FPT-20P-M03)

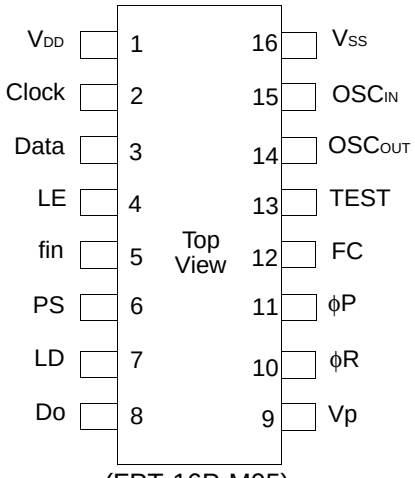
■ PIN ASSIGNMENTS

SSOP-20 pin



(FPT-20P-M03)

SSOP-16 pin



(FPT-16P-M05)

■ PIN DESCRIPTIONS

Pin no.		Pin name	I/O	Descriptions
SSOP 16	SSOP 20			
1	1	V_{DD}	–	Power supply voltage
2	2	Clock	I	Clock input for the shift register.(Schmitt trigger input) Data is shifted into the shift register on the rising edge of the clock.
–	3	NC	–	No connection
3	4	Data	I	Serial data input using binary code.*(Schmitt trigger input)*
4	5	LE	I	Load enable signal input *(Schmitt trigger input)* When LE is high, the data in the shift register is transferred to a latch, according to the control bit in the serial data.
5	6	fin	I	Prescaler input. A bias circuit and amplifier are at input port. Connection with an external VCO should be done by AC coupling.
6	7	PS	I	Power saving mode control. This pin must be set at “L” at Power-ON. PS = “H” ; Normal mode PS = “L” ; Power saving mode
–	8	NC	–	No connection
7	9	LD	O	Lock detector signal output. When a PLL is locking, LD outputs “H”. When a PLL is not locking, LD outputs “L”.
8	10	Do	O	Charge pump output. Phase of the charge pump can be reversed by FC input. The Do output may be inverted by FC input. The relationships between the programmable reference divider output (fr) and the programmable divider output (fp) are shown below; fr > fp :“H” level (FC = “L”), “L” level (FC = “H”) fr = fp : High impedance fr < fp :“L” level (FC = “L”), “H” level (FC = “H”)
9	11	Vp	–	Power supply for the charge pump.
10	12	ϕR	O	Phase comparator output pin (for external charge pump). Relation between the programmable reference divider output (fr) and the programmable divider output (fp) are shown below; When FC = “L” fr > fp : ϕR = “L” level, ϕP = “L” level fr = fp : ϕR = “L” level, ϕP = High impedance fr < fp : ϕR = “H” level, ϕP = High impedance When FC = “H” fr > fp : ϕR = “H” level, ϕP = High impedance fr = fp : ϕR = “L” level, ϕP = High impedance fr < fp : ϕR = “L” level, ϕP = “L” level
–	13	NC	–	No connection
11	14	ϕP	O	Phase comparator output pin (for external charge pump). Refer to Pin description for ϕR. ϕP pin is a Nch open drain output.
12	15	FC	I	Phase comparator input select pin.
13	16	TEST	I	Test mode select pin. *(Pull down resistor)* Please set this pin to ground or open usually.

(Continued)

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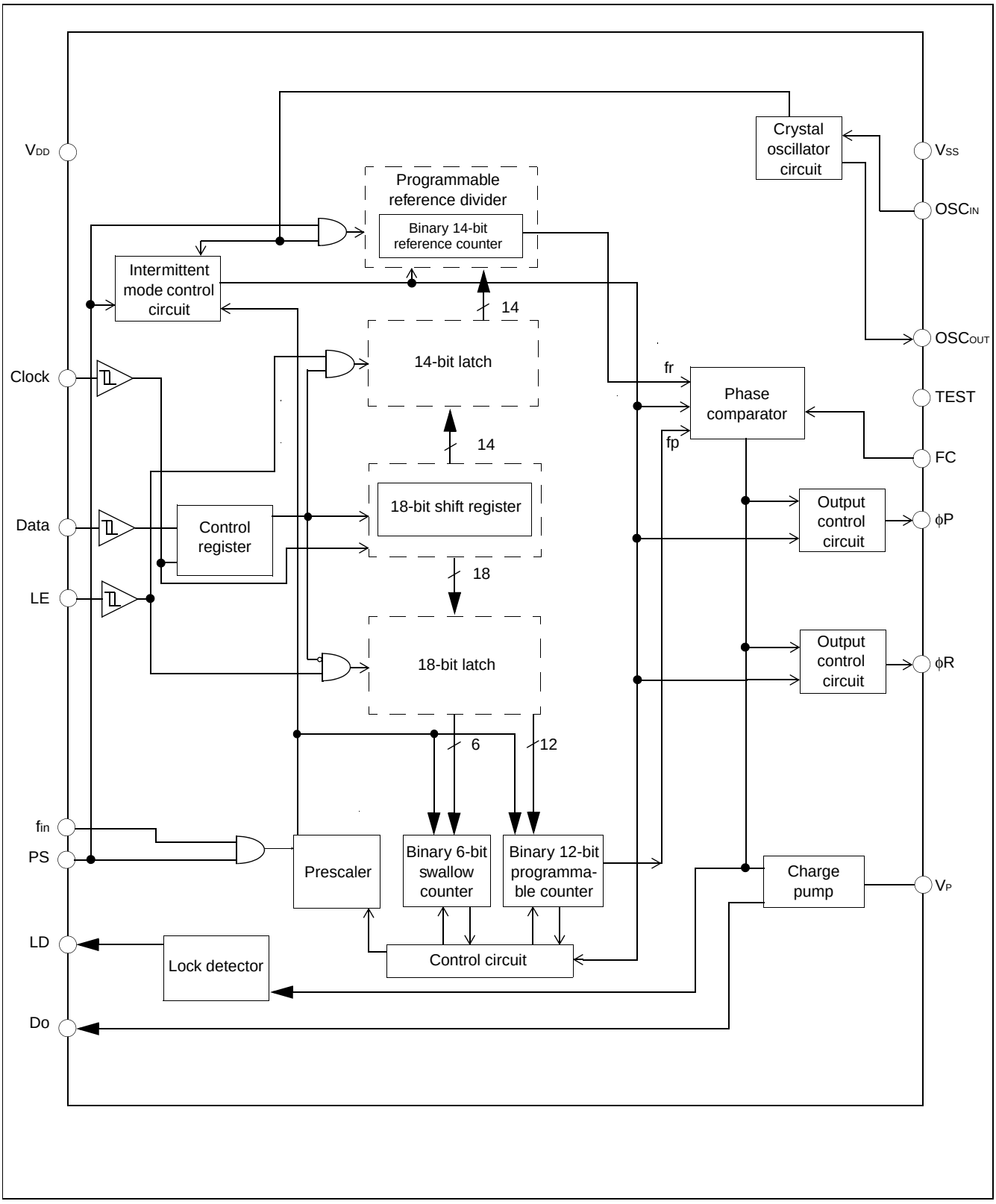
Pin no.		Pin name	I/O	Descriptions
SSOP 16	SSOP 20			
14	17	OSC_{OUT}	O	Oscillator output. Connection for an external crystal.
–	18	NC	–	No connection
15	19	OSC_{IN}	I	Programmable reference divider input. Oscillator input. Clock can be input to OSC_{IN} from outside. In the case, please leave OSC_{OUT} pin open and make connection with OSC_{IN} as AC coupling.
16	20	V_{SS}	–	Ground pin.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit	Remark
		Min.	Max.		
Power supply voltage	V_{DD}, V_P	GND–0.5	+2.0	V	
Input voltage	V_{IN}	GND–0.5	V_{DD} +0.5	V	
Output voltage	V_{OUT}	GND–0.5	V_{DD} +0.5	V	
Output current	I_{OUT}	–10	+10	mA	
Storage temperature	T_{stg}	–40	+125	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark	
		Min.	Typ.	Max.			
Power supply voltage	V_{DD}, V_P	1.0	–	1.5	V	For 220 MHz	$V_{DD} = V_P$
		1.2	–	1.5		For 330 MHz	
		1.3	–	1.5		For 450 MHz	
Input voltage	V_{IN}	GND	–	V_{DD}	V		
Operating temperature	Ta	–20	–	+60	°C		

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(For 220 MHz :V_{DD} = Vp = 1.0 to 1.5 V, Ta = –20 to +60°C)
(For 330 MHz :V_{DD} = Vp = 1.2 to 1.5 V, Ta = –20 to +60°C)
(For 450 MHz :V_{DD} = Vp = 1.3 to 1.5 V, Ta = –20 to +60°C)

Parameter			Symbol	Condition	Value			Unit
					Min.	Typ.*3	Max.*4	
Power supply current		Active Mode	I_{DD} *1	(V_{DD}=1.0V/220MHz) (V_{DD}=1.2V/330MHz) (V_{DD}=1.3V/450MHz)	– – –	0.6 1.0 1.3	1.2 1.8 2.2	mA
Power saving current		Power saving mode	I_{DDS} *2	(V_{DD}=1.0V) (V_{DD}=1.2V) (V_{DD}=1.3V)	– – –	50 70 80	250 300 350	µA
Operating frequency		fin	fin	Programmable divider (V_{DD}=1.0 to 1.5V) (V_{DD}=1.2 to 1.5V) (V_{DD}=1.3 to 1.5V)	 10 10 10	 – – –	 220 330 450	MHz
		OSC_{IN}	f_{OSC}	Programmable reference divider	5	–	20	MHz
Input sensitivity	fin		Vfin	AC coupling	–2.0	–	–	dBm
	OSCin		V_{OSC}	AC coupling	–2.0	–	–	dBm
Input voltage	Except for fin and OSCin	H level	V_{IH}	–	V_{DD} – 0.2	–	–	V
		L level	V_{IL}	–	–	–	0.2	
Input current	Except for fin, OSCin and TEST	H level	I_{IH}	V_{IN}=V_{DD}	–	–	+1.0	µA
		L level	I_{IL}	V_{IN}=GND	–1.0	–	–	
Output voltage	Except for OSC_{OUT} and ϕP	H level	V_{OH}	I_{OH} = –0.2 mA	V_{DD} – 0.2	–	–	V
		L level	V_{OL}	I_{OL} = 0.2 mA	–	–	0.2	
	ϕP	L level	V_{OL}	I_{OL} = 0.2 mA	–	–	0.2	V
High impedance cutoff current	Do		I_{OFF1}	V_{OUT} = GND to V_P	–100	–	100	nA
	ϕP		I_{OFF2}	V_{OUT} = V_{DD}	–	–	100	nA

*1: Conditions; Inputs except for fin, OSC_{IN} and TEST are grounded, Outputs are opened.
Specifying the current flowing in V_{DD} and Vp at operating state under conditions of V_{DD} = Vp, fin = 220 MHz, or 330 MHz, and OSCIN = 12.8 MHz.
The current at locking state shows I_{DD} Supply current (P.20).

*2: Conditions; PS = Low, Inputs except for fin, OSC_{IN} and TEST are grounded, Outputs are opened.

*3: Condition; Ta = 25°C

*4: Condition; Ta = –20 to +60°C

■ FUNCTION DESCRIPTIONS

1. Pulse Swallow Function

The divide ratio can be calculated using the following equation:

$f_{VCO} = [(M \times N) + A] \times f_{OSC} \div R \quad (A < N)$

f_{VCO}	:	Output frequency of external voltage controlled oscillator (VCO)
N	:	Preset divide ratio of binary 12-bit programmable counter (5 to 4,095)
A	:	Preset divide ratio of binary 6-bit swallow counter (0 to 63)
f_{OSC}	:	Output frequency of the reference frequency oscillator
R	:	Preset divide ratio of binary 14-bit programmable reference counter (5 to 16,383)
M	:	Preset modulus of dual modulus prescaler (64)

2. Circuit Description

(1) Intermittent operation

The intermittent operation of the MB15C02 refers to the process of activating and deactivating its internal circuit thus saving power dissipation otherwise consumed by the circuit. If the circuit is simply restarted from the power saving state, however, the phase relation between the reference frequency (fr) and the programmable frequency (fp), which are the input to the phase comparator, is not stable even when they are of the same value. This may cause the phase comparator to generate an excessively large error signal, resulting in an out-of-synth lock frequency

To preclude the occurrence of this problem, the MB15C02 has an intermittent mode control circuit which forces the frequencies into phase with each other when the IC is reactivated, thus minimizing the error signal and resultant lock frequency fluctuations. The intermittent mode control circuit is controlled by the PS pin. Setting pin PS high provides the normal operation mode and setting the pin low provides the power saving mode. The MB15C02 behavior in the active and power saving modes is summarized below.

Active mode (PS = “H”)
All MB15C02 circuits are active and provide the normal operation.

Power saving mode (PS = “L”)
The MB15C02 stops any circuits that consume power heavily as well as cause little inconvenience when deactivated and enters the low-power dissipation state. Do, ϕR, ϕP, and LD pins take the same state as when the PLL is locked. Do pin becomes a high-impedance state and the input voltage to the voltage control oscillator (VCO) is maintained at the same level as in active mode(that is, locked state) according to a time constant of a low pass filter (LPF). Consequently , the output frequency from the VCO (f_{VCO}) is maintained at approximately the lock frequency.

Applying the intermittent operation by alternating the active and power saving modes, and also forcing the phases of fr and fp to synchronize when it switches from stand by to active modes, the MB15C02 can keep the power dissipation of its entire circuitry to the minimum.

(2) Programmable divider

The f_{VCO} input through fin pin is divided by the programmable divider and then output to the phase comparator as fp. It consists of a dual modulus prescaler, a 6-bit binary swallow counter, a 12-bit binary programmable counter, and a controller which controls the divide ratio of the prescaler

Divide ratio range:
Prescaler : M = 64, M+1=65
Swallow counter : A = 0 to 63
Programmable counter : N = 5 to 4095

The MB15C02 uses the pulse swallow method; consequently, the divide rations of the swallow and programmable counters must satisfy the relationship N>A.

The total divide ratio of the programmable divider is calculated as follows:
Total divide ratio = $(M + 1) \times A + M \times (N – A) = M \times N + A = 64 \times N + A$

When N is set within $5 \leq N \leq 63$, the possible divide ratio A of the swallow counter can take values $0 \leq A \leq N-1$ because N must be greater than A. For example, $0 \leq A \leq 19$ is allowed when N=20 but $20 \leq A \leq 63$ is not allowed in that case. Consequently, $N \geq 64$ must be satisfied for the total divider to be set within $0 \leq A \leq 63$.

The fp and fin have the following relation:
$fp = fin / (64 \times N + A)$

(3) Programmable reference divider

The programmable reference divider divides the reference oscillation frequency(fosc) from the crystal oscillator connected between OSCin and OSCout pins or from the external oscillator input taken in directly through OSCin, pin and then, sends the resultant fr to the phase comparator. It consists of a 14-bit binary programmable reference counter. When the output from the external oscillator is to be input directly to OSCin, pin the connection must be AC coupled and OSCout pin is left open. Also, to prevent OSCout from malfunctioning, its traces on the printed circuit board must be kept minimal or eliminated entirely; whenever possible, it must be free of any form of load.
The following divider is used:
Programmable reference counter : R = 5 to 16383

The fr and fosc have the following relation:
fr = fosc / R

(4) Phase comparator

The phase comparator detects the phase difference between the outputs fr and fp from the dividers and generates an error signal that is proportional to phase difference. The outputs from the phase comparator include 1) Do which takes on one of the three states, namely, “L” (low), “H” (high), and “Z” (high impedance), and is sent to the LPF, 2)ϕR, 3)ϕP, 4)LD which indicates the PLL lock or unlock states.

(a) Phase comparator

The phase comparator detects the phase error between fr and fp, then generates an error signal that is proportional to the phase error. The roles of the fr and fp supplied to the phase comparator may be reversed by switching the logical input level of pin FC. This inverts the logical level of the Do output. The logical level of Do output may be selected according to the characteristics of the external LPF and the VCO. (Refer to Table 1.)

Table. 1 Phase comparator inputs/output relationships

Output / Phase relation	FC = “L”			FC = “H”		
	Do	**ϕR**	**ϕP**	**Do**	**ϕR**	**ϕP**
fr > fp	H	L	L	L	H	Z
fr = fp	Z	L	Z	Z	L	Z
fr < fp	L	H	Z	H	L	L

(b) Charge pump

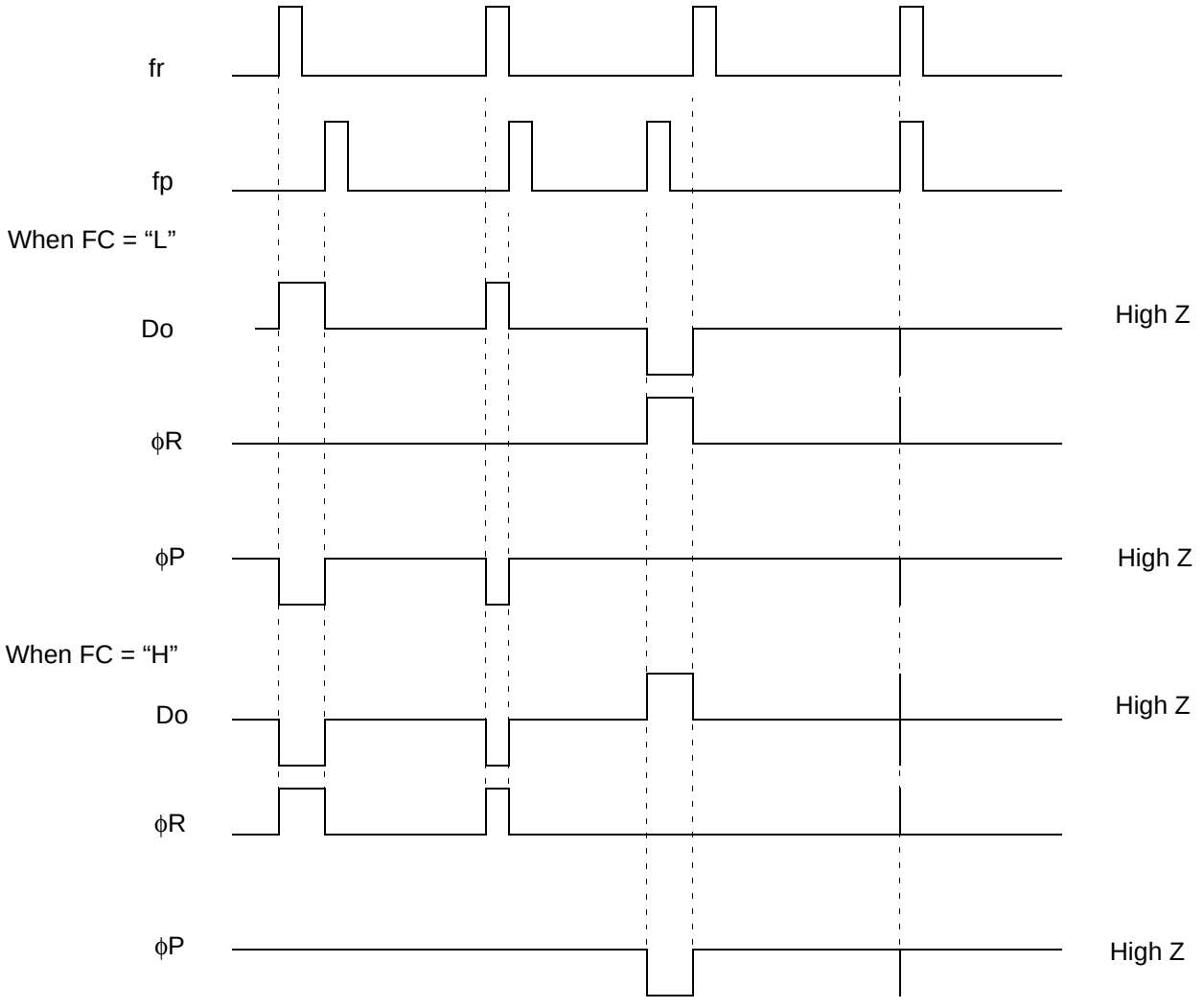
The charge pump is available in two forms: internal external.

Internal charge pump output (Do)

External charge pump outputs (ϕR, ϕP)

(c) Phase comparator input/output waveforms

The phase comparator outputs logic levels summarized in Table 1, according to the phase error between fr and fp. Note that ϕP is an Nch open drain output. The pulse width of the phase comparator outputs are identical and equal to the phase error between fr and fp as shown in Figure 1.



High Z : High impedance state

fp : Nch open output

Figure 1. Phase comparator input/output waveform

(d) Lock detector

The lock detector detects the lock and unlock states of the PLL. The lock detector outputs “H” when the PLL enters the lock state and outputs “L” when the PLL enters the unlock state as shown in Figure 2. When PS = “L”, the lock detector outputs “H” compulsorily.

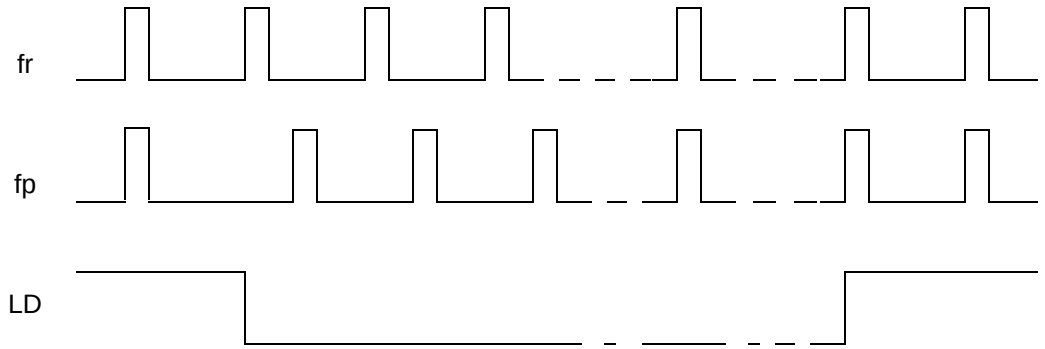


Figure 2. Phase comparator input/output waveforms (Lock detector)

4. Setting the Divide Ratio

(1) Serial data format

The format of the serial data is shown is Figure 3. The serial data is composed of a control bit and divide ratio setting data. The control bit selects the programmable divider or programmable reference divider.
In case of the programmable divider, serial data consists of 18 bits(6 bits for the swallow counter and 12 bits for the programmable counter) and 1 control bit as shown in Figure 3.1. In case of the programmable reference divider, the serial data consists of 14 divider bits and 1 control bit as shown in Figure 3.2.
The control bit is set to 0 to identify the serial data for the programmable divider and to 1 to select the serial data for the programmable reference divider.

Figure 3. Serial data format

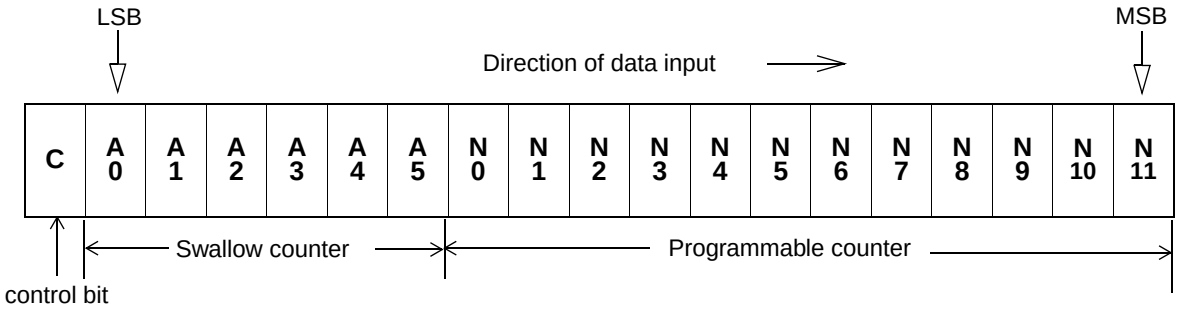


Figure 3.1. Divide ratio for the programmable divider

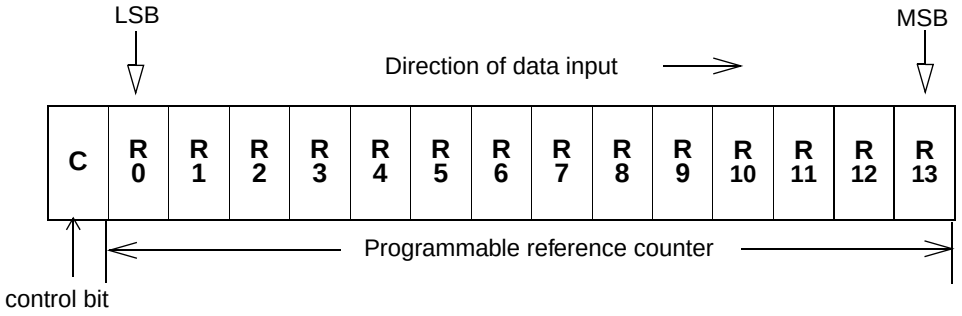


Figure 3.2. Divide ratio for the programmable reference divider

(2) The flow of serial data

Serial data is received via data pin in synchronization with the clock input and loaded into shift register which contains the divide ratio setting data and into the control register which contains the control bit. The logical product (through the AND gate in Figure 4) of LE and the control register output (i.e., control bit) is fed to the enable input of the latches. Accordingly, when LE is set high, the latch for the divider identified by the control bit is enabled and the divide ratio data from the shift register is loaded into the selected counter (s).

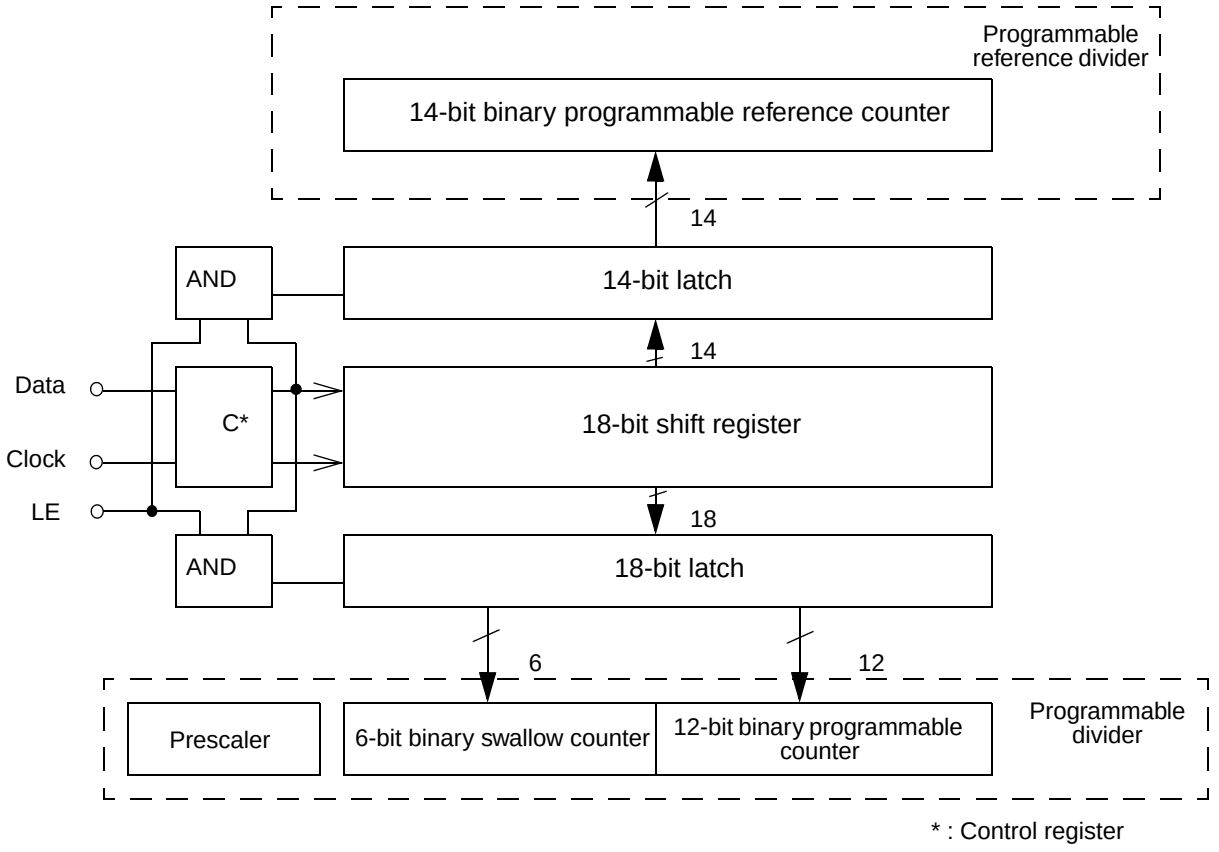


Figure 4. The flow of serial data

(3) Setting the divide ratio for the programmable divider

Columns A0 to A5 of Table 2.1 represent the divide ratio of the swallow counter and columns N0 to N11 of Table2.2 represent the divide ratio of programmable counter.

Table. 2 Divide ratio for the programmable divider

Table.2.1 Swallow counter divider A

Divide ratio (A)	A0	A1	A2	A3	A4	A5
0	0	0	0	0	0	0
1	1	0	0	0	0	0
.	.	.	.	.	.	.
63	1	1	1	1	1	1

Table2.2 Programmable counter divider N

Divide ratio (N)	N0	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11
5	1	0	1	0	0	0	0	0	0	0	0	0
6	0	1	1	0	0	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.	.	.	.	.
4095	1	1	1	1	1	1	1	1	1	1	1	1

Note: Less than 5 is prohibited.

(4) Setting the divide ratio for the programmable reference divider

Columns R0-R13 of Table 3 represent the divide ratio of the programmable reference counter. The control bit is set to 1.

Table.3 Divide ratio for the programmable reference divider

Divide ratio (R)	R 0	R 1	R 2	R 3	R 4	R 5	R 6	R 7	R 8	R 9	R 10	R 11	R 12	R 13
5	1	0	1	0	0	0	0	0	0	0	0	0	0	0
6	0	1	1	0	0	0	0	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(5) Setting data input timing

The MB15C02 uses 19 bits of serial data for the programmable divider and 15 bits for the programmable reference divider. When more bits of serial data than defined for the target divider are received, only the last valid serial data bits are effective.
To set the divide ratio for the MB15C02 dividers, it is necessary to supply the Data, Clock, and LE signals at the timing shown in Figure 5.

t_1 (≥1 μs): Data setup time t_2 (≥1 μs): Data hold time t_3 (≥ μs): Clock pulse width

t_4 (≥1 μs): LE setup time to the rising edge of last clock t_5 (≥1 μs): LE pulse width

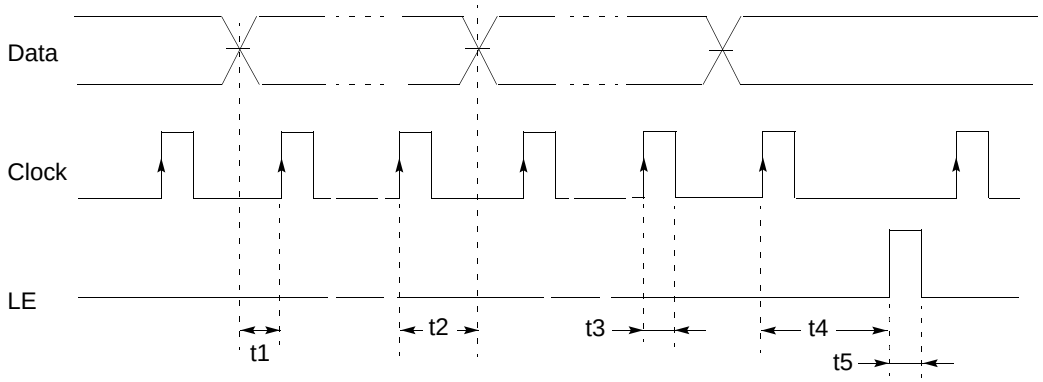


Figure 5. Serial data input timing

Since the divide rations are unpredictable when the MB15C02 is turned on, it is necessary to initialize the divide ratio for both dividers at power-on time. As shown in Figure 6, after setting the divide ratio for one of the dividers (e.g., programmable reference divider), set LE to “H” level before setting the divide ratio for the other dividers (e.g., programmable divider). To change the divide ratio of one of the divider after initialization, input the serial data only for that divider (the divide ratio for the other divider is preserved).

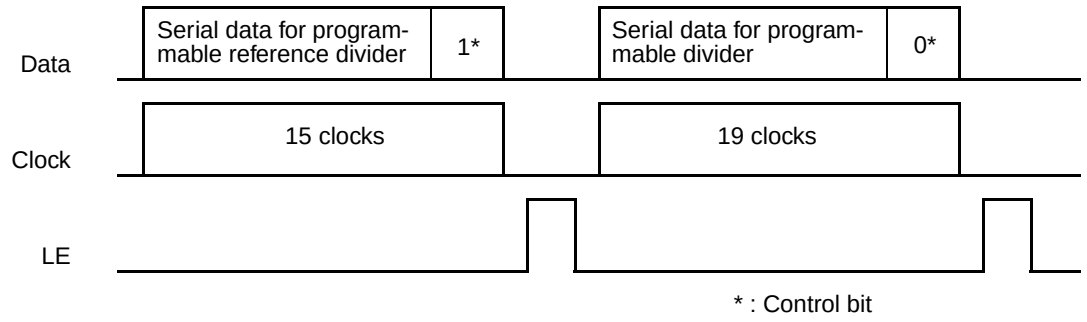
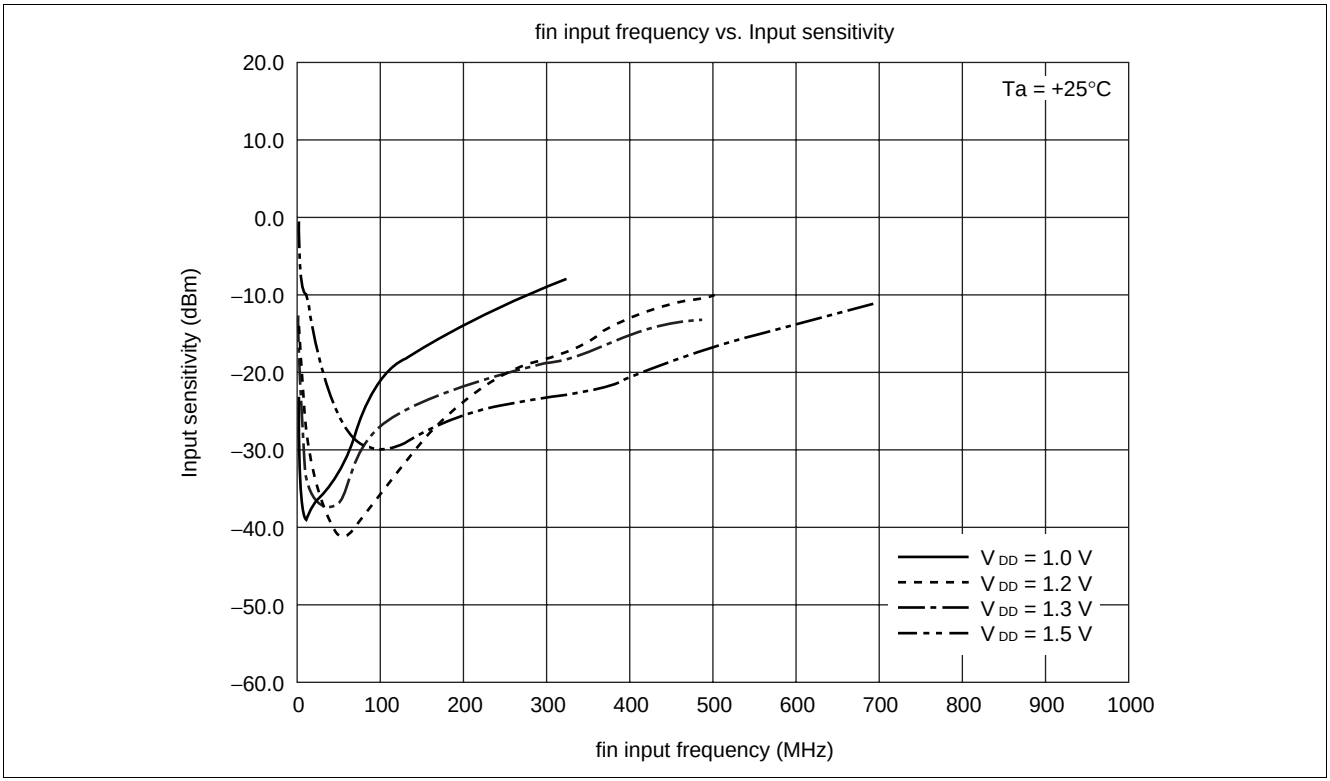


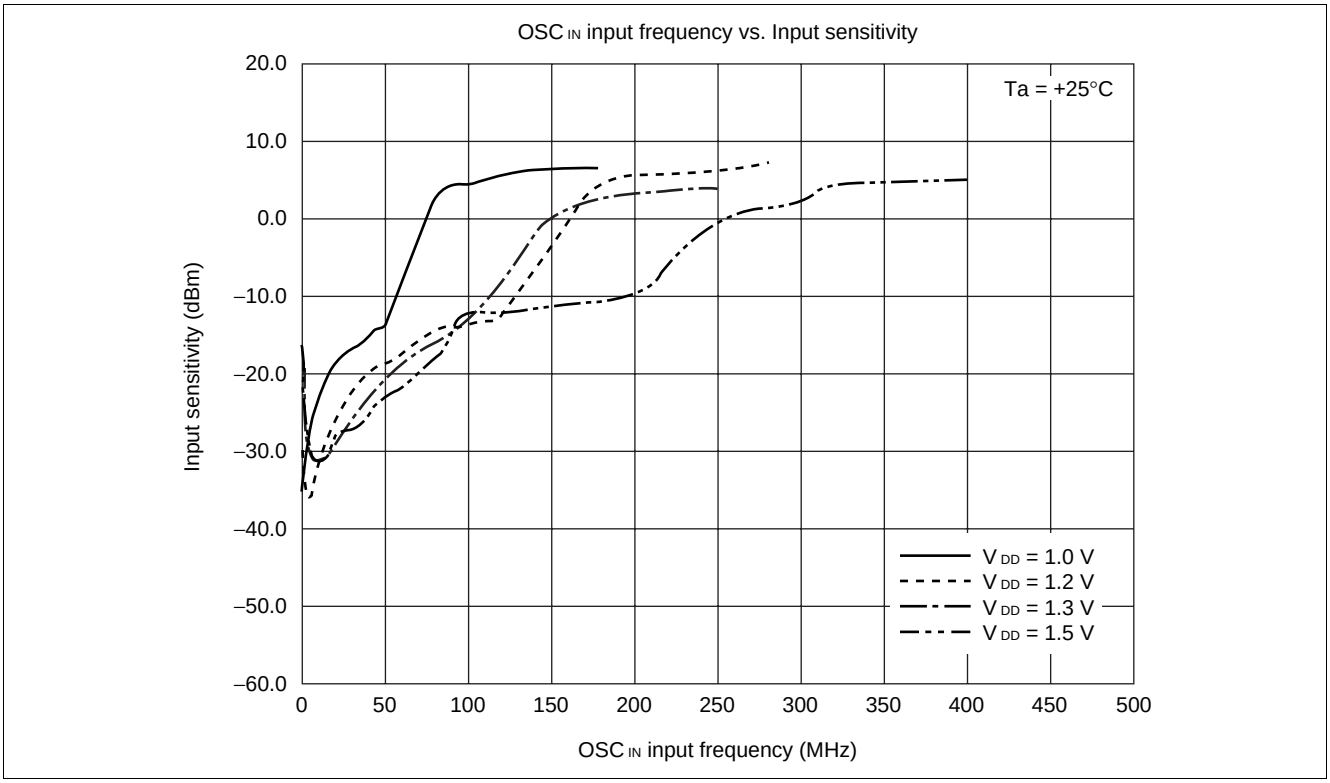
Figure 6. Inputting serial data(Setting divisors)

■ TYPICAL CHARACTERISTICS

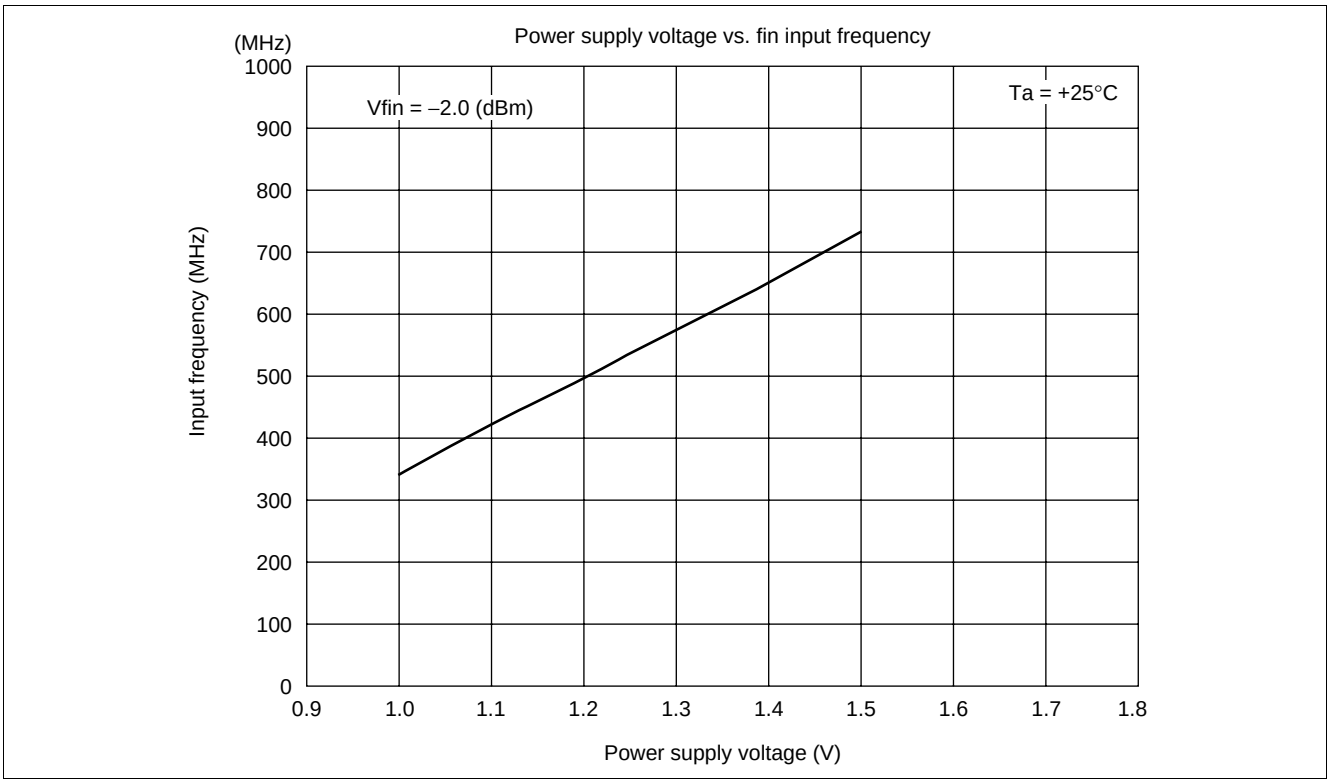
1. fin Input Sensitivity



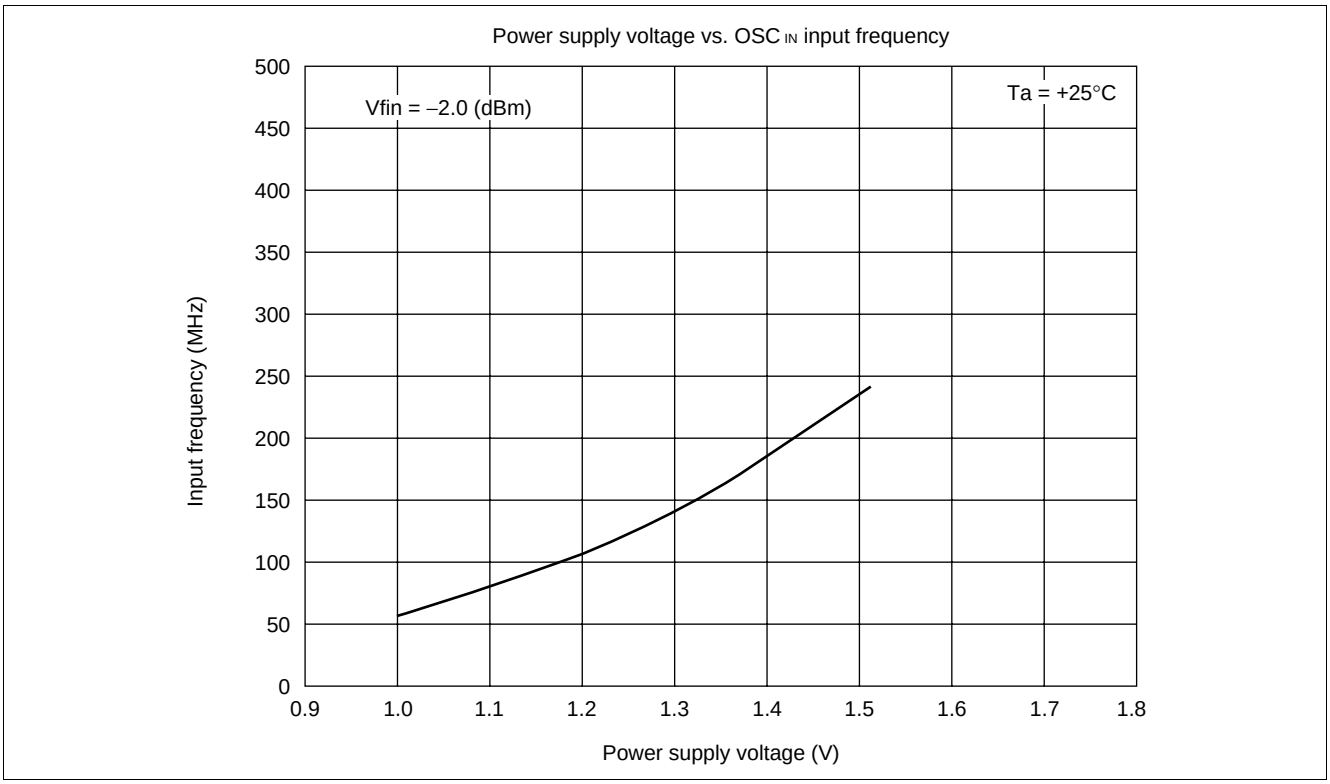
2. OSC_{IN} Input Sensitivity



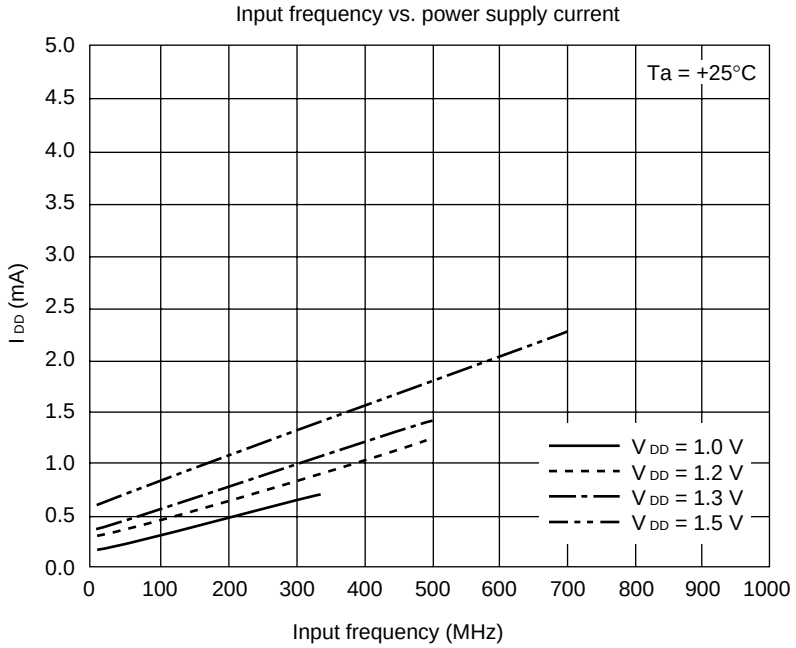
3. fin Power Supply Voltage



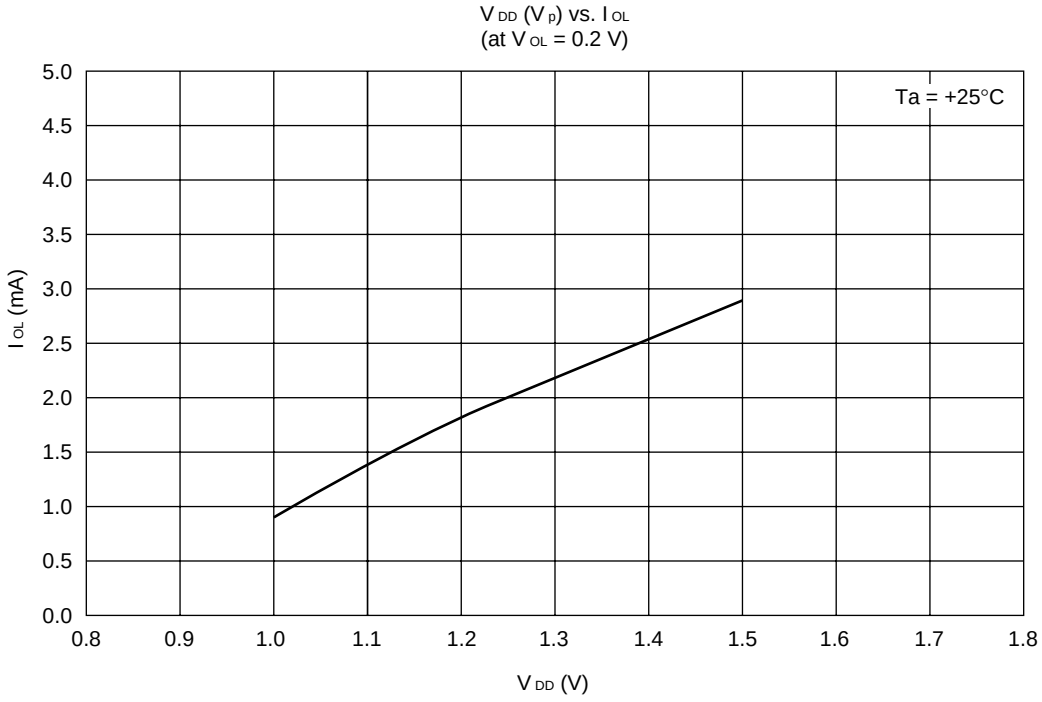
4. OSC_{IN} Power Supply Voltage

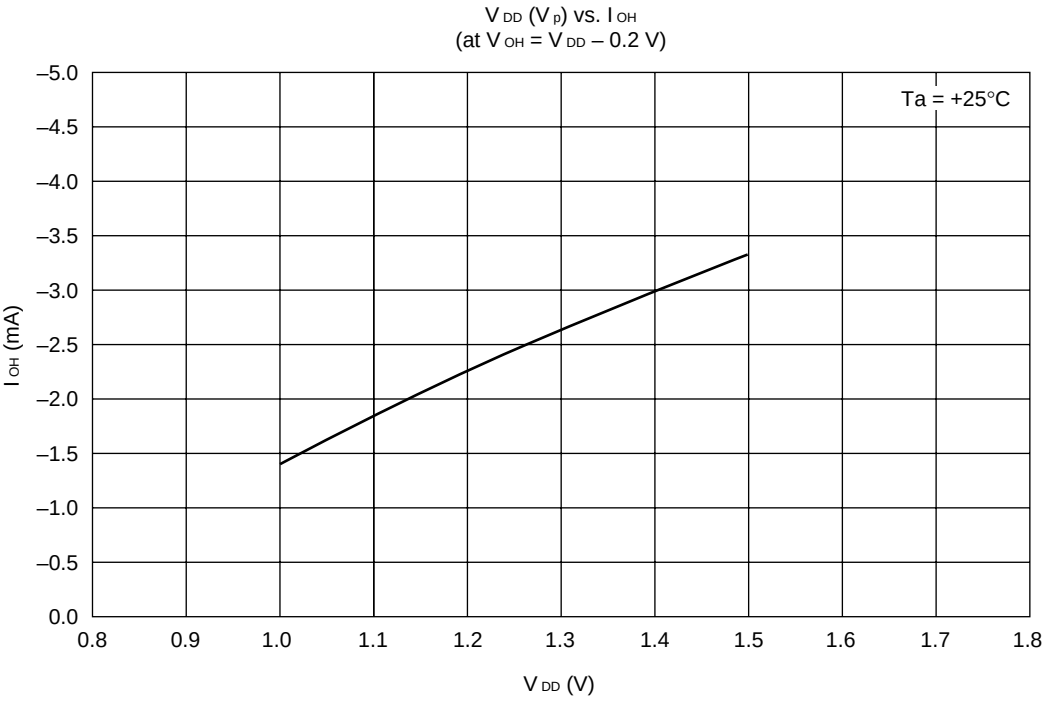


5. I_{DD} Power Supply Current

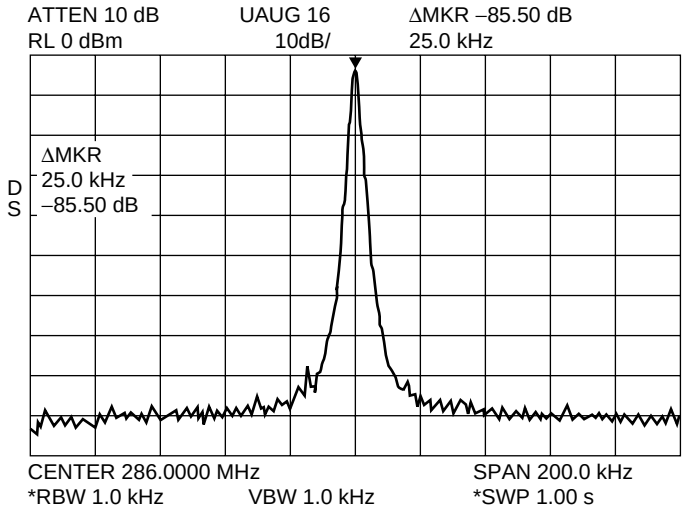


6. Do (Charge Pump) Power Supply Voltage

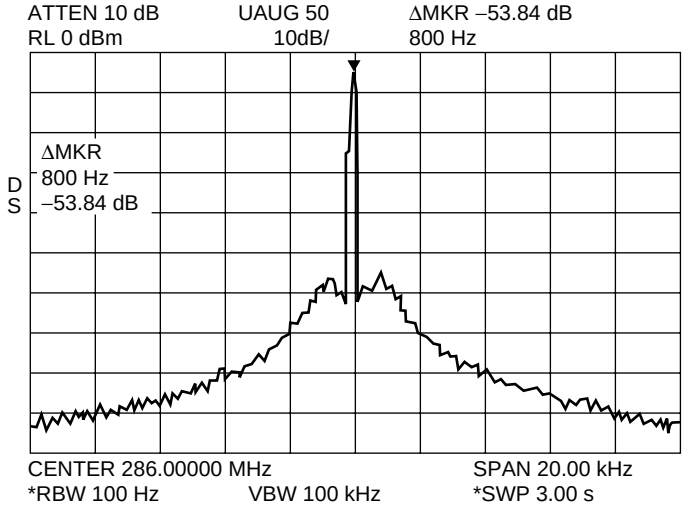




7. Spectrum Wave Form

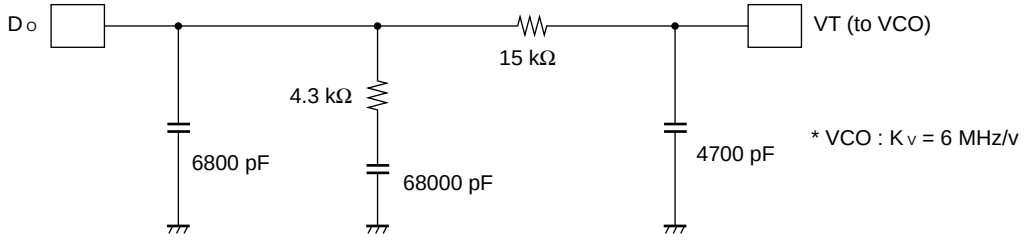


- LOCK Frequency : 286.0 MHz
  (fr = 25 kHz)
- V_{DD} = 1.2 V, V_p = 1.2 V
  Ta = +25°C



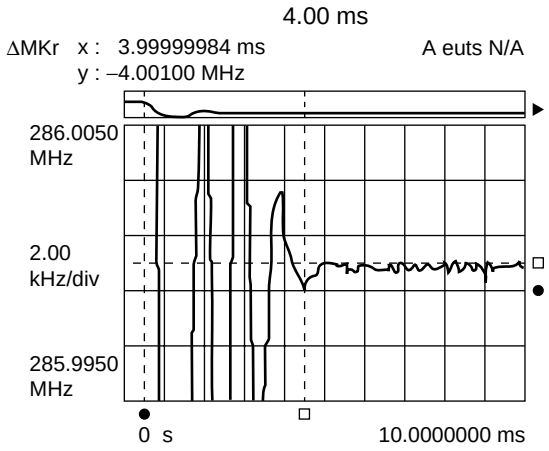
- LOCK Frequency : 286.0 MHz
  (fr = 25 kHz)
- V_{DD} = 1.2 V, V_p = 1.2 V
  Ta = +25°C

- Test circuit

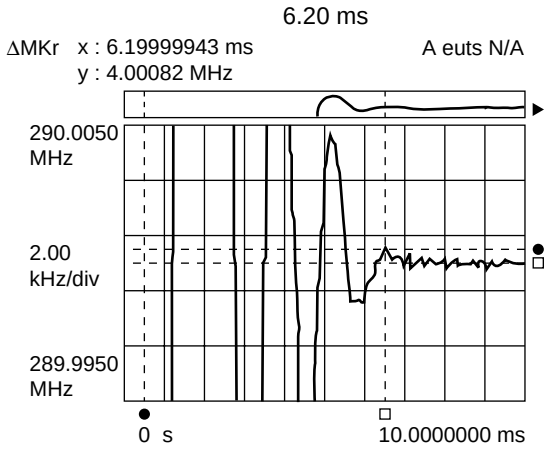


8. Lock Up Time

- LOCK Frequency: 290.0 MHz to 286.0 MHz
  (fr = 25 kHz)
- V_{DD} = 1.2 V, V_P = 1.2 V, Ta = +25°C
  290.0 MHz → 286.0 MHz, within ± 1 kHz



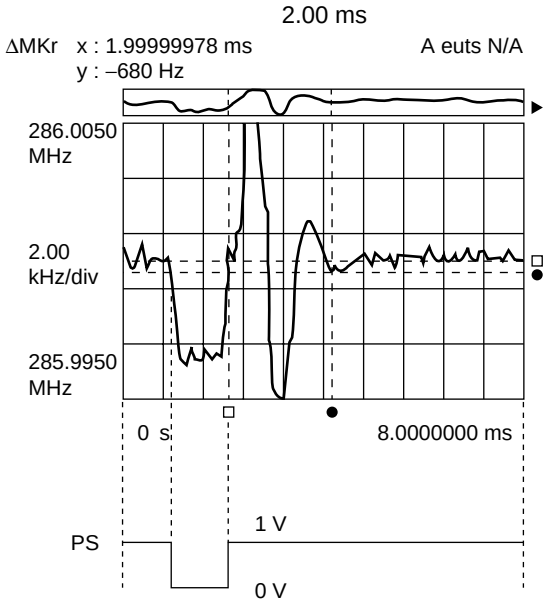
- LOCK Frequency: 286.0 MHz to 290.0 MHz
  (fr = 25 kHz)
- V_{DD} = 1.2 V, V_P = 1.2 V, Ta = +25°C
  286.0 MHz → 290.0 MHz, within ± 1 kHz



(Continued)

(Continued)

- LOCK Frequency: PS on to 286.0 MHz
  (fr = 25 kHz)
- V_{DD} = 1.2 V, V_P = 1.2 V, Ta = +25°C
  PS ON → 286.0 MHz, within ± 1 kHz



■ USAGE PRECAUTIONS

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

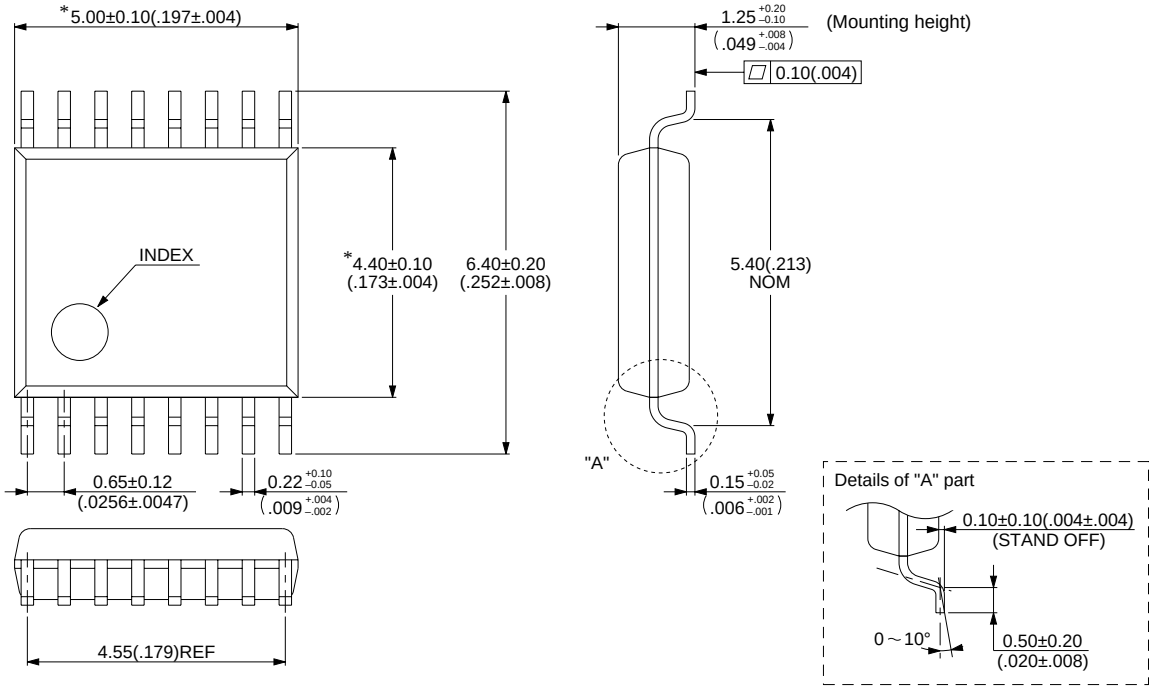
■ ORDERING INFORMATION

Parts number	Package	Remarks
MB15C02PFV1	16-pin Plastic SSOP (FPT-16P-M05)	
MB15C02PFV2	20-pin Plastic SSOP (FPT-20P-M03)	

■ PACKAGE DIMENSIONS

16 pins, Plastic SSOP
(FPT-16P-M05)

*: These dimensions do not include resin protrusion.



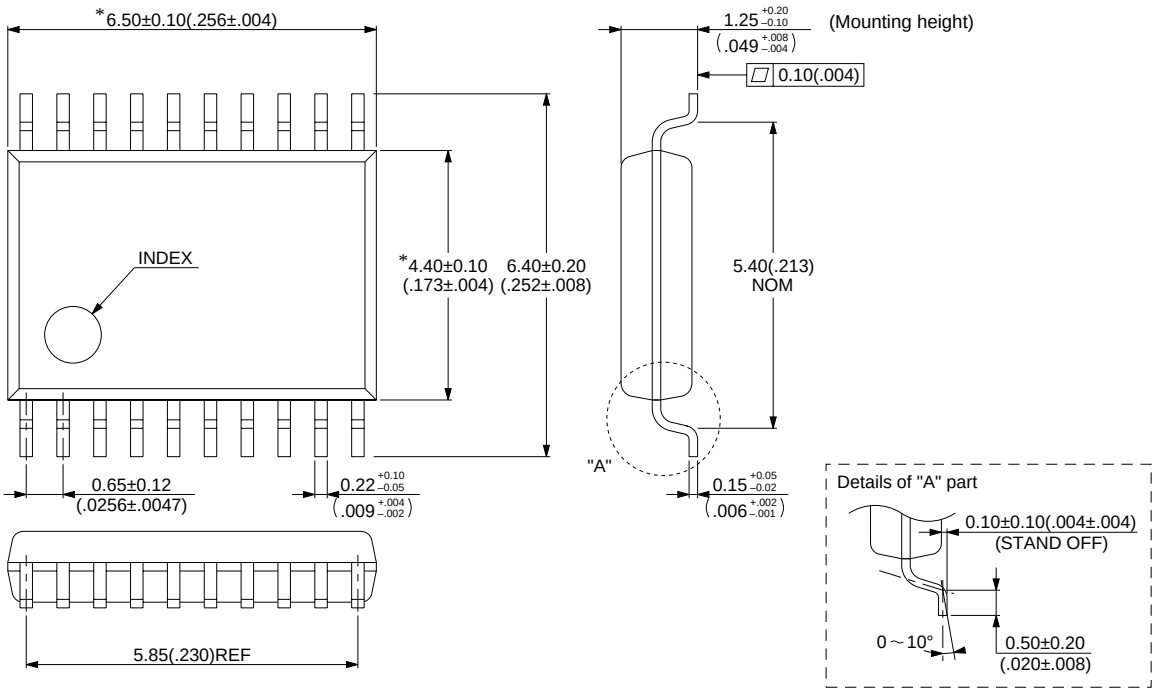
Dimensions in mm (inches)

(Continued)

(Continued)

20 pins, Plastic SSOP
(FPT-20P-M03)

*: These dimensions do not include resin protrusion.



Dimensions in mm (inches)

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