262144-word x 9-bit High Speed Synchronous Static RAM

Description

The CXK77920TM/YM is a high speed CMOS synchronous static RAM with common I/O pins, organized as 262144-word-by-9-bit. This synchronous SRAM integrates input registers, high speed SRAM and output registers onto a single monolithic IC. All input signals are latched at the positive edge of an external clock (CLK). The RAM data from the previous cycle is presented at the positive edge of the subsequent clock cycle. Write operation is initiated by the positive edge of CLK and is internally self-timed. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals. 90MHz operation is obtained from a single 5V power supply.

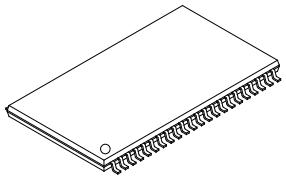
Function

There are three possible user transactions with the STRAM: Read operation, write operation and deselect operation.

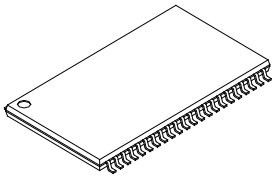
- The read operation requires $\overline{WE}$ = "HIGH" and $\overline{OE}$ = $\overline{CE}$ = "LOW" on the positive edge of CLK.

  The memory location pointed to by the contents of the Address registers is read internally and the contents of the location are captured in the Data-out registers on the next positive edge of CLK. The state of Data-out will reflect the contents of the Data-out registers.
- The write operation requires $\overline{CE}$ = $\overline{WE}$ = "LOW" on the positive edge of CLK. The memory location pointed to by the contents of the Address registers is written with the contents of the Data-in registers. The write operation is entirely self-timed, eliminating critical timing edges.
- The deselect cycle requires $\overline{CE}$ = "HIGH" or $\overline{OE}$ = $\overline{WE}$ = "HIGH" on the positive edge of CLK. Write operation and internal read operation are disabled during the clock cycle. The data outputs are forced to a high impedance state during the next clock cycle. During the deselect cycle by $\overline{CE}$ = "HIGH", STRAM turns to power down mode.

CXK77920TM
44pin TSOP (II)
(Plastic)



CXK77920YM
44pin TSOP (II)
(Plastic)



Structure

Silicon gate CMOS IC

Features

- Fast cycle time:

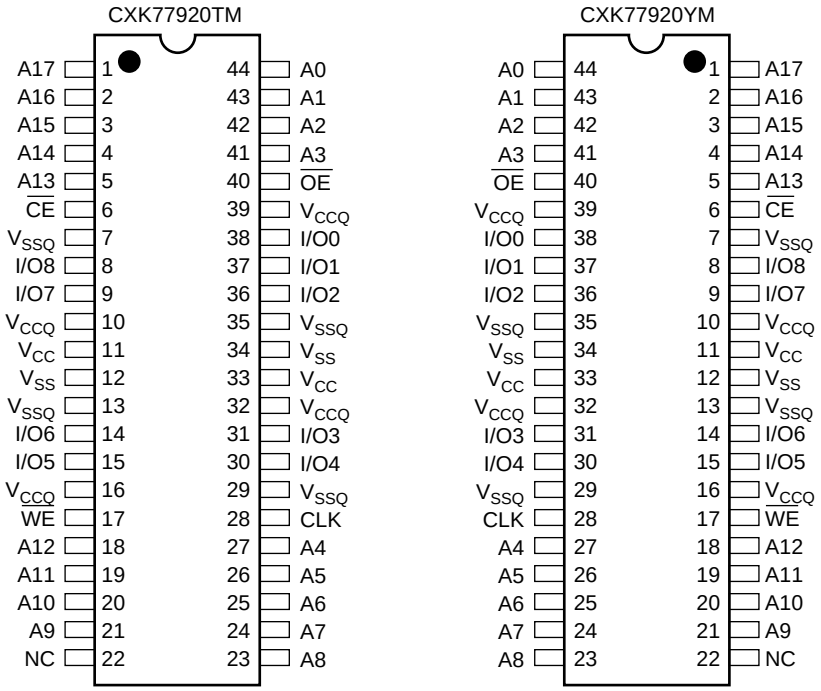
	(Cycle)	(Frequency)
CXK77920TM/YM-11	11.0ns	90MHz
CXK77920TM/YM-12	12.5ns	80MHz
CXK77920TM/YM-15	15.0ns	66.7MHz

- Fast clock to data valid

CXK77920TM/YM-11	6.0ns
CXK77920TM/YM-12	6.5ns
CXK77920TM/YM-15	7.0ns

- High speed, low power consumption
- Single +5V power supply: 5V±5%
- Separate output power supply: 3.15 to 5.25V
- Inputs and outputs are TTL compatible (3.3V I/O compatible)
- Common data input and output
- All inputs and outputs are registered on a single clock edge
- Self-timed write cycle
- Package line-up:
  400mil, 44 pin TSOP II with 0.8mm pitch

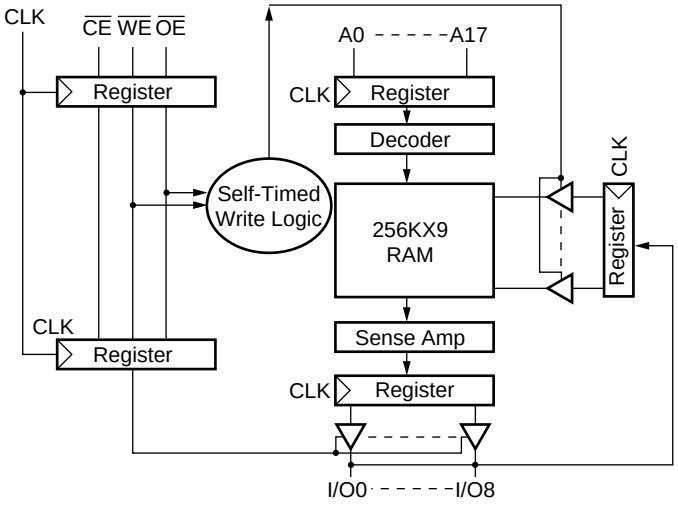
Pin Configuration (Top View)



Pin Description (1)

Symbol	Description
A0 to A17	Address input
I/O0 to I/O8	Data input/output
CLK	Clock
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
V_{CCQ}	Output power supply
V_{CC}	+5V power supply
V_{SS}/V_{SSQ}	Ground

Block Diagram



Pin Description (2)

CLK (Clock, positive edge triggered)

All timing is controlled by the rising or positive edge of CLK. All synchronous input and output signals are registered on the positive edge of CLK with set-up and hold times referenced to that edge. Since only one edge of CLK is referenced, the duty cycle of CLK is not critical.

A0 to A17 (Address)

The Address inputs are decoded on-chip to select one of 262,144 words. The state of the Address inputs is registered into the Address register on the positive edge of CLK. The Address inputs must be valid during every positive edge with all set-up and hold times referenced to that edge.

I/O0 to I/O8 (Data input/output)

I/O terminals are three-state and data input/output common. The state is defined by the Control block (refer to the truth table on page 4).

The data inputs for write operation must be valid during every positive edge of CLK with all set-up and hold times referenced to that edge. The data outputs are triggered by the positive edge of CLK and the contents of the Output-Registers are presented.

$\overline{WE}$ (Synchronous Write Enable, active low)

$\overline{WE}$ is used to indicate whether a read or write operation is to be performed. $\overline{WE}$ is “LOW” to perform a write operation. $\overline{WE}$ is registered on every positive edge of CLK with set-up and hold times referenced to that edge. The internal timing required to store data into the memory array is self-timed.

$\overline{CE}$ (Synchronous Chip Enable, active low)

$\overline{CE}$ is used to select the Synchronous SRAM when low (or deselect when high). When selected, the Synchronous SRAM will perform a read or write operation (refer to the truth table on page 4). The state of $\overline{CE}$ is registered on every positive edge of CLK with set-up and hold times referenced to that edge.

$\overline{OE}$ (Synchronous Output Enable, active low)

$\overline{OE}$ is used to indicate that a read operation is to be performed. If the Synchronous SRAM is selected, the $\overline{OE}$ is low to perform a read operation (refer to the truth table on page 4). The state of $\overline{OE}$ is registered on every positive edge of CLK with set-up and hold times referenced to that edge.

Absolute Maximum Ratings

(Ta = +25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	–0.5 to +7.0	V
Input voltage	V_{IN}	–0.5 to V_{CC}+0.5	V
Output voltage	V_O	–0.5 to V_{CC}+0.5	V
Allowable power dissipaiton	P_D	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	–55 to +150	°C
Soldering temperature • time	T_{solder}	235 • 10	°C • sec

Truth Table

CLK	$\overline{CE}$ (tn)	$\overline{WE}$ (tn)	$\overline{OE}$ (tn)	Mode	I/O0 to I/O8	V_{CC} Current
↑	H	X	X	Deselect	Hi-Z	I_{SB}
↑	L	H	H	Read	Hi-Z	I_{CC}
↑	L	H	L	Read	Data out (1)	I_{CC}
↑	L	L	X	Write	Data in	I_{CC}

NOTES:

1. Data comes out on the next positive edge of CLK.

X: “H” or “L”

DC Recommended Operating Conditions

(Ta = +25°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Output supply voltage	V_{CCQ}	3.15	—	5.25	V
Input high voltage	V_{IH}	2.2	—	V_{CC} +0.3	V
Input low voltage	V_{IL}	–0.3(1)	—	0.8	V

NOTE:

1. V_{IL} = –1.5V min. for pulse width less than 1ns.

Electrical Characteristics

DC Characteristics

(V_{CC} = 5V ±5%, GND = 0V, Ta = 0 to = +70°C)

Item	Symbol	Test Conditions		Min.	Max.	Unit
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}		–1	1	µA
Output leakage current	I_{LO}	V_O = GND to V_{CC} $\overline{OE}$ = V_{IH}		–1	1	µA
Average operating current	I_{CC}	Duty = 100% I_{OUT} = 0mA	Cycle = 90MHz	—	180	mA
			Cycle = 80MHz	—	170	
			Cycle = 66.7MHz	—	160	
Standby current	I_{SB}	$\overline{CE} \geq V_{IH}$ Cycle Min, Duty = 100%		—	130	mA
Output high voltage	V_{OH}	I_{OH} = –2.0mA		2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 4.0mA		—	0.4	V

I/O Capacitance

(Ta = +25°C, f = 1MHz)

Item	Symbol	Test Conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	5	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

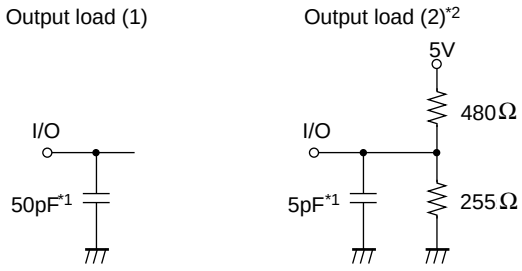
NOTE: This parameter is sampled and is not 100% tested.

AC Characteristics

AC Test Conditions

(V_{CC} = 5V±5%, Ta = 0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH} = 3.0V
Input pulse low level	V_{IL} = 0V
Input rise time	tr = 3ns
Input fall time	tf = 3ns
Input reference level	1.5V
Output reference level	1.5V
Output load conditions	Figure 1



*1. Including scope and jig capacitance.

*2. t_{CKHQZ}, t_{CKHQX}

Figure 1

Read Cycle

Item	Symbol	-11		-12		-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{CKHCKH}	11	—	12.5	—	15	—	ns
Clock high pulse width	t_{CKHCKL}	3.5	—	4.0	—	5.0	—	ns
Clock low pulse width	t_{CKLCKH}	3.5	—	4.0	—	5.0	—	ns
Clock to data valid	t_{CKHQV}	—	6.0	—	6.5	—	7.0	ns
Address setup to clock high	t_{AVCKH}	2.5	—	2.5	—	3.0	—	ns
Address hold from clock high	t_{CKHAX}	0.5	—	0.5	—	0.5	—	ns
Chip enable setup to clock high	t_{CEVCKH}	2.5	—	2.5	—	3.0	—	ns
Chip enable hold from clock high	t_{CKHCEX}	0.5	—	0.5	—	0.5	—	ns
Output enable setup to clock high	t_{OEVCKH}	2.5	—	2.5	—	3.0	—	ns
Output enable hold from clock high	t_{CKHOEX}	0.5	—	0.5	—	0.5	—	ns
Clock high to output low-Z	t_{CKHQX}(1)	1.5	—	1.5	—	1.5	—	ns
Clock high to output high-Z	t_{CKHQZ}(1)	—	4.5	—	5.0	—	6.0	ns

NOTE:

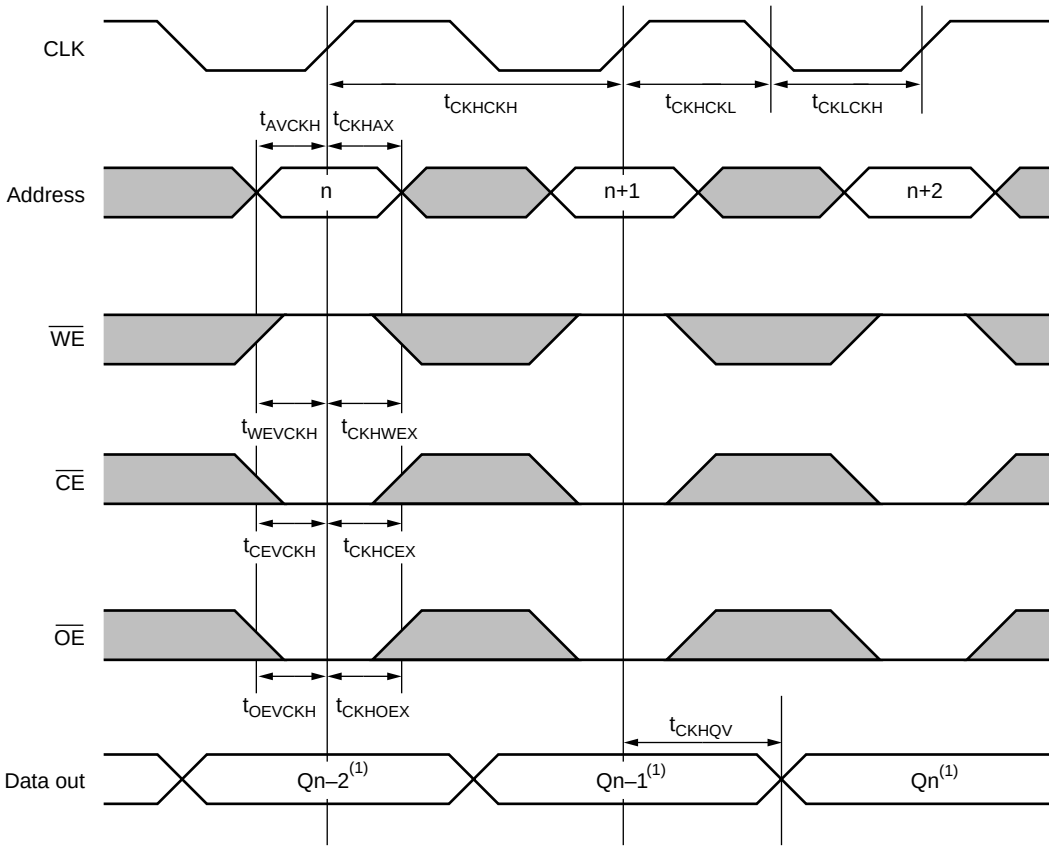
1. Transition is measured +200mV from steady voltage with specified loading in Figure 1-(2). This parameter is sampled and is not 100% tested.

Write Cycle

Item	Symbol	-11		-12		-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{CKHCKH}	11	—	12.5	—	15	—	ns
Clock high pulse width	t_{CKHCKL}	3.5	—	4.0	—	5.0	—	ns
Clock low pulse width	t_{CKLCKH}	3.5	—	4.0	—	5.0	—	ns
Address setup to clock high	t_{AVCKH}	2.5	—	2.5	—	3.0	—	ns
Address hold from clock high	t_{CKHAX}	0.5	—	0.5	—	0.5	—	ns
Chip enable setup to clock high	t_{CEVCKH}	2.5	—	2.5	—	3.0	—	ns
Chip enable hold from clock high	t_{CKHCEX}	0.5	—	0.5	—	0.5	—	ns
Write enable setup to clock high	t_{WEVCKH}	2.5	—	2.5	—	3.0	—	ns
Write enable hold from clock high	t_{CKHWEX}	0.5	—	0.5	—	0.5	—	ns
Input data setup to clock high	t_{DVCKH}	2.5	—	2.5	—	3.0	—	ns
Input data hold from clock high	t_{CKHDX}	0.5	—	0.5	—	0.5	—	ns

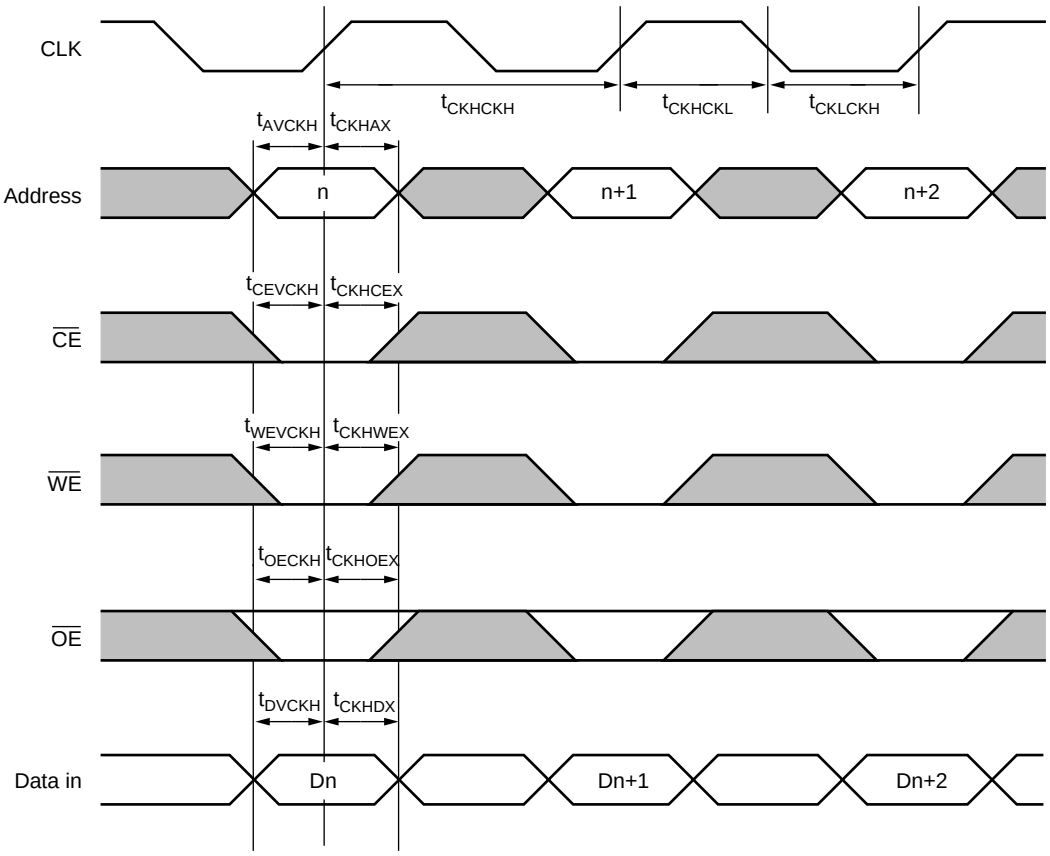
Timing Waveform

Read Cycle

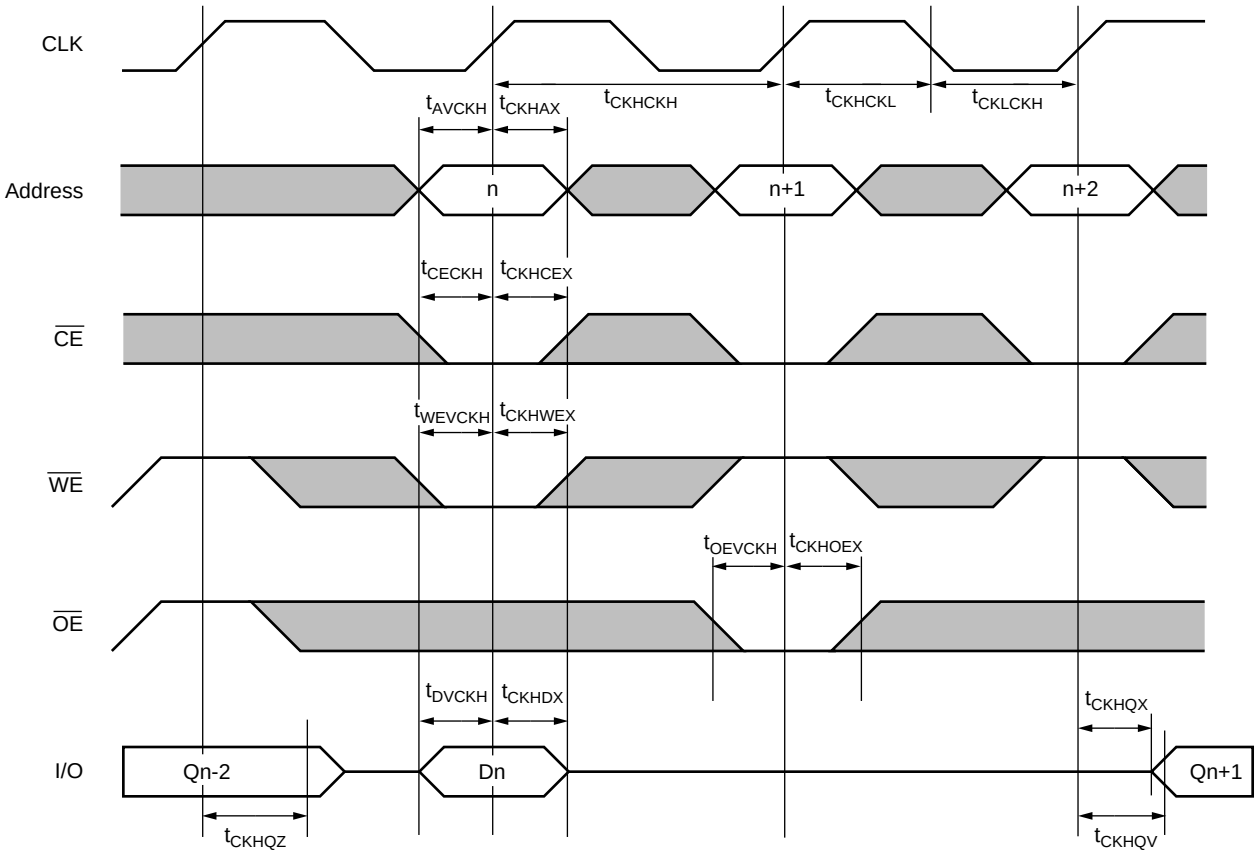


NOTE:
1. Valid data from CLK high is the data from the previous cycle.

Write Cycle: $\overline{OE}$ = VIH or VIL

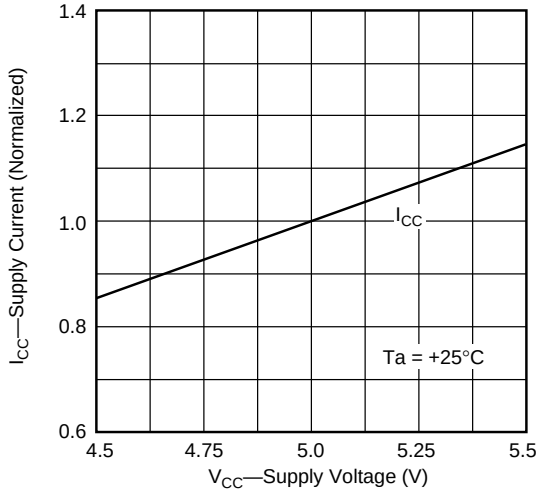


Read/Write Cycle

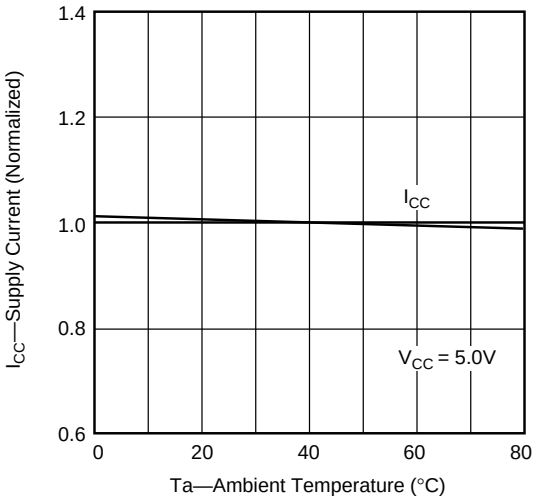


Example of Representative Characteristics

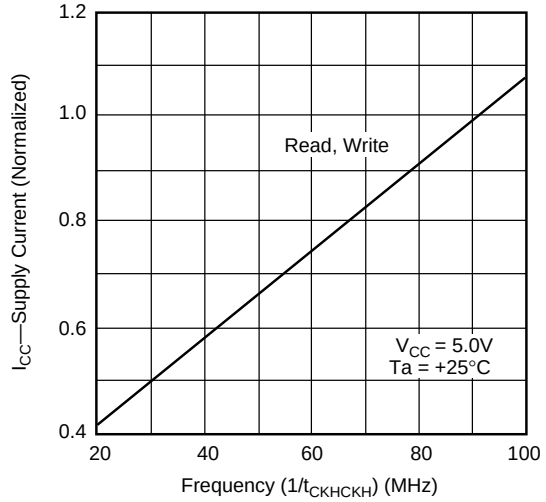
Supply Current vs. Supply Voltage



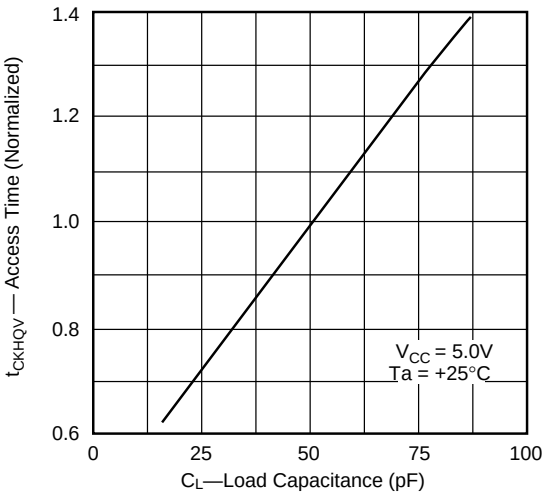
Supply Current vs. Ambient Temperature



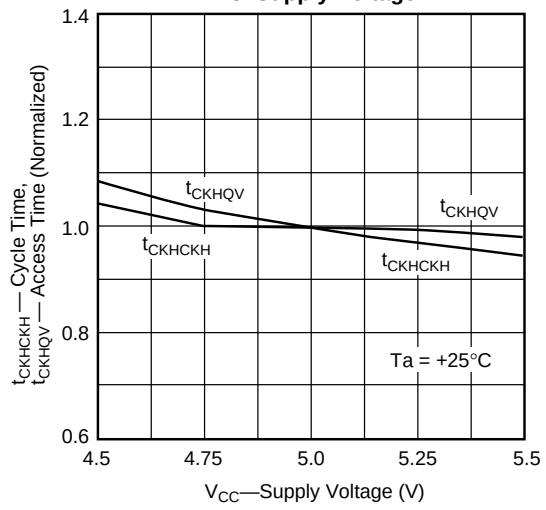
Supply Current vs. Frequency



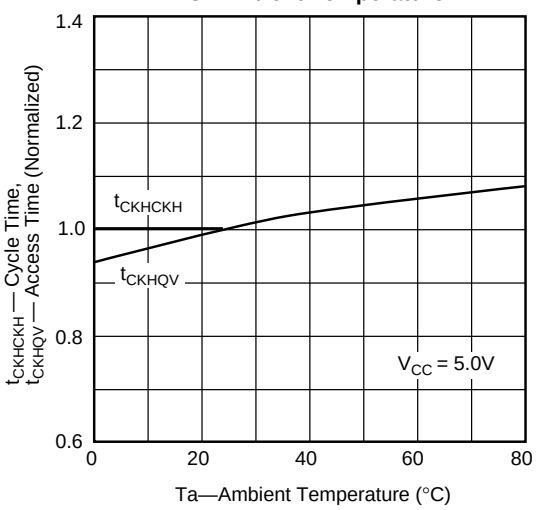
Access Time vs. Load Capacitance



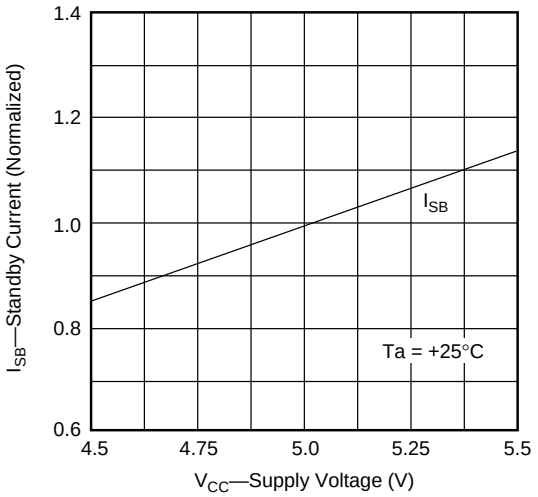
Cycle Time (minimum) / Access Time vs. Supply Voltage



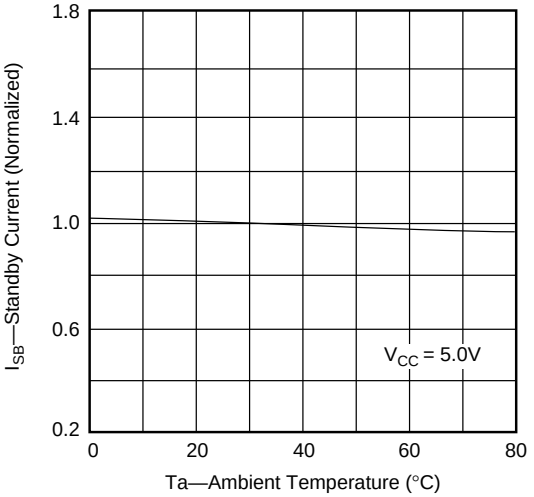
Cycle Time (minimum) / Access Time vs. Ambient Temperature



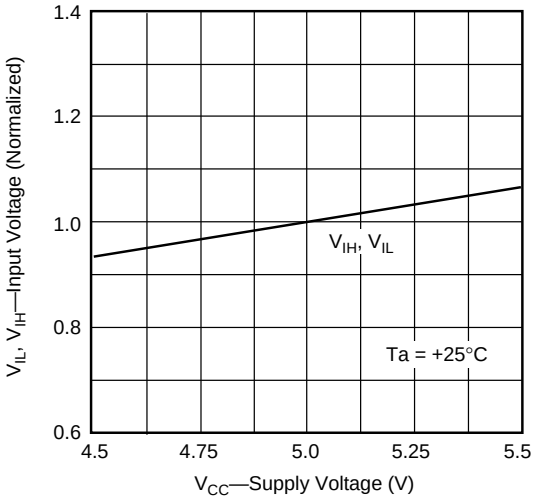
Standby Current vs. Supply Voltage



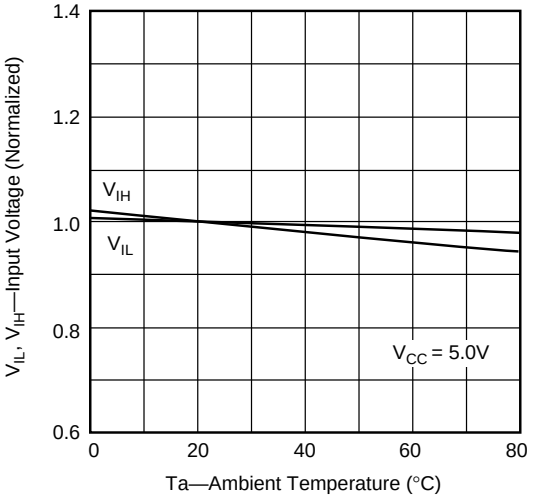
Standby Current vs. Ambient Temperature



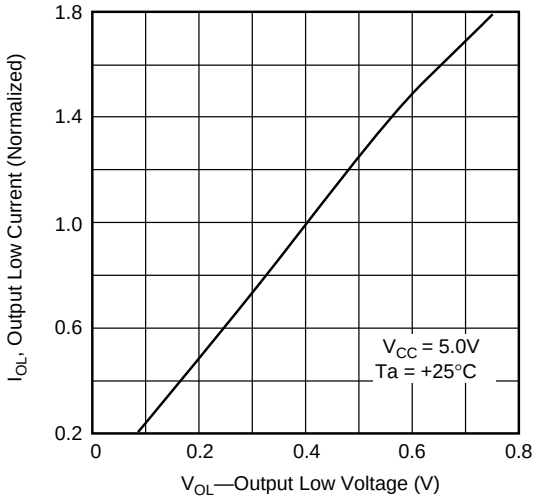
Input Voltage Level vs. Supply Voltage



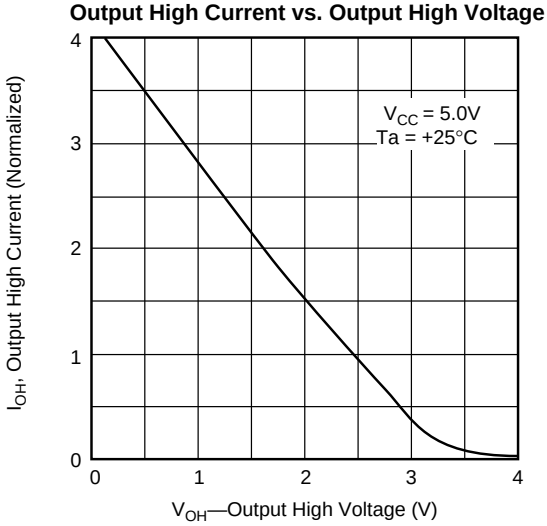
Input Voltage Level vs. Ambient Temperature



Output Low Current vs. Output Low Voltage



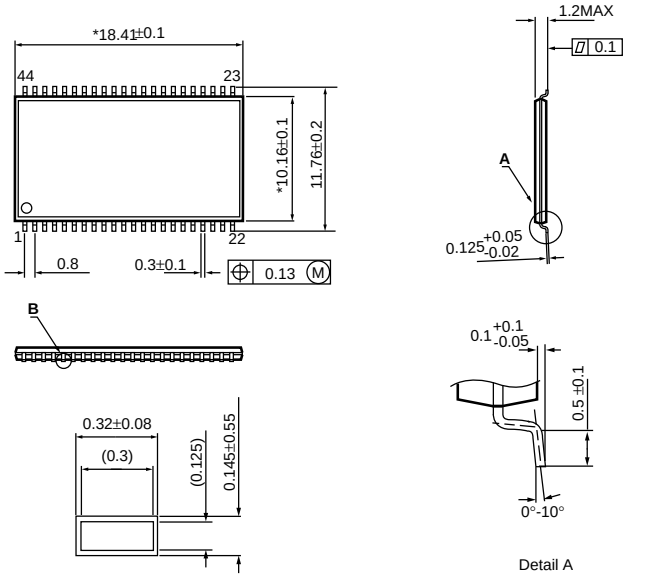
Output High Current vs. Output High Voltage



Package Dimensions Unit: mm

CXK77920TM

44 PIN TSOP (II) (PLASTIC) 400MIL



NOTE>Dimension "*" does not include mold protrusion.

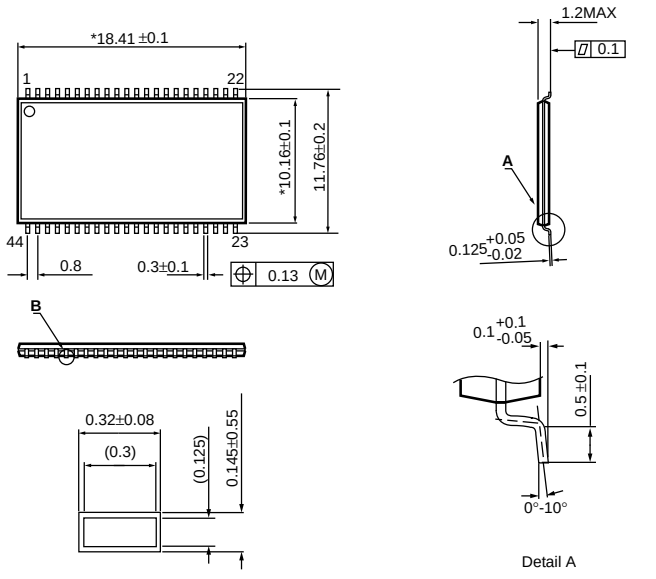
SONY CODE	TSOP(II)-44P-L01
EIAJ CODE	TSOP(II)044-P-0400-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.5g

CXK77920YM

44 PIN TSOP (II) (PLASTIC) 400MIL



NOTE>Dimension "*" does not include mold protrusion.

SONY CODE	TSOP(II)-44P-L01R
EIAJ CODE	TSOP(II)044-P-0400-B
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.5g